

MC74LVX125

Quad Bus Buffer With 5 V-Tolerant Inputs

The MC74LVX125 is an advanced high speed CMOS quad bus buffer. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

The MC74LVX125 requires the 3-state control input (\overline{OE}) to be set High to place the output into the high impedance state.

Features

- High Speed: $t_{PD} = 4.4$ ns (Typ) at $V_{CC} = 3.3$ V
- Low Power Dissipation: $I_{CC} = 4 \mu A$ (Max) at $T_A = 25^\circ C$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: $V_{OLP} = 0.5$ V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: Human Body Model > 2000 V
Machine Model > 200 V
- These Devices are Pb-Free and are RoHS Compliant

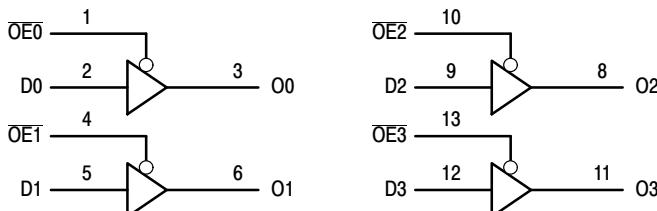


Figure 1. Logic Diagram

PIN NAMES

Pins	Function
\overline{OE}	Output Enable Inputs
Dn	Data Inputs
On	3-State Outputs

FUNCTION TABLE

INPUTS		OUTPUTS
\overline{OE}	Dn	On
L	L	L
L	H	H
H	X	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions Are Acceptable, for I_{CC} reasons, DO NOT FLOAT Inputs



ON Semiconductor®

<http://onsemi.com>

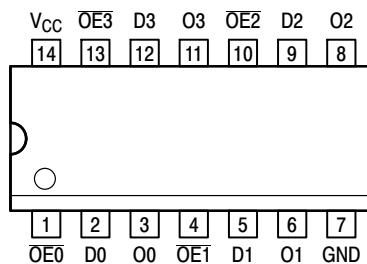


SOIC-14 NB
D SUFFIX
CASE 751A

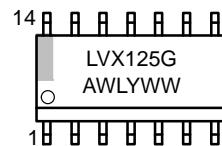


TSSOP-14
DT SUFFIX
CASE 948G

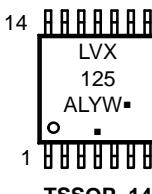
PIN ASSIGNMENT



MARKING DIAGRAMS



SOIC-14 NB



TSSOP-14

LVX125 = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ▀ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MC74LVX125

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +7.0	V
V_{in}	DC Input Voltage	-0.5 to +7.0	V
V_{out}	DC Output Voltage	-0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current	-20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation	180	mW
T_{stg}	Storage Temperature	-65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-40	+85	°C
$\Delta t/\Delta V$	Input Rise and Fall Time	0	100	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	$T_A = 25^\circ C$			$T_A = -40 \text{ to } 85^\circ C$		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High-Level Input Voltage		2.0	1.5			1.5		V
			3.0	2.0			2.0		
			3.6	2.4			2.4		
V_{IL}	Low-Level Input Voltage		2.0			0.5		0.5	V
			3.0			0.8		0.8	
			3.6			0.8		0.8	
V_{OH}	High-Level Output Voltage ($V_{in} = V_{IH}$ or V_{IL})	$I_{OH} = -50\mu A$ $I_{OH} = -50\mu A$ $I_{OH} = -4mA$	2.0	1.9	2.0		1.9		V
			3.0	2.9	3.0		2.9		
			3.0	2.58			2.48		
V_{OL}	Low-Level Output Voltage ($V_{in} = V_{IH}$ or V_{IL})	$I_{OL} = 50\mu A$ $I_{OL} = 50\mu A$ $I_{OL} = 4mA$	2.0		0.0	0.1		0.1	V
			3.0		0.0	0.1		0.1	
			3.0			0.36		0.44	
I_{in}	Input Leakage Current	$V_{in} = 5.5V$ or GND	3.6			± 0.1		± 1.0	µA
I_{OZ}	Maximum Three-State Leakage Current	$V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	3.6			± 0.25		± 2.5	µA
I_{CC}	Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	3.6			4.0		40.0	µA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	
t_{PLH} , t_{PHL}	Propagation Delay Input to Output	$V_{CC} = 2.7\text{V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		5.8 8.3	10.1 13.6	1.0 1.0	13.5 17.0	ns
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		4.4 6.9	6.2 9.7	1.0 1.0	8.5 12.0	
t_{PZL} , t_{PZH}	Output Enable Time \overline{OE} to O	$V_{CC} = 2.7\text{V}$ $C_L = 15\text{pF}$ $R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$		5.3 7.8	9.3 12.8	1.0 1.0	12.5 16.0	ns
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$ $R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$		4.0 6.5	5.6 9.1	1.0 1.0	7.5 11.0	
t_{PLZ} , t_{PHZ}	Output Disable Time \overline{OE} to O	$V_{CC} = 2.7\text{V}$ $C_L = 50\text{pF}$ $R_L = 1\text{k}\Omega$		10.0	15.7	1.0	19.0	ns
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 50\text{pF}$ $R_L = 1\text{k}\Omega$		8.3	11.2	1.0	13.0	
t_{OSHL} t_{OSLH}	Output-to-Output Skew (Note 1)	$V_{CC} = 2.7\text{V}$ $C_L = 50\text{pF}$ $V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 50\text{pF}$			1.5 1.5		1.5 1.5	ns

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
		Min	Typ	Max	Min	Max	
C_{in}	Input Capacitance		4	10		10	pF
C_{out}	Maximum Three-State Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 2)		14				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(\text{OPR})} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/4$ (per bit). C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$, $C_L = 50\text{pF}$, $V_{CC} = 3.3\text{V}$, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25^\circ\text{C}$			Unit
		Typ	Max		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.5	V	
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	-0.3	-0.5	V	
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V	
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V	

SWITCHING WAVEFORMS

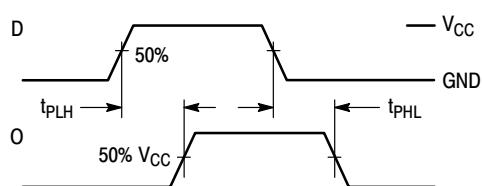


Figure 2.

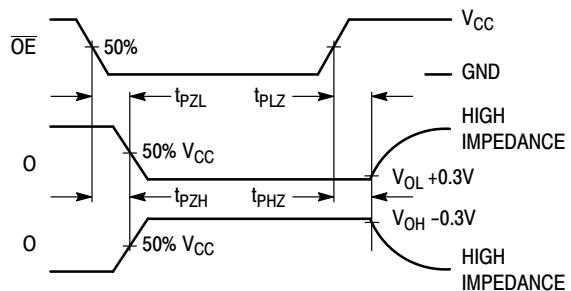
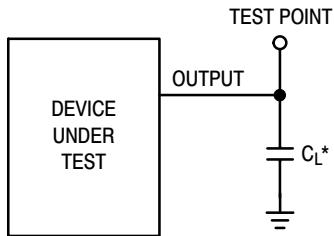


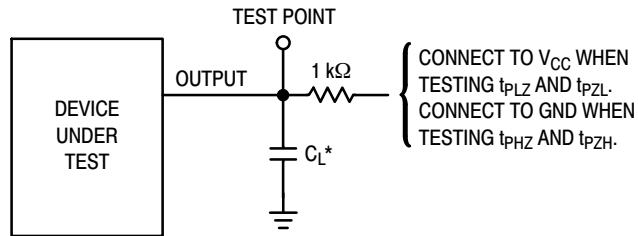
Figure 3.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 4. Propagation Delay Test Circuit



*Includes all probe and jig capacitance

Figure 5. Three-State Test Circuit

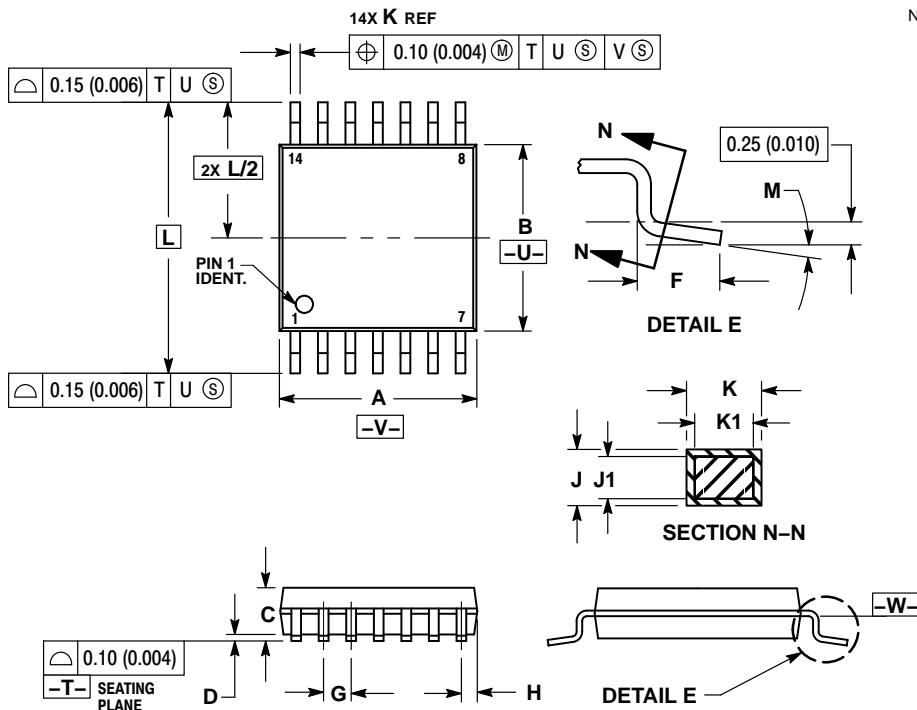
ORDERING INFORMATION

Device	Package	Shipping [†]
MC74LVX125DG	SOIC-14 NB (Pb-Free)	55 Units / Rail
MC74LVX125DR2G	SOIC-14 NB (Pb-Free)	2500 Tape & Reel
MC74LVX125DTG	TSSOP-14 (Pb-Free)	96 Units / Rail
MC74LVX125DTR2G	TSSOP-14 (Pb-Free)	2500 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

TSSOP-14
CASE 948G
ISSUE B

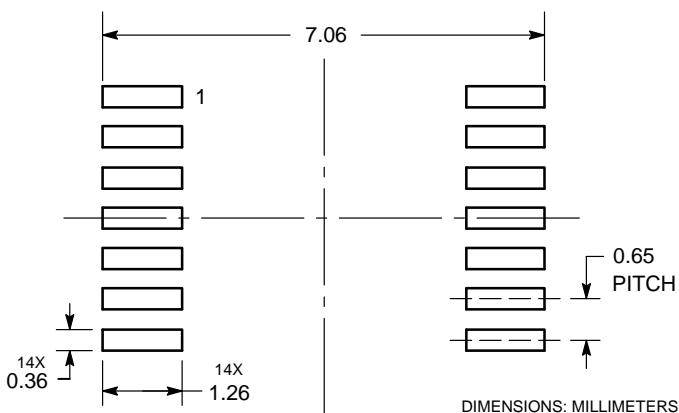


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT*

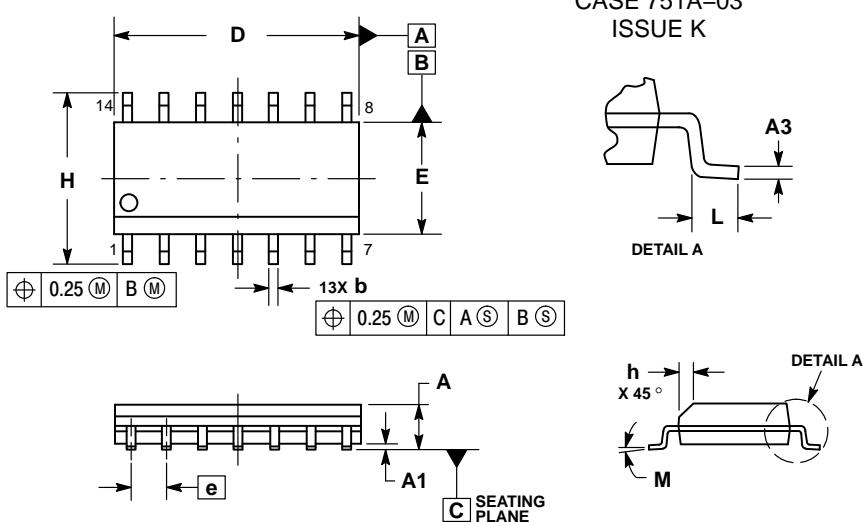


DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74LVX125

PACKAGE DIMENSIONS

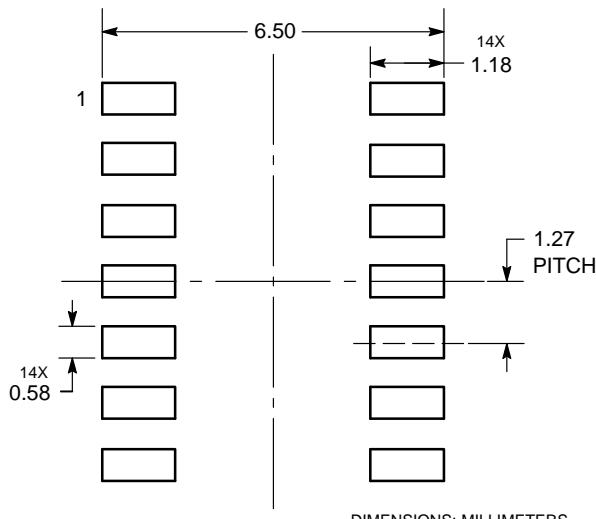


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and the  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free

USA/Canada

Europe, Middle East and Africa Technical Support:

Phone: 421 33 790 2910

Japan Customer Focus Center

Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative