3.3V DIFFERENTIAL LVPECL-to-LVTTL TRANSLATOR

SY100EPT21L

FEATURES

- **3.3V power supply**
- **1.9ns typical propagation delay**
- **275MHz f_{MAX} (Clock bit stream, not pseudo-random)**
- **Differential LVPECL inputs**
- **24mA LVTTL outputs**
- **Flow-through pinouts**
- **Internal input resistors: pulldown on D, pulldown and pullup on /D**
- **Q output will default LOW with inputs open or at GND**
- **V_{BB} output**
- **Available in 8-pin MSOP and SOIC package**

DESCRIPTION

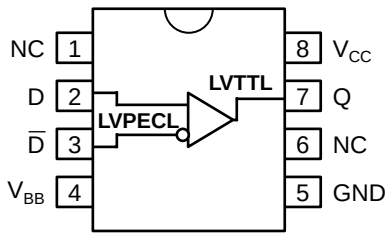
The SY100EPT21L is a single differential LVPECL-to-LVTTL translator using a single +3.3V power supply. Because LVPECL (Low Voltage Positive ECL) levels are used, only +3.3V and ground are required. The small outline 8-lead SOIC package and low skew single gate design make the EPT21L ideal for applications that require the translation of a clock or data signal where minimal space, low power, and low cost are critical.

V_{BB} allows a differential, single-ended, or AC-coupled interface to the device. If used, the V_{BB} output should be bypassed to V_{CC} with 0.01µF capacitor.

Under open input conditions, the /D will be biased at a $V_{CC}/2$ voltage level and the D input will be pulled to ground. This condition will force the Q output low to provide added stability.

The 100EPT is compatible with positive ECL 100K logic levels.

PIN CONFIGURATION/BLOCK DIAGRAM



(Available in 8-pin SOIC and 8-pin MSOP)

PIN NAMES

Pin	Function
Q	LVTTL Output
D, /D	Differential LVPECL Input Pair
V_{CC}	Positive Supply
V_{BB}	Output Reference Voltage
GND	Ground

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Paramter	Value	Unit
V_{CC}	Power Supply Voltage	–0.5 to +3.8	V
V_I	PECL Input Voltage	0V to V_{CC}+0.5	V
V_O	Voltage Applied to Output at HIGH State	–0.5 to V_{CC}	V
I_O	Current Applied to Output at LOW State	Twice the Rated I_{OL}	mA
T_{store}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	–40 to +85	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

TRUTH TABLE

D	/D	Q
L	H	L
H	L	H
Open	Open	L

LVTTL DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V ±5%

		T_A = –40°C		T_A = 0°C		T_A = +25°C			T_A = +85°C			
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Max.**	**Unit**	**Condition**
I_{OS}	Output Short Circuit Current	–80	–275	–80	–275	–80	—	–275	–80	–275	mA	V_{OUT} = 0V
I_{CC}	Power Supply Current	—	20	—	20	—	14	20	—	20	mA	
V_{OH}	Output HIGH Voltage	2.0	—	2.0	—	2.0	—	—	2.0	—	V	I_{OH} = –3.0mA
V_{OL}	Output LOW Voltage	—	0.5	—	0.5	—	—	0.5	—	0.5	V	I_{OL} = 24mA

LVPECL DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V ±5%

		T_A = –40°C		T_A = 0°C		T_A = +25°C			T_A = +85°C			
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Max.**	**Unit**	**Condition**
I_{IH}	Input HIGH Current	—	150	—	150	—	—	150	—	150	µA	
I_{IL}	Input LOW Current D /D	0.5 –300	— —	0.5 –300	— —	0.5 –300	— —	— —	0.5 –300	— —	µA	
V_{IH}	Input HIGH Voltage(2) 100EPT	2135	2420	2135	2420	2135	—	2420	2135	2420		
V_{IL}	Input LOW Voltage(2) 100EPT	1490	1825	1490	1825	1490	—	1825	1490	1825		
V_{BB}	Reference Output(2) 100EPT	1920	2040	1920	2040	1920	1980	2040	1920	2040		

NOTES:

1. These values are for V_{cc} = 3.3V. Level Specifications will vary 1:1 V_{cc}.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V ±5%

Symbol	Parameter	T_A = –40°C		T_A = 0°C		T_A = +25°C			T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay	1.5	2.5	1.5	2.5	1.5	1.9	2.5	1.5	2.5	ns	C_L = 20pF
t_{skpp}	Part-to-Part Skew(1,2)	—	0.5	—	0.5	—	—	0.5	—	0.5	ns	C_L = 20pF
f_{MAX}	Maximum Input Frequency(3,4)	275	—	275	—	275	—	—	275	—	MHz	C_L = 20pF
V_{CMR}	Common Mode Range	1.2	V_{CC}	1.2	V_{CC}	1.2	—	V_{CC}	1.2	V_{CC}	V	
V_{PP}	Minimum Peak-to-Peak Input(5)	100	—	100	—	100	—	—	100	—	mV	
t_r t_f	Output Rise/Fall Time (1.0V to 2.0V)	0.5	1.0	0.5	1.0	0.5	—	1.0	0.5	1.0	ns	C_L = 20pF

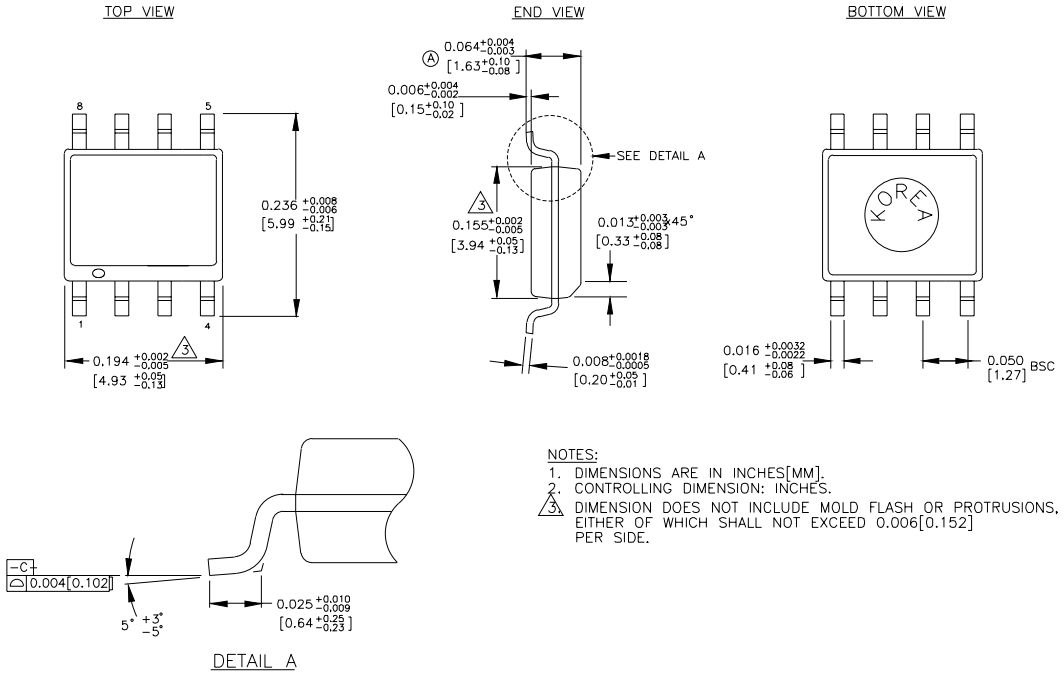
NOTES:

1. Part-to-Part Skew considering HIGH-to-HIGH transitions at common V_{CC} level.
2. These parameters are guaranteed but not tested.
3. Frequency at which output levels will meet a 0.8V to 2.0V minimum swing.
4. The f_{MAX} value is specified as the minimum guaranteed maximum frequency. Actual operational maximum frequency may be greater.
5. 100mV input guarantees full logic at output.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range	V_{CC} Range (V)
SY100EPT21LZC	Z8-1	Commercial	+3.3V ±5%
SY100EPT21LZCTR	Z8-1	Commercial	+3.3V ±5%
SY100EPT21LKC	K8-1	Commercial	+3.3V ±5%
SY100EPT21LKCTR	K8-1	Commercial	+3.3V ±5%

8 LEAD PLASTIC SOIC (Z8-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.152] PER SIDE.

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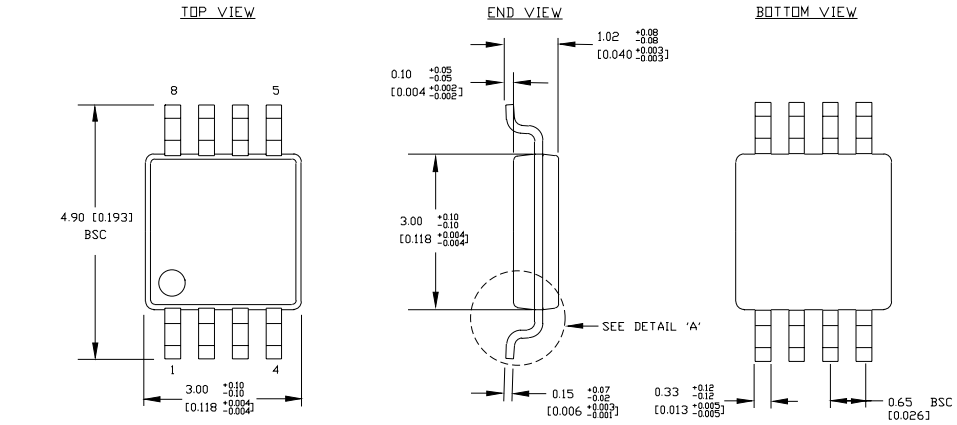
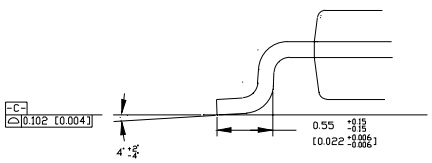
8 LEAD MSOP (K8-1)





DETAIL A

NOTES:
1. DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.20 [0.008] PER SIDE.

Rev. 01

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