

1. General description

The 74ALVT162821 is a 20-bit positive-edge triggered D-type flip-flop with 30 Ω termination resistors and 3-state outputs

The device can be used as two 10-bit flip-flops or one 20-bit flip-flop. The device features two clocks (1CP and 2CP) and two output enables (1 \overline{OE} and 2 \overline{OE}), each controlling 10-bits. The flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (nCP) transition. A HIGH on n \overline{OE} causes the outputs to assume a high-impedance OFF-state. Operation of the n \overline{OE} input does not affect the state of the flip-flops. Bus hold data inputs eliminate the need for external pull-up resistors to define unused inputs

2. Features and benefits

- Wide supply voltage range from 2.3 V to 3.6 V
- Overvoltage tolerant inputs to 5.5 V
- BiCMOS high speed and output drive
- Outputs include series resistance of 30 Ω making external termination resistors unnecessary
- No bus current loading when output is tied to 5 V bus
- Direct interface with TTL levels
- I_{OFF} circuitry provides partial Power-down mode operation
- 20-bit positive-edge triggered register
- 5 V I/O compatible
- Multiple V_{CC} and GND pins minimize switching noise
- Bus hold on data inputs
- Live insertion and extraction permitted
- Power-up reset
- Power-up 3-state
- Output capability: +12 mA and -12 mA
- Latch-up protection:
 - JESD17: exceeds 500 mA
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to 85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package				Version
	Temperature range	Name	Description		
74ALVT162821DGG	-40 °C to +85 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm		SOT364-1

20-bit bus interface D-type flip-flop; positive-edge trigger with $30\ \Omega$ termination resistors; 3-state

4. Functional diagram

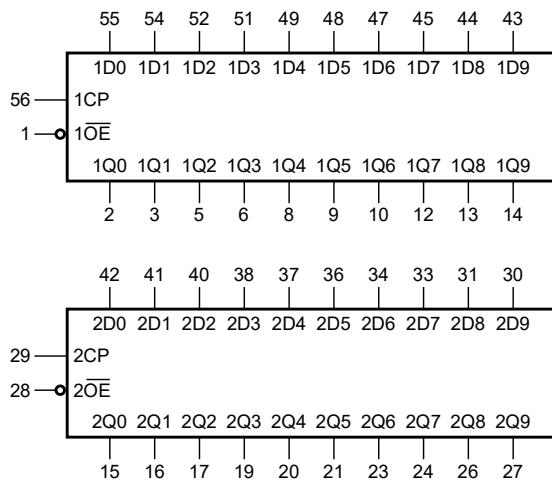


Fig. 1. Logic symbol

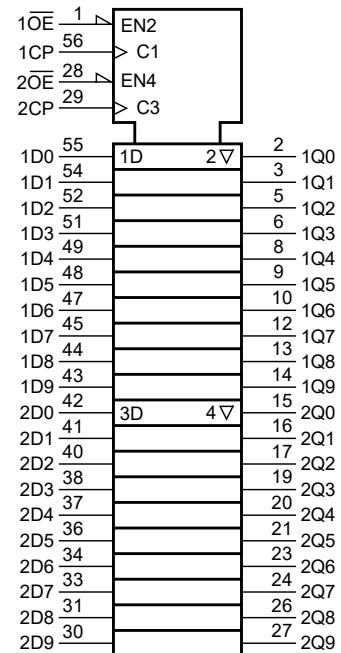


Fig. 2. IEC logic symbol

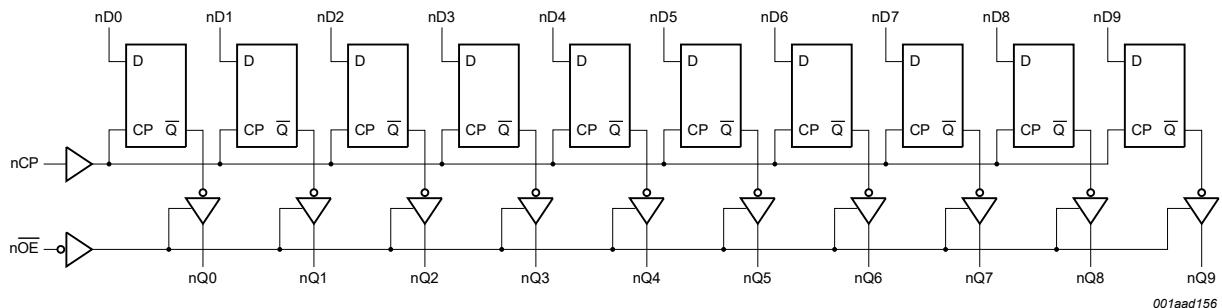


Fig. 3. Logic diagram

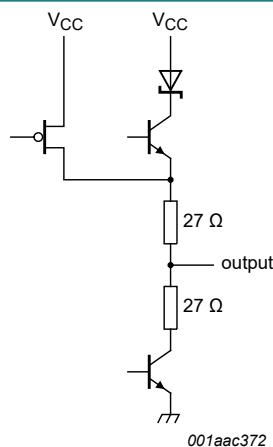


Fig. 4. Schematic of each output

5. Pinning information

5.1. Pinning

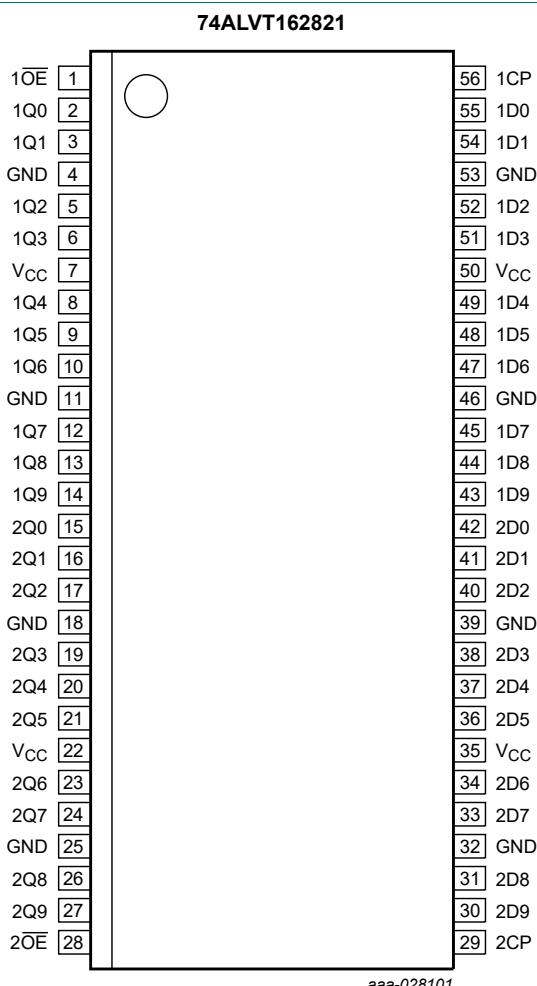


Fig. 5. Pin configuration SOT364-1 (TSSOP56)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1D0, 1D1, 1D2, 1D3, 1D4, 1D5, 1D6, 1D7, 1D8, 1D9	55, 54, 52, 51, 49, 48, 47, 45, 44, 43	data inputs
1Q0, 1Q1, 1Q2, 1Q3, 1Q4, 1Q5, 1Q6, 1Q7, 1Q8, 1Q9	2, 3, 5, 6, 8, 9, 10, 12, 13, 14	data outputs
2D0, 2D1, 2D2, 2D3, 2D4, 2D5, 2D6, 2D7, 2D8, 2D9	42, 41, 40, 38, 37, 36, 34, 33, 31, 30	data inputs
2Q0, 2Q1, 2Q2, 2Q3, 2Q4, 2Q5, 2Q6, 2Q7, 2Q8, 2Q9	15, 16, 17, 19, 20, 21, 23, 24, 26, 27	data outputs
1OE, 2OE	1, 28	output enable inputs (active LOW)
1CP, 2CP	56, 29	clock pulse inputs (active rising edge)
GND	4, 11, 18, 25, 32, 39, 46, 53	ground (0 V)
V _{CC}	7, 22, 35, 50	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;

L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;

NC = no change; X = don't care;

Z = high-impedance OFF-state; ↑ = LOW-to-HIGH clock transition.

Operating mode	Input			Internal register	Output
	nOE	nCP	nDn		
Load and read register	L	↑	l	L	L
	L	↑	h		
Hold	L	NC	X	NC	NC
Disable outputs	H	NC	X	NC	Z
	H	↑	nDn	nDn	Z

20-bit bus interface D-type flip-flop; positive-edge trigger with 30 Ω termination resistors; 3-state

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V_{CC}	supply voltage		-0.5	+4.6	V	
V_I	input voltage	[1]	-1.2	+7.0	V	
V_O	output voltage	output in OFF-state or HIGH-state	[1]	-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < 0$ V	-	-50	mA	
I_{OK}	output clamping current	$V_O < 0$ V	-	-50	mA	
I_O	output current	output in LOW-state	-	128	mA	
		output in HIGH-state	-	-64	mA	
T_{stg}	storage temperature		-65	+150	°C	
T_j	junction temperature	[2]	-	150	°C	

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	$V_{CC} = 2.5$ V ± 0.2 V	$V_{CC} = 3.3$ V ± 0.3 V	Unit		
			Min	Max			
V_{CC}	supply voltage		2.3	2.7	3.0	3.6	V
V_I	input voltage		0	5.5	0	5.5	V
I_{OH}	HIGH-level output current		-	-8	-	-12	mA
I_{OL}	LOW-level output current	none	-	12	-	12	mA
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	-	10	-	10	ns/V
T_{amb}	ambient temperature	free-air	-40	+85	-40	+85	°C

9. Static characteristics

Table 6. Static characteristicsAt recommended operating conditions; $T_{amb} = -40$ °C to +85 °C; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit	
$V_{CC} = 2.5$ V ± 0.2 V							
V_{IK}	input clamping voltage	$V_{CC} = 2.3$ V; $I_{IK} = -18$ mA	-	-0.85	-1.2	V	
V_{IH}	HIGH-level input voltage		1.7	-	-	V	
V_{IL}	LOW-level input voltage		-	-	0.7	V	
V_{OH}	HIGH-level output voltage	$V_{CC} = 2.3$ V to 3.6 V; $I_O = -100$ μ A	$V_{CC} - 0.2$	V_{CC}	-	V	
		$V_{CC} = 2.3$ V; $I_O = -8$ mA	1.8	2.1	-	V	
V_{OL}	LOW-level output voltage	$V_{CC} = 2.3$ V; $I_O = 100$ μ A	-	0.07	0.2	V	
		$V_{CC} = 2.3$ V; $I_O = 24$ mA	-	0.3	0.5	V	
		$V_{CC} = 2.3$ V; $I_O = 8$ mA	-	-	0.4	V	
$V_{OL(pu)}$	power-up LOW-level output voltage	$V_{CC} = 2.7$ V; $I_O = 1$ mA; $V_I = V_{CC}$ or GND	[2]	-	-	0.55	V

20-bit bus interface D-type flip-flop; positive-edge trigger with 30 Ω termination resistors; 3-state

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_I	input leakage current	all input pins				
		$V_{CC} = 0 \text{ V or } 2.7 \text{ V}; V_I = 5.5 \text{ V}$	-	0.1	10	μA
		control pins				
		$V_{CC} = 2.7 \text{ V}; V_I = V_{CC} \text{ or GND}$	-	0.1	± 1	μA
		data pins; [3]				
		$V_{CC} = 2.7 \text{ V}; V_I = V_{CC}$	-	0.1	1	μA
I_{OFF}	power-off leakage current	$V_{CC} = 0 \text{ V}; V_I \text{ or } V_O = 0 \text{ V to } 4.5 \text{ V}$	-	0.1	± 100	μA
I_{BHL}	bus hold LOW current	data inputs; $V_{CC} = 2.3 \text{ V}; V_I = 0.7 \text{ V}$	-	90	-	μA
I_{BHH}	bus hold HIGH current	data inputs; $V_{CC} = 2.3 \text{ V}; V_I = 1.7 \text{ V}$	-	-10	-	μA
I_{EX}	external current	output in HIGH-state when $V_O > V_{CC}$; $V_O = 5.5 \text{ V}; V_{CC} = 2.3 \text{ V}$	-	10	125	μA
$I_{O(\text{pu/pd})}$	power-up/power-down output current	$V_{CC} \leq 1.2 \text{ V}; V_O = 0.5 \text{ V to } V_{CC}$; $V_I = \text{GND or } V_{CC}$; $n\overline{OE} = \text{don't care}$	[4]	-	1	± 100 μA
I_{OZ}	OFF-state output current	$V_{CC} = 2.7 \text{ V}; V_I = V_{IL} \text{ or } V_{IH}$				
		output HIGH-state; $V_O = 2.3 \text{ V}$	-	0.5	5	μA
		output LOW-state; $V_O = 0.5 \text{ V}$	-	0.5	-5	μA
I_{CC}	supply current	$V_{CC} = 2.7 \text{ V}; V_I = \text{GND or } V_{CC}; I_O = 0 \text{ A}$				
		outputs HIGH-state	-	0.04	0.1	mA
		outputs LOW-state	-	2.3	4.5	mA
		outputs disabled [5]		0.04	0.1	mA
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$; one input at $V_{CC} - 0.6 \text{ V}$; other inputs at V_{CC} or GND	[6]	-	0.04	0.4 mA
C_I	input capacitance	$V_I = 0 \text{ V or } V_{CC}$	-	3	-	pF
C_O	output capacitance	$V_O = 0 \text{ V or } V_{CC}$	-	9	-	pF
$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$						
V_{IK}	input clamping voltage	$V_{CC} = 3.0 \text{ V}; I_{IK} = -18 \text{ mA}$	-	-0.85	-1.2	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}; I_O = -100 \mu\text{A}$	$V_{CC} - 0.2$	V_{CC}	-	V
		$V_{CC} = 3.0 \text{ V}; I_O = -32 \text{ mA}$	2.0	2.3	-	V
V_{OL}	LOW-level output voltage	$V_{CC} = 3.0 \text{ V}$				
		$I_O = 100 \mu\text{A}$	-	0.07	0.2	V
		$I_O = 16 \text{ mA}$	-	0.25	0.4	V
		$I_O = 32 \text{ mA}$	-	0.3	0.5	V
		$I_O = 64 \text{ mA}$	-	0.4	0.55	V
$V_{OL(\text{pu})}$	power-up LOW-level output voltage	$V_{CC} = 3.6 \text{ V}; I_O = 1 \text{ mA}; V_I = V_{CC} \text{ or GND}$	[2]	-	-	0.55 V

20-bit bus interface D-type flip-flop; positive-edge trigger with 30 Ω termination resistors; 3-state

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit	
I _I	input leakage current	all input pins;					
		V _{CC} = 0 V or 3.6 V; V _I = 5.5V	-	0.1	10	μA	
		control pins					
		V _{CC} = 3.6 V; V _I = V _{CC} or GND	-	0.1	±1	μA	
		data pins; [3]					
		V _{CC} = 3.6 V; V _I = V _{CC}	-	0.5	1	μA	
		V _{CC} = 3.6 V; V _I = 0 V	-	0.1	-5	μA	
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 0 V to 4.5 V	-	0.1	±100	μA	
I _{BHL}	bus hold LOW current	data inputs; V _{CC} = 3 V; V _I = 0.8 V	75	130	-	μA	
I _{BHH}	bus hold HIGH current	data inputs; V _{CC} = 3 V; V _I = 2.0 V	-75	-140	-	μA	
I _{BHLO}	bus hold LOW overdrive current	data inputs; V _{CC} = 3.6 V; V _I = 0 V to 3.6 V [7]	500	-	-	μA	
I _{BHHO}	bus hold HIGH overdrive current	data inputs; V _{CC} = 3.6 V; V _I = 0 V to 3.6 V [7]	-500	-	-	μA	
I _{EX}	external current	output in HIGH-state when V _O > V _{CC} ; V _O = 5.5 V; V _{CC} = 3.0 V	-	10	125	μA	
I _{O(pu/pd)}	power-up/power-down output current	V _{CC} ≤ 1.2 V; V _O = 0.5 V to V _{CC} ; V _I = GND or V _{CC} ; n _{OE} = don't care	[8]	-	1	±100	μA
I _{OZ}	OFF-state output current	V _{CC} = 3.6 V; V _I = V _{IL} or V _{IH}					
		output HIGH-state; V _O = 3.0 V	-	0.5	5	μA	
		output LOW-state; V _O = 0.5 V	-	0.5	-5	μA	
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = GND or V _{CC} ; I _O = 0 A					
		outputs HIGH-state	-	0.07	0.1	mA	
		outputs LOW-state	-	5.1	7	mA	
		outputs disabled [5]	-	0.07	0.1	mA	
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 3 V to 3.6 V; one input at V _{CC} - 0.6 V; other inputs at V _{CC} or GND	[6]	-	0.04	0.4	mA
C _I	input capacitance	V _I = 0 V or V _{CC}	-	3	-	pF	
C _O	output capacitance	V _O = 0 V or V _{CC}	-	9	-	pF	

[1] All typical values for V_{CC} = 2.5 V ± 0.2 V are measured at V_{CC} = 2.5 V and T_{amb} = 25 °C.

All typical values for V_{CC} = 3.3 V ± 0.3 V are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

[2] For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

[3] Unused pins at V_{CC} or GND.

[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms.

From V_{CC} = 1.2 V to (2.5 ± 0.2) V a transition time of 100 μs is permitted. This parameter is valid for T_{amb} = 25 °C only.

[5] I_{CC} with outputs disabled is measured with outputs pulled to V_{CC} or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

[7] This is the bus hold overdrive current required to force the input to the opposite logic state.

[8] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms.

From V_{CC} = 1.2 V to (3.3 ± 0.3) V a transition time of 100 μs is permitted. This parameter is valid for T_{amb} = 25 °C only.

10. Dynamic characteristics

Table 7. Dynamic characteristics

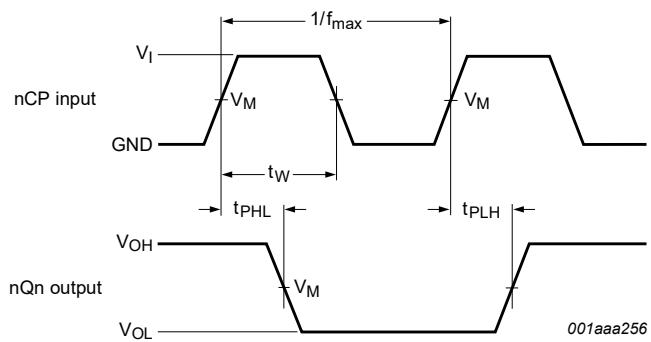
Voltages are referenced to GND (ground = 0 V); T_{amb} = -40 °C to +85 °C; for test circuit see Fig. 9.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$V_{CC} = 2.5\ V \pm 0.2\ V$						
t_{PLH}	LOW to HIGH propagation delay	nCP to nQn; see Fig. 6	1.0	4.4	7.0	ns
t_{PHL}	HIGH to LOW propagation delay	nCP to nQn; see Fig. 6	1.0	3.8	6.4	ns
t_{PZH}	OFF-state to HIGH propagation delay	\bar{OE} to nQn; see Fig. 8	1.5	4.6	7.5	ns
t_{PZL}	OFF-state to LOW propagation delay	\bar{OE} to nQn; see Fig. 8	1.0	2.8	4.6	ns
t_{PHZ}	HIGH to OFF-state propagation delay	\bar{OE} to nQn; see Fig. 8	1.5	3.5	5.5	ns
t_{PLZ}	LOW to OFF-state propagation delay	\bar{OE} to nQn; see Fig. 8	1.0	3.7	5.7	ns
t_{su}	set-up time	nDn to nCP HIGH; see Fig. 7	1.5	0.1	-	ns
		nDn to nCP LOW; see Fig. 7	2.0	0.5	-	ns
t_h	hold time	nDn to nCP HIGH; see Fig. 7	0.3	-0.5	-	ns
		nDn to nCP LOW; see Fig. 7	0.5	-0.1	-	ns
t_w	pulse width	nCP HIGH or LOW; see Fig. 6	1.5	-	-	ns
f_{max}	maximum frequency	nCP; see Fig. 6	150	-	-	MHz
$V_{CC} = 3.3\ V \pm 0.3\ V$						
t_{PLH}	LOW to HIGH propagation delay	nCP to nQn; see Fig. 6	1.0	3.2	5.0	ns
t_{PHL}	HIGH to LOW propagation delay	nCP to nQn; see Fig. 6	1.0	3.2	4.7	ns
t_{PZH}	OFF-state to HIGH propagation delay	\bar{OE} to nQn; see Fig. 8	1.0	3.4	5.6	ns
t_{PZL}	OFF-state to LOW propagation delay	\bar{OE} to nQn; see Fig. 8	0.5	2.3	3.7	ns
t_{PHZ}	HIGH to OFF-state propagation delay	\bar{OE} to nQn; see Fig. 8	1.5	3.7	5.4	ns
t_{PLZ}	LOW to OFF-state propagation delay	\bar{OE} to nQn; see Fig. 8	1.5	3.0	4.3	ns
t_{su}	set-up time	nDn to nCP HIGH or LOW; see Fig. 7	1.5	0.1	-	ns
t_h	hold time HIGH	nDn to nCP HIGH or LOW; see Fig. 7	0.5	0.1	-	ns
t_w	pulse width	nCP HIGH or LOW; see Fig. 6	1.5	-	-	ns
f_{max}	maximum frequency	nCP; see Fig. 6	150	-	-	MHz

[1] All typical values for $V_{CC} = 2.5\ V \pm 0.2\ V$ are measured at $V_{CC} = 2.5\ V$ and $T_{amb} = 25\ ^\circ C$.

All typical values for $V_{CC} = 3.3\ V \pm 0.3\ V$ are measured at $V_{CC} = 3.3\ V$ and $T_{amb} = 25\ ^\circ C$.

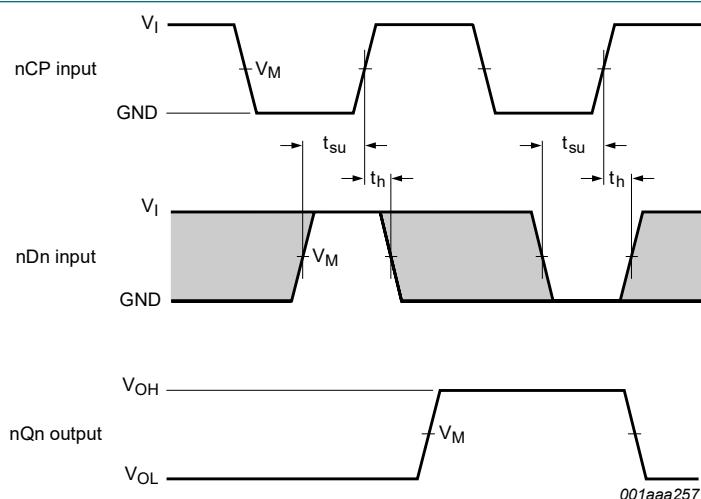
10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. Propagation delay clock input (nCP) to output (nQn), clock pulse (nCP) width and maximum clock frequency



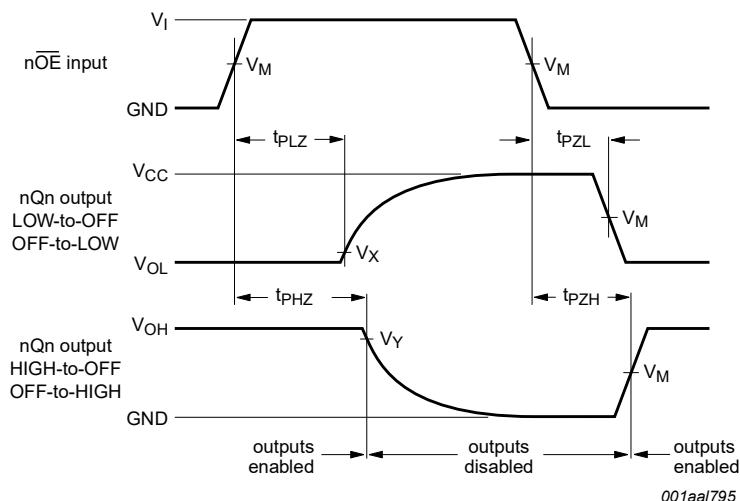
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 7. Set-up times and hold times from input (nDn) to clock (nCP)

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Measurement points are given in [Table 8](#).

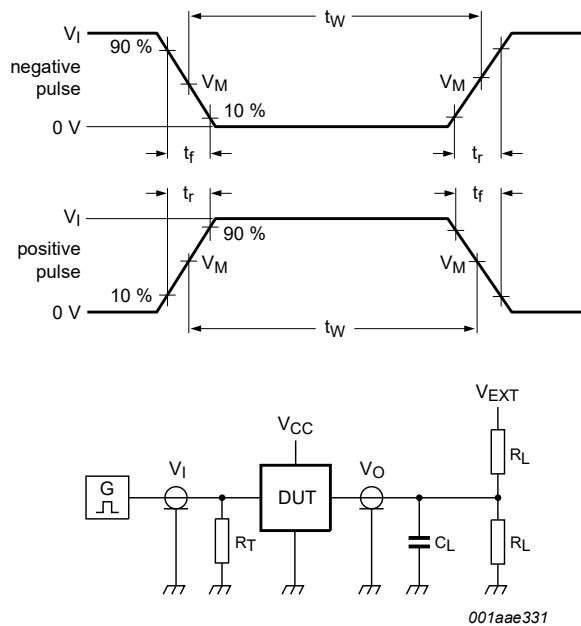
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 8. OFF-state to HIGH and LOW propagation delays and LOW and HIGH to OFF-state propagation delays

Table 8. Measurement points

V_{CC}	Input		Output		
	V_I	V_M	V_M	V_X	V_Y
$V_{CC} \leq 2.7\ V$	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15\ V$	$V_{OH} - 0.15\ V$
$V_{CC} \geq 3.0\ V$	$3.0\ V$	$1.5\ V$	$1.5\ V$	$V_{OL} + 0.3\ V$	$V_{OH} - 0.3\ V$

20-bit bus interface D-type flip-flop; positive-edge trigger with 30Ω termination resistors; 3-state



Test data is given in [Table 9](#).

Definitions test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

V_{EXT} = Test voltage for switching times.

Fig. 9. Test circuit for measuring switching times

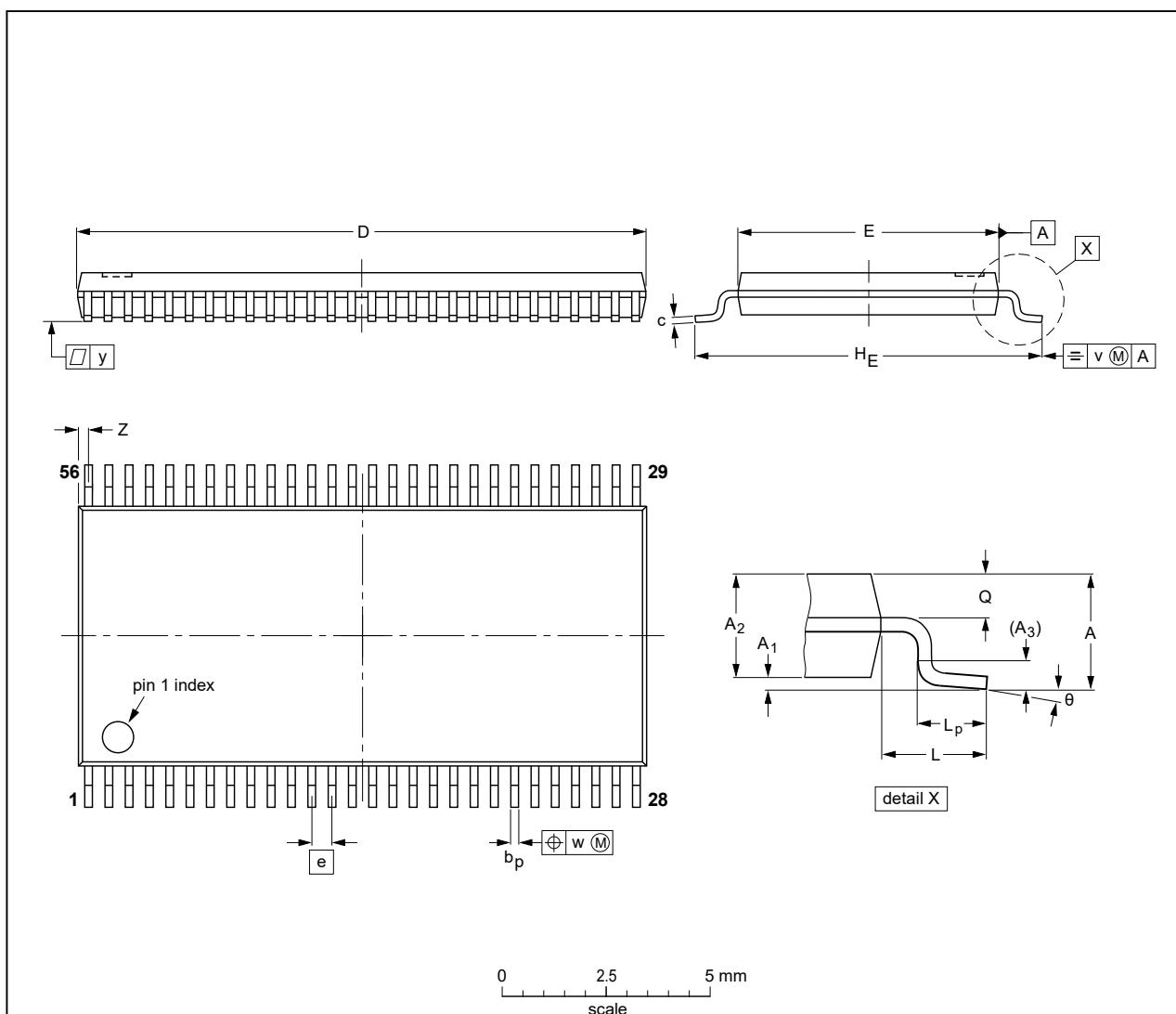
Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_I	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
3.0 V or V_{CC} whichever is less	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	GND	6 V or $V_{CC} \times 2$	open

11. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	z	θ
mm	1.2 0.05	0.15 0.85	1.05	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT364-1		MO-153				99-12-27 03-02-19

Fig. 10. Package outline SOT364-1 (TSSOP56)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVT162821 v.6	20240625	Product data sheet	-	74ALVT162821 v.5
Modifications:	<ul style="list-style-type: none"> Section 2: ESD specification updated according to the latest JEDEC standard. 			
74ALVT162821 v.5	20201019	Product data sheet	-	74ALVT162821 v.4
Modifications:	<ul style="list-style-type: none"> Type number 74ALVT162821DGG (SOT371-1 / SSOP56) removed. Section 1 and Section 2 updated. Table 4: Derating values for P_{tot} total power dissipation updated. 			
74ALVT162821 v.4	20180124	Product data sheet	-	74ALVT162821 v.3
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 			
74ALVT162821 v.3	19981002	Product data sheet	-	74ALVT162821 v.2
74ALVT162821 v.2	19980213	Product specification	-	74ALVT162821 v.1
74ALVT162821 v.1	19971117	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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