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- Typical V<sub>OLP</sub> (Output Ground Bounce)
  <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot) >2 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Inputs Accept Voltages to 5.5 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

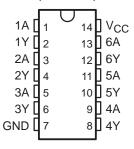
#### description

The SN54LVC14A hex Schmitt-trigger inverter is designed for 2.7-V to 3.6-V  $V_{CC}$  operation, and the SN74LVC14A hex Schmitt-trigger inverter is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

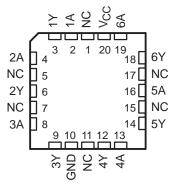
The devices contain six independent inverters, and perform the Boolean function  $Y = \overline{A}$ .

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

#### SN54LVC14A . . . J OR W PACKAGE SN74LVC14A . . . D, DB, DGV, OR PW PACKAGE (TOP VIEW)



## SN54LVC14 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

#### **ORDERING INFORMATION**

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	SOIC – D	Tube	SN74LVC14AD	LVC14A
	3010 - 0	Tape and reel	SN74LVC14ADR	LVC14A
–40°C to 85°C	SSOP – DB	Tape and reel	SN74LVC14ADBR	LC14A
	TSSOP - PW	Tape and reel	SN74LVC14APWR	LC14A
	TVSOP - DGV	Tape and reel	SN74LVC14ADGVR	LC14A
	CDIP – J	Tube	SNJ54LVC14AJ	SNJ54LVC14AJ
–55°C to 125°C	CFP – W	Tube	SNJ54LVC14AW	SNJ54LVC14AW
	LCCC – FK	Tube	SNJ54LVC14AFK	SNJ54LVC14AFK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



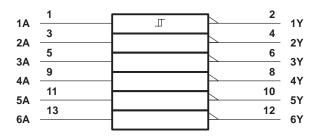
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## FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
Н	L
L	Н

#### logic symbol†



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, DGV, J, PW, and W packages.

#### logic diagram, each inverter (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>		0.5 V to 6.5 V
Input voltage range, V <sub>I</sub> (see Note 1)		–0.5 V to 6.5 V
Output voltage range, V <sub>O</sub> (see Notes 1 and 2)		$V \text{ to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{IK}(V_I < 0)$		–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)		−50 mA
Continuous output current, IO		±50 mA
Continuous current through V <sub>CC</sub> or GND		±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 3):	: D package	86°C/W
	DB package	96°C/W
	DGV package	127°C/W
	PW package	113°C/W
Storage temperature range, T <sub>stq</sub>		. −65°C to 150°C

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
- 3. The package thermal impedance is calculated in accordance with JESD 51-7.



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#### recommended operating conditions (see Note 4)

			SN54LVC14A		SN74L\	UNIT		
			MIN	MAX	MIN	MAX	UNIT	
\/aa	Supply voltage	Operating	2	3.6	1.65	3.6	V	
Vcc	Supply voltage	Data retention only	1.5		1.5		V	
٧ı	Input voltage		0	5.5	0	5.5	V	
VO	Output voltage		0	Vcc	0	VCC	V	
		V <sub>CC</sub> = 1.65 V				-4	mA	
	High-level output current	V <sub>CC</sub> = 2.3 V				-8		
ЮН		V <sub>CC</sub> = 2.7 V		-12		-12		
		V <sub>CC</sub> = 3 V		-24		-24		
		V <sub>CC</sub> = 1.65 V				4		
	Low-level output current	V <sub>CC</sub> = 2.3 V				8	mA	
IOL		V <sub>CC</sub> = 2.7 V		12		12		
		V <sub>CC</sub> = 3 V		24		24		
T <sub>A</sub>	Operating free-air temperature		-55	125	-40	85	°C	

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# SN54LVC14A, SN74LVC14A HEX SCHMITT-TRIGGER INVERTERS

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#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS	l .,	SN5	4LVC14A	SN7	4LVC14A	UNIT
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP <sup>†</sup> MAX	MIN	TYP <sup>†</sup> MAX	UNII
V <sub>T+</sub>		2.7 V	0.8	2	0.8	2	
Positive-going		3 V	0.8	2	0.8	2	V
threshold		3.6 V	0.8	2	0.8	2	
V <sub>T</sub> _		2.7 V	0.4	1.4	0.4	1.4	
Negative-going		3 V	0.6	1.5	0.6	1.5	V
threshold		3.6 V	0.8	1.8	0.8	1.8	
ΔVΤ		2.7 V	0.3	1.1	0.3	1.1	
Hysteresis		3 V	0.3	1.2	0.3	1.2	V
$(V_{T+} - V_{T-})$		3.6 V	0.3	1.2	0.3	1.2	
	Jan - 100 m	1.65 V to 3.6 V			V <sub>CC</sub> -0.2		
	ΙΟΗ = -100 μΑ	2.7 V to 3.6 V	V <sub>CC</sub> -0.2				٧
	I <sub>OH</sub> = -4 mA	1.65 V			1.2		
Voн	I <sub>OH</sub> = -8 mA	2.3 V			1.7		
	I <sub>OH</sub> = -12 mA	2.7 V	2.2		2.2		
		3 V	2.4		2.4		
	I <sub>OH</sub> = -24 mA	3 V	2.2		2.2		
	lo 100 uA	1.65 V to 3.6 V				0.2	
	I <sub>OL</sub> = 100 μA	2.7 V to 3.6 V		0.2			
Voi	I <sub>OL</sub> = 4 mA	1.65 V				0.45	V
VOL	I <sub>OL</sub> = 8 mA	2.3 V				0.7	·
	I <sub>OL</sub> = 12 mA	2.7 V		0.4		0.4	
	I <sub>OL</sub> = 24 mA	3 V		0.55		0.55	.
ΙĮ	V <sub>I</sub> = 5.5 V or GND	3.6 V		±5		±5	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		10		10	μΑ
ΔlCC	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V		500		500	μА
C <sub>i</sub>	$V_I = V_{CC}$ or GND	3.3 V		5		5	pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

#### switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

			SN54LVC14A				
PARAMETER	FROM (INPUT)	1 1/00 = 27 1/1 00		V <sub>CC</sub> = 2.7 V		3.3 V 3 V	UNIT
			MIN	MAX	MIN	MAX	
<sup>t</sup> pd	A	Y		7.5	1	6.4	ns



### SN54LVC14A, SN74LVC14A HEX SCHMITT-TRIGGER INVERTERS

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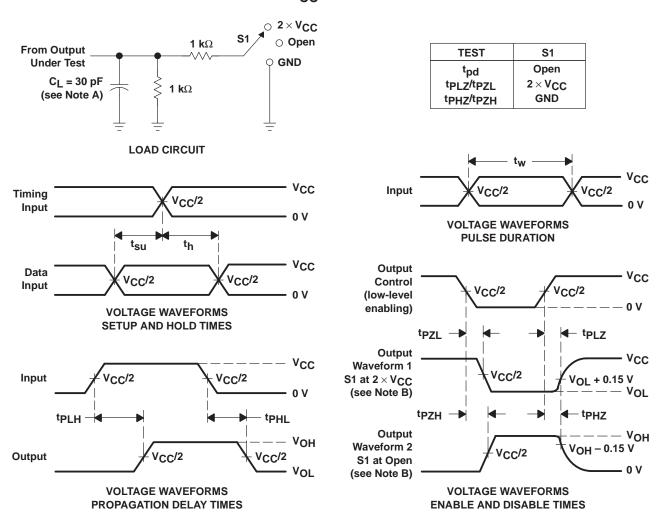
# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER		TO (OUTPUT)	SN74LVC14A					
	FROM (INPUT)		V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V ± 0.2 V	V <sub>CC</sub> = 2.7 V	V <sub>CC</sub> = 3.3 V ± 0.3 V	UNIT	
			TYP	MIN MAX	MIN MAX	MIN MAX		
<sup>t</sup> pd	А	Y	13.7	7.8	7.5	1 6.4	ns	
<sup>t</sup> sk(o)						1	ns	

### operating characteristics, $T_A = 25^{\circ}C$

PARAMETER		TEST	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT
	FARAWETER	CONDITIONS TYP TYP TYP		TYP	UNIT	
C <sub>pd</sub>	Power dissipation capacitance per inverter	f = 10 MHz	11	12	15	pF

## PARAMETER MEASUREMENT INFORMATION V<sub>CC</sub> = 1.8 V



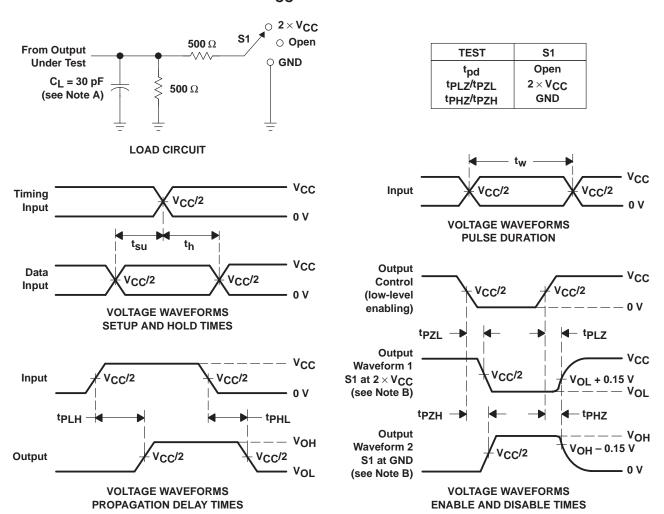
NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_Q = 50 \Omega$ ,  $t_f \leq 2$  ns.  $t_f \leq 2$  ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



## PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

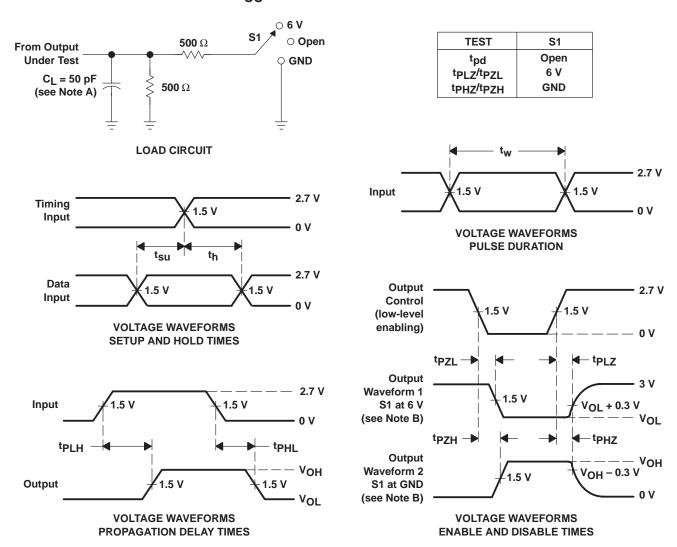


NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O$  = 50  $\Omega_{\rm i}$   $t_f$   $\leq$  2 ns.  $t_f$   $\leq$  2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

#### PARAMETER MEASUREMENT INFORMATION $V_{CC}$ = 2.7 V AND 3.3 V $\pm$ 0.3 V



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzi and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



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