WMS7130 / 7131

NON-VOLATILE DIGITAL POTENTIOMETERS

WITH UP/DOWN (3-WIRE) INTERFACE,

10KOHM, 50KOHM, 100KOHM RESISTANCE

32 TAPS

WITHOUT / WITH OUTPUT BUFFER

Publication Release Date: July 2003
Revision 1.0

1. GENERAL DESCRIPTION

The WMS7130/7131 is a single channel 32-tap non-volatile linear digital potentiometer available in 10KΩ, 50KΩ and 100KΩ resistance. The device consists of Up/Down serial interface, tap register, decoder, resistor array, wiper switches, NV memory and control logics.

The WMS7130 device can be configured as a two-terminal variable resistor or a three-terminal voltage divider without an output buffer, but the WMS7131 device, which has a built-in output buffer, can only be configured as a three-terminal voltage divider. Both devices can be used in a wide variety of applications.

The output of the potentiometer is determined by its wiper position, which varies linearly between its end terminals, R_A/V_A and R_B/V_B. The wiper position, $R_w/V_{w,}$ is controlled by Up/Down serial interface ($\overline{CS}$, $\overline{INC}$ and U/$\overline{D}$) through the Tap Register (TR). In addition, the wiper position can also be stored into a non-volatile memory location (NVMEM0), which is then automatically recalled upon power up.

2. FEATURES

- Drop-in replacement for many popular parts
- Single linear-taper channel
- 32 taps
- 10K, 50K and 100K end-to-end resistance
- V_{SS} to V_{DD} terminal voltages
- Automatic recall of wiper position when power-on
- Potentiometer control through Up/Down (3-wire) serial interface
- Endurance 100,000 cycles
- Data retention 100 years
- Package options:
  - 8-pin PDIP, SOIC or MSOP
- Industrial temperature range: -40° to 85°C
- Single supply operation : 2.7V to 5.5V

3. BLOCK DIAGRAM

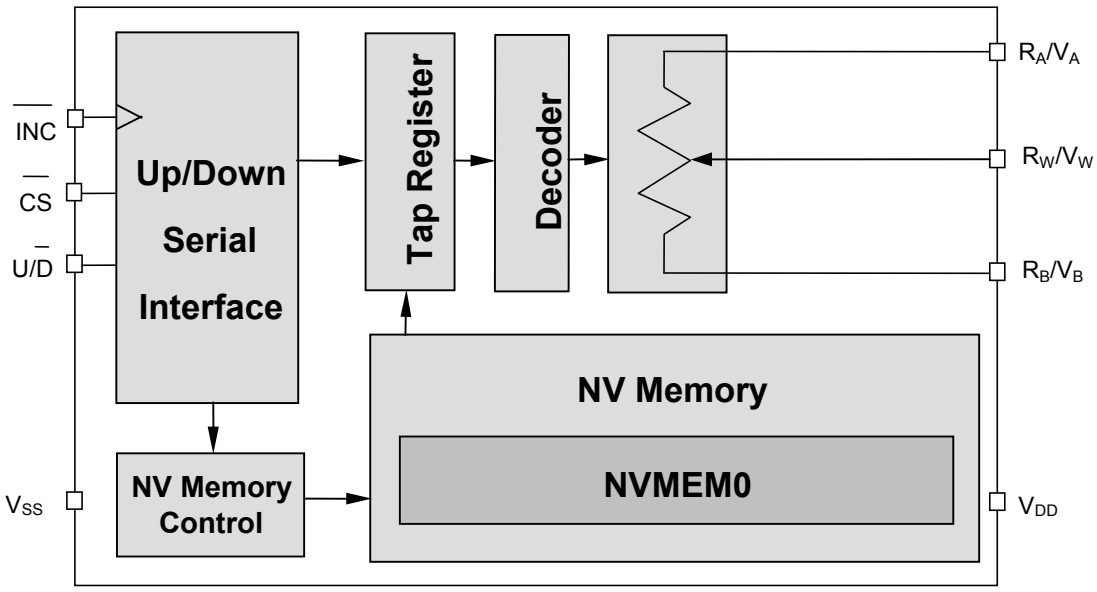

FIGURE 1 – WMS7130 BLOCK DIAGRAM (Rheostat/Divider Mode)

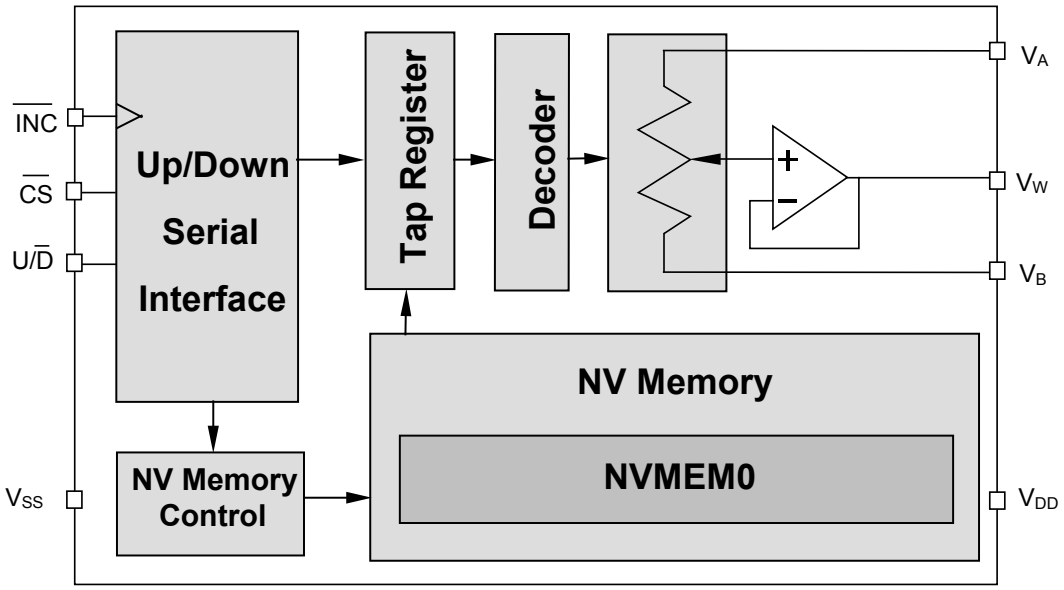

FIGURE 2 – WMS7131 BLOCK DIAGRAM (Divider Mode)

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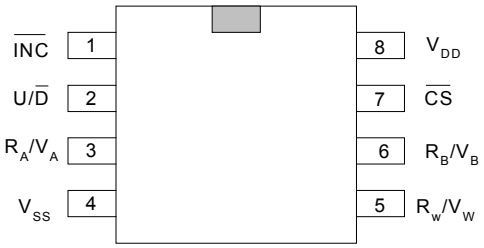
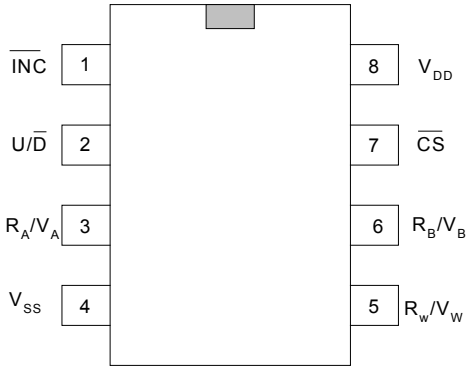
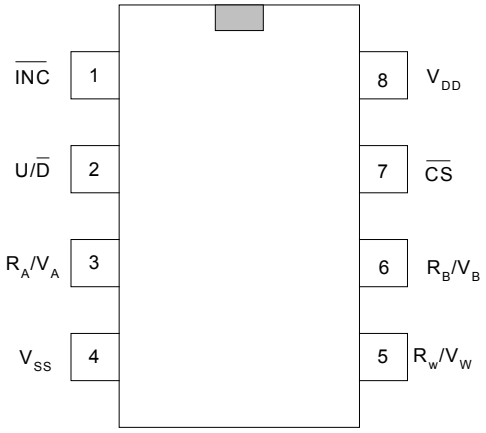
5. PIN CONFIGURATION



8-MSOP



8-SOIC



8-PDIP

6. PIN DESCRIPTION

TABLE 1 – PIN DESCRIPTION

Pin Name	Description
$\overline{CS}$	**Chip Select:** When $\overline{CS}$ is LOW, the device is enabled. When $\overline{CS}$ is HIGH, the part is deselected and is in standby mode
U/$\overline{D}$	**Up/Down Control:** HIGH state enables the wiper to move towards the R_A / V_A terminal, while LOW state implies the wiper moves towards the R_B / V_B terminal
$\overline{INC}$	**Increment Control:** When $\overline{CS}$ is LOW, a HIGH-LOW transition on $\overline{INC}$ will move the wiper one increment either up or down based on the U/$\overline{D}$ input
R_A/V_A	**High terminal** of the device
R_B/V_B	**Low terminal** of the device
R_W/V_W	**Wiper Terminal:** Output of the resistor array is determined by the $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$ inputs
V_{SS}	Ground pin, logic ground reference
V_{DD}	Power Supply

Notes: The terminology of high and low terminals above references to the relative position of the terminal with respect to the wiper moving direction and not the voltage potential of the terminal.

7. FUNCTIONAL DESCRIPTION

7.1. RHEOSTAT AND DIVIDER OPERATIONS

The WMS7130 device can operate as either a two-terminal variable resistor or a three-terminal voltage divider without an output buffer. However, the WMS7131 can only operate in a three-terminal voltage divider with an output buffer.

7.1.1. Rheostat Configuration

In the rheostat mode, the WMS7130 can be configured as a two-terminal resistive element, where one terminal is connected to one end of the resistor (R_A or R_B) and the other terminal is the wiper (R_W). The moving direction of the wiper depends upon the setting of U/$\overline{D}$ control signal. When the U/$\overline{D}$ is set to Up, then the wiper moves towards R_A. Conversely, when the U/$\overline{D}$ is set to Down, then the wiper moves towards R_B. The wiper movement to either direction is controlled by toggling the $\overline{INC}$ signal from HIGH to LOW.

This configuration controls the resistance between the wiper and either end. The wiper resistance can be adjusted by either changing the wiper position or loading a stored wiper position value from NVMEM0 upon power up.

7.1.2. Divider Configuration

Additionally, the WMS7130 can also be configured as a voltage divider. With an input voltage applied to one end (usually V_A), the ground is connected to the other end (usually V_B). These input voltages cannot exceed the V_{DD} level or go below the V_{SS} level. The voltage on the wiper, V_W, is proportional to the wiper position with respect to the voltage difference between V_A and V_B. The moving direction of the wiper depends upon the setting of the U/$\overline{D}$ control signal. When the U/$\overline{D}$ is set to Up, then the wiper moves towards V_A. Conversely, when the U/$\overline{D}$ is set to Down, then the wiper moves towards V_B. The wiper movement to either direction is controlled by toggling the $\overline{INC}$ signal from HIGH to LOW.

Nevertheless, the WMS7131 can only be configured as a voltage divider and operate similarly as the WMS7130 device. The only difference is WMS7131 has an output buffer, but WMS7130 doesn't have.

Besides, the resistance cannot be directly measured in this configuration.

7.2. NON-VOLATILE MEMORY (NVMEM0)

The WMS7130/7131 has one NVMEM0 location available for storing the current wiper position via the Up/Down serial interface. This stored value is automatically recalled and loaded into the tap register upon power up.

7.3. SERIAL DATA INTERFACE

The WMS7130/7131 device has a 3-wire Up/Down Serial Interface consisting of $\overline{CS}$, $\overline{INC}$ and U/$\overline{D}$ control signals. The key features of this interface include:

- Enabling the device
- Determining the moving direction of the wiper
- Increment/Decrement operation on the wiper
- Non-volatile storage of the present wiper position into the NVMEM0 for automatic recall at power up
- Entering into the standby mode

7.4. OPERATION OVERVIEW

The wiper position can be changed either up or down by operating the $\overline{CS}$, U/$\overline{D}$ and $\overline{INC}$ control signals.

When $\overline{CS}$ is LOW, the device is selected and the wiper can be moved by toggling the $\overline{INC}$. As a result, the wiper moves up when U/$\overline{D}$ is HIGH and moves down when U/$\overline{D}$ is LOW. The status of the U/$\overline{D}$ can be changed even though the $\overline{CS}$ remains LOW. This allows the system to enable the device and then move the wiper position either up or down until the desired position is reached.

When the wiper is already at the lowest position, further Down operation won't change the wiper position. Similarly, when the wiper is at the highest position, further Up operation won't change the wiper position too.

The current wiper position can be automatically stored into the NVMEM0 each time the $\overline{CS}$ goes from LOW to HIGH while the $\overline{INC}$ remains HIGH. Adversely, if the $\overline{INC}$ is LOW when the $\overline{CS}$ goes HIGH, the wiper position cannot be stored. Meanwhile, the NVMEM0 content is automatically loaded into the wiper during power on.

When the $\overline{CS}$ is held HIGH, the device enters into Standby mode and the wiper position cannot be changed. Changing the $\overline{CS}$ to LOW exits the Standby mode and enables the device again.

The operating modes of Up/Down interface are summarized in the table below:

$\overline{CS}$	U/$\overline{D}$	$\overline{INC}$	Operation
LOW	HIGH	↓ HIGH to LOW	Move Wiper toward R_A/V_A
LOW	LOW	↓ HIGH to LOW	Move Wiper toward R_B/V_B
↑ LOW to HIGH	x	HIGH	Store Current Wiper Position
↑ LOW to HIGH	x	LOW	No Store, Return to Standby
HIGH	x	x	Standby

Note: x means don't care

8. TIMING DIAGRAMS

Conditions: V_{DD} = +2.7V to 5.5V, $V_A = V_{DD}$, V_B = 0V, T = 25°C

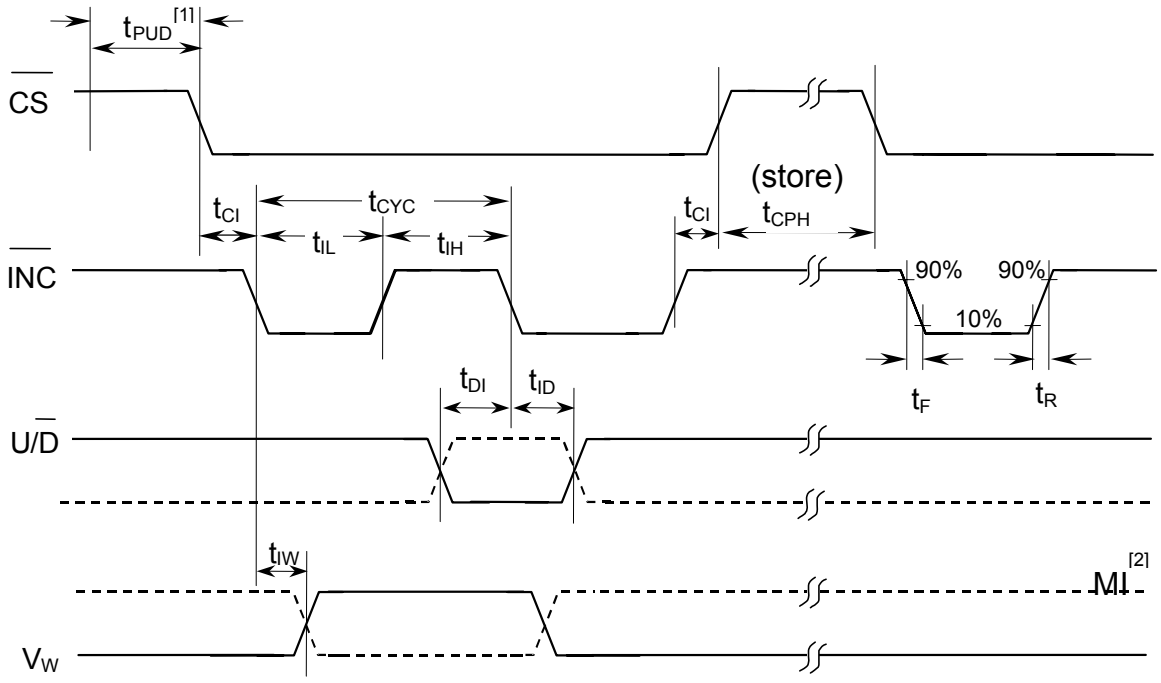


FIGURE 3 –WMS7130/1 TIMING DIAGRAM

Note:

[1] This only applies to the Power-Up sequence.

[2] MI in the AC Timing diagram (Figure 3) refers to the minimum incremental change in the wiper output due to a change in the wiper position.

TABLE 10 – TIMING PARAMETERS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
$\overline{CS}$ to $\overline{INC}$ Setup	t_{CI}	100		ns
U/$\overline{D}$ to $\overline{INC}$ Setup	t_{DI}	50		ns
U/$\overline{D}$ to $\overline{INC}$ Hold	t_{ID}	100		ns
$\overline{INC}$ LOW Period	t_{IL}	250		ns
$\overline{INC}$ HIGH Period	t_{IH}	250		ns
$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	t_{IC}	1		µs
$\overline{CS}$ Deselect Time (NO STORE)	t_{CPH}	100		ns
$\overline{CS}$ Deselect Time (STORE)	t_{CPH}	15 (2.7V) 30 (5.5V)		ms
$\overline{INC}$ to Wiper Change	t_{IW}		5	µs
$\overline{INC}$ Cycle Time	t_{CYC}	1		µs
$\overline{INC}$ Input Rise and Fall Time	t_R, t_F		500	µs
Power-Up Delay	t_{PUD}		1	ms
V_{CC} Power-Up rate	t_R V_{CC}	0.2 (13ms 0-2.7V)	50 (54µs 0-2.7V)	V/ms

9. ABSOLUTE MAXIMUM RATINGS & OPERATING CONDITIONS

TABLE 11 – ABSOLUTE MAXIMUM RATINGS (PACKAGED PARTS) [1]

Conditions	Values
Junction temperature	150ºC
Storage temperature	-65º to +150ºC
Voltage applied to any pad	(V_{ss} – 0.3V) to (V_{DD} + 0.3V)
Lead temperature (soldering – 10 seconds)	300ºC
V_{SS} – V_{DD}	-0.3 to 7.0V

TABLE 12 – OPERATING CONDITIONS (PACKAGED PARTS)

Conditions	Values
Industrial operating temperature	-40ºC to +85ºC
Supply voltage (V_{DD})	+2.7V to +5.5V
Ground voltage (V_{SS})	0V

[1] Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device performance and reliability. Functional operation is not implied at these conditions.

10. ELECTRICAL CHARACTERISTICS

TABLE 12 – ELECTRICAL CHARACTERISTICS (Packaged parts)

PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONDS [5]
Rheostat Mode						
Nominal Resistance	R	-20		+20	%	T=25ºC, Wiper open
Different Non Linearity [2]	R-DNL	-1	±0.2	+1	LSB	[6]
Integral Non Linearity [2]	R-INL	-1	±0.4	+1	LSB	[6]
Tempo [1]	$\Delta R_{AB}/\Delta T$		300		ppm/°C	
Wiper Resistance [2]	R_W		50		Ω	V_{DD}=5V, I=V_{DD}/R_{Total} [7]
			80		Ω	V_{DD}=2.7V, I=V_{DD}/R_{Total} [7]
Wiper Current	I_W	-1		1	mA	
Divider Mode						
Resolution	N	8			Bits	
Different Non Linearity [2]	DNL	-1	±0.4	+1	LSB	
Integral Non Linearity [2]	INL	-1	±0.4	+1	LSB	
Temperature Coefficient [1]	$\Delta W/\Delta T$		+20		ppm/°C	Wiper at center
Full Scale Error	V_{FSE}	-1		0	LSB	Wiper at highest position
Zero Scale Error	V_{ZSE}	0		1	LSB	Wiper at lowest position
Resistor Terminal						
Voltage Range	V_A, V_B, V_W	V_{SS}		V_{DD}	V	
Terminal Capacitance [1]	C_A, C_B		30		pF	
Wiper Capacitance [1]			30		pF	
Dynamic Characteristics [1]						
Bandwidth –3dB	BW_{10K}		1.5		MHz	V_{DD}=5V, B =VSS
	BW_{50K}		300		KHz	Wiper at center
	BW_{100K}		200		KHz	
Analog Output (Buffer enables)						
Amp Output Current	I_{OUT}	3			mA	V_O=1/2 scale
Amp Output Resistance	Rout		1	10	Ω	I_L = 100uA
Total Harmonic Distortion [1]	THD			0.08	%	A =2.5V, V_{DD}=5V, f=1kHz, V_{IN}=1V_{RMS}
Digital Inputs/Outputs						
Input High Voltage	V_{IH}	0.7xV_{DD}			V	
Input Low Voltage	V_{IL}			0.3xV_{DD}	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL}=2mA

TABLE 12 – ELECTRICAL CHARACTERISTICS (Packaged parts) – Cont'd

PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONDS [5]
Input Leakage Current	I_{LI}	-1		+1	uA	$\overline{CS}$=V_{DD},Vin=Vss ~ V_{DD}
Output Leakage Current	I_{Lo}	-1		+1	uA	$\overline{CS}$=V_{DD},Vin=V_{SS} ~ V_{DD}
Input Capacitance [1]	C_{IN}		25		pF	V_{DD}=5V, fc = 1Mhz
Output Capacitance [1]	C_{OUT}		25		pF	V_{DD}=5V, fc = 1Mhz
Power Requirements						
Operating Voltage	V_{DD}	2.7		5.5	V	
Operating Current	I_{DDR}, I_{DDW}		1	2	mA	All operations
Standby Current	I_{SA} [3]		0.5	1	mA	Buffer = ON $\overline{CS}$ = HIGH, no load
	I_{SB} [4]		0.1	1	uA	Buffer = OFF $\overline{CS}$ = HIGH, no load
Power Supply Rejection Ratio	PSRR			1	LSB/V	V_{DD}=5V±10%, Wiper at center

Notes:

[1] Not subject to production test.

[2] LSB = (R_A/V_A – R_B/V_B) / (T - 1); DNL = (V_i - V_{i+1}) / LSB + 1 (if increment) or = (V_i - V_{i+1}) / LSB - 1 (if decrement); INL = (V_i - i*LSB) / LSB; where i = [0, (T -1)] and T = # of taps of the device.

[3] WMS7131 only.

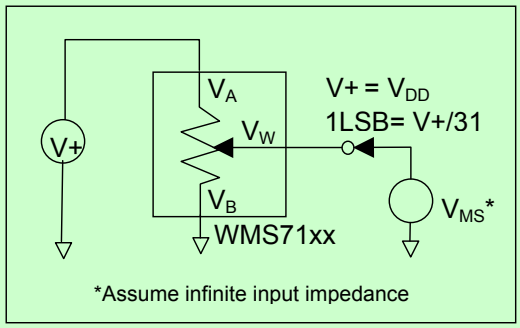
[4] WMS7130 only.

[5] Conditions: V_{CC} = 2.7 to 5.5V, T = 25ºC and timing measured at 50% level, unless stated.

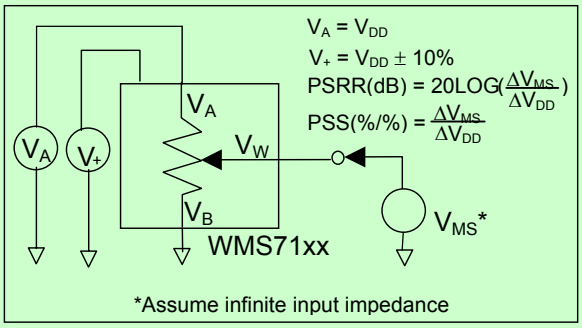
[6] Only guarantee by design.

[7] R_{total} = end-to-end resistance.

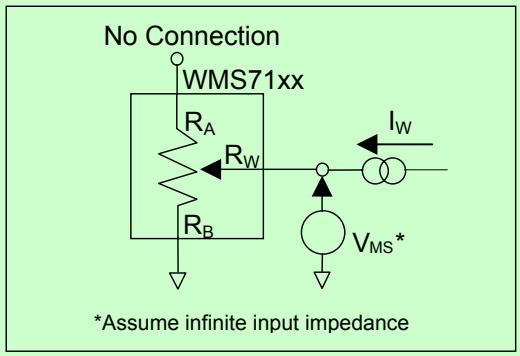
10.1 TEST CIRCUITS



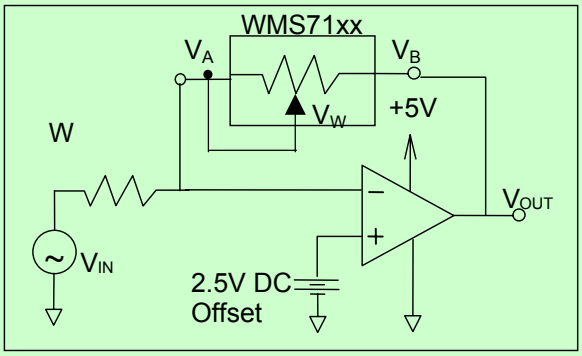
Potentiometer divider nonlinearity error test circuit (INL, DNL)



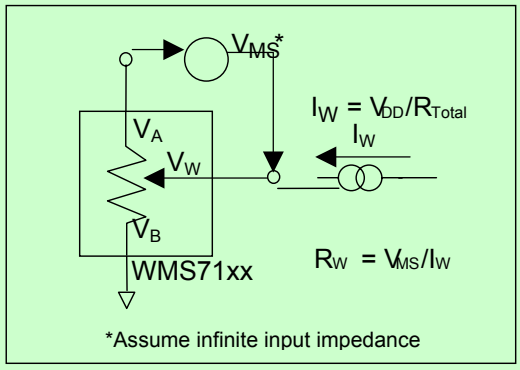
Power supply sensitivity test circuit (PSS, PSRR)



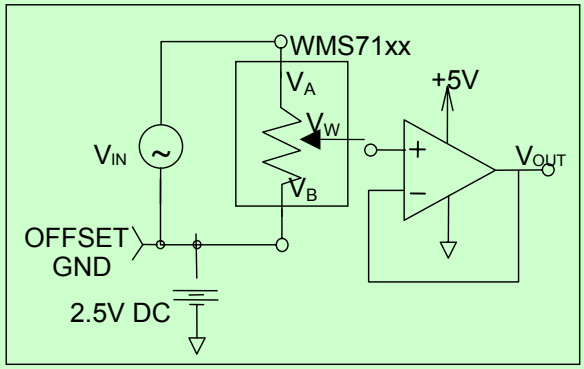
Resistor position nonlinearity error test circuit (Rheostat Operation: R-INL, R-DNL)



Capacitance test circuit



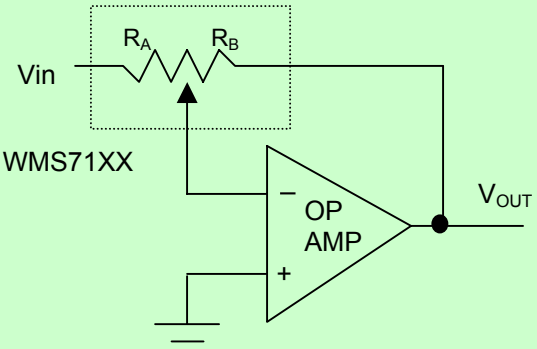
Wiper resistance test circuit



Gain *vs.* frequency test circuit

FIGURE 4 – TEST CIRCUITS

11. TYPICAL APPLICATION CIRCUITS



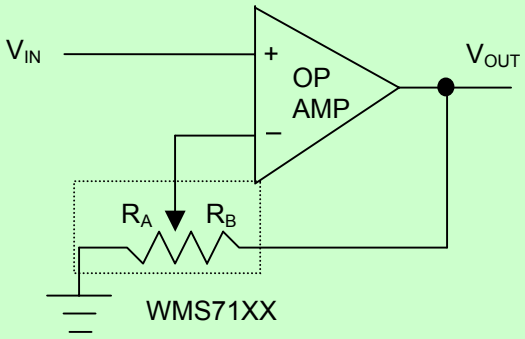
$$V_{OUT} = - V_{IN} \frac{R_B}{R_A}$$

$$R_A = \frac{R_{AB}\ (32-W)}{32}, \quad R_B = \frac{R_{AB}*W}{32}$$

R_{AB} = Total resistance of potentiometer

W = Wiper setting for WMS71XX

FIGURE 5 – PROGRAMMABLE INVERTING GAIN AMPLIFIER USING THE WMS7130/7131



$$V_{OUT} = V_{IN} \left(1+\frac{R_B}{R_A}\right)$$

$$R_A = \frac{R_{AB}\ (32-W)}{32}, \quad R_B = \frac{R_{AB}*W}{32}$$

R_{AB} = Total resistance of potentiometer

W = Wiper setting for WMS71XX

FIGURE 6 – PROGRAMMABLE NON-INVERTING GAIN AMPLIFIER USING THE WMS7130/7131

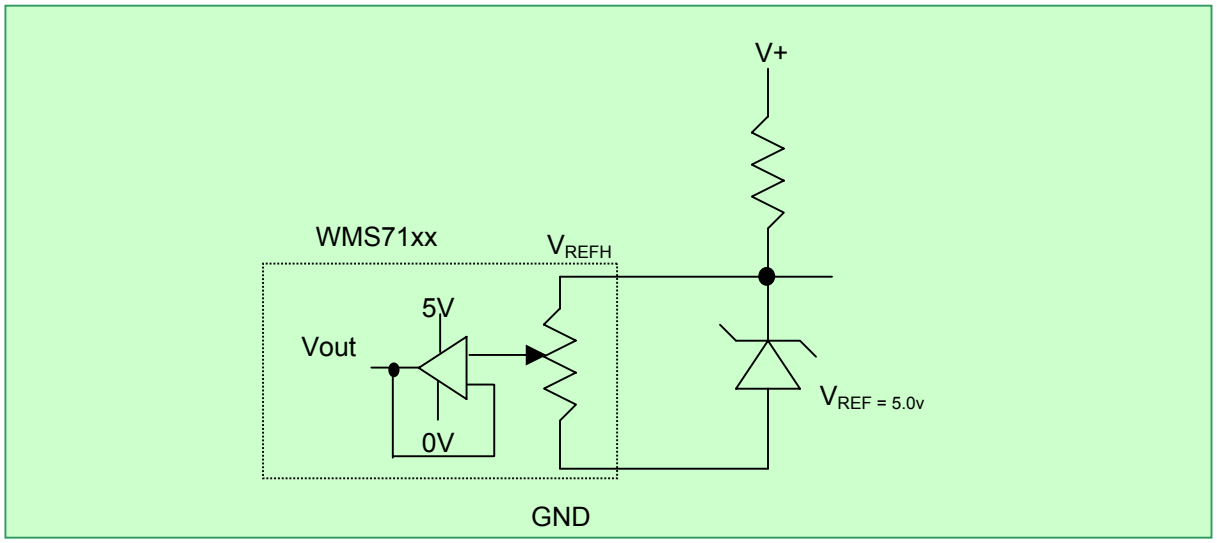


FIGURE 7 – WMS7131 TRIMMING VOLTAGE REFERENCE

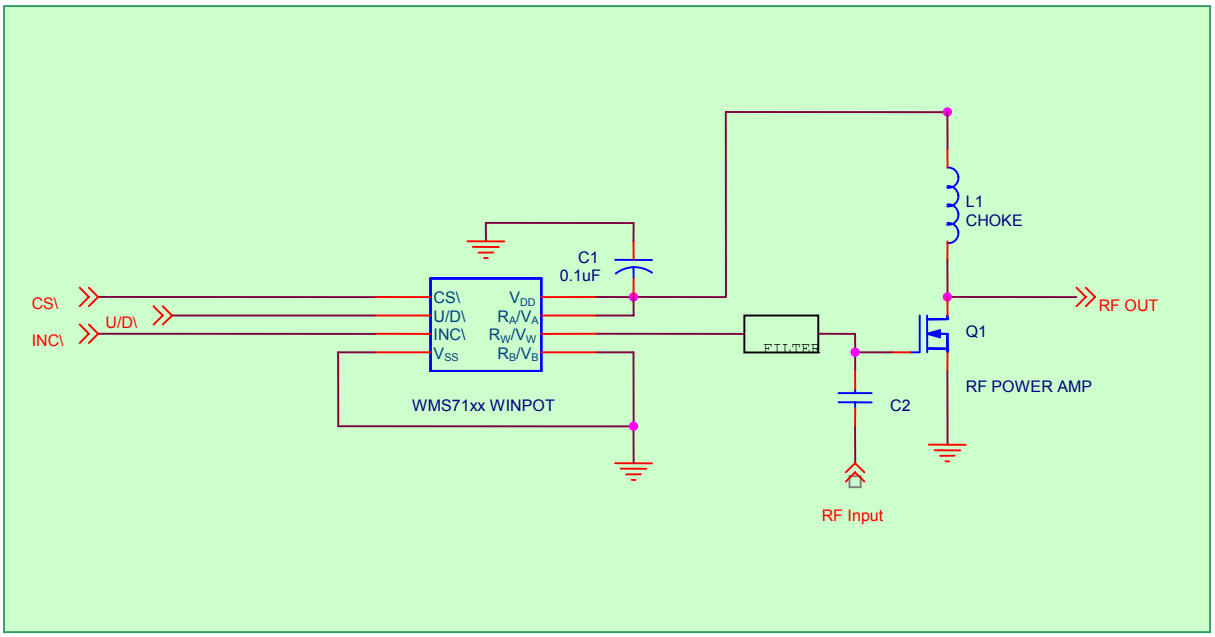


FIGURE 8 – WMS7131 RF AMP CONTROL

11.1. LAYOUT CONSIDERATIONS

Use a 0.1μF bypass capacitor as close as possible to the V_{DD} pin. This is recommended for best performance. Often this can be done by placing the surface mount capacitor on the bottom side of the PC board, directly between the V_{DD} and V_{SS} pins. Care should be taken to separate the analog and digital traces. Sensitive traces should not run under the device or close to the bypass capacitors.

A dedicated plane for analog ground helps in reducing ground noise for sensitive analog signals.

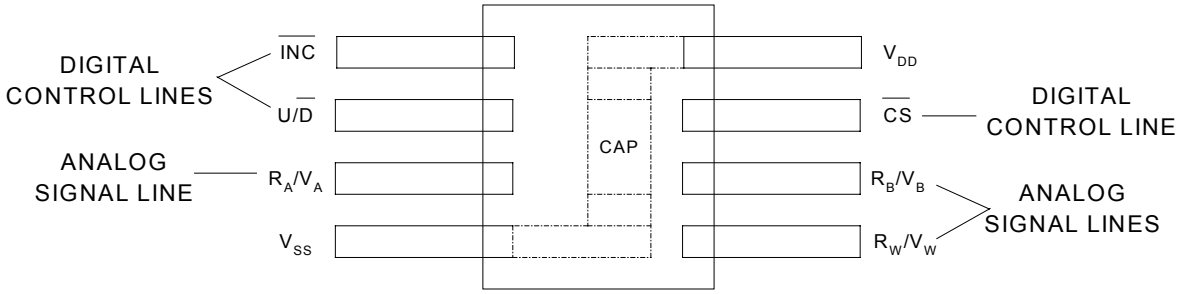
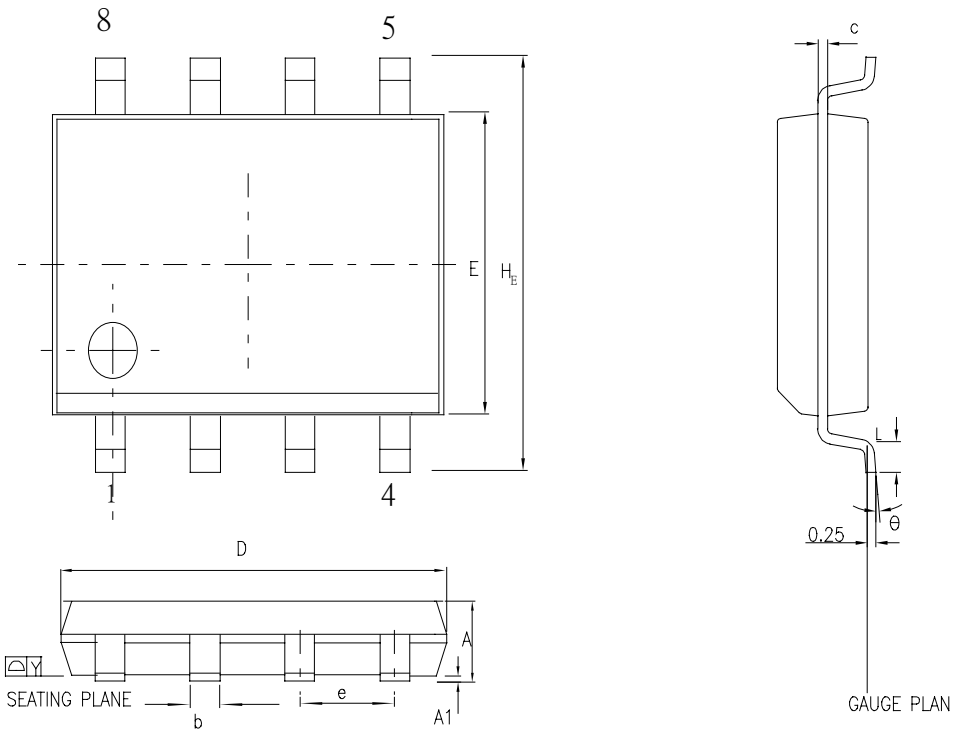


FIGURE 9 – WMS7130/7131 LAYOUT

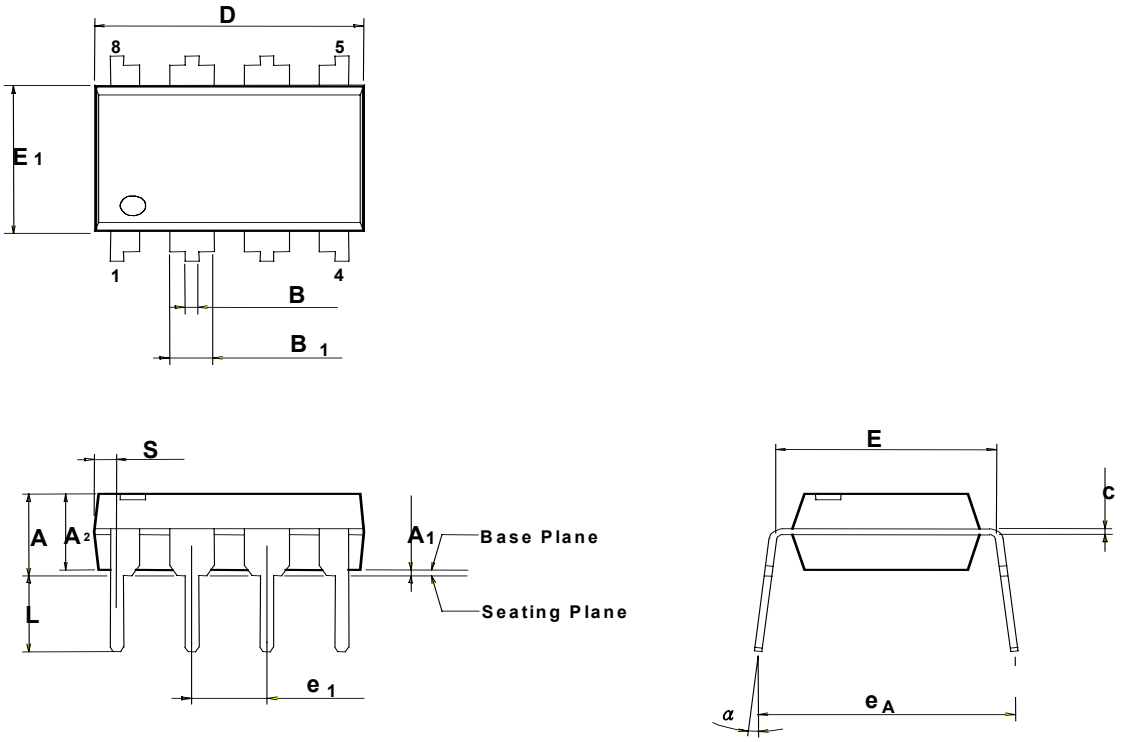
12. PACKAGE DRAWINGS AND DIMENSIONS



Control demensions are in milmeters .

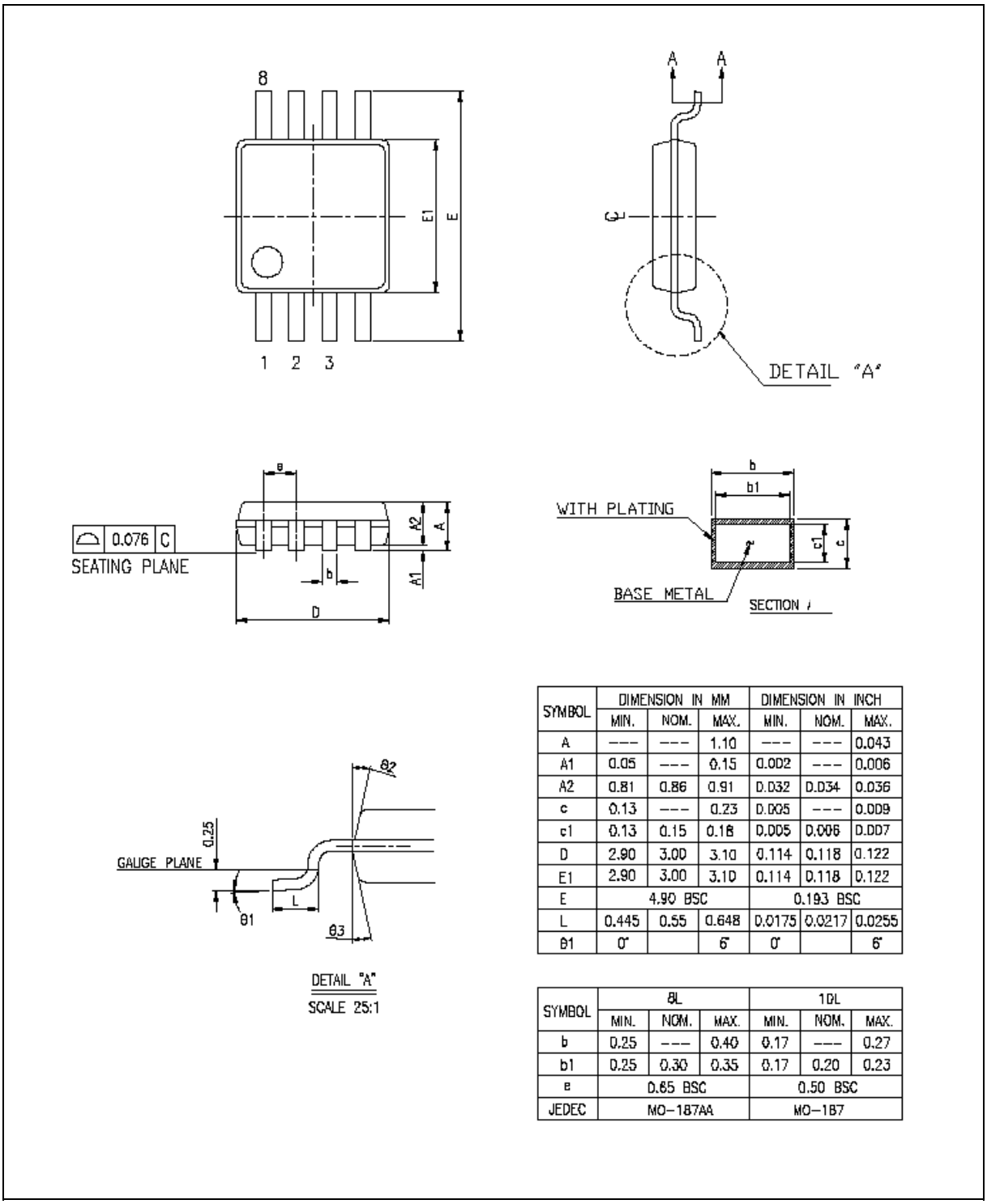
SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
E	3.80	4.00	0.150	0.157
D	4.80	5.00	0.188	0.196
e	1.27 BSC		0.050 BSC	
H_E	5.80	6.20	0.228	0.244
Y	—	0.10	—	0.004
L	0.40	1.27	0.016	0.050
θ	0	10	0	10

FIGURE 10: 8L 150MIL SOIC



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.175	—	—	4.45
A_1	0.010	—	—	0.25	—	—
A_2	0.125	0.130	0.135	3.18	3.30	3.43
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.058	0.060	0.064	1.47	1.52	1.63
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	0.360	0.380	—	9.14	9.65
E	0.290	0.300	0.310	7.37	7.62	7.87
E_1	0.245	0.250	0.255	6.22	6.35	6.48
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
α	0	—	15	0	—	15
e_A	0.335	0.355	0.375	8.51	9.02	9.53
S	—	—	0.045	—	—	1.14

FIGURE 11: 8L 300MIL PDIP



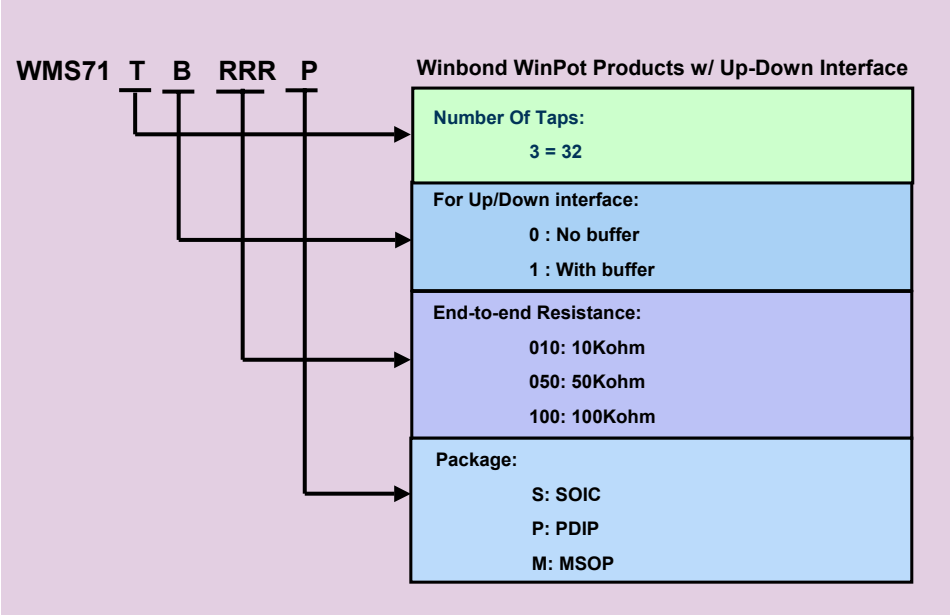
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.10	---	---	0.043
A1	0.05	---	0.15	0.002	---	0.006
A2	0.81	0.86	0.91	0.032	0.034	0.036
c	0.13	---	0.23	0.005	---	0.009
c1	0.13	0.15	0.18	0.005	0.006	0.007
D	2.90	3.00	3.10	0.114	0.118	0.122
E1	2.90	3.00	3.10	0.114	0.118	0.122
E	4.90 BSC			0.193 BSC		
L	0.445	0.55	0.648	0.0175	0.0217	0.0255
θ1	0°		6°	0°		6°

SYMBOL	8L			10L		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.25	---	0.40	0.17	---	0.27
b1	0.25	0.30	0.35	0.17	0.20	0.23
e	0.65 BSC			0.50 BSC		
JEDEC	MO-187AA			MO-187		

FIGURE 12: 8L 3MM MSOP

13. ORDERING INFORMATION

Winbond's WinPot Part Number Description:



Output Buffer	End-to-End Resistance	SOIC	PDIP	MSOP
NO	10K	WMS7130**010S**	WMS7130**010P**	WMS7130**010M**
	50K	WMS7130**050S**	WMS7130**050P**	WMS7130**050M**
	100K	WMS7130**100S**	WMS7130**100P**	WMS7130**100M**
YES	10K	WMS7131**010S**	WMS7131**010P**	WMS7131**010M**
	50K	WMS7131**050S**	WMS7131**050P**	WMS7131**050M**
	100K	WMS7131**100S**	WMS7131**100P**	WMS7131**100M**

For the latest product information, access Winbond's worldwide website at http://www.winbond-usa.com

14. VERSION HISTORY

VERSION	DATE	DESCRIPTION
1.0	July 2003	Initial issue

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