

FEATURES

- Max. toggle frequency of 800MHz
- Differential outputs
- IEE min. of -80mA
- ESD protection of 2000V
- Industry standard 100K ECL levels
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- 150% faster than National or Signetics
- 40% lower power than National or Signetics
- Function and pinout compatible with National and Signetics F100K
- Available in Cerdip, CerpacK and PLCC

DESCRIPTION

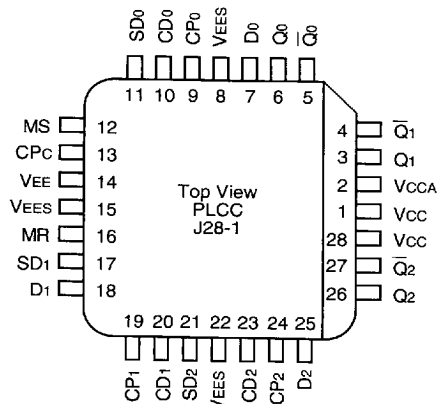
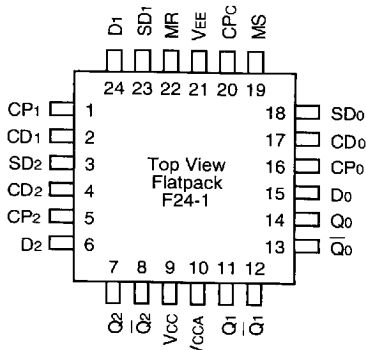
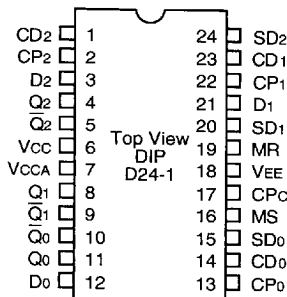
The SY100S331 offers three D-type, edge-triggered master/slave flip-flops with true and complement outputs, designed for use in high-performance ECL systems. Each flip-flop is controlled by a common clock (CP_c), as well as its own clock pulse (CP_n). The resultant clock signal controlling the flip-flop is the logical OR operation of these two clock signals. Data enters the master when both CP_c and CP_n are LOW and enters the slave on the rising edge of either CP_c or CP_n (or both).

Additional control signals include Master Set (MS) and Master Reset (MR) inputs. Each flip-flop also has its own Direct Set (SD_n) and Direct Clear (CD_n) signals. The MR, MS, SD_n and DC_n signals override the clock signals. The inputs on this device have 75KΩ pull-down resistors.

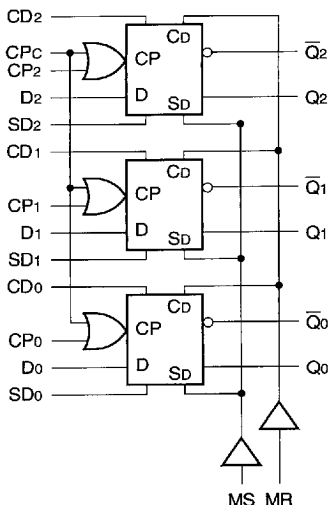
PIN NAMES

Pin	Function
CP ₀ - CP ₂	Individual Clock Inputs
CP _c	Common Clock Input
D ₀ - D ₂	Data Inputs
CD ₀ - CD ₂	Individual Direct Clear Inputs
SD _n	Individual Direct Set Inputs
MR	Master Reset Input
MS	Master Set Input
Q ₀ - Q ₂	Data Outputs
$\bar{Q}_0$ - $\bar{Q}_2$	Complementary Data Outputs
VEES	VEE Substrate
VCCA	VCCO for ECL Outputs

PIN CONFIGURATIONS



BLOCK DIAGRAM



TRUTH TABLES

Asynchronous Operation ⁽¹⁾					
Inputs					Outputs
D _n	CP _n	CP _c	MS SD _n	MR DC _n	Q _n (t+1)
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

NOTE:

1. H = High Voltage Level, L = Low Voltage Level, X = Don't Care, U = Undefined, t = Time before CP Positive Transition, t+1 = Time after CP Positive Transition, u = Low-to-High Transition

Synchronous Operation ⁽¹⁾					
Inputs					Outputs
D _n	CP _n	CP _c	MS SD _n	MR DC _n	Q _n
L	u	L	L	L	L
H	u	L	L	L	H
L	L	u	L	L	L
H	L	u	L	L	H
X	L	L	L	L	Q _n (t)
X	H	X	L	L	Q _n (t)
X	X	H	L	L	Q _n (t)

NOTE:

1. H = High Voltage Level, L = Low Voltage Level, X = Don't Care, U = Undefined, t = Time before CP Positive Transition, t+1 = Time after CP Positive Transition, u = Low-to-High Transition

DC ELECTRICAL CHARACTERISTICS

V_{EE} = -4.2V to -5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I _{IH}	Input HIGH Current, All Inputs	—	—	200	μA	V _{IN} = V _{IH} (Max.)
I _{EE}	Power Supply Current	-80	-65	-35	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

VEE = -4.2V to -5.5V unless otherwise specified, VCC = VCCA = GND, TA = 0°C to +85°C

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
fmax	Toggle Frequency	800	—	800	—	800	—	MHz	—
tPLH tPHL	Propagation Delay CPc to Output	300	900	300	900	300	900	ps	—
tPLH tPHL	Propagation Delay CPn to Output	300	900	300	900	300	900	ps	—
tPLH tPHL	Propagation Delay CDn, SDn to Output	300	1000	300	1000	300	1000	ps	—
tPLH tPHL	Propagation Delay MS, MR to Output	300	1100	300	1100	300	1100	ps	—
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	—
ts	Set-up Time Dn	400	—	400	—	400	—	ps	—
	CDn, SDn (Release Time)	500	—	500	—	500	—		
	MS, MR (Release Time)	800	—	800	—	800	—		
tn	Hold Time Dn	300	—	300	—	300	—	ps	—
tpw (H)	Pulse Width HIGH CPn, CPc, DCn SDn, MR, MS	800	—	800	—	800	—	ps	—

CERPACK

VEE = -4.2V to -5.5V unless otherwise specified, VCC = VCCA = GND, TA = 0°C to +85°C

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
fmax	Toggle Frequency	800	—	800	—	800	—	MHz	—
tPLH tPHL	Propagation Delay CPc to Output	300	800	300	800	300	800	ps	—
tPLH tPHL	Propagation Delay CPn to Output	300	800	300	800	300	800	ps	—
tPLH tPHL	Propagation Delay CDn, SDn to Output	300	900	300	900	300	900	ps	—
tPLH tPHL	Propagation Delay MS, MR to Output	300	1000	300	1000	300	1000	ps	—
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	—
ts	Set-up Time Dn	400	—	400	—	400	—	ps	—
	CDn, SDn (Release Time)	500	—	500	—	500	—		
	MS, MR (Release Time)	800	—	800	—	800	—		
tn	Hold Time Dn	300	—	300	—	300	—	ps	—
tpw (H)	Pulse Width HIGH CPn, CPc, DCn SDn, MR, MS	800	—	800	—	800	—	ps	—

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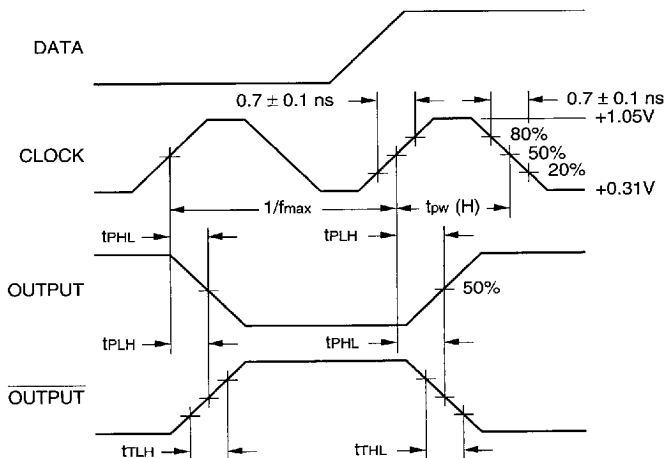
AC ELECTRICAL CHARACTERISTICS (CONT'D.)

PLCC

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_A = 0^{\circ}C$ to $+85^{\circ}C$

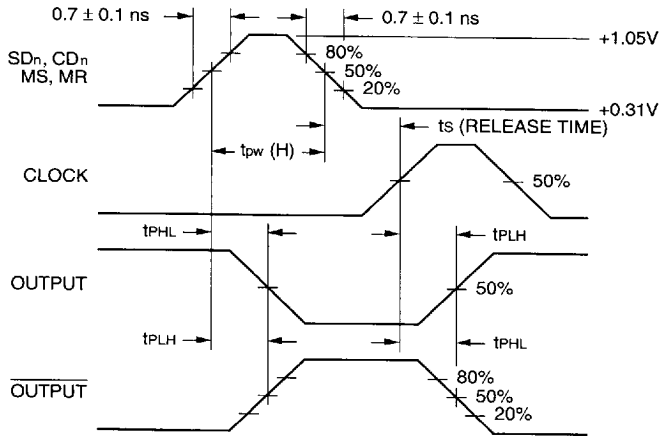
Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{max}	Toggle Frequency	800	—	800	—	800	—	MHz	—
t_{PLH} t_{PHL}	Propagation Delay CP_c to Output	300	700	300	700	300	700	ps	—
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	300	700	300	700	300	700	ps	—
t_{PLH} t_{PHL}	Propagation Delay CD_n , SD_n to Output	300	800	300	800	300	800	ps	—
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	300	900	300	900	300	900	ps	—
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	—
t_s	Set-up Time D_n CD_n , SD_n (Release Time) MS, MR (Release Time)	400 500 800	— — —	400 500 800	— — —	400 500 800	— — —	ps	—
t_h	Hold Time D_n	300	—	300	—	300	—	ps	—
$t_{pw}(H)$	Pulse Width HIGH CP_n , CP_c , DC_n SD_n , MR, MS	800	—	800	—	800	—	ps	—

TIMING DIAGRAMS



Propagation Delay (Clock) and Transition Times

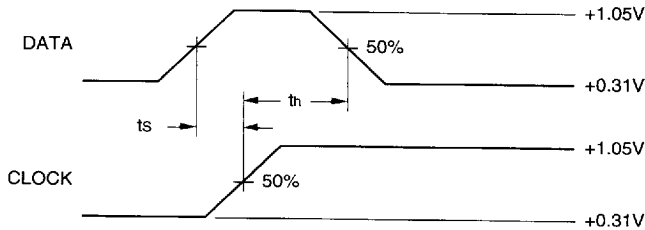
TIMING DIAGRAMS (CONT'D.)



Propagation Delay (Sets and Resets)

NOTE:

SD_n uses complement of DATA and complement of OUTPUT waveforms.



Data Setup and Hold Time

NOTES:

ts is the minimum time before the transition of the clock that information must be present at the data input.

th is the minimum time after the transition of the clock that information must remain unchanged at the data input.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S331DC	D24-1	Commercial
SY100S331FC	F24-1	Commercial
SY100S331JC	J28-1	Commercial
SY100S331JCTR	J28-1	Commercial