iC-TW4 PROGRAMMABLE INTERPOLATOR WITH AUTOMATIC OFFSET CORRECTION

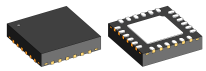
FEATURES

- Realtime interpolation with selectable factors of x2, x4, x5, x8, x10, x16, x20, x25, x32, x50, x64
- Differential signal and index gating inputs
- Input voltage range of 10 mVpp diff. to 1.5 Vpp diff.
- Maximum input frequency of 300 kHz (to x8), 150 kHz (x10 to x16), 75 kHz (x20 and up)
- Selectable hysteresis of 2.8 ° to 15.6 °
- Averaging filter over 16 samples
- Latency less than 1 µs
- Differential encoder quadrature outputs
- Electronic index signal generation
- Startup behaviour: ABZ state defined by absolute sensor position within a period
- Automatic offset correction for sensor and interpolator circuit
- Static pin programming with four external resistors
- Low power consumption from single-ended 3.3 V to 5 V supply
- Extended temperature range of -40 to +125 °C

APPLICATIONS

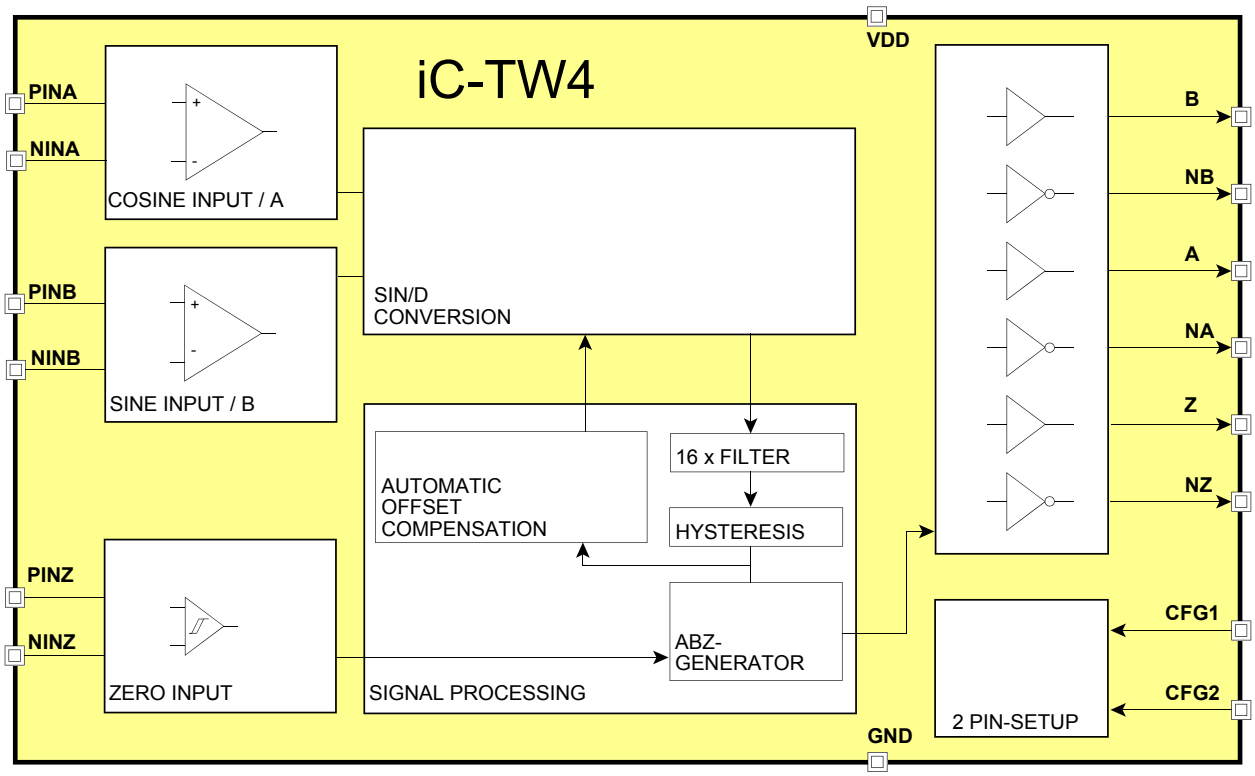
- Optical and magnetic position sensors
- Rotary encoders
- Linear encoders
- Space constraint embedded solutions

PACKAGES



QFN24

BLOCK DIAGRAM



DESCRIPTION

iC-TW4, operating on single-ended supplies of 3.3 V to 5 V, is a low cost interpolation device featuring an automatic signal conditioning and differential encoder quadrature outputs for cable drive.

The chip is pin configured with four external resistors and needs no micro controller or EEPROM for operation or configuration. An adaptive algorithm is used to automatically cancel sensor and input amplifier offset voltages, therefore eliminating the need for cumbersome system calibration.

The pin configuration selects for the interpolation between factors of x2 and x64, and adapts the input gain to cope with differential sensor signals between 10 mVpp to 1.5 Vpp.

The interpolation engine accepts two differential sinusoidal input signals (sine and cosine) to produce a highly interpolated incremental output signal. Sensor bridges are directly interfaced with no external components required.

iC-TW4 can also operate on single-ended input signals when tying the negative input terminals to the signal reference, usually VDD/2.

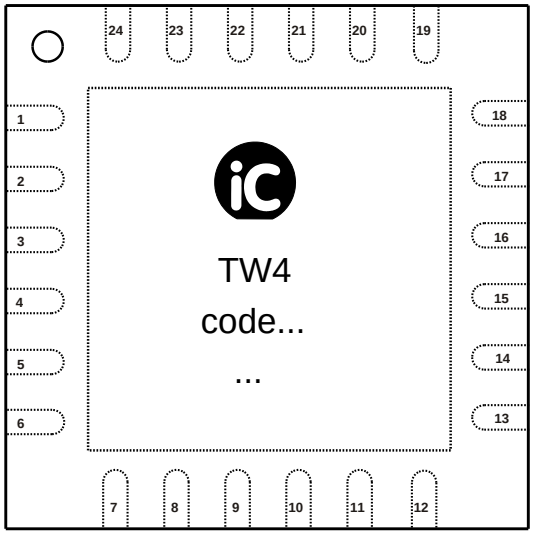
The index gating inputs can interface a wide range of index sensors, a Hall switch or MR bridge sensor, for instance. iC-TW4 generates the index pulse for every sine/cosine signal period that is released by the gating signal. The pulse output is one increment wide and is located at the positive crossover of the A versus the B inputs. By swapping pins PINA and NINA or pins PINB and NINB it is possible to achieve any desired phase relationship of the Z output versus the A and B outputs, respectively.

The device also supports a variety of test modes for device verification and production test. A built in power-on-reset circuit keeps the device in reset mode until the applied power supply voltage permits reliable operation.

CONTENTS

PACKAGING INFORMATION

PIN CONFIGURATION QFN24 4 mm x 4 mm



PIN FUNCTIONS

No.	Name	Function
1	n.c.	n.c.
2	NZ	Index Output Z-
3	B	Index Output B+
4	NB	Index Output B-
5	A	Index Output A+
6	n.c.	n.c.
7	n.c.	n.c.
8	NA	Index Output A-
9	GND	Ground
10	CFG1	Configuration Pin 1
11	CFG2	Configuration Pin 2
12	n.c.	n.c.
13	n.c.	n.c.
14	PINB	Pos. Signal Input Channel B
15	NINB	Neg. Signal Input Channel B
16	NINA	Neg. Signal Input Channel A
17	PINA	Pos. Signal Input Channel A
18	n.c.	n.c.
19	n.c.	n.c.
20	PINZ	Pos. Index Enable Input
21	NINZ	Neg. Index Enable Input
22	VDD	+3 V to 5 V Power Supply
23	Z	Index Output Z+
24	n.c.	n.c.
TP		*Thermal Pad*

The *Thermal Pad* of the QFN package (bottom side) is to be connected to a ground plane on the PCB which must have GND potential.

Only pin 1 marking on top or bottom defines the package orientation (iC-TW4 label and coding is subject to change).

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these values damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VDD	Voltage at VDD	referenced to GND	-0.3	6	V
G002	V()	Voltage at PINA, NINA, PINB, NINB, PINZ, NINZ, A, NA, B, NB, Z, NZ, CFG1, CFG2	referenced to GND	-0.3	VDD + 0.5	V
G003	I()	Current in PINA, NINA, PINB, NINB, PINZ, NINZ, CFG1, CFG2, A, NA, B, NB, Z, NZ		-20	20	mA
G004	Vd	ESD Susceptibility Of Signal Output Pins: A, NA, B, NB, Z, NZ	HBM, 100 pF discharged through 1.5kΩ		2	kV
G005	Vd	ESD Susceptibility Of Remaining Pins: PINA, NINA, PINB, NINB, PINZ, NINZ, CFG1, CFG2	HBM, 100 pF discharged through 1.5kΩ		1.5	kV
G006	Tj	Junction Temerature		-40	125	°C
G007	T_S	Storage Temperature		-40	125	°C

THERMAL DATA

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature		-40		125	°C
T02	Rthaj	Thermal Resistance Chip To Ambient	QFN24 surface mounted to PCB, following JEDEC 51		32		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 3.0...5.5 V, Tj = -40...+125 °C, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VDD	Permissible Supply Voltage VDD		3.0		5.5	V
002	I(VDD)	Total Supply Current	VDD = 3.3 V; f()in = 0 Hz VDD = 3.3 V; f()in = 100 kHz VDD = 5.5 V; f()in = 0 Hz VDD = 5.5 V; f()in = 100 kHz			5 8 10 15	mA mA mA mA
003	Vc()hi	Clamp-Voltage hi at all pins	Vc()hi = V() - VDD; I() = 10 mA	0.5		1.2	V
004	Vc()lo	Clamp-Voltage lo at all pins	I() = -10 mA	-1.2		-0.3	V
Amplifier Inputs PINA, NINA, PINB, NINB							
A01	Vin()sig	Permissible Input Voltage Range		1.4		VDD - 1.2	V
A02	ΔG	Nominal Gain Step Size			6.0		dB
A03	AGA()	Absolute Gain Accuracy			±1		dB
A04	CGM	Gain Matching	G(CHA) vs. G(CHB)	0.85		1.15	
A05	Vos()in	Input Referred Offset Voltage		-12		12	mV
A06	Vosr()out	Output Referred Offset Correction Range			±248		mV
A07	fmax()in	Maximum Input Frequency For Offset Correction				fosc /20000	
A08	Ilk()	Input Current	V() = 0 .. VDD	-50		50	nA
Oscillator							
B01	fosc	Internal Oscillator Frequency	VDD = 3.0 V	15		24	MHz
B02	Δf(T)	Frequency Variation	Tj = -40 to 125°C, VDD const.	-20		0	%
B03	Δf(V)	Frequency Variation	VDD = 3.0 V to 5.5 V, Tj const.	0		25	%
Zero Input Signals PINZ, NINZ							
C01	Vin()sig	Permissible Input Signal Range		0.0		VDD	V
C02	Vin()os	Input Referred Offset Voltage		-15		15	mV
C03	Ilk()	Input Current	V() = 0 .. VDD	-50		50	nA
Digital Outputs A, NA, B, NB, Z, NZ							
D01	I()max	Permissible DC Load Current	source and sink, per pin	-10		10	mA
D02	Vs()hi	Output Saturation Voltage hi	Vs()hi = V(VDD) -V(); I() = -6 mA; VDD = 3.3 V +/- 10 % VDD = 5 V +/- 10 %			 0.65 0.5	 V V
D03	Isc()hi	Short-Circuit Current hi	V() = GND; short-circuit time 10 ms maximum	-100		-10	mA
D04	Vs()lo	Output Saturation Voltage lo	I() = 6 mA; VDD = 3.3 V +/- 10 % VDD = 5 V +/- 10 %			 0.5 0.35	 V V
D05	Isc()lo	Short-Circuit Current lo	V() = VDD; short-circuit time 10 ms maximum	10		140	mA
D06	tr()	Rise Time	V(): 10 to 90%, VDD = 3.3 V, CL() = 10 pF			4	ns
D07	tf()	Fall Time	V(): 90 to 10%, VDD = 3.3 V, CL() = 10 pF			4	ns
D08	twhi	Duty Cyle at Output A, B	referred to period T, see Fig. 1		50		%
D09	tAB	Output Phase A vs. B	referred to period T, see Fig. 1		25		%
D10	tMTD	Minimum Transition Distance	see Fig. 1		1/fosc		

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 3.0...5.5 V, Tj = -40...+125 °C, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Signal Processing							
E01	AAabsOff	Absolute Angular Accuracy with offset error	referred to 360° input period; Vin = 1.2 Vpp diff; IPF = x64; initial error with offset at maximum	-45		45	DEG
E02	AAabs	Absolute Angular Accuracy following offset compensation	referred to 360° input period; Vin = 1.2 Vpp diff; IPF = x64; fin() = 35 Hz . . . 700 Hz (constant); offset correction completed after > 160 input signal periods	-7		7	DEG
E03	AArel	Relative Angular Accuracy	see condition E02, but: IPF = x64 IPF = x2 to x32	 -30 -20		 30 20	 % %
E04	ABrel	Relative Angular Accuracy A vs. B			1/2 AArel		%
Power-On-Reset And Configuration							
F01	VDDon	Turn-on Threshold VDD (power on release)			1.8		V
F02	tp()on	Startup Delay				35	ms

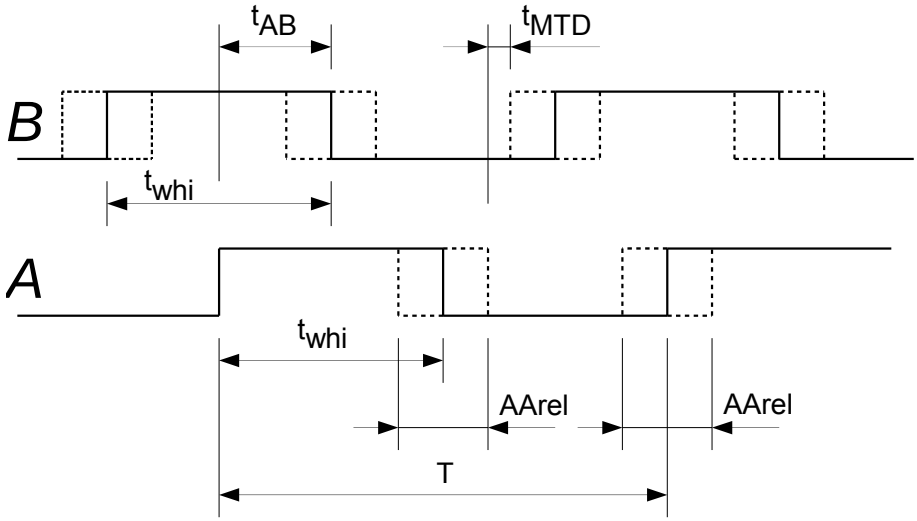


Figure 1: Relative phase distance.

INPUT STAGE

Programmable Gain Amplifier

A programmable gain amplifier (PGA) with output referred offset adjustment is used as input stage, shown in Figure 2. The gain is common for both channel A and B and is programmed through pin CFG2.

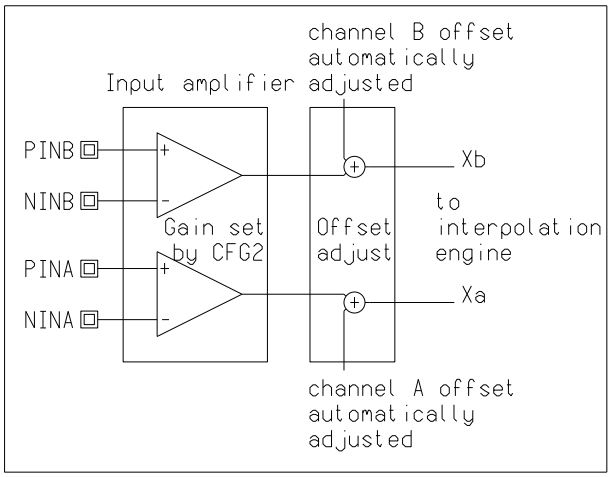


Figure 2: Input stage

Automated Offset Adjustment

Offset adjustment is provided at the output of the input amplifier. The offset correction is performed automatically and continuously. Amplifier offset and sensor offset are both eliminated offering a true plug-and-play system. Additional device or sensor calibration is not required as the iC-TW4 does all calibration automatically. In addition, the effect of temperature dependent offset drift of both the amplifier and the sensor is eliminated.

The sensor signal must satisfy the range limits introduced by Table 5 as well as the requirements of Equation 1. If the sensor offset exceeds the correction range, the tracking engine is not able to converge.

Equation 1:

$$V_{AOFS}{}^2 + V_{BOFS}{}^2 < (V_{IN} - 12\,mV)^2$$

Parameter	Description	Unit
V_{AOFS}	Sensor offset input A	mV
V_{BOFS}	Sensor offset input B	mV
V_{IN}	Input signal amplitude (peak-peak)	mV

Table 4: Sensor signal parameters.

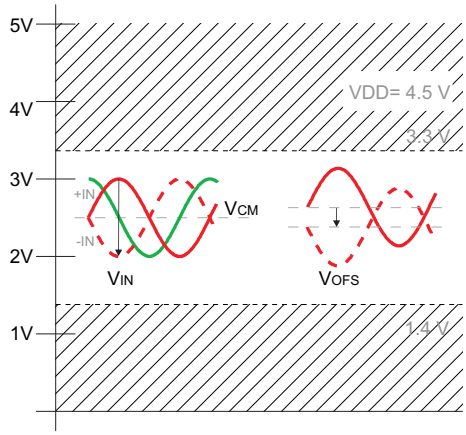


Figure 3: Permissible input voltage range at VDD = 5 V +/- 10 %.

CFG2 Config.	Input Signal Range $V_{IN\ peak\text{-}peak}$	Offset Correction Range $V_{OFS\ max}$
0	400 mV - 750 mV 400 mV max. @VDD = 3.0 V	± 400 mV
1	200 mV - 400 mV	± 232 mV
2	100 mV - 200 mV	± 112 mV
3	50 mV - 100 mV	± 50 mV
4	25 mV - 50 mV	± 19 mV
5	12.5 mV - 25 mV	± 3.5 mV

Table 5: Input signal and offset correction ranges.

Example of Setting the Input Signal Range (CFG2)

Assuming a sin/cos sensor is connected to inputs A and B with the following characteristics:
$V_{IN\ peak\text{-}peak}$ = 60 mV, V_{AOFS} = 5 mV, V_{BOFS} = 10 mV

Input signal range #3 (50 mV - 100 mV) needs to be selected allowing offset correction of up to 50 mV. As the sensor's offset voltage is less than 10 mV, the offset correction range is not exceeded.
However, Equation 1 must also be considered:

$$V_{AOFS}{}^2 + V_{BOFS}{}^2 < (V_{IN} - 12\,mV)^2$$

In our case

$$5^2 + 10^2 < (60 - 12)^2$$

$$25 + 100 < 2304$$

which is OK.

Limits of Automated Offset Adjustment

Repeated short moves of greater than 1 input cycle and less than 2 input cycles can cause the automated offset adjustment function to temporarily adapt incorrectly, resulting in excessive offset correction values. Offset correction values return to normal when sensor input moves again become greater than 2 input cycles.

CONFIGURATION

The iC-TW4 is configured by applying the appropriate voltage and impedance on its configuration pins CFG1 and CFG2.

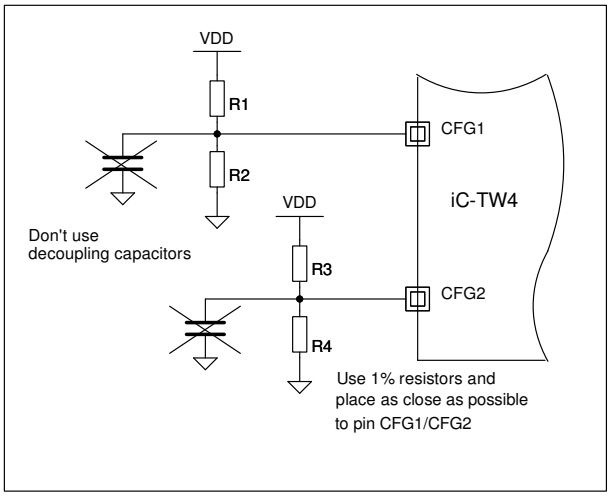


Figure 4: Configuration by pins CFG1 and CFG2.

A two-resistor voltage divider is sufficient to generate the required configuration voltage. The resistor divider must be connected to VDD and GND of iC-TW4. The resistors should be placed as close as possible to pin CFG1 and CFG2 and no decoupling capacitor should be used. The resistors tolerance must be 1 % to guarantee reliable operation across all parametric corners.

NB: The configuration applied to pins CFG1 and CFG2 is not permitted to change during operation or unpredictable behaviour can result. In order to change the configuration a Power-On-Reset (POR) must be executed (power cycling).

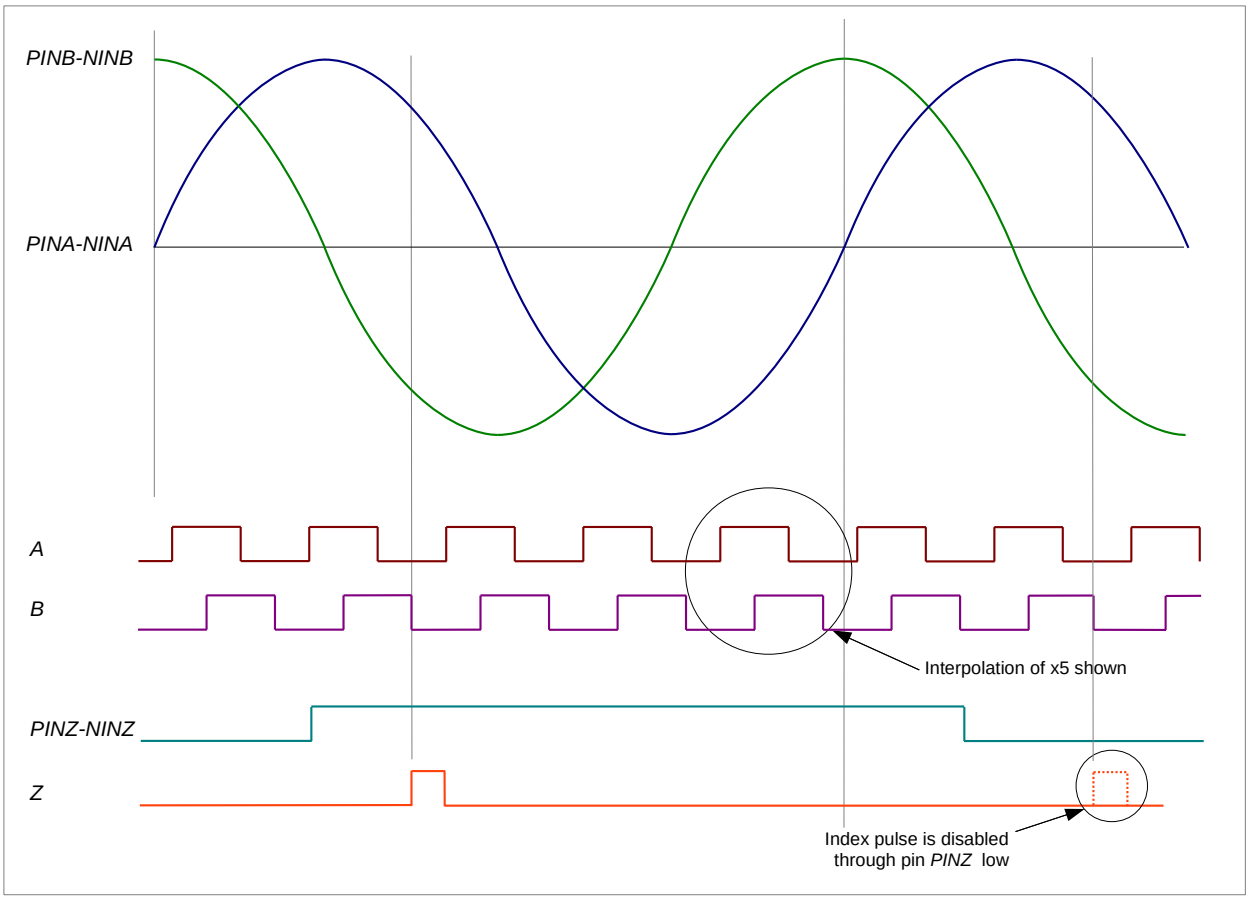


Figure 5: Principle interpolation function and index generation.

Interpolation

The interpolation factor IPF is configured through pin CFG1. The recommended resister values shown in Table 6 should be used.

IPF(Interpol.)	Hysteresis	[V] at CFG1	R1 [kΩ]	R2 [kΩ]
x2 (8)	10.4 °	0.13 * VDD	22.6	3.48
x2 (8)	15.6 °	0.13 * VDD	562	86.6
x4 (16)	10.4 °	0.2 * VDD	15.0	3.74
x4 (16)	15.6 °	0.2 * VDD	374	93.1
x5 (20)	10.4 °	0.27 * VDD	11.3	4.12
x5 (20)	15.6 °	0.27 * VDD	280	102
x8 (32)	10.4 °	0.33 * VDD	8.87	4.53
x8 (32)	15.6 °	0.33 * VDD	226	113
x10 (40)	5.6 °	0.4 * VDD	7.50	4.99
x10 (40)	10.4 °	0.4 * VDD	187	124
x16 (64)	5.6 °	0.46 * VDD	6.49	5.62
x16 (64)	10.4 °	0.46 * VDD	162	140
x20 (80)	2.8 °	0.54 * VDD	5.62	6.49
x20 (80)	5.6 °	0.54 * VDD	140	162
x25 (100)	2.8 °	0.6 * VDD	4.99	7.50
x25 (100)	5.6 °	0.6 * VDD	124	187
x32 (128)	2.8 °	0.67 * VDD	4.53	8.87
x32 (128)	5.6 °	0.67 * VDD	113	226
x50 (200)	2.8 °	0.73 * VDD	4.12	11.3
x50 (200)	5.6 °	0.73 * VDD	102	280
x64 (256)	2.8 °	0.8 * VDD	3.74	15.0
x64 (256)	5.6 °	0.8 * VDD	93.1	374

Table 6: Interpolation configuration

Performance

The device performance depends primarily on the selected interpolation rate. However, parametric manufacturing tolerances as well as power supply voltage and temperature has a defining impact on corner performance. Typical performance refers to nominal wafer parameters. Due to manufacturing variations the actual performance can be ±20 % of stated typical performance.

Interpolation factor	Maximum input frequency
x2, x4, x5, x8	typ. 300 kHz
x10, x16	typ. 150 kHz
x20, x25, x32, x50, x64	typ. 75 kHz
Notes	Typical performance at 25 °C. Max. input frequency at 125 °C is up to 10 % lower.

Table 7: Maximum input frequency

Index Generation

The iC-TW4 generates a one increment long index output pulse on pin Z and NZ when the differential voltage between pin PINA and pin NINA is equal to the voltage between pin NINB and PINB. Refer to Figure 5 for an illustration. Outputs A and B are always low when Z is high.

The output pulse on pin Z, respectively pin NZ, is only generated if the differential voltage between the gating inputs PINZ and NINZ is positive. If the voltage between the gating inputs PINZ and NINZ is negative, no output pulse is generated.

NB: In case the timing specifications t_{setup} and t_{hold} are not satisfied (refer to Table 10), the Z output might not be properly generated.

Amplification

The input amplifier gain is configured through pin CFG2. The recommended resistor values are shown in Table 8. 1 % tolerance resistors must be used.

No.	Input Signal Range $V_{IN\ peak\text{-}peak}$ [$V_{IN\ peak\text{-}peak\ differential}$]	Voltage at CFG2 [V]	R3 [kΩ]	R4 [kΩ]
0	400 mV - 750 mV [800 mV - 1.5 V]	0.13 * VDD	22.6	3.48
1	200 mV - 400 mV [400 mV - 800 V]	0.20 * VDD	15.0	3.74
2	100 mV - 200 mV [200 mV - 400 V]	0.27 * VDD	11.3	4.12
3	50 mV - 100 mV [100 mV - 200 V]	0.33 * VDD	8.87	4.53
4	25 mV - 50 mV [50 mV - 100 V]	0.40 * VDD	7.50	4.99
5	12.5 mV - 25 mV [25 mV - 50 V]	0.46 * VDD	6.49	5.62
6	test only	0.54 * VDD	5.62	6.49
7	test only	0.60 * VDD	4.99	7.50
8	reserved	0.67 * VDD	4.53	8.87
9	reserved	0.73 * VDD	4.12	11.3
10	reserved	0.80 * VDD	3.74	15.0
11	test only	0.92 * VDD	1.37	15.68

Table 8: Gain configuration

Test Modes

The iC-TW4 supports a variety of test modes. With the exception of index calibration mode all test modes are used for device verification and production test only. Please refer to section **"Index Gating"** on page 10 for details on how to use the index calibration mode.

Test mode	[V] at CFG1	Z at CFG1	[V] at CFG2	Z at CFG2
PGA A	0.8 * VDD	< 3 kΩ	Refer to table 8	> 75 kΩ
PGA B	0.8 * VDD	> 75 kΩ	Refer to table 8	> 75 kΩ
Calib 1	0.87 * VDD	> 75 kΩ	Refer to table 8	< 3 kΩ
Index Calib. Mode	0.87 * VDD	< 3 kΩ	Refer to table 8	< 3 kΩ
Offset	0.87 * VDD	< 3 kΩ	Refer to table 8	> 75 kΩ
Vc	0.87 * VDD	> 75 kΩ	Refer to table 8	> 75 kΩ

Table 9: Test modes

INDEX GATING

The iC-TW4 can interface to a wide range of index gating sources. Most commonly used are the digital Hall sensor and the MR sensor bridge. The digital Hall sensor provides a large swing input signal to the iC-TW4. Depending on the polarity of the Hall it is either connected to pin NINZ or PINZ. Most Hall sensors use an open drain stage pulling the output low in the presence of a magnetic field. The unused terminal NINZ or PINZ should be biased to an adequate mid voltage level to guarantee good noise margin. Refer to Figure 6 for sample configurations.

A MR sensor differential bridge can also be used to gate the index. Typically, the MR sensor provides a small signal amplitude. In addition, residual side lobes are present that can trigger double indexing. It might be necessary to externally adjust the sensor offset in order to fine-tune the desired threshold.

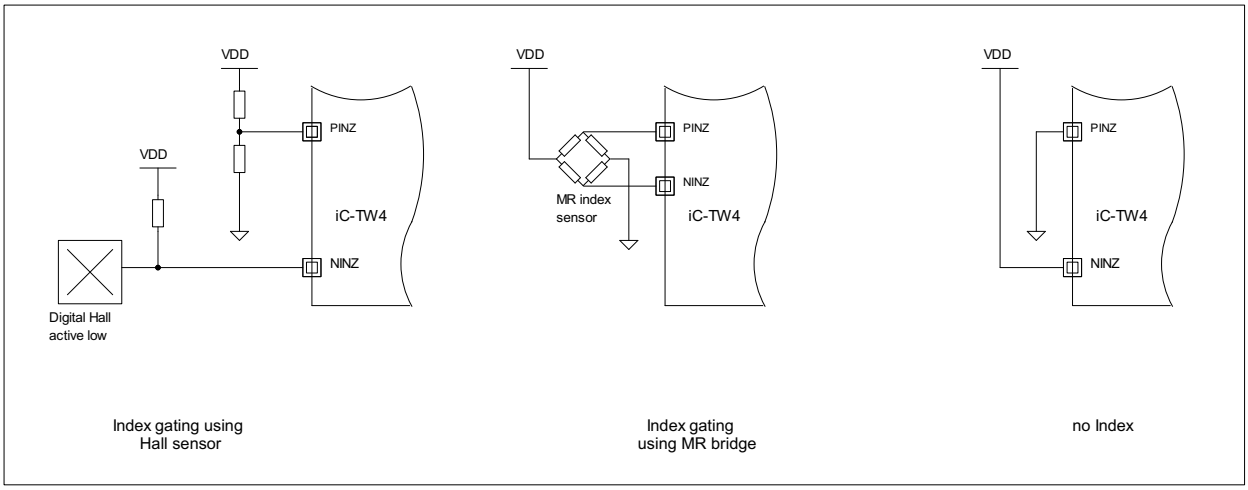


Figure 6: Index configuration

Index Calibration Mode
The iC-TW4 provides an index calibration mode, which allows the internal gating window to be observed. This simplifies product calibration as variation in sensor offset can be easily compensated for.

The calibration mode is enabled via pins CFG1 and CFG2, refer to Table 9. The internal index gating window can now be observed on pin B.

Index gating should be calibrated at sine/cosine input frequencies below 5 kHz to minimize the effect of latency. Timings shown in Table 10 are valid for input frequencies below 5 kHz. Once the timing is satisfied according to Table 10, correct operation is guaranteed up to the maximum input frequency as specified in electrical characteristics No. A07.

Parameter	Description	Min
t_{setup}	Index window setup time before rising edge of Z	0.8 µs
t_{hold}	Index window hold time after falling edge of Z	0.8 µs

Table 10: Index gating timing requirements.

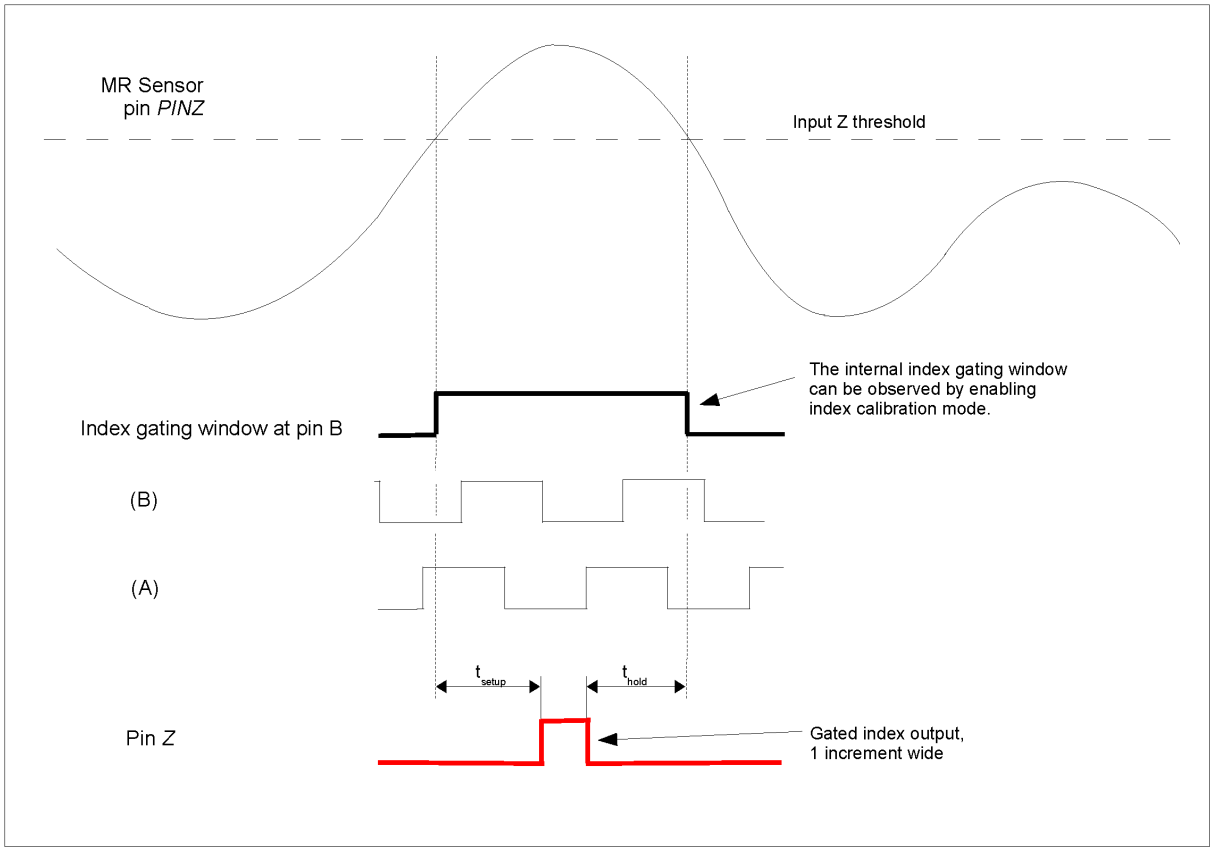


Figure 7: Example of correctly set index gating window. The side lobes are below the threshold line and no parasitic triggering occurs.

START UP

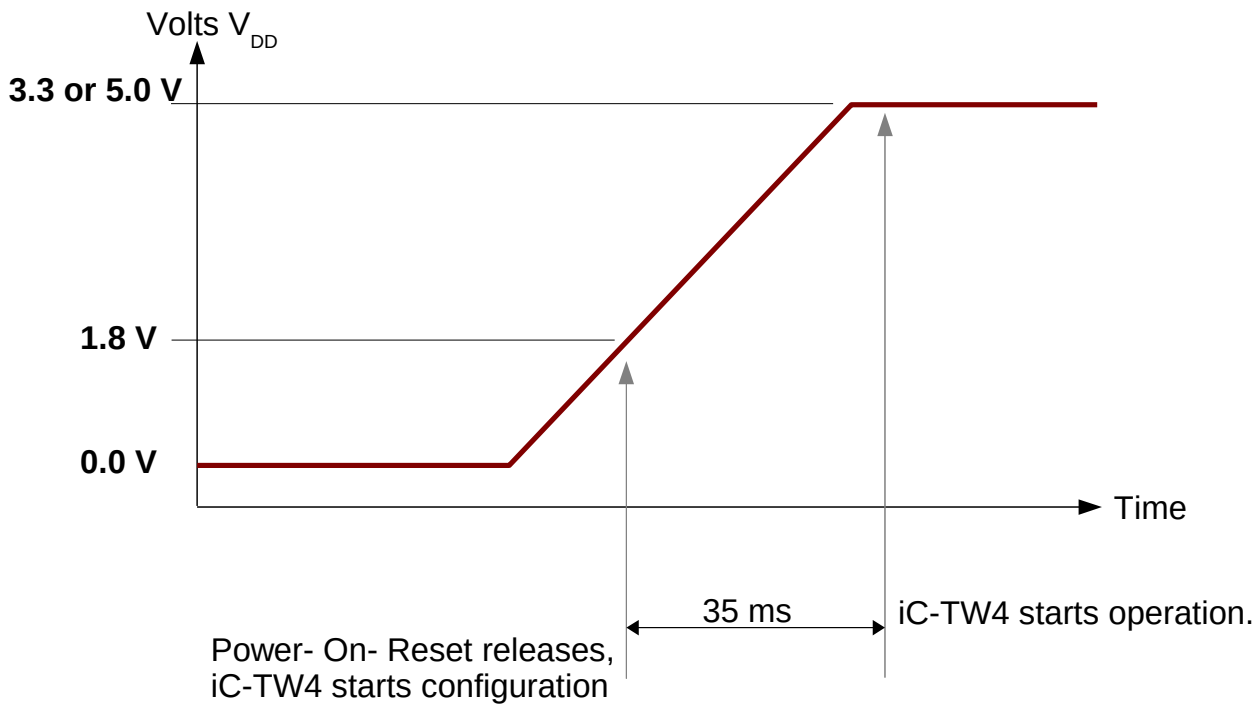


Figure 8: Power supply ramp-up

The iC-TW4 contains built-in Power-On-Reset (POR) circuitry. The POR keeps the device in reset as long as the applied power supply voltage does not allow reliable operation. Once the power supply ramps up above 1.8 V, the POR releases the reset and the iC-TW4 starts the configuration cycle. 35 ms after the device goes out of reset, normal operation begins.

The A/B signals on start-up follow reproducible the stable input signal state with a stable A/B output state. No A/B bursts are output on start-up with a stable input signal state. The state of the A/B output signals is defined by the absolute sensor position within a period. The phase relationship between Z and A/B is defined and persists.

Due to hysteresis it is possible that the A/B output differs on start-up from the levels on power down.

To avoid A/B output toggling while startup it is important that the power supply ramp-up is sufficiently fast and the input signals are stable as soon as normal operation begins. In applications where startup A/B toggling is acceptable, no precaution must be taken, as the iC-TW4 will properly power-up on an indefinitely slow supply rise time.

TYPICAL APPLICATIONS

Figure 9 shows a device setup with an unipolar sensor signal. With the resistors R1, R2, R3, R4 and R5 it is possible to adjust to the sensor signal (compensation of amplitude, reference voltage, and sensor supply).

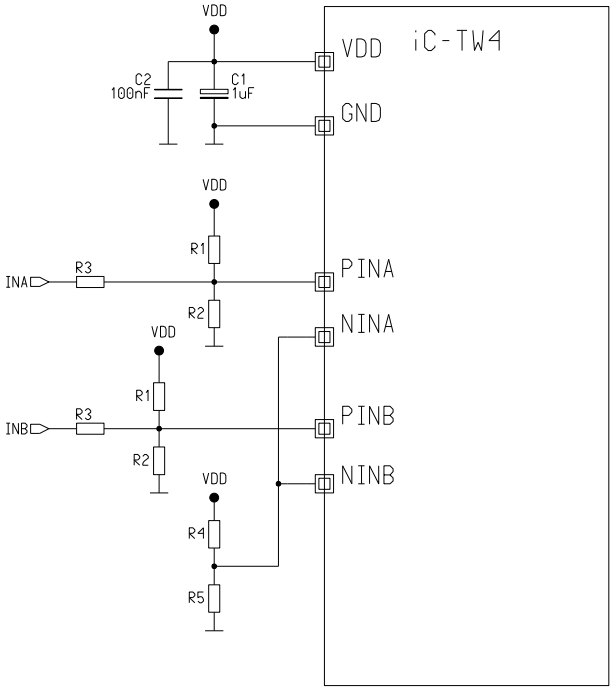


Figure 9: Unipolar sensor signal adaption using resistors

Figure 10 shows a typical device setup with a sensor being connected to the input stages via differential bridges. Index gating uses a differential bridge as well. Note also that it is advisable to decouple the supply voltage with a capacitor. Resistor sizes on pins CFG1 and CFG2 need to be chosen in accordance with the desired operation mode. Refer to Table 6 for more details.

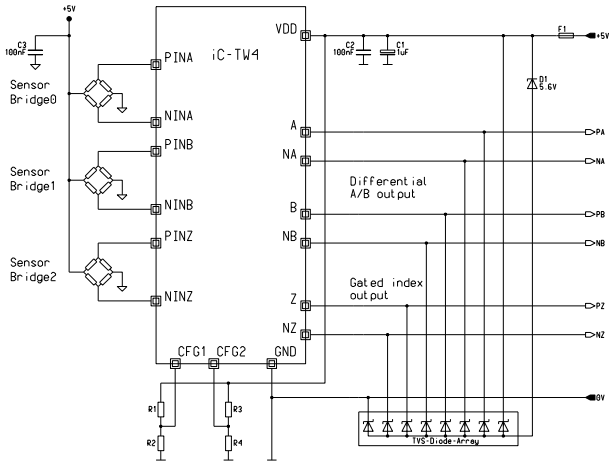


Figure 10: Device setup using bridges

ORDERING INFORMATION

Type	Package	Order Designation
iC-TW4 Evaluation board	24 pin QFN, 4 mm x 4 mm	iC-TW4 QFN24 iC-TW4 EVAL TW41D

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