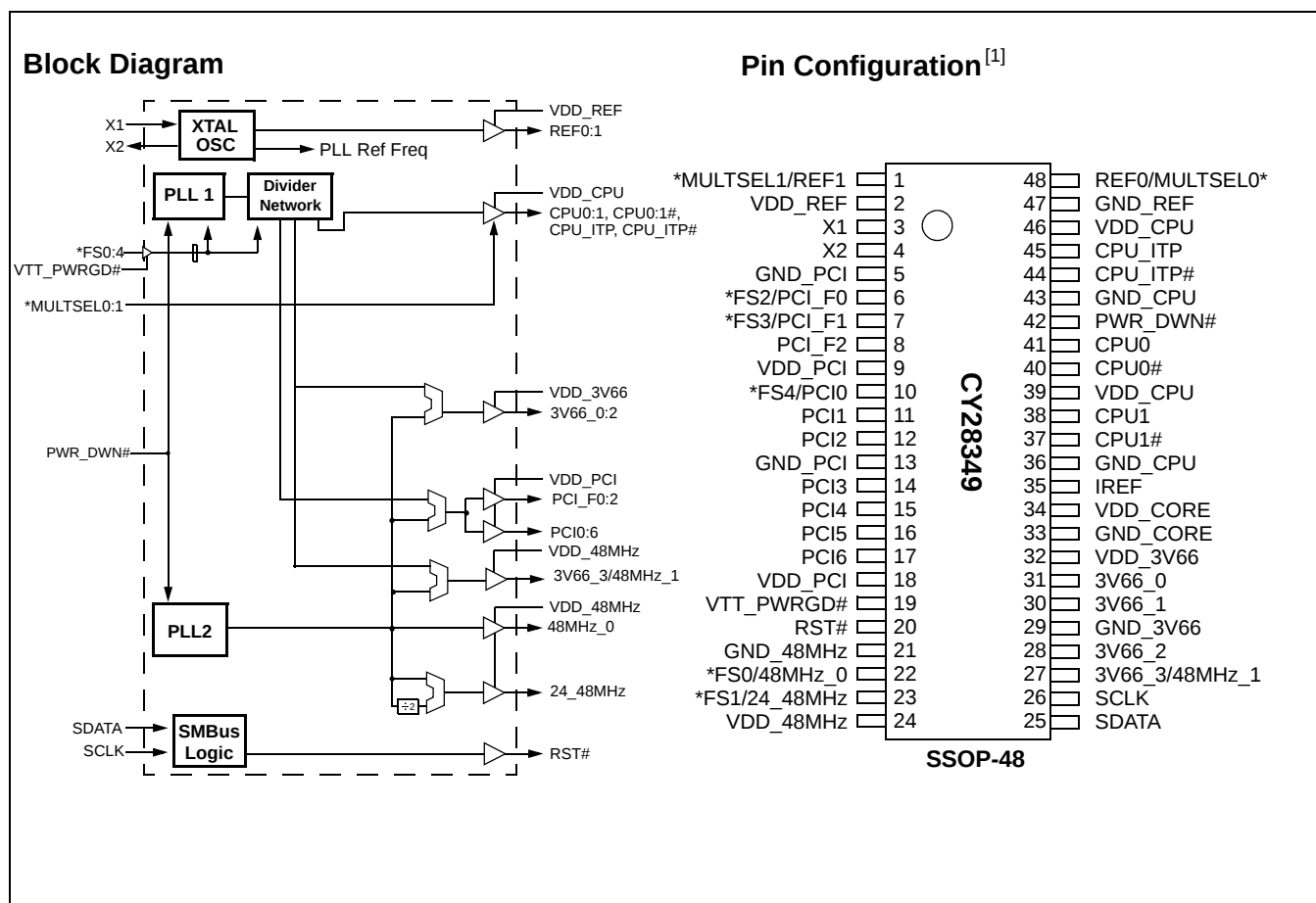


# FTG for Intel® Pentium® 4 CPU and Chipsets

## Features

- Compatible to Intel® CK-Titan & CK-408 Clock Synthesizer/Driver Specifications
- System frequency synthesizer for Intel Brookdale 845 and Brookdale - G Pentium® 4 Chipsets
- Programmable clock output frequency with less than 1 MHz increment
- Integrated fail-safe Watchdog timer for system recovery
- Automatically switch to HW selected or SW programmed clock frequency when watchdog timer time-out
- Fixed 3V66 and PCI output frequency mode
- Capable of generating system RESET after a Watchdog timer time-out occurs or a change in output frequency via SMBus interface
- Support SMBus byte read/write and block read/write operations to simplify system BIOS development
- Vendor ID and Revision ID support
- Programmable drive strength support
- Programmable output skew support
- Power management control inputs
- Available in 48-pin SSOP

| CPU | 3V66 | PCI  | REF | 48M | 24_48M |
|-----|------|------|-----|-----|--------|
| x 3 | x 4  | x 10 | x 2 | x 1 | x 1    |



### Note:

1. Signals marked with "\*" and "^" have internal pull-up and pull-down resistors respectively.

**Pin Definitions**

| Pin Name          | Pin No.                | Pin Type | Pin Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------------------|------------------------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| X1                | 3                      | I        | <b>Crystal Connection or External Reference Frequency Input:</b> This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input.                                                                                                                                                                                                                                                                                                                                                                                                           |
| X2                | 4                      | O        | <b>Crystal Connection:</b> Connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| REF0/MULTSEL0     | 48                     | I/O      | <b>Reference Clock 0/Current Multiplier Selection 0:</b> 3.3V 14.318-MHz clock output. This pin also serves as a power-on strap option to determine the current multiplier for the CPU clock outputs. The MULTSEL1:0 definitions are as follows:<br>MULTSEL1:0<br>00 = loh is 4 x IREF<br>01 = loh is 5 x IREF<br>10 = loh is 6 x IREF<br>11 = loh is 7 x IREF                                                                                                                                                                                                                                                   |
| REF1/MULTSEL1     | 1                      | I/O      | <b>Reference Clock 1/Current Multiplier Selection 1:</b> 3.3V 14.318-MHz clock output. This pin also serves as a power-on strap option to determine the current multiplier for the CPU clock outputs. The MULTSEL1:0 definitions are as follows:<br>MULTSEL1:0<br>00 = loh is 4 x IREF<br>01 = loh is 5 x IREF<br>10 = loh is 6 x IREF<br>11 = loh is 7 x IREF                                                                                                                                                                                                                                                   |
| CPU0:1, CPU0:1#   | 41, 38, 40, 37         | O        | <b>CPU Clock Outputs:</b> Frequency is set by the FS0:4 inputs or through serial input interface.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| CPU_ITP, CPU_ITP# | 44, 45                 | I/O      | <b>CPU Clock Output for ITP:</b> Frequency is set by the FS0:4 inputs or through serial input interface.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 3V66_0:2          | 31, 30, 28             | O        | <b>66 MHz Clock Outputs:</b> 3.3V fixed 66-MHz clock.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| PCI_F0/FS2        | 6                      | I/O      | <b>Free-running PCI Output 0/Frequency Select 2:</b> 3.3V free-running PCI output. This pin also serves as a power-on strap option to determine device operating frequency as described in the Frequency Selection Table.                                                                                                                                                                                                                                                                                                                                                                                        |
| PCI_F1/FS3        | 7                      | I/O      | <b>Free-running PCI Output 1/Frequency Select 3:</b> 3.3V free-running PCI output. This pin also serves as a power-on strap option to determine device operating frequency as described in Table 4.                                                                                                                                                                                                                                                                                                                                                                                                              |
| PCI_F2            | 8                      | I/O      | <b>Free-running PCI Output 2:</b> 3.3V free-running PCI output.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| PCI0/FS4          | 10                     | I/O      | <b>PCI Output 0/Frequency Select 4:</b> 3.3V PCI output. This pin also serves as a power-on strap option to determine device operating frequency as described in Table 4.                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| PCI1:6            | 11, 12, 14, 15, 16, 17 | O        | <b>PCI Clock Output 1 to 6:</b> 3.3V PCI clock outputs.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 48MHz_0/FS0       | 22                     | I/O      | <b>48 MHz Output/Frequency Select 0:</b> 3.3V fixed 48-MHz, non-spread spectrum output. This pin also serves as a power-on strap option to determine device operating frequency as described in Table 4. This output will be used as the reference clock for USB host controller in Intel 845 (Brookdale) platforms. For Intel Brookdale - G platforms, this output will be used as the VCH reference clock.                                                                                                                                                                                                     |
| 24_48MHz/FS1      | 23                     | I/O      | <b>24 or 48MHz Output/Frequency Select 1:</b> 3.3V fixed 24 MHz or 48 MHz non-spread spectrum output. This pin also serves as a power-on strap option to determine device operating frequency as described in Table 4. This output will be used as the reference clock for SIO devices in Intel® 845 (Brookdale) platforms. For Intel® Brookdale - G platforms, this output will be used as the reference clock for both USB host controller and SIO devices. We recommend system designer to configure this output as 48 MHz and "HIGH Drive" by setting Byte [5], Bit [0] and Byte [9], Bit [7], respectively. |
| 3V66_3/48MHz_1    | 27                     | O        | <b>48 MHz or 66 MHz Output:</b> 3.3V output.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

**Pin Definitions** (continued)

| Pin Name                                                    | Pin No.                      | Pin Type          | Pin Description                                                                                                                                                                                                                                                                          |
|-------------------------------------------------------------|------------------------------|-------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PWR_DWN#                                                    | 42                           | I                 | <b>Power Down Control:</b> 3.3V LVTTL compatible input that places the device in power down mode when held low.                                                                                                                                                                          |
| SCLK                                                        | 26                           | I                 | <b>SMBus Clock Input:</b> Clock pin for serial interface.                                                                                                                                                                                                                                |
| SDATA                                                       | 25                           | I/O               | <b>SMBus Data Input:</b> Data pin for serial interface.                                                                                                                                                                                                                                  |
| RST#                                                        | 20                           | O<br>(open-drain) | <b>System Reset Output:</b> Open-drain system reset output.                                                                                                                                                                                                                              |
| IREF                                                        | 35                           | I                 | <b>Current Reference for CPU output:</b> A precision resistor is attached to this pin which is connected to the internal current reference.                                                                                                                                              |
| VTT_PWRGD#                                                  | 19                           | I                 | <b>Powergood from Voltage Regulator Module (VRM):</b> 3.3V LVTTL input. VTT_PWRGD# is a level-sensitive strobe used to determine when FS0:4 and MULTSEL0:1 inputs are valid and OK to be sampled (Active LOW). Once VTT_PWRGD# is sampled LOW, the status of this input will be ignored. |
| VDD_REF,<br>VDD_PCI,<br>VDD_48MHz,<br>VDD_3V66,<br>VDD_CPU  | 2, 9, 18, 24,<br>32, 39, 46  | P                 | <b>3.3V Power Connection:</b> Power supply for CPU outputs buffers, 3V66 output buffers, PCI output buffers, reference output buffers and 48-MHz output buffers. Connect to 3.3V.                                                                                                        |
| GND_PCI,<br>GND_48MHz,<br>GND_3V66,<br>GND_CPU,<br>GND_REF, | 5, 13, 21, 29,<br>36, 43, 47 | G                 | <b>Ground Connection:</b> Connect all ground pins to the common system ground plane.                                                                                                                                                                                                     |
| VDD_CORE                                                    | 34                           | P                 | <b>3.3V Analog Power Connection:</b> Power supply for core logic, PLL circuitry. Connect to 3.3V.                                                                                                                                                                                        |
| GND_CORE                                                    | 33                           | G                 | <b>Analog Ground Connection:</b> Ground for core logic, PLL circuitry.                                                                                                                                                                                                                   |

**Swing Select Functions**

| MULTSEL1 | MULTSEL0 | Board Target Trace/Term Z | Reference R, IREF = $V_{DD}/(3 \cdot R_r)$ | Output Current             | $V_{OH}$ @ Z |
|----------|----------|---------------------------|--------------------------------------------|----------------------------|--------------|
| 0        | 0        | 50Ω                       | Rr = 221 1%,<br>IREF = 5.00 mA             | $I_{OH} = 4 \cdot I_{ref}$ | 1.0V @ 50    |
| 0        | 0        | 60Ω                       | Rr = 221 1%,<br>IREF = 5.00 mA             | $I_{OH} = 4 \cdot I_{ref}$ | 1.2V @ 60    |
| 0        | 1        | 50Ω                       | Rr = 221 1%,<br>IREF = 5.00 mA             | $I_{OH} = 5 \cdot I_{ref}$ | 1.25V @ 50   |
| 0        | 1        | 60Ω                       | Rr = 221 1%,<br>IREF = 5.00 mA             | $I_{OH} = 5 \cdot I_{ref}$ | 1.5V @ 60    |
| 1        | 0        | 50Ω                       | Rr = 221 1%,<br>IREF = 5.00 mA             | $I_{OH} = 6 \cdot I_{ref}$ | 1.5V @ 50    |
| 1        | 0        | 60Ω                       | Rr = 221 1%,<br>IREF = 5.00 mA             | $I_{OH} = 6 \cdot I_{ref}$ | 1.8V @ 60    |
| 1        | 1        | 50Ω                       | Rr = 221 1%,<br>IREF = 5.00 mA             | $I_{OH} = 7 \cdot I_{ref}$ | 1.75V @ 50   |
| 1        | 1        | 60Ω                       | Rr = 221 1%,<br>IREF = 5.00 mA             | $I_{OH} = 7 \cdot I_{ref}$ | 2.1V @ 60    |
| 0        | 0        | 50Ω                       | Rr = 475 1%,<br>IREF = 2.32 mA             | $I_{OH} = 4 \cdot I_{ref}$ | 0.47V @ 50   |
| 0        | 0        | 60Ω                       | Rr = 475 1%,<br>IREF = 2.32 mA             | $I_{OH} = 4 \cdot I_{ref}$ | 0.56V @ 60   |
| 0        | 1        | 50Ω                       | Rr = 475 1%,<br>IREF = 2.32 mA             | $I_{OH} = 5 \cdot I_{ref}$ | 0.58V @ 50   |
| 0        | 1        | 60Ω                       | Rr = 475 1%,<br>IREF = 2.32 mA             | $I_{OH} = 5 \cdot I_{ref}$ | 0.7V @ 60    |
| 1        | 0        | 50Ω                       | Rr = 475 1%,<br>IREF = 2.32 mA             | $I_{OH} = 6 \cdot I_{ref}$ | 0.7V @ 50    |
| 1        | 0        | 60Ω                       | Rr = 475 1%,<br>IREF = 2.32 mA             | $I_{OH} = 6 \cdot I_{ref}$ | 0.84V @ 60   |
| 1        | 1        | 50Ω                       | Rr = 475 1%,<br>IREF = 2.32 mA             | $I_{OH} = 7 \cdot I_{ref}$ | 0.81V @ 50   |
| 1        | 1        | 60Ω                       | Rr = 475 1%,<br>IREF = 2.32 mA             | $I_{OH} = 7 \cdot I_{ref}$ | 0.97V @ 60   |

## Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions such as individual clock output buffers, etc. can be individually enabled or disabled.

The register associated with the Serial Data Interface initializes to its default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions.

## Data Protocol

The clock driver serial protocol accepts Byte Write, byte read, Block Write and Block Read operation from the controller. For Block Write/Read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For Byte Write and Byte Read operations, the system controller can access individual indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 1*.

The Block Write and Block Read protocol is outlined in *Table 2* while *Table 3* outlines the corresponding byte write and byte read protocol.

The slave receiver address is 11010010 (D2h).

**Table 1. Command Code Definition**

| Bit | Descriptions                                                                                                                 |
|-----|------------------------------------------------------------------------------------------------------------------------------|
| 7   | 0 = Block Read or Block Write operation<br>1 = Byte Read or Byte Write operation                                             |
| 6:0 | Byte offset for Byte Read or Byte Write operation. For Block Read or Block Write operations, these bits should be '0000000'. |

**Table 2. Block Read and Block Write Protocol**

| Block Write Protocol |                                                                | Block Read Protocol |                                                                |
|----------------------|----------------------------------------------------------------|---------------------|----------------------------------------------------------------|
| Bit                  | Description                                                    | Bit                 | Description                                                    |
| 1                    | Start                                                          | 1                   | Start                                                          |
| 2:8                  | Slave address – 7 bits                                         | 2:8                 | Slave address – 7 bits                                         |
| 9                    | Write                                                          | 9                   | Write                                                          |
| 10                   | Acknowledge from slave                                         | 10                  | Acknowledge from slave                                         |
| 11:18                | Command Code – 8 bits<br>'00000000' stands for block operation | 11:18               | Command Code – 8 bits<br>'00000000' stands for block operation |
| 19                   | Acknowledge from slave                                         | 19                  | Acknowledge from slave                                         |
| 20:27                | Byte Count – 8 bits                                            | 20                  | Repeat start                                                   |
| 28                   | Acknowledge from slave                                         | 21:27               | Slave address – 7 bits                                         |
| 29:36                | Data byte 0 – 8 bits                                           | 28                  | Read                                                           |
| 37                   | Acknowledge from slave                                         | 29                  | Acknowledge from slave                                         |
| 38:45                | Data byte 1 – 8 bits                                           | 30:37               | Byte count from slave – 8 bits                                 |
| 46                   | Acknowledge from slave                                         | 38                  | Acknowledge                                                    |
| ...                  | Data Byte N/Slave Acknowledge...                               | 39:46               | Data byte from slave – 8 bits                                  |
| ...                  | Data Byte N – 8 bits                                           | 47                  | Acknowledge                                                    |
| ...                  | Acknowledge from slave                                         | 48:55               | Data byte from slave – 8 bits                                  |
| ...                  | Stop                                                           | 56                  | Acknowledge                                                    |
|                      |                                                                | ...                 | Data bytes from slave/Acknowledge                              |
|                      |                                                                | ...                 | Data byte N from slave – 8 bits                                |
|                      |                                                                | ...                 | Not Acknowledge                                                |
|                      |                                                                | ...                 | Stop                                                           |

**Table 3. Byte Read and Byte Write Protocol**

| Byte Write Protocol |                                                                                                                                               | Byte Read Protocol |                                                                                                                                               |
|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| Bit                 | Description                                                                                                                                   | Bit                | Description                                                                                                                                   |
| 1                   | Start                                                                                                                                         | 1                  | Start                                                                                                                                         |
| 2:8                 | Slave address – 7 bits                                                                                                                        | 2:8                | Slave address – 7 bits                                                                                                                        |
| 9                   | Write                                                                                                                                         | 9                  | Write                                                                                                                                         |
| 10                  | Acknowledge from slave                                                                                                                        | 10                 | Acknowledge from slave                                                                                                                        |
| 11:18               | Command Code – 8 bits<br>'1xxxxxx' stands for byte operation<br>bit[6:0] of the command code represents the offset of the byte to be accessed | 11:18              | Command Code – 8 bits<br>'1xxxxxx' stands for byte operation<br>bit[6:0] of the command code represents the offset of the byte to be accessed |
| 19                  | Acknowledge from slave                                                                                                                        | 19                 | Acknowledge from slave                                                                                                                        |
| 20:27               | Data byte – 8 bits                                                                                                                            | 20                 | Repeat start                                                                                                                                  |
| 28                  | Acknowledge from slave                                                                                                                        | 21:27              | Slave address – 7 bits                                                                                                                        |
| 29                  | Stop                                                                                                                                          | 28                 | Read                                                                                                                                          |
|                     |                                                                                                                                               | 29                 | Acknowledge from slave                                                                                                                        |
|                     |                                                                                                                                               | 30:37              | Data byte from slave – 8 bits                                                                                                                 |
|                     |                                                                                                                                               | 38                 | Not Acknowledge                                                                                                                               |
|                     |                                                                                                                                               | 39                 | Stop                                                                                                                                          |

## Data Byte Configuration Map

### Data Byte 0

| Bit   | Pin# | Name           | Description                                                                                                                                                         | Power On Default |
|-------|------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
| Bit 7 | --   | Spread Select2 | '000' = OFF<br>'001' = Reserved<br>'010' = Reserved<br>'011' = Reserved<br>'100' = $\pm 0.25\%$<br>'101' = $- 0.5\%$<br>'110' = $\pm 0.5\%$<br>'111' = $\pm 0.38\%$ | 0                |
| Bit 6 | --   | Spread Select1 |                                                                                                                                                                     | 0                |
| Bit 5 | --   | Spread Select0 |                                                                                                                                                                     | 0                |
| Bit 4 | --   | SEL4           |                                                                                                                                                                     | 0                |
| Bit 3 | --   | SEL3           |                                                                                                                                                                     | 0                |
| Bit 2 | --   | SEL2           | SW Frequency selection bits. See <i>Table 4</i> .                                                                                                                   | 0                |
| Bit 1 | --   | SEL1           |                                                                                                                                                                     | 0                |
| Bit 0 | --   | SEL0           |                                                                                                                                                                     | 0                |

### Data Byte 1

| Bit   | Pin#   | Name        | Description       | Power On Default |
|-------|--------|-------------|-------------------|------------------|
| Bit 7 | 38, 37 | CPU1, CPU1# | (Active/Inactive) | 1                |
| Bit 6 | 41, 40 | CPU0, CPU0# | (Active/Inactive) | 1                |
| Bit 5 | 22     | 48MHz       | (Active/Inactive) | 1                |
| Bit 4 | 23     | 24_48MHz    | (Active/Inactive) | 1                |
| Bit 3 | 27     | 3V66_3      | (Active/Inactive) | 1                |

**Data Byte 1 (continued)**

| Bit   | Pin# | Name   | Description       | Power On Default |
|-------|------|--------|-------------------|------------------|
| Bit 2 | 28   | 3V66_2 | (Active/Inactive) | 1                |
| Bit 1 | 30   | 3V66_1 | (Active/Inactive) | 1                |
| Bit 0 | 31   | 3V66_0 | (Active/Inactive) | 1                |

**Data Byte 2**

| Bit   | Pin# | Name     | Pin Description   | Power On Default |
|-------|------|----------|-------------------|------------------|
| Bit 7 | --   | Reserved | Reserved          | 0                |
| Bit 6 | 17   | PCI6     | (Active/Inactive) | 1                |
| Bit 5 | 16   | PCI5     | (Active/Inactive) | 1                |
| Bit 4 | 15   | PCI4     | (Active/Inactive) | 1                |
| Bit 3 | 14   | PCI3     | (Active/Inactive) | 1                |
| Bit 2 | 12   | PCI2     | (Active/Inactive) | 1                |
| Bit 1 | 11   | PCI1     | (Active/Inactive) | 1                |
| Bit 0 | 10   | PCI0     | (Active/Inactive) | 1                |

**Data Byte 3**

| Bit   | Pin#   | Name              | Pin Description   | Power On Default |
|-------|--------|-------------------|-------------------|------------------|
| Bit 7 | 8      | PCI_F2            | (Active/Inactive) | 1                |
| Bit 6 | 7      | PCI_F1            | (Active/Inactive) | 1                |
| Bit 5 | 6      | PCI_F0            | (Active/Inactive) | 1                |
| Bit 4 | --     | Reserved          | Reserved          | 0                |
| Bit 3 | 44, 45 | CPU_ITP, CPU_ITP# | (Active/Inactive) | 1                |
| Bit 2 | --     | Reserved          | Reserved          | 0                |
| Bit 1 | 1      | REF1              | (Active/Inactive) | 1                |
| Bit 0 | 48     | REF0              | (Active/Inactive) | 1                |

**Data Byte 4**

| Bit   | Pin# | Name             | Pin Description                                                                                                                                                                                     | Power On Default |
|-------|------|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
| Bit 7 | --   | MULTSEL_Override | This bit control the selection of IREF multiple.<br>0 = HW control; IREF multiplier is determined by MULTSEL[0:1] input pins<br>1 = SW control; IREF multiplier is determined by Byte[4], Bit[5:6]. | 0                |
| Bit 6 | --   | SW_MULTSEL1      | IREF multiplier<br>00 = loh is 4 x IREF<br>01 = loh is 5 x IREF<br>10 = loh is 6 x IREF<br>11 = loh is 7 x IREF                                                                                     | 0                |
| Bit 5 | --   | SW_MULTSEL0      |                                                                                                                                                                                                     | 0                |
| Bit 4 | --   | Reserved         | Reserved                                                                                                                                                                                            | Reserved         |
| Bit 3 | --   | Reserved         | Reserved                                                                                                                                                                                            | Reserved         |
| Bit 2 | --   | Reserved         | Reserved                                                                                                                                                                                            | Reserved         |
| Bit 1 | --   | Reserved         | Reserved                                                                                                                                                                                            | Reserved         |
| Bit 0 | --   | Reserved         | Reserved                                                                                                                                                                                            | Reserved         |

**Data Byte 5**

| Bit   | Pin# | Name              | Pin Description                                                                                             | Power On Default |
|-------|------|-------------------|-------------------------------------------------------------------------------------------------------------|------------------|
| Bit 7 | 10   | Latched FS4 input | Latched FS[4:0] inputs. These bits are read only.                                                           | X                |
| Bit 6 | 7    | Latched FS3 input |                                                                                                             | X                |
| Bit 5 | 6    | Latched FS2 input |                                                                                                             | X                |
| Bit 4 | 23   | Latched FS1 input |                                                                                                             | X                |
| Bit 3 | 22   | Latched FS0 input |                                                                                                             | X                |
| Bit 2 | --   | FS_Override       | 0 = Select operating frequency by FS[4:0] input pins<br>1 = Select operating frequency by SEL[4:0] settings | 0                |
| Bit 1 | 27   | SEL 3V66          | 0 = 48-MHz output on pin 27<br>1 = 66-MHz output on pin 27                                                  | 0                |
| Bit 0 | 23   | SEL 48MHZ         | 0 = 24-MHz<br>1 = 48-MHz                                                                                    | 0                |

**Data Byte 6**

| Bit   | Pin# | Name         | Pin Description                                                     | Power On Default |
|-------|------|--------------|---------------------------------------------------------------------|------------------|
| Bit 7 |      | Revision_ID3 | Revision ID bit[3]                                                  | 0                |
| Bit 6 |      | Revision_ID2 | Revision ID bit[2]                                                  | 0                |
| Bit 5 |      | Revision_ID1 | Revision ID bit[1]                                                  | 0                |
| Bit 4 |      | Revision_ID0 | Revision ID bit[0]                                                  | 0                |
| Bit 3 |      | Vendor_ID3   | Bit[3] of Cypress Semiconductor's Vendor ID. This bit is read only. | 1                |
| Bit 2 |      | Vendor_ID2   | Bit[2] of Cypress Semiconductor's Vendor ID. This bit is read only. | 0                |
| Bit 1 |      | Vendor_ID1   | Bit[1] of Cypress Semiconductor's Vendor ID. This bit is read only. | 0                |
| Bit 0 |      | Vendor_ID0   | Bit[0] of Cypress Semiconductor's Vendor ID. This bit is read only. | 0                |

**Data Byte 7**

| Bit   | Pin# | Name     | Pin Description | Power On Default |
|-------|------|----------|-----------------|------------------|
| Bit 7 | --   | Reserved | Reserved        | 0                |
| Bit 6 | --   | Reserved | Reserved        | 0                |
| Bit 5 | --   | Reserved | Reserved        | 0                |
| Bit 4 | --   | Reserved | Reserved        | 0                |
| Bit 3 | --   | Reserved | Reserved        | 0                |
| Bit 2 | --   | Reserved | Reserved        | 0                |
| Bit 1 | --   | Reserved | Reserved        | 0                |
| Bit 0 | --   | Reserved | Reserved        | 0                |

**Data Byte 8**

| Bit   | Pin# | Name     | Pin Description | Power On Default |
|-------|------|----------|-----------------|------------------|
| Bit 7 | --   | Reserved | Reserved        | 0                |
| Bit 6 | --   | Reserved | Reserved        | 0                |

**Data Byte 8 (continued)**

| Bit   | Pin# | Name          | Pin Description                                                                                                                                                                                                                                                                                                                                                                                                | Power On Default |
|-------|------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
| Bit 5 | --   | WD_TIMER4     | These bits store the time-out value of the Watchdog Timer. The scale of the timer is determine by the prescaler. The timer can support a value of 150 ms to 4.8 sec when the pre-scaler is set to 150 ms. If the prescaler is set to 2.5 sec, it can support a value from 2.5 sec to 80 sec. When the Watchdog Timer reaches "0," it will set the WD_TO_STATUS bit and generate Reset if RST_EN_WD is enabled. | 1                |
| Bit 4 | --   | WD_TIMER3     |                                                                                                                                                                                                                                                                                                                                                                                                                | 1                |
| Bit 3 | --   | WD_TIMER2     |                                                                                                                                                                                                                                                                                                                                                                                                                | 1                |
| Bit 2 | --   | WD_TIMER1     |                                                                                                                                                                                                                                                                                                                                                                                                                | 1                |
| Bit 1 | --   | WD_TIMER0     |                                                                                                                                                                                                                                                                                                                                                                                                                | 1                |
| Bit 0 | --   | WD_PRE_SCALER | 0 = 150 ms<br>1 = 2.5 sec                                                                                                                                                                                                                                                                                                                                                                                      | 0                |

**Data Byte 9**

| Bit   | Pin# | Name         | Pin Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Power On Default |
|-------|------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
| Bit 7 | --   | 48MHz_DRV    | 48MHz and 24_48MHz clock output drive strength<br>0 = Normal<br>1 = High Drive<br>(Recommend to set to high drive if this output is being used to drive both USB and SIO devices in Intel Brookdale - G platforms)                                                                                                                                                                                                                                                                                                                  | 0                |
| Bit 6 | --   | PCI_DRV      | PCI clock output drive strength<br>0 = Normal<br>1 = High Drive                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 0                |
| Bit 5 | --   | 3V66_DRV     | 3V66 clock output drive strength<br>0 = Normal<br>1 = High Drive                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 0                |
| Bit 4 | --   | RST_EN_WD    | This bit will enable the generation of a Reset pulse when a watchdog timer time-out occurs.<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                                                                                                                          | 0                |
| Bit 3 | --   | RST_EN_FC    | This bit will enable the generation of a Reset pulse after a frequency change occurs.<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                                                                                                                                | 0                |
| Bit 2 | --   | WD_TO_STATUS | Watchdog Timer Time-out Status bit<br>0 = No time-out occurs (Read); Ignore (Write)<br>1 = time-out occurred (Read); Clear WD_TO_STATUS (Write)                                                                                                                                                                                                                                                                                                                                                                                     | 0                |
| Bit 1 | --   | WD_EN        | 0 = Stop and reload Watchdog Timer<br>1 = Enable Watchdog Timer. It will start counting down after a frequency change occurs.<br><b>Note:</b> CY28349 will generate system reset, reload a recovery frequency, and lock itself into a recovery frequency mode after a Watchdog Timer time-out occurs. Under recovery frequency mode, CY28349 will not respond to any attempt to change output frequency via the SMBus control bytes. System software can unlock CY28349 from its recovery frequency mode by clearing the WD_EN bit. | 0                |
| Bit 0 | --   | Reserved     | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 0                |

**Data Byte 10**

| Bit   | Pin# | Name           | Pin Description                                                                                                                                         | Power On Default |
|-------|------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
| Bit 7 | --   | CPU_Skew2      | CPU skew control<br>000 = Normal<br>001 = -150 ps<br>010 = -300 ps<br>011 = -450 ps<br>100 = +150 ps<br>101 = +300 ps<br>110 = +450 ps<br>111 = +600 ps | 0                |
| Bit 6 | --   | CPU_Skew1      |                                                                                                                                                         | 0                |
| Bit 5 | --   | CPU_Skew0      |                                                                                                                                                         | 0                |
| Bit 4 | --   | Fixed 3V66/PCI |                                                                                                                                                         | 0                |
| Bit 3 | --   | PCI_Skew1      | PCI skew control<br>00 = Normal<br>01 = -500 ps<br>10 = Reserved<br>11 = +500 ps                                                                        | 0                |
| Bit 2 | --   | PCI_Skew0      |                                                                                                                                                         | 0                |
| Bit 1 | --   | 3V66_Skew1     | 3V66 skew control<br>00 = Normal<br>01 = -150 ps<br>10 = +150 ps<br>11 = +300 ps                                                                        | 0                |
| Bit 0 | --   | 3V66_Skew0     |                                                                                                                                                         | 0                |

**Data Byte 11**

| Bit   | Pin# | Name         | Pin Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Power On Default |
|-------|------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
| Bit 7 | --   | ROCV_FREQ_N7 | If ROCV_FREQ_SEL is set, the values programmed in ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0] will be used to determine the recovery CPU output frequency when a Watchdog Timer time-out occurs.<br>The setting of FS_Override bit determines the frequency ratio for CPU and other output clocks. When FS_Override bit is cleared, the same frequency ratio stated in the Latched FS[4:0] register will be used. When it is set, the frequency ratio stated in the SEL[4:0] register will be used. | 0                |
| Bit 6 | --   | ROCV_FREQ_N6 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 0                |
| Bit 5 | --   | ROCV_FREQ_N5 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 0                |
| Bit 4 | --   | ROCV_FREQ_N4 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 0                |
| Bit 3 | --   | ROCV_FREQ_N3 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 0                |
| Bit 2 | --   | ROCV_FREQ_N2 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 0                |
| Bit 1 | --   | ROCV_FREQ_N1 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 0                |
| Bit 0 | --   | ROCV_FREQ_N0 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 0                |

**Data Byte 12**

| Bit   | Pin# | Name          | Pin Description                                                                                                                                                                                                                                                                                                      | Power On Default |
|-------|------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
| Bit 7 | --   | ROCV_FREQ_SEL | ROCV_FREQ_SEL determines the source of the recover frequency when a Watchdog Timer time-out occurs. The clock generator will automatically switch to the recovery CPU frequency based on the selection on ROCV_FREQ_SEL.<br>0 = From latched FS[4:0]<br>1 = From the settings of ROCV_FREQ_N[7:0] & ROCV_FREQ_M[6:0] | 0                |

**Data Byte 12 (continued)**

| Bit   | Pin# | Name         | Pin Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Power On Default |
|-------|------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
| Bit 6 | --   | ROCV_FREQ_M6 | If ROCV_FREQ_SEL is set, the values programmed in ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0] will be used to determine the recovery CPU output frequency when a Watchdog Timer time-out occurs. The setting of FS_Override bit determines the frequency ratio for CPU and other output clocks. When FS_Override bit is cleared, the same frequency ratio stated in the Latched FS[4:0] register will be used. When it is set, the frequency ratio stated in the SEL[4:0] register will be used. | 0                |
| Bit 5 | --   | ROCV_FREQ_M5 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 0                |
| Bit 4 | --   | ROCV_FREQ_M4 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 0                |
| Bit 3 | --   | ROCV_FREQ_M3 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 0                |
| Bit 2 | --   | ROCV_FREQ_M2 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 0                |
| Bit 1 | --   | ROCV_FREQ_M1 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 0                |
| Bit 0 | --   | ROCV_FREQ_M0 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 0                |

**Data Byte 13**

| Bit   | Pin# | Name        | Pin Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Power On Default |
|-------|------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
| Bit 7 | --   | CPU_FSEL_N7 | If Prog_Freq_EN is set, the values programmed in CPU_FSEL_N[7:0] and CPU_FSEL_M[6:0] will be used to determine the CPU output frequency. The new frequency will start to load whenever CPU_FSELM[6:0] is updated. The setting of FS_Override bit determines the frequency ratio for CPU and other output clocks. When it is cleared, the same frequency ratio stated in the Latched FS[4:0] register will be used. When it is set, the frequency ratio stated in the SEL[4:0] register will be used. | 0                |
| Bit 6 | --   | CPU_FSEL_N6 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 0                |
| Bit 5 | --   | CPU_FSEL_N5 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 0                |
| Bit 4 | --   | CPU_FSEL_N4 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 0                |
| Bit 3 | --   | CPU_FSEL_N3 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 0                |
| Bit 2 | --   | CPU_FSEL_N2 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 0                |
| Bit 1 | --   | CPU_FSEL_N1 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 0                |
| Bit 0 | --   | CPU_FSEL_N0 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 0                |

**Data Byte 14**

| Bit   | Pin# | Name        | Pin Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Power On Default |
|-------|------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
| Bit 7 | --   | Pro_Freq_EN | Programmable output frequencies enabled<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                                                                                                                                               | 0                |
| Bit 6 | --   | CPU_FSEL_M6 | If Prog_Freq_EN is set, the values programmed in CPU_FSEL_N[7:0] and CPU_FSEL_M[6:0] will be used to determine the CPU output frequency. The new frequency will start to load whenever CPU_FSELM[6:0] is updated. The setting of FS_Override bit determines the frequency ratio for CPU and other output clocks. When it is cleared, the same frequency ratio stated in the Latched FS[4:0] register will be used. When it is set, the frequency ratio stated in the SEL[4:0] register will be used. | 0                |
| Bit 5 | --   | CPU_FSEL_M5 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 0                |
| Bit 4 | --   | CPU_FSEL_M4 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 0                |
| Bit 3 | --   | CPU_FSEL_M3 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 0                |
| Bit 2 | --   | CPU_FSEL_M2 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 0                |
| Bit 1 | --   | CPU_FSEL_M1 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 0                |
| Bit 0 | --   | CPU_FSEL_M0 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 0                |

**Data Byte 15**

| Bit   | Pin# | Name             | Pin Description          | Power On Default |
|-------|------|------------------|--------------------------|------------------|
| Bit 7 | --   | Reserved         | Reserved                 | 0                |
| Bit 6 | --   | Reserved         | Reserved                 | 0                |
| Bit 5 | --   | Reserved         | Reserved                 | 0                |
| Bit 4 | --   | Reserved         | Reserved                 | 0                |
| Bit 3 | --   | Reserved         | Reserved                 | 0                |
| Bit 2 | --   | Reserved         | Reserved                 | 0                |
| Bit 1 | --   | Vendor Test Mode | Reserved. Write with "1" | 1                |
| Bit 0 | --   | Vendor Test Mode | Reserved. Write with "1" | 1                |

**Data Byte 16**

| Bit   | Pin# | Name     | Pin Description | Power On Default |
|-------|------|----------|-----------------|------------------|
| Bit 7 | --   | Reserved | Reserved        | 0                |
| Bit 6 | --   | Reserved | Reserved        | 0                |
| Bit 5 | --   | Reserved | Reserved        | 0                |
| Bit 4 | --   | Reserved | Reserved        | 0                |
| Bit 3 | --   | Reserved | Reserved        | 0                |
| Bit 2 | --   | Reserved | Reserved        | 0                |
| Bit 1 | --   | Reserved | Reserved        | 0                |
| Bit 0 | --   | Reserved | Reserved        | 0                |

**Data Byte 17**

| Bit   | Pin# | Name     | Pin Description | Power On Default |
|-------|------|----------|-----------------|------------------|
| Bit 7 | --   | Reserved | Reserved        | 0                |
| Bit 6 | --   | Reserved | Reserved        | 0                |
| Bit 5 | --   | Reserved | Reserved        | 0                |
| Bit 4 | --   | Reserved | Reserved        | 0                |
| Bit 3 | --   | Reserved | Reserved        | 0                |
| Bit 2 | --   | Reserved | Reserved        | 0                |
| Bit 1 | --   | Reserved | Reserved        | 0                |
| Bit 0 | --   | Reserved | Reserved        | 0                |

**Table 4. Frequency Selection Table**

| Input Conditions |      |      |      |      | Output Frequency |      |      | PLL Gear Constants (G) |
|------------------|------|------|------|------|------------------|------|------|------------------------|
| FS4              | FS3  | FS2  | FS1  | FS0  | CPU              | 3V66 | PCI  |                        |
| SEL4             | SEL3 | SEL2 | SEL1 | SEL0 |                  |      |      |                        |
| 0                | 0    | 0    | 0    | 0    | 100.7            | 67.1 | 33.6 | 48.00741               |
| 0                | 0    | 0    | 0    | 1    | 100.9            | 67.3 | 33.6 | 48.00741               |
| 0                | 0    | 0    | 1    | 0    | 108.0            | 72.0 | 36.0 | 48.00741               |
| 0                | 0    | 0    | 1    | 1    | 101.2            | 67.5 | 33.7 | 48.00741               |
| 0                | 0    | 1    | 0    | 0    | 114.0            | 76.0 | 38.0 | 48.00741               |
| 0                | 0    | 1    | 0    | 1    | 117.0            | 78.0 | 39.0 | 48.00741               |
| 0                | 0    | 1    | 1    | 0    | 120.0            | 80.0 | 40.0 | 48.00741               |
| 0                | 0    | 1    | 1    | 1    | 123.0            | 82.0 | 41.0 | 48.00741               |
| 0                | 1    | 0    | 0    | 0    | 126.0            | 63.0 | 31.5 | 48.00741               |
| 0                | 1    | 0    | 0    | 1    | 130.0            | 65.0 | 32.5 | 48.00741               |
| 0                | 1    | 0    | 1    | 0    | 133.9            | 67.0 | 33.5 | 48.00741               |
| 0                | 1    | 0    | 1    | 1    | 134.2            | 67.1 | 33.6 | 48.00741               |
| 0                | 1    | 1    | 0    | 0    | 134.5            | 67.3 | 33.6 | 48.00741               |
| 0                | 1    | 1    | 0    | 1    | 148.0            | 74.0 | 37.0 | 48.00741               |
| 0                | 1    | 1    | 1    | 0    | 152.0            | 76.0 | 38.0 | 48.00741               |
| 0                | 1    | 1    | 1    | 1    | 156.0            | 78.0 | 39.0 | 48.00741               |
| 1                | 0    | 0    | 0    | 0    | 160.0            | 80.0 | 40.0 | 48.00741               |
| 1                | 0    | 0    | 0    | 1    | 164.0            | 82.0 | 41.0 | 48.00741               |

**Table 4. Frequency Selection Table**

| Input Conditions |      |      |      |      | Output Frequency |      |      | PLL Gear Constants (G) |
|------------------|------|------|------|------|------------------|------|------|------------------------|
| FS4              | FS3  | FS2  | FS1  | FS0  | CPU              | 3V66 | PCI  |                        |
| SEL4             | SEL3 | SEL2 | SEL1 | SEL0 |                  |      |      |                        |
| 1                | 0    | 0    | 1    | 0    | 167.4            | 66.9 | 33.5 | 48.00741               |
| 1                | 0    | 0    | 1    | 1    | 170.0            | 68.0 | 34.0 | 48.00741               |
| 1                | 0    | 1    | 0    | 0    | 175.0            | 70.0 | 35.0 | 48.00741               |
| 1                | 0    | 1    | 0    | 1    | 180.0            | 72.0 | 36.0 | 48.00741               |
| 1                | 0    | 1    | 1    | 0    | 185.0            | 74.0 | 37.0 | 48.00741               |
| 1                | 0    | 1    | 1    | 1    | 190.0            | 76.0 | 38.0 | 48.00741               |
| 1                | 1    | 0    | 0    | 0    | 166.8            | 66.7 | 33.4 | 48.00741               |
| 1                | 1    | 0    | 0    | 1    | 100.2            | 66.8 | 33.4 | 48.00741               |
| 1                | 1    | 0    | 1    | 0    | 133.6            | 66.8 | 33.4 | 48.00741               |
| 1                | 1    | 0    | 1    | 1    | 200.4            | 66.8 | 33.4 | 48.00741               |
| 1                | 1    | 1    | 0    | 0    | 166.6            | 66.6 | 33.3 | 48.00741               |
| 1                | 1    | 1    | 0    | 1    | 100.0            | 66.6 | 33.3 | 48.00741               |
| 1                | 1    | 1    | 1    | 0    | 200.0            | 66.6 | 33.3 | 48.00741               |
| 1                | 1    | 1    | 1    | 1    | 133.3            | 66.6 | 33.3 | 48.00741               |

### Programmable Output Frequency, Watchdog Timer and Recovery Output Frequency Functional Description

The Programmable Output Frequency feature allows users to generate any CPU output frequency from the range of 50 MHz to 248 MHz. Cypress offers the most dynamic and the simplest programming interface for system developers to utilize this feature in their platforms.

The Watchdog Timer and Recovery Output Frequency features allow users to implement a recovery mechanism when the system hangs or gets unstable. System BIOS or other control software can enable the Watchdog Timer before they attempt to make a frequency change. If the system hangs and a Watchdog Timer time-out occurs, a system reset will be generated and a recovery frequency will be activated.

All of the related registers are summarized in *Table 5*.

**Table 5. Register Summary**

| Name          | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Pro_Freq_EN   | Programmable output frequencies enabled<br>0 = Disabled (default)<br>1 = Enabled<br>When it is disabled, the operating output frequency will be determined by either the latched value of FS[4:0] inputs or the programmed value of SEL[4:0]. If FS_Override bit is clear, latched FS[4:0] inputs will be used. If FS_Override bit is set, programmed value of SEL[4:0] will be used.<br>When it is enabled, the CPU output frequency will be determined by the programmed value of CPUFSEL_N, CPUFSEL_M and the PLL Gear Constant. The program value of FS_Override, SEL[4:0] or the latched value of FS[4:0] will determine the PLL Gear Constant and the frequency ratio between CPU and other frequency outputs |
| FS_Override   | When Pro_Freq_EN is cleared or disabled,<br>0 = Select operating frequency by FS input pins (default)<br>1 = Select operating frequency by SEL bits in SMBus control bytes<br>When Pro_Freq_EN is set or enabled,<br>0 = Frequency output ratio between CPU and other frequency groups and the PLL Gear Constant are based on the latched value of FS input pins (default)<br>1 = Frequency output ratio between CPU and other frequency groups and the PLL Gear Constant are based on the programmed value of SEL bits in SMBus control bytes                                                                                                                                                                      |
| ROCV_FREQ_SEL | ROCV_FREQ_SEL determines the source of the recover frequency when a Watchdog timer time-out occurs. The clock generator will automatically switch to the recovery CPU frequency based on the selection on ROCV_FREQ_SEL.<br>0 = From latched FS[4:0]<br>1 = From the settings of ROCV_FREQ_N[7:0] & ROCV_FREQ_M[6:0]                                                                                                                                                                                                                                                                                                                                                                                                |

**Table 5. Register Summary** (continued)

| Name                                  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|---------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CPU_FSEL_N,<br>CPU_FSEL_M             | When Prog_Freq_EN is set or enabled, the values programmed in CPU_FSEL_N[7:0] and CPU_FSEL_M[6:0] determines the CPU output frequency. The new frequency will start to load whenever there is an update to either CPU_FSEL_N[7:0] or CPU_FSEL_M[6:0]. Therefore, it is recommended to use Word or Block write to update both registers within the same SMBus bus operation. The setting of FS_Override bit determines the frequency ratio for CPU, AGP and PIC. When FS_Override is cleared or disabled, the frequency ratio follows the latched value of the FS input pins. When FS_Override is set or enabled, the frequency ratio follows the programmed value of SEL bits in SMBus control bytes.        |
| ROCV_FREQ_N[7:0],<br>ROCV_FREQ_M[6:0] | When ROCV_FREQ_SEL is set, the values programmed in ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0] will be used to determine the recovery CPU output frequency when a Watchdog Timer time-out occurs. The setting of FS_Override bit determines the frequency ratio for CPU, AGP and PIC. When it is cleared, the same frequency ratio stated in the Latched FS[4:0] register will be used. When it is set, the frequency ratio stated in the SEL[4:0] register will be used. The new frequency will start to load whenever there is an update to either ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0]. Therefore, it is recommended to use Word or Block Write to update both registers within the same SMBus bus operation. |
| WD_EN                                 | 0 = Stop and reload Watchdog Timer<br>1 = Enable Watchdog timer. It will start counting down after a frequency change occurs.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| WD_TO_STATUS                          | Watchdog Timer Time-out Status bit<br>0 = No time-out occurs (READ); Ignore (WRITE)<br>1 = Time-out occurred (READ); Clear WD_TO_STATUS (WRITE)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| WD_TIMER[4:0]                         | These bits store the time-out value of the Watchdog timer. The scale of the timer is determined by the pre-scaler.<br>The timer can support a value of 150 ms to 4.8 sec when the prescaler is set to 150 ms. If the prescaler is set to 2.5 sec, it can support a value from 2.5 sec to 80 sec.<br>When the Watchdog timer reaches "0", it will set the WD_TO_STATUS bit.                                                                                                                                                                                                                                                                                                                                   |
| WD_PRE_SCALER                         | 0 = 150 ms<br>1 = 2.5 sec                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| RST_EN_WD                             | This bit will enable the generation of a Reset pulse when a Watchdog timer time-out occurs.<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| RST_EN_FC                             | This bit will enable the generation of a Reset pulse after a frequency change occurs.<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

**Program the CPU Output Frequency**

When the programmable output frequency feature is enabled (Pro\_Freq\_EN bit is set), the CPU output frequency is determined by the following equation:

$$F_{cpu} = G * (N+3)/(M+3)$$

"N" and "M" are the values programmed in Programmable Frequency Select N-Value Register and M-Value Register, respectively.

"G" stands for the PLL Gear Constant, which is determined by the programmed value of FS[4:0] or SEL[4:0]. The value is listed in *Table 4*.

The ratio of (N+3) and (M+3) need to be greater than "1" [(N+3)/(M+3) > 1].

The following table lists set of N and M values for different frequency output ranges. This example uses a fixed value for the M-Value Register and selects the CPU output frequency by changing the value of the N-Value Register.

**Table 6. Examples of N and M Value for Different CPU Frequency Range**

| Frequency Ranges | Gear Constants | Fixed Value for M-Value Register | Range of N-Value Register for Different CPU Frequency |
|------------------|----------------|----------------------------------|-------------------------------------------------------|
| 50 MHz–129 MHz   | 48.00741       | 93                               | 97–255                                                |
| 130 MHz–248 MHz  | 48.00741       | 45                               | 127–245                                               |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage.....–0.5 to +7.0V

Input Voltage..... –0.5V to  $V_{DD}+0.5$

Storage Temperature (Non-Condensing) ....–65°C to +150°C

Max. Soldering Temperature (10 sec) ..... +260°C

Junction Temperature..... +150°C

Package Power Dissipation..... 1W

Static Discharge Voltage .....  
(per MIL-STD-883, Method 3015) ..... >2000V

## Operating Conditions<sup>[2]</sup> Over which Electrical Parameters are Guaranteed

| Parameter                                                                                                      | Description                                           | Min.   | Max.     | Unit |
|----------------------------------------------------------------------------------------------------------------|-------------------------------------------------------|--------|----------|------|
| $V_{DD\_REF}$ , $V_{DD\_PCI}$ , $V_{DD\_CORE}$ ,<br>$V_{DD\_3V66}$ , $V_{DD\_48\text{ MHz}}$ , $V_{DD\_CPU}$ , | 3.3V Supply Voltages                                  | 3.135  | 3.465    | V    |
| $T_A$                                                                                                          | Operating Temperature, Ambient                        | 0      | 70       | °C   |
| $C_{in}$                                                                                                       | Input Pin Capacitance                                 |        | 5        | pF   |
| $C_{XTAL}$                                                                                                     | XTAL Pin Capacitance                                  |        | 22.5     | pF   |
| $C_L$                                                                                                          | Max. Capacitive Load on<br>48MHz, REF<br>PCICLK, 3V66 |        | 20<br>30 | pF   |
| $f_{(REF)}$                                                                                                    | Reference Frequency, Oscillator Nominal Value         | 14.318 | 14.318   | MHz  |

## Electrical Characteristics Over the Operating Range

| Parameter   | Description               | Test Conditions                                                      | Min.                      | Max. | Unit |
|-------------|---------------------------|----------------------------------------------------------------------|---------------------------|------|------|
| $V_{IH}$    | High-level Input Voltage  | Except Crystal Pads. Threshold voltage for crystal pads = $V_{DD}/2$ | 2.0                       |      | V    |
| $V_{IL}$    | Low-level Input Voltage   | Except Crystal Pads                                                  |                           | 0.8  | V    |
| $V_{OH}$    | High-level Output Voltage | 48MHz, REF, 3V66                                                     | $I_{OH} = -1\text{ mA}$   | 2.4  | V    |
|             |                           | PCI                                                                  |                           | 2.4  | V    |
| $V_{OL}$    | Low-level Output Voltage  | 48MHz, REF, 3V66                                                     | $I_{OL} = 1\text{ mA}$    | 0.4  | V    |
|             |                           | PCI                                                                  |                           | 0.55 | V    |
| $I_{IH}$    | Input High Current        | $0 \leq V_{IN} \leq V_{DD}$                                          | –5                        | 5    | mA   |
| $I_{IL}$    | Input Low Current         | $0 \leq V_{IN} \leq V_{DD}$                                          | –5                        | 5    | mA   |
| $I_{OH}$    | High-level Output Current | CPU<br>For $I_{OH} = 6 \cdot I_{Ref}$ Configuration                  | Type X1, $V_{OH} = 0.65V$ | 12.9 | mA   |
|             |                           |                                                                      | Type X1, $V_{OH} = 0.74V$ | 14.9 |      |
|             |                           | REF, 48 MHz                                                          | Type 3, $V_{OH} = 1.00V$  | –29  |      |
|             |                           |                                                                      | Type 3, $V_{OH} = 3.135V$ | –23  |      |
|             |                           | 3V66, PCI                                                            | Type 5, $V_{OH} = 1.00V$  | –33  |      |
|             |                           |                                                                      | Type 5, $V_{OH} = 3.135V$ | –33  |      |
| $I_{OL}$    | Low-level Output Current  | REF, 48MHz                                                           | Type 3, $V_{OL} = 1.95V$  | 29   | mA   |
|             |                           |                                                                      | Type 3, $V_{OL} = 0.4V$   | 27   |      |
|             |                           | 3V66, PCI,                                                           | Type 5, $V_{OL} = 1.95V$  | 30   |      |
|             |                           |                                                                      | Type 5, $V_{OL} = 0.4V$   | 38   |      |
| $I_{OZ}$    | Output Leakage Current    | Three-state                                                          |                           | 10   | mA   |
| $I_{DD3}$   | 3.3V Power Supply Current | $V_{DD\_CORE}/V_{DD33} = 3.465V$ , $F_{CPU} = 133\text{ MHz}$        |                           | 250  | mA   |
| $I_{DDPD3}$ | 3.3V Shutdown Current     | $V_{DD\_CORE}/V_{DDQ3} = 3.465V$                                     | 20                        | 40   | mA   |

### Note:

2. Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

**Switching Characteristics<sup>[3]</sup> Over the Operating Range**

| Parameter       | Output     | Description                      | Test Conditions                                                           | Min.        | Max.           | Unit |
|-----------------|------------|----------------------------------|---------------------------------------------------------------------------|-------------|----------------|------|
| $t_1$           | All        | Output Duty Cycle <sup>[4]</sup> | $t_{1A}/(t_{1B})$                                                         | 45          | 55             | %    |
| $t_2$           | CPU        | Rise Time                        | Measured at 20% to 80% of $V_{oh}$                                        | 175         | 700            | ps   |
| $t_2$           | 48MHz, REF | Rising Edge Rate                 | Between 0.4V and 2.4V                                                     | 0.5         | 2.0            | V/ns |
| $t_2$           | PCI, 3V66, | Rising Edge Rate                 | Between 0.4V and 2.4V                                                     | 1.0         | 4.0            | V/ns |
| $t_3$           | CPU        | Fall Time                        | Measured at 80% to 20% of $V_{oh}$                                        | 175         | 700            | ps   |
| $t_3$           | 48MHz, REF | Falling Edge Rate                | Between 2.4V and 0.4V                                                     | 0.5         | 2.0            | V/ns |
| $t_3$           | PCI, 3V66  | Falling Edge Rate                | Between 2.4V and 0.4V                                                     | 1.0         | 4.0            | V/ns |
| $t_4$           | CPU        | CPU-CPU Skew                     | Measured at Crossover                                                     |             | 150            | ps   |
| $t_5$           | 3V66 [0:1] | 3V66-3V66 Skew                   | Measured at 1.5V                                                          |             | 500            | ps   |
| $t_6$           | PCI        | PCI-PCI Skew                     | Measured at 1.5V                                                          |             | 500            | ps   |
| $t_7$           | 3V66, PCI  | 3V66-PCI Clock Skew              | 3V66 leads. Measured at 1.5V                                              | 1.5         | 3.5            | ns   |
| $t_8$           | CPU        | Cycle-Cycle Clock Jitter         | Measured at Crossover $t_8 = t_{8A} - t_{8B}$<br>With all outputs running |             | 200            | ps   |
| $t_9$           | 3V66       | Cycle-Cycle Clock Jitter         | Measured at 1.5V $t_9 = t_{9A} - t_{9B}$                                  |             | 250            | ps   |
| $t_9$           | 48MHz      | Cycle-Cycle Clock Jitter         | Measured at 1.5V $t_9 = t_{9A} - t_{9B}$                                  |             | 350            | ps   |
| $t_9$           | PCI        | Cycle-Cycle Clock Jitter         | Measured at 1.5V $t_9 = t_{9A} - t_{9B}$                                  |             | 500            | ps   |
| $t_9$           | REF        | Cycle-Cycle Clock Jitter         | Measured at 1.5V $t_9 = t_{9A} - t_{9B}$                                  |             | 1000           | ps   |
|                 | CPU, PCI   | Settle Time                      | CPU and PCI clock stabilization from power-up                             |             | 3              | ms   |
|                 | CPU        | Rise/Fall Matching               | Measured with test loads <sup>[5, 6]</sup>                                |             | 20%            |      |
|                 | CPU        | Overshoot                        | Measured with test loads <sup>[6]</sup>                                   |             | $V_{oh} + 0.2$ | V    |
|                 | CPU        | Undershoot                       | Measured with test loads <sup>[6]</sup>                                   | -0.2        |                | V    |
| $V_{oh}$        | CPU        | High-level Output Voltage        | Measured with test loads <sup>[6]</sup>                                   | 0.65        | 0.74           | V    |
| $V_{ol}$        | CPU        | Low-level Output Voltage         | Measured with test loads <sup>[6]</sup>                                   | 0.0         | 0.05           | V    |
| $V_{crossover}$ | CPU        | Crossover Voltage                | Measured with test loads <sup>[6]</sup>                                   | 45% of 0.65 | 55% of 0.74    | V    |

**Notes:**

3. All parameters specified with loaded outputs.

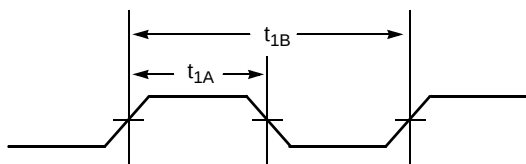
4. Duty cycle is measured at 1.5V when  $V_{DD} = 3.3V$ . When  $V_{DD} = 2.5V$ , duty cycle is measured at 1.25V.

5. Determined as a fraction of  $2 \cdot (Trp - Trn) / (Trp + Trn)$  Where Trp is a rising edge and Trn is an intersecting falling edge.

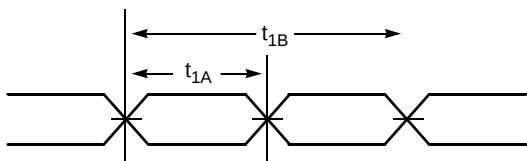
6. The test load is  $R_s = 33.2\Omega$ ,  $R_p = 49.9\Omega$  in test circuit.

## Switching Waveforms

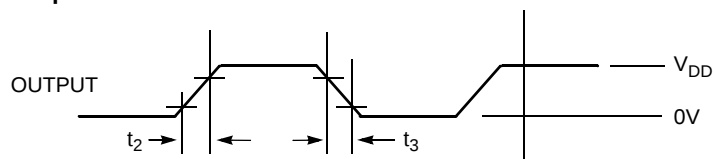
### Duty Cycle Timing (Single Ended Output)



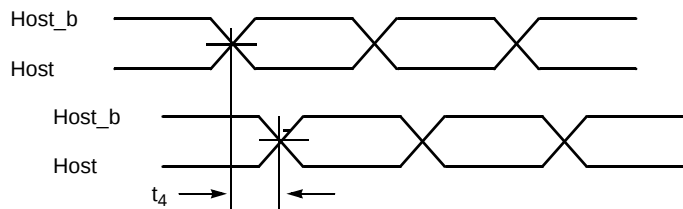
### Duty Cycle Timing (CPU Differential Output)



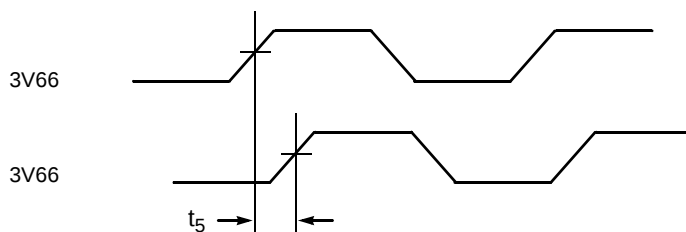
### All Outputs Rise/Fall Time



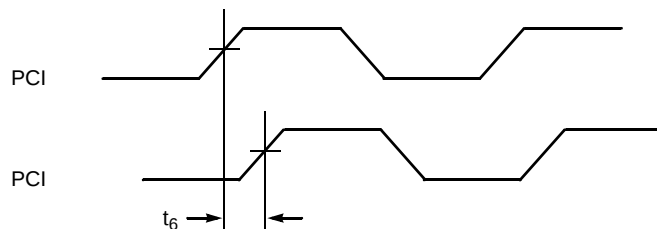
### CPU-CPU Clock Skew

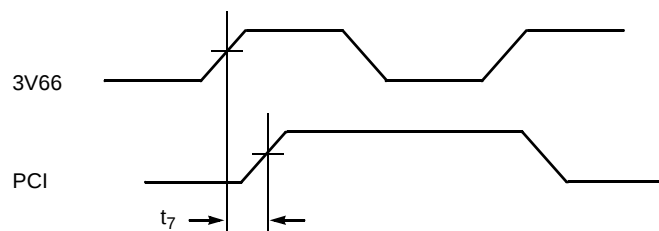
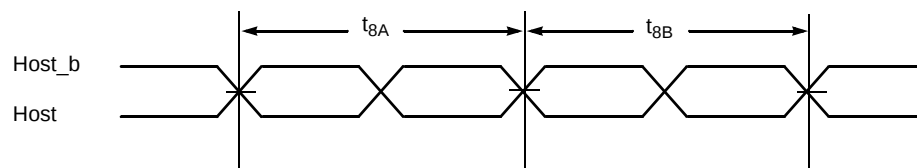
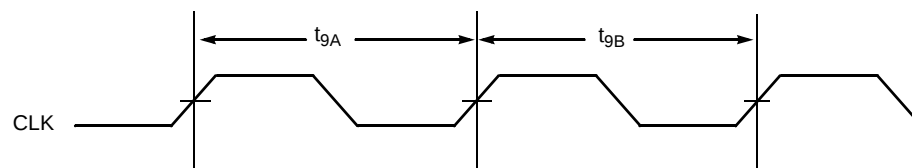


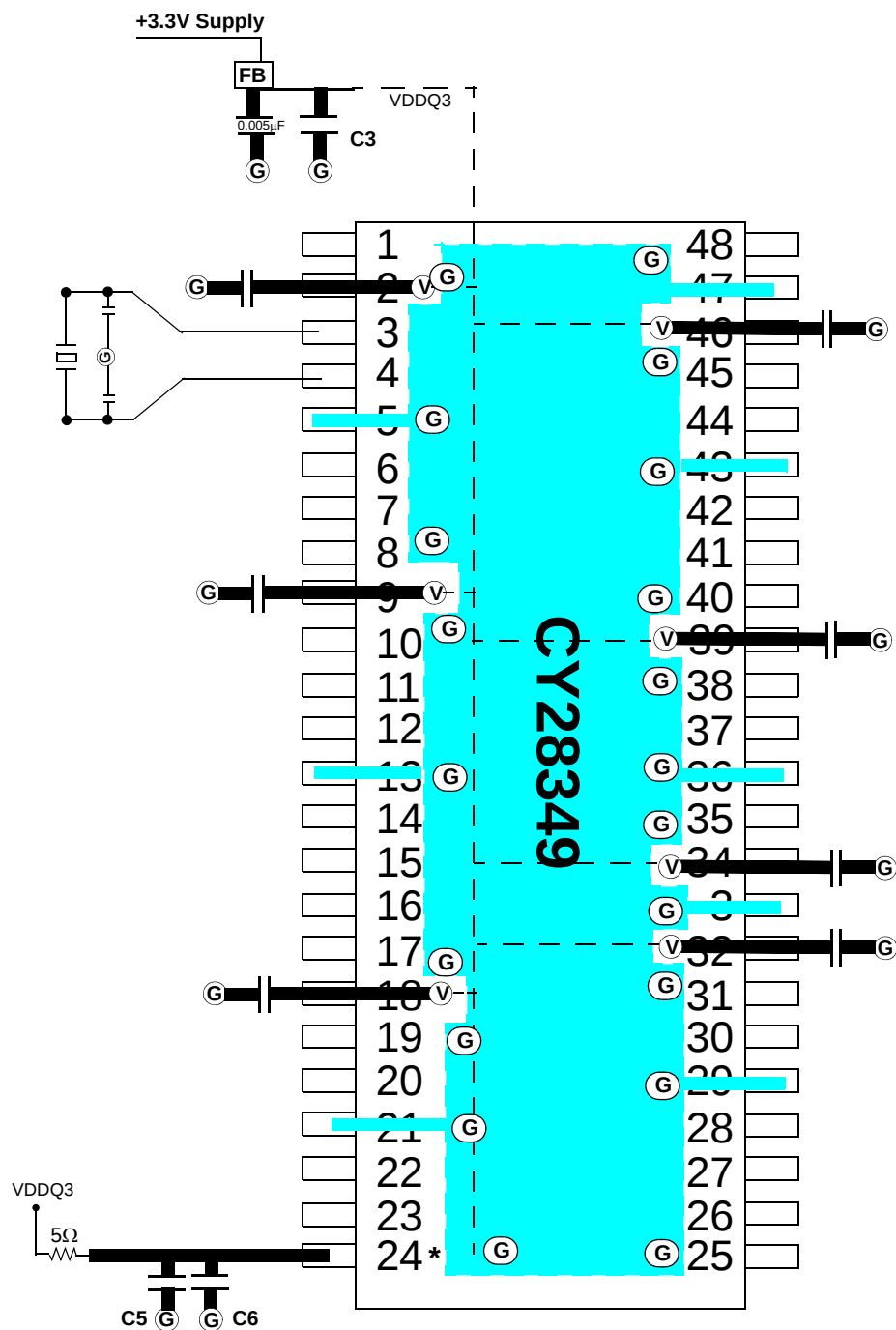
### 3V66-3V66 Clock Skew



### PCI-PCI Clock Skew



**Switching Waveforms (continued)**
**3V66-PCI Clock Skew**

**CPU Clock Cycle-Cycle Jitter**

**Cycle-Cycle Clock Jitter**


**Layout Example**


**FB = Dale ILB1206 - 300 (300  $\Omega$  @ 100 MHz)**

**Ceramic Caps C3 = 10–22  $\mu\text{F}$  C4 = 0.005  $\mu\text{F}$  C5 = 10  $\mu\text{F}$  C6 = 0.1  $\mu\text{F}$**

**(G) = VIA to GND plane layer (V) = VIA to respective supply plane layer**

**Note: Each supply plane or strip should have a ferrite bead and capacitors**

**All bypass caps = 0.1  $\mu\text{F}$  ceramic**

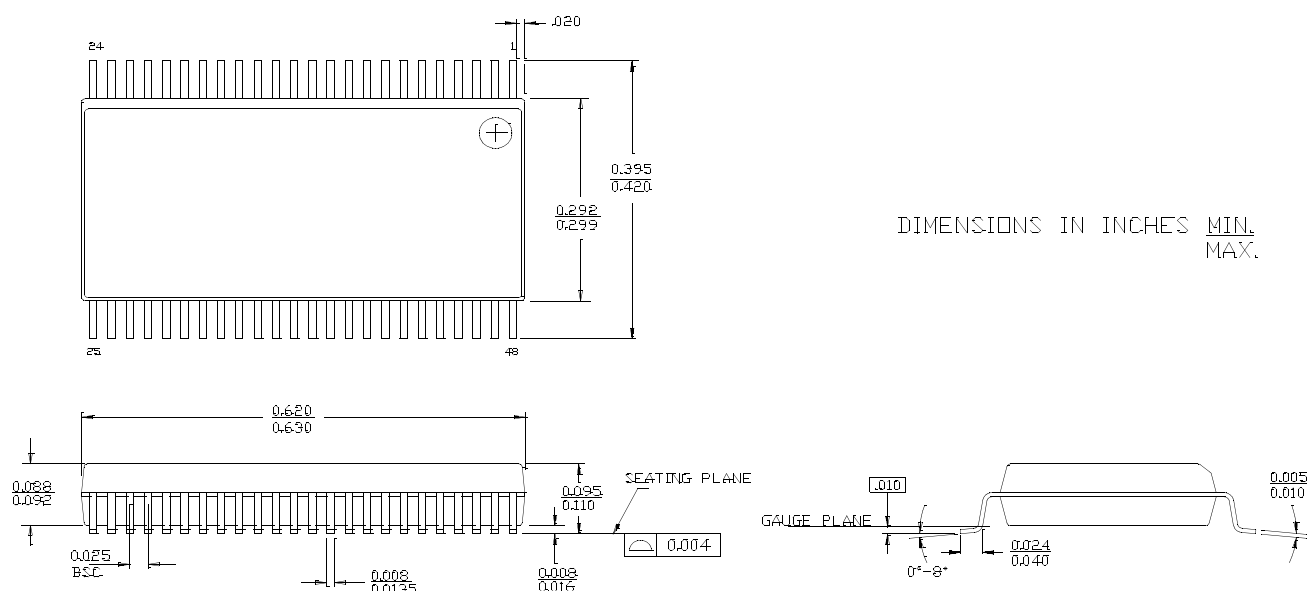
**\* For use with onboard video using 48 MHz for Dot Clock or connect to VDDQ3**

## Ordering Information

| Ordering Code    | Package Type                                               | Operating Range |
|------------------|------------------------------------------------------------|-----------------|
| CY28349OC        | 48-pin Small Shrunk Outline Package (SSOP)                 | Commercial      |
| CY28349OCT       | 48-pin Small Shrunk Outline Package (SSOP) - Tape and Reel | Commercial      |
| <b>Lead-free</b> |                                                            |                 |
| CY28349OXC       | 48-pin Small Shrunk Outline Package (SSOP)                 | Commercial      |
| CY28349OXCT      | 48-pin Small Shrunk Outline Package (SSOP) - Tape and Reel | Commercial      |

## Package Diagram

**48-Lead Shrunk Small Outline Package O48**



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