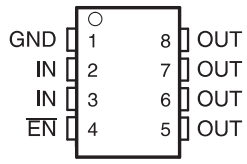
POWER-DISTRIBUTION SWITCHES

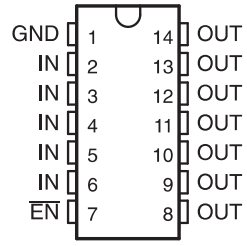
FEATURES

- **33-mΩ (5-V Input) High-Side MOSFET Switch**
- **Short-Circuit and Thermal Protection**
- **Operating Range . . . 2.7 V to 5.5 V**
- **Logic-Level Enable Input**
- **Typical Rise Time. . . 6.1 ms**
- **Undervoltage Lockout**
- **Maximum Standby Supply Current. . . 10 µA**
- **No Drain-Source Back-Gate Diode**
- **Available in 8-pin SOIC and 14-Pin TSSOP Packages**
- **Ambient Temperature Range, –40°C to 85°C**
- **2-kV Human-Body-Model, 200-V Machine-Model ESD Protection**

D PACKAGE
(TOP VIEW)



PWP PACKAGE
(TOP VIEW)



DESCRIPTION

The TPS201xA family of power distribution switches is intended for applications where heavy capacitive loads and short circuits are likely to be encountered. These devices are 50-mΩ N-channel MOSFET high-side power switches. The switch is controlled by a logic enable compatible with 5-V logic and 3-V logic. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the TPS201xA limits the output current to a safe level by switching into a constant-current mode. When continuous heavy overloads and short circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until valid input voltage is present.

GENERAL SWITCH CATALOG

33 mΩ, single	80 mΩ, single	80 mΩ, dual	80 mΩ, dual	80 mΩ, triple	80 mΩ, quad	80 mΩ, quad
TPS201xA 0.2 A - 2 A	TPS2014 600 mA	TPS2042B 500 mA	TPS2080 500 mA	TPS2043B 500 mA	TPS2044B 500 mA	TPS2085 500 mA
TPS202x 0.2 A - 2 A	TPS2015 1 A	TPS2052B 500 mA	TPS2081 500 mA	TPS2053B 500 mA	TPS2054B 500 mA	TPS2086 500 mA
TPS203x 0.2 A - 2 A	TPS2041B 500 mA	TPS2046B 250 mA	TPS2082 500 mA	TPS2047B 250 mA	TPS2048A 250 mA	TPS2087 500 mA
	TPS2051B 500 mA	TPS2056 250 mA	TPS2090 250 mA	TPS2057A 250 mA	TPS2058 250 mA	TPS2095 250 mA
	TPS2045A 250 mA	TPS2062 1 A	TPS2091 250 mA	TPS2063 1 A		TPS2096 250 mA
	TPS2049 100 mA	TPS2066 1 A	TPS2092 250 mA	TPS2067 1 A		TPS2097 250 mA
	TPS2055A 250 mA	TPS2060 1.5 A				
	TPS2061 1 A	TPS2064 1.5 A				
	TPS2065 1 A					
	TPS2068 1.5 A					
	TPS2069 1.5 A					

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

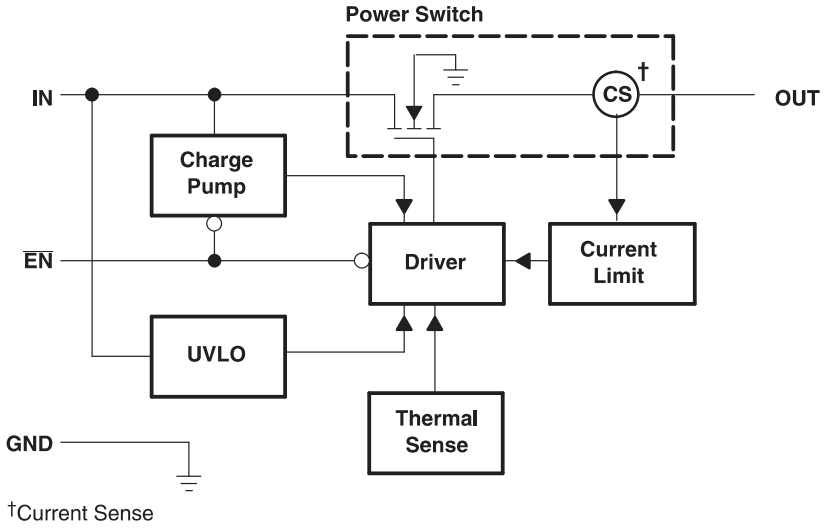
The TPS201xA devices differ only in short-circuit current threshold. The TPS2010A limits at 0.3-A load, the TPS2011 at 0.9-A load, the TPS2012A at 1.5-A load, and the TPS2013A at 2.2-A load (see Available Options). The TPS201xA is available in an 8-pin small-outline integrated-circuit (SOIC) package and in a 14-pin thin-shrink small-outline package (TSSOP) and operates over a junction temperature range of -40°C to 125°C.)

AVAILABLE OPTIONS

T_A	ENABLE	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A)	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (A)	PACKAGED DEVICES(1)	
				SMALL OUTLINE (D)(2)	TSSOP (PWP)(3)
–40°C to 85°C	Active low	0.2	0.3	TPS2010AD	TPS2010APWPR
		0.6	0.9	TPS2011AD	TPS2011APWPR
		1	1.5	TPS2012AD	TPS2012APWPR
		1.5	2.2	TPS2013AD	TPS2013APWPR

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2010DR)
(3) The PWP package is only available left-end taped-and-reeled.

TPS201xA FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	D	PWP		
$\overline{EN}$	4	7	I	Enable input. Logic low turns on power switch.
GND	1	1	I	Ground
IN	2, 3	2–6	I	Input voltage
OUT	5–8	8–14	O	Power-switch output

DETAILED DESCRIPTION

POWER SWITCH

The power switch is an N-channel MOSFET with a maximum on-state resistance of 50 mΩ ($V_{I(IN)}$ = 5V). Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled.

CHARGE PUMP

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

DRIVER

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 9-ms range.

ENABLE ($\overline{EN}$)

The logic enable disables the power switch, the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10 µA when a logic high is present on $\overline{EN}$. A logic zero input on $\overline{EN}$ restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

CURRENT SENSE

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver, in turn, reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant current mode and holds the current constant while varying the voltage on the load.

THERMAL SENSE

An internal thermal-sense circuit shuts off the power switch when the junction temperature rises to approximately 140°C. Hysteresis is built into the thermal sense circuit. After the device has cooled approximately 20°C, the switch turns back on. The switch continues to cycle off and on until the fault is removed.

UNDERVOLTAGE LOCKOUT

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE	UNIT
$V_{I(IN)}$	Input voltage range(2)		–0.3 to 6	V
$V_{O(OUT)}$	Output voltage range(2)		–0.3 to $V_{I(IN)}$ + 0.3	V
$V_{I(EN)}$	Input voltage range		–0.3 to 6	V
$I_{O(OUT)}$	Continuous output current		Internally Limited	
	Continuous total power dissipation		See Dissipation Rating Table	
T_J	Operating virtual junction temperature range		–40 to 125	°C
T_{stg}	Storage temperature range		–65 to 150	°C
	Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds		260	°C
ESD	Electrostatic discharge protection	Human body model	2	kV
		Machine model	200	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND.

DISSIPATION RATINGS

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
PWP	700 mW	5.6 mW/°C	448 mW	364 mW

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{I(IN)}$	Input voltage		2.7	5.5	V
V_{IH}			0	5.5	
I_O	Continuous output current	TPS2010A	0	0.2	A
		TPS2011A	0	0.6	
		TPS2012A	0	1	
		TPS2013A	0	1.5	
T_J	Operating virtual junction temperature		–40	125	°C

ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = rated current, $\overline{EN}$ = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]				MIN	TYP	MAX	UNIT
POWER SWITCH									
$r_{DS(on)}$	Static drain-source on-state resistance	$V_{I(IN)}$ = 5 V,	T_J = 25°C,	I_O = 1.5 A	TPS2013A		33	36	mΩ
		$V_{I(IN)}$ = 5 V,	T_J = 85°C,	I_O = 1.5 A			38	46	
		$V_{I(IN)}$ = 5 V,	T_J = 125°C,	I_O = 1.5 A			44	50	
		$V_{I(IN)}$ = 3.3 V,	T_J = 25°C,	I_O = 1.5 A			37	41	
		$V_{I(IN)}$ = 3.3 V,	T_J = 85°C,	I_O = 1.5 A			43	52	
		$V_{I(IN)}$ = 3.3 V,	T_J = 125°C,	I_O = 1.5 A			51	61	
		$V_{I(IN)}$ = 5 V,	T_J = 25°C,	I_O = 0.18 A	TPS2010A		30	34	mΩ
		$V_{I(IN)}$ = 5 V,	T_J = 85°C,	I_O = 0.18 A			35	41	
		$V_{I(IN)}$ = 5 V,	T_J = 125°C,	I_O = 0.18 A			39	47	
		$V_{I(IN)}$ = 3.3 V,	T_J = 25°C,	I_O = 0.18 A			33	37	
		$V_{I(IN)}$ = 3.3 V,	T_J = 85°C,	I_O = 0.18 A			39	46	
		$V_{I(IN)}$ = 3.3 V,	T_J = 125°C,	I_O = 0.18 A			44	56	
t_r	Rise time, output	$V_{I(IN)}$ = 5.5 V,	T_J = 25°C,	C_L = 1 µF,	R_L = 10 Ω		6.1		ms
		$V_{I(IN)}$ = 2.7 V,	T_J = 25°C,	C_L = 1 µF,	R_L = 10 Ω		8.6		
t_f	Rise time, output	$V_{I(IN)}$ = 5.5 V,	T_J = 25°C,	C_L = 1 µF,	R_L = 10 Ω		3.4		ms
		$V_{I(IN)}$ = 2.7 V,	T_J = 25°C,	C_L = 1 µF,	R_L = 10 Ω		3		
ENABLE INPUT ($\overline{EN}$)									
V_{IH}	High-level input voltage	2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V				2			V
V_{IL}	Low-level input voltage	4.5 V ≤ $V_{I(IN)}$ ≤ 5.5 V						0.8	V
		2.7 V ≤ $V_{I(IN)}$ ≤ 4.5 V						0.5	
I_I	Input current	$\overline{EN}$ = 0 V or $\overline{EN}$ = $V_{I(IN)}$				–0.5		0.5	µA
t_{on}	Turnon time	C_L = 100 µF,		R_L = 10 Ω				20	ms
t_{off}	Turnoff time	C_L = 100 µF,		R_L = 10 Ω				40	ms
CURRENT LIMIT									
I_{OS}	Short-circuit output current	T_J = 25°C, V_I = 5.5 V, OUT connected to GND, Device enable into short circuit			TPS2010A	0.22	0.3	0.4	A
					TPS2011A	0.66	0.9	1.1	
					TPS2012A	1.1	1.5	1.8	
					TPS2013A	1.65	2.2	2.7	

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

ELECTRICAL CHARACTERISTICS (Continued)

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = rated current, $\overline{EN}$ = 0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]			MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
Supply current, low-level output	No Load on OUT	$\overline{EN}$ = $V_{I(IN)}$	T_J = 25°C		0.3	1	µA
			–40°C ≤ T_J ≤ 125°C			10	
Supply current, high-level output	No Load on OUT	$\overline{EN}$ = 0 V	T_J = 25°C		58	75	µA
			–40°C ≤ T_J ≤ 125°C		75	100	
Leakage current	OUT connected to ground	$\overline{EN}$ = $V_{I(IN)}$	–40°C ≤ T_J ≤ 125°C		10		µA
UNDERVOLTAGE LOCKOUT							
Low-level input voltage				2		2.5	V
Hysteresis	T_J = 25°C				100		mV

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

PARAMETER MEASUREMENT INFORMATION

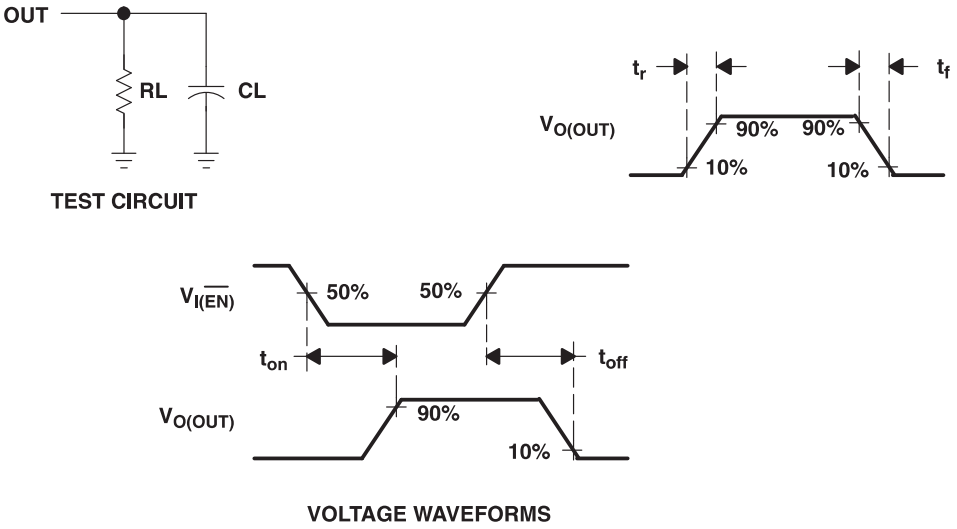


Figure 1. Test Circuit and Voltage Waveforms

Table 1. Timing Diagrams

	FIGURE
Turnon Delay and Rise Time	2
Turnoff Delay and Fall Time	3
Turnon Delay and Rise TIME with 1-µF Load	4
Turnoff Delay and Rise TIME with 1-µF Load	5
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3.7-Ω Load Connected to an Enabled TPS2011A Device	14
2.6-Ω Load Connected to an Enabled TPS2011A Device	15
2.6-Ω Load Connected to an Enabled TPS2012A Device	16
1.2-Ω Load Connected to an Enabled TPS2012A Device	17
1.2-Ω Load Connected to an Enabled TPS2013A Device	18
0.9-Ω Load Connected to an Enabled TPS2013A Device	19

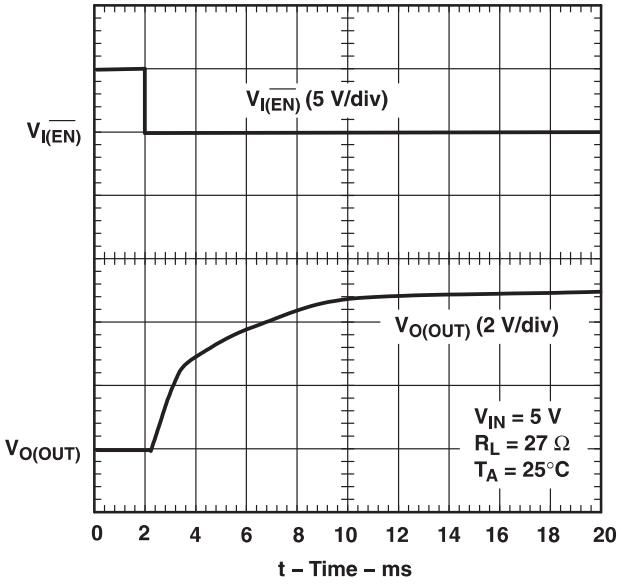

Figure 2. Turnon Delay and Rise Time

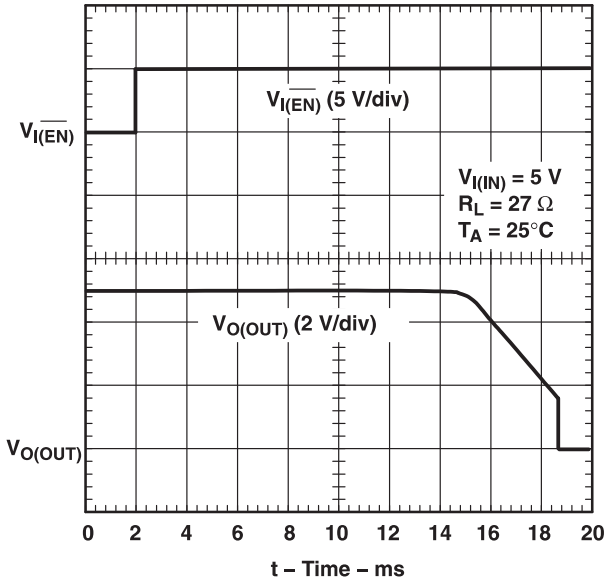

Figure 3. Turnoff Delay and Fall Time

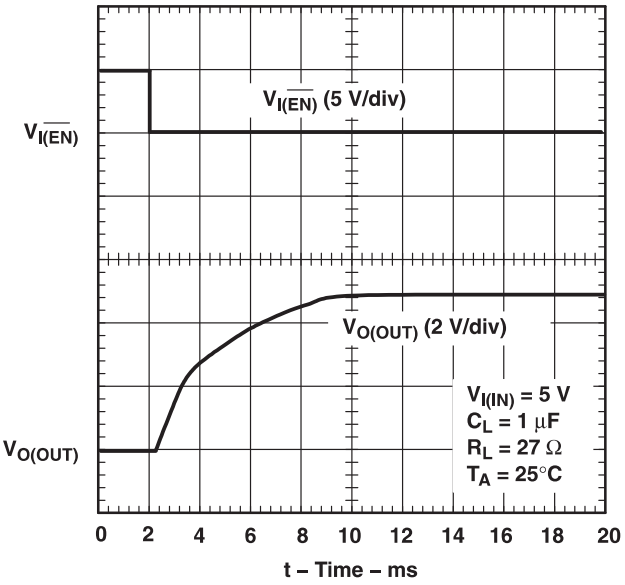

Figure 4. Turnon Delay and Rise Time With 1-μF Load

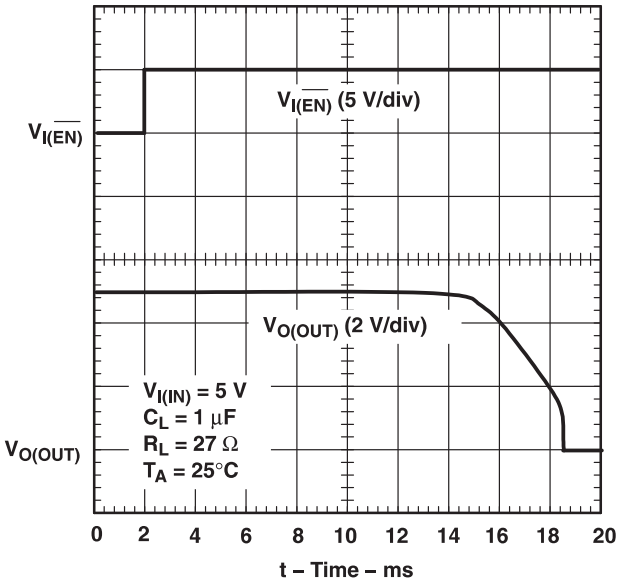

Figure 5. Turnoff Delay and Fall Time With 1-μF Load

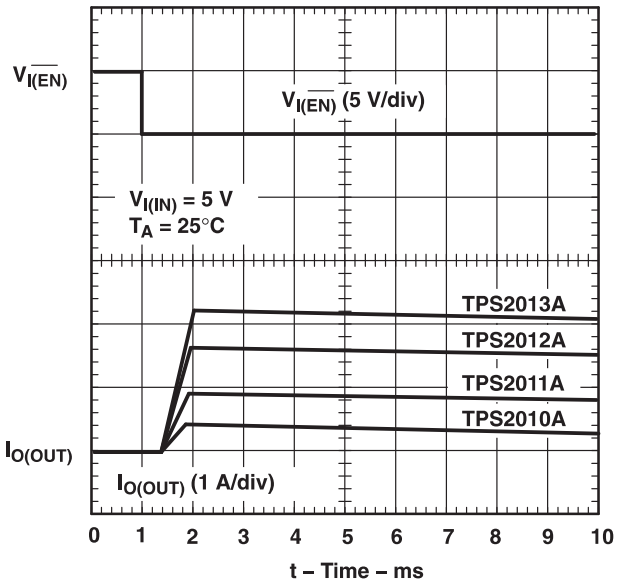

Figure 6. Device Enabled Into Short

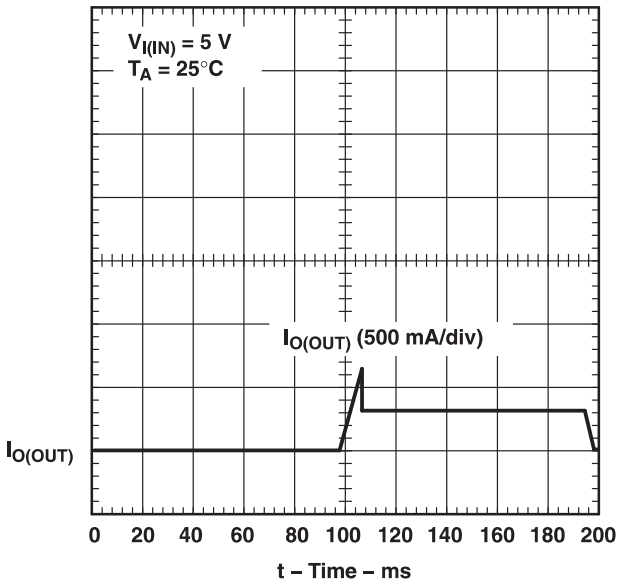

Figure 7. TPS2010A, Ramped Load on Enabled Device

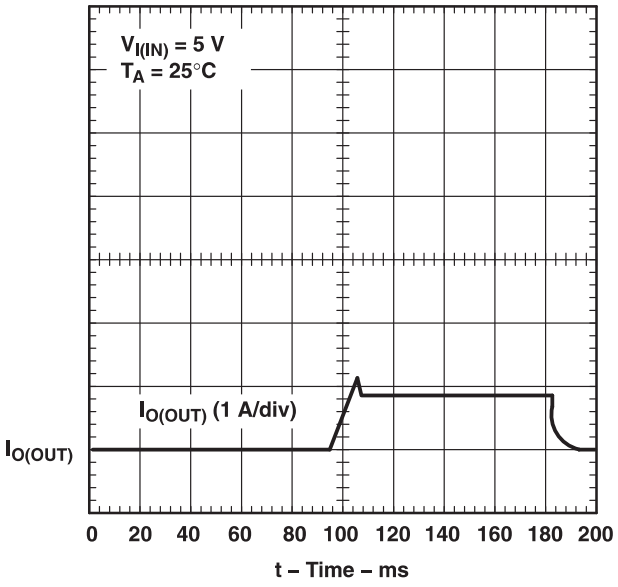

Figure 8. TPS2011A, Ramped Load on Enabled Device

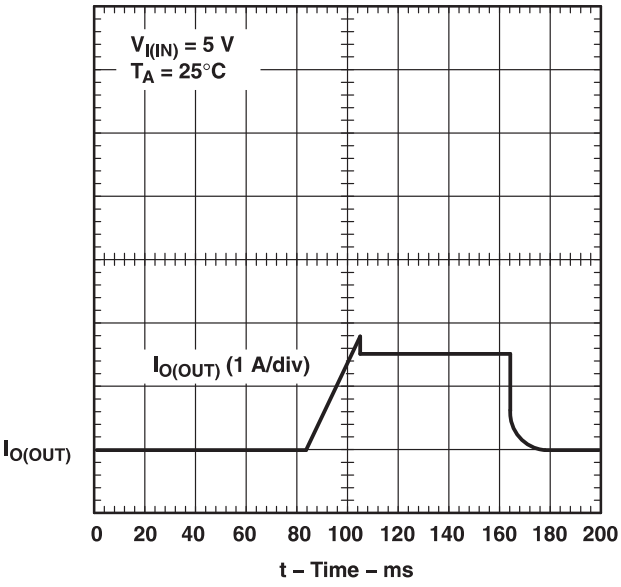

Figure 9. TPS2012A, Ramped Load on Enabled Device

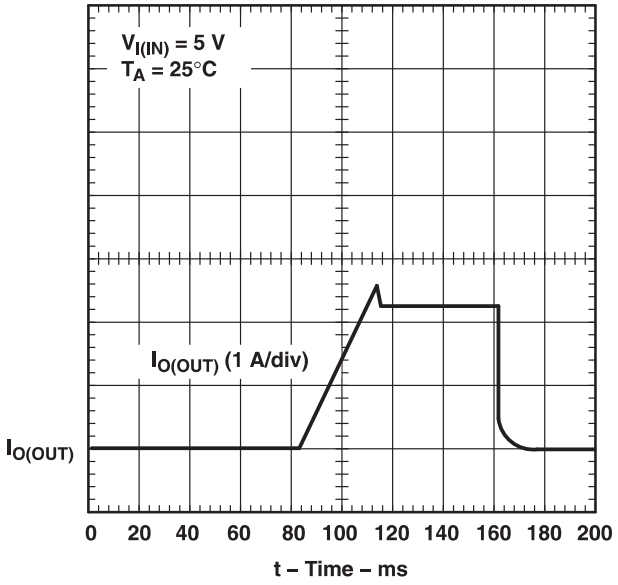

Figure 10. TPS2013A, Ramped Load on Enabled Device

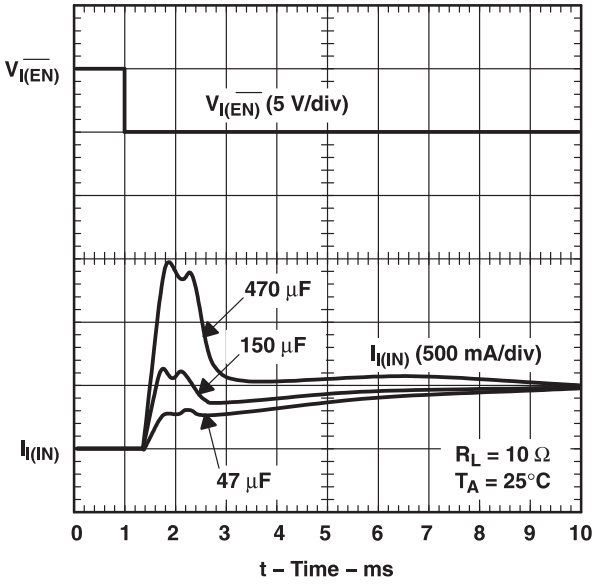

Figure 11. TPS2013A, Inrush Current

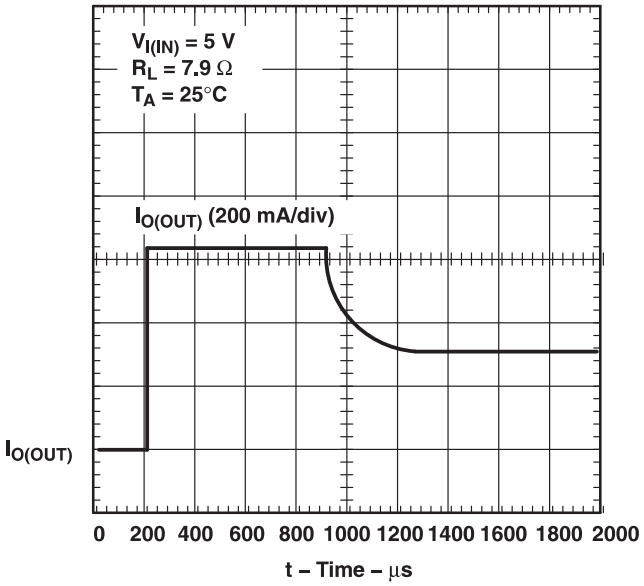

Figure 12. 7.9-Ω Load Connected to an Enabled TPS2010A Device

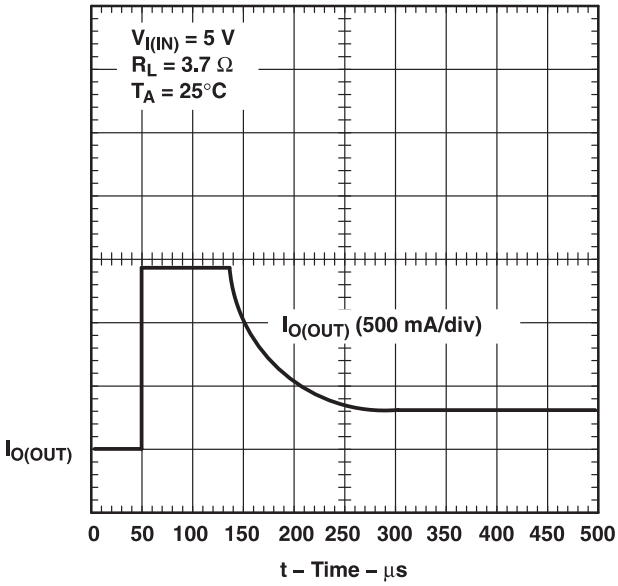

Figure 13. 3.7-Ω Load Connected to an Enabled TPS2010A Device

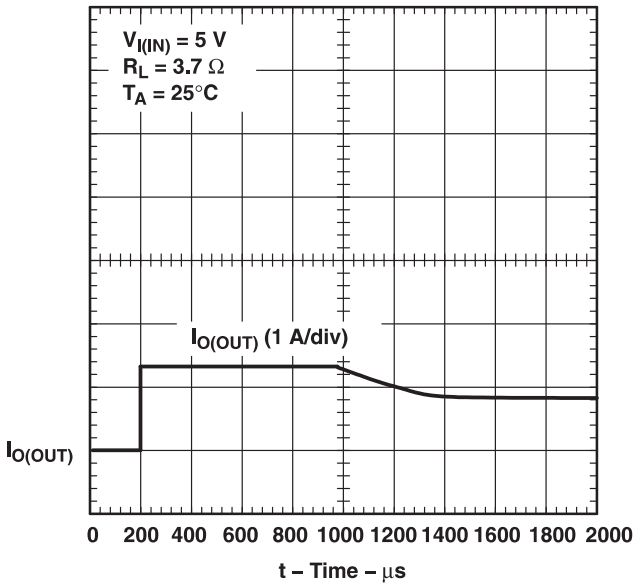

Figure 14. 3.7-Ω Load Connected to an Enabled TPS2011A Device

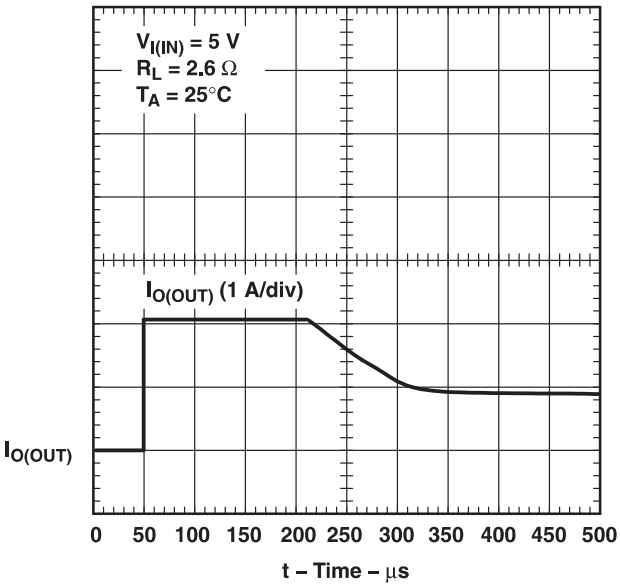

Figure 15. 2.6-Ω Load Connected to an Enabled TPS2011A Device

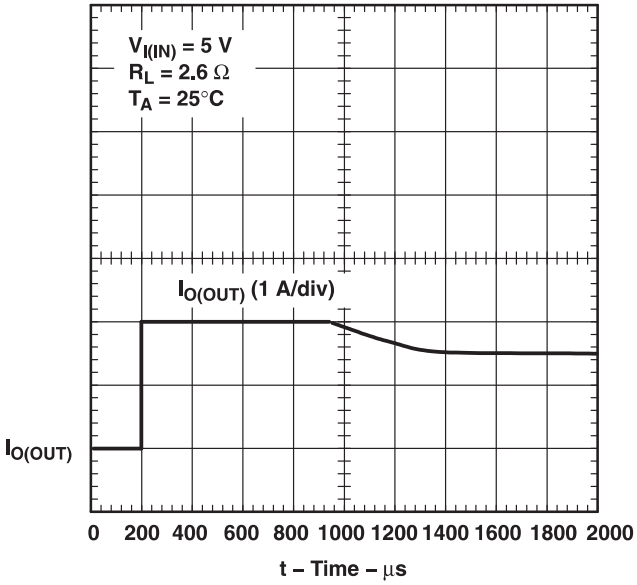

Figure 16. 2.6-Ω Load Connected to an Enabled TPS2012A Device

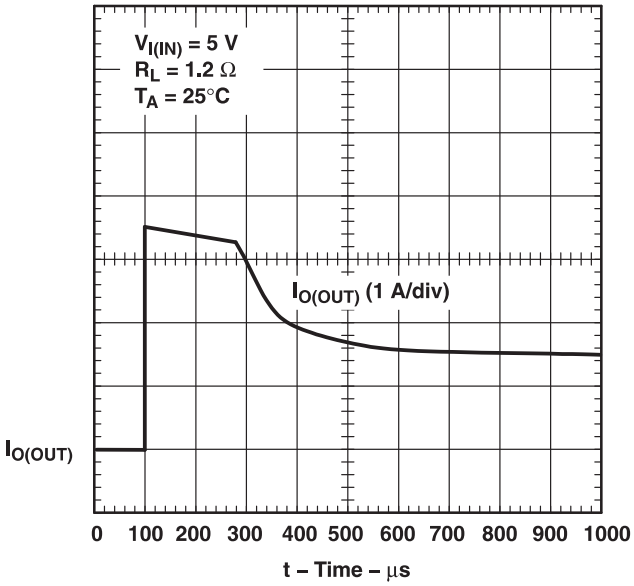

Figure 17. 1.2-Ω Load Connected to an Enabled TPS2012A Device

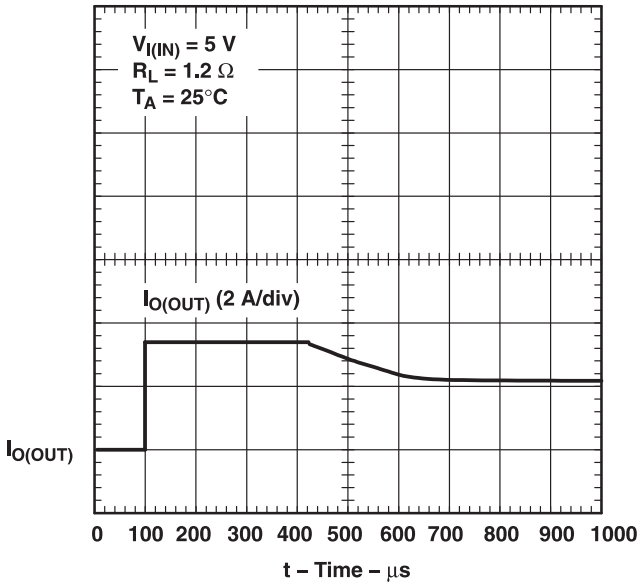

Figure 18. 1.2-Ω Load Connected to an Enabled TPS2013A Device

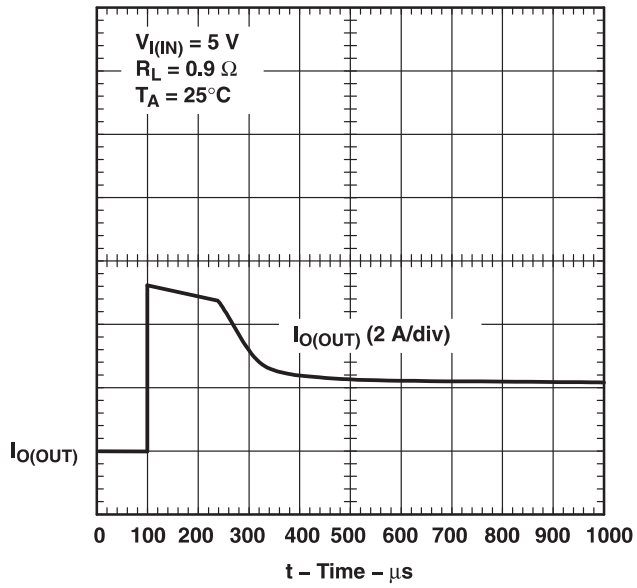

Figure 19. 0.9-Ω Load Connected to an Enabled TPS2013A Device

TYPICAL CHARACTERISTICS

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$t_{d(on)}$	Turnon delay time	vs Output voltage	20
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t_r	Rise time	vs Load current	22
t_f	Fall time	vs Load current	23
	Supply current (enabled)	vs Junction temperature	24
	Supply current (disabled)	vs Junction temperature	25
	Supply current (enabled)	vs Input voltage	26
	Supply current (disabled)	vs Input voltage	27
I_{OS}	Short-circuit current limit	vs Input voltage	28
		vs Junction temperature	29
$r_{DS(on)}$	Static drain-source on-state resistance	vs Input voltage	30
		vs Junction temperature	31
		vs Input voltage	32
		vs Junction temperature	33
	Undervoltage lockout	Input voltage vs Temperature	34

TURNON DELAY TIME vs OUTPUT VOLTAGE

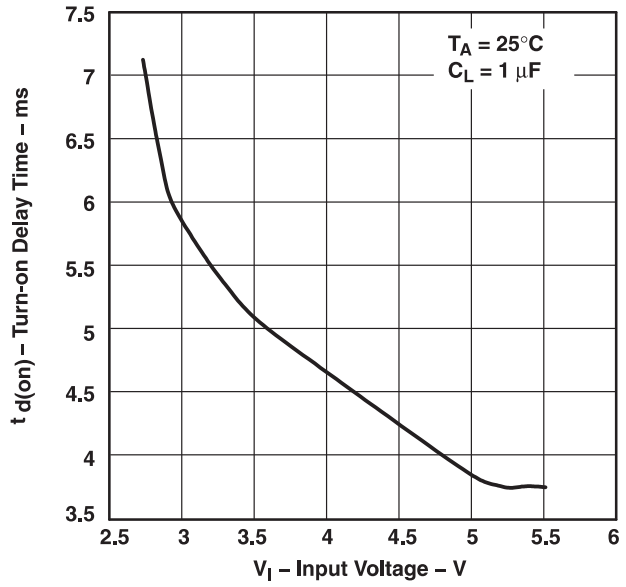


Figure 20.

TURNOFF DELAY TIME vs INPUT VOLTAGE

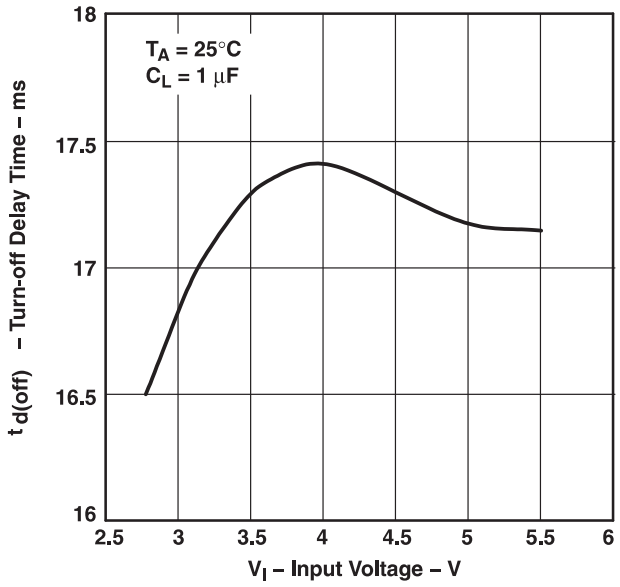


Figure 21.

RISE TIME
vs
LOAD CURRENT

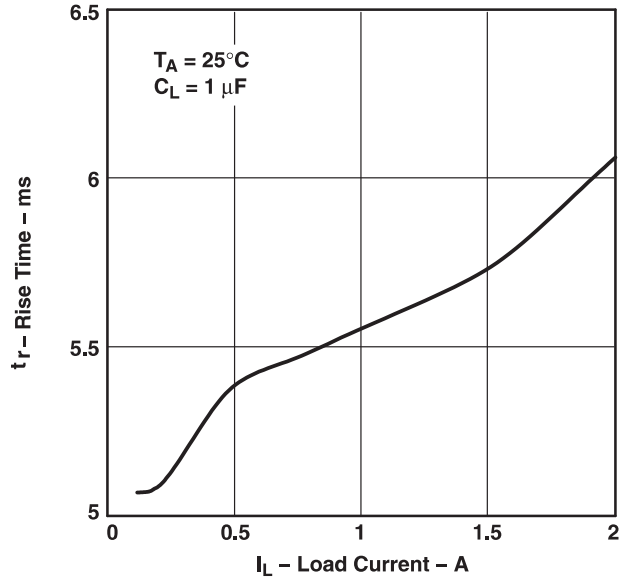


Figure 22.

FALL TIME
vs
LOAD CURRENT

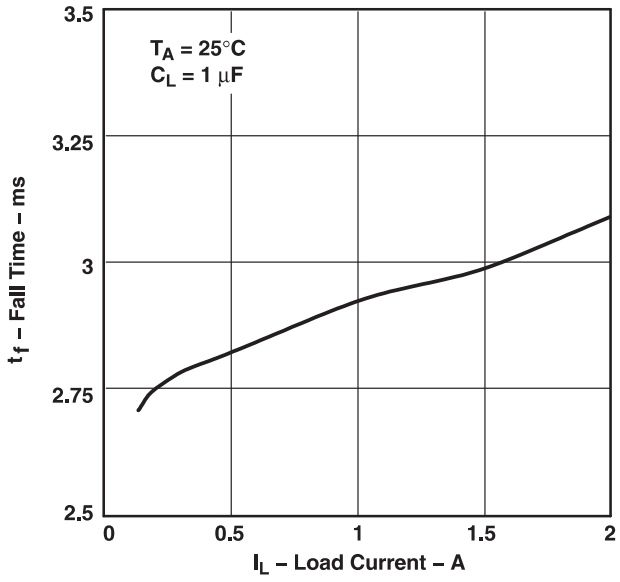


Figure 23.

SUPPLY CURRENT (ENABLED)
vs
JUNCTION TEMPERATURE

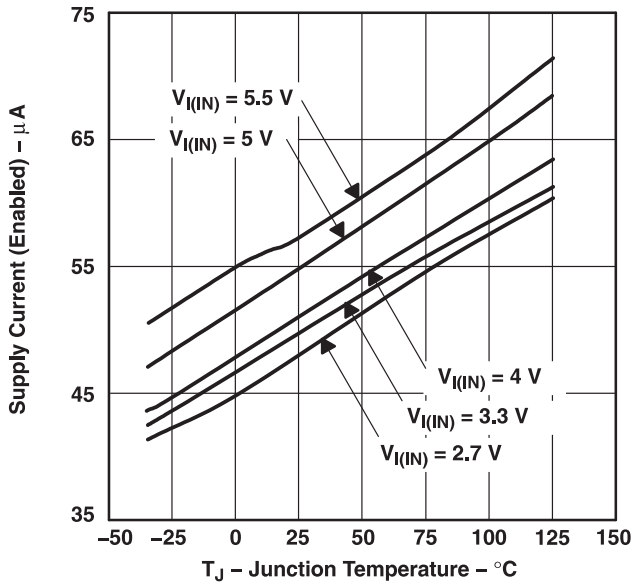


Figure 24.

SUPPLY CURRENT (DISABLED)
vs
JUNCTION TEMPERATURE

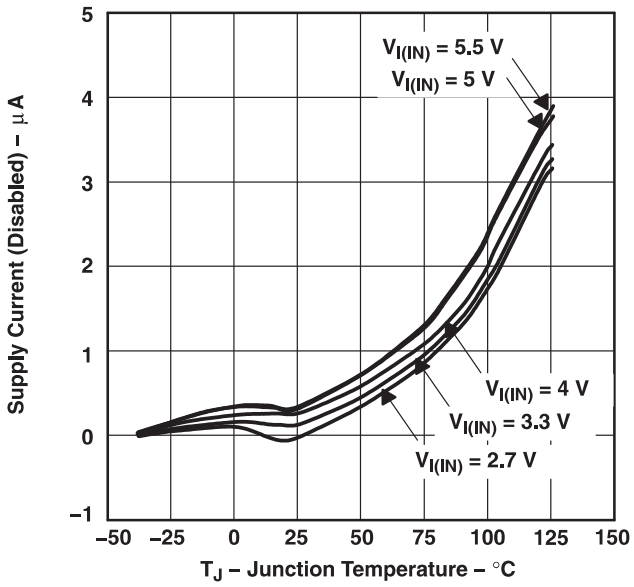


Figure 25.

SUPPLY CURRENT (ENABLED)
vs
INPUT VOLTAGE

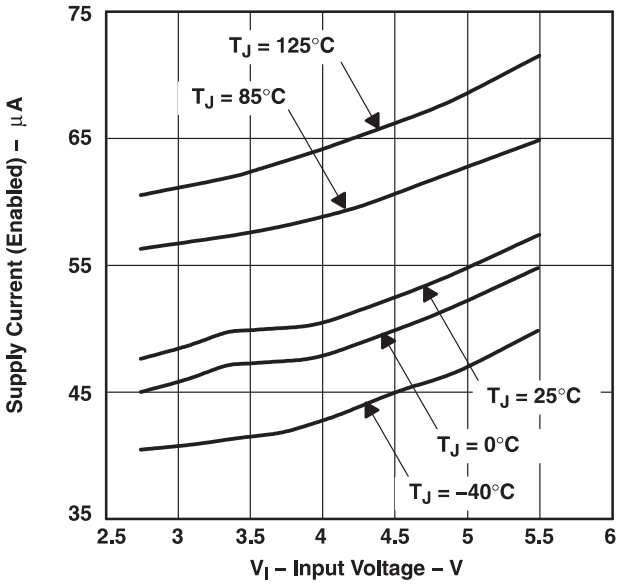


Figure 26.

SUPPLY CURRENT (DISABLED)
vs
INPUT VOLTAGE

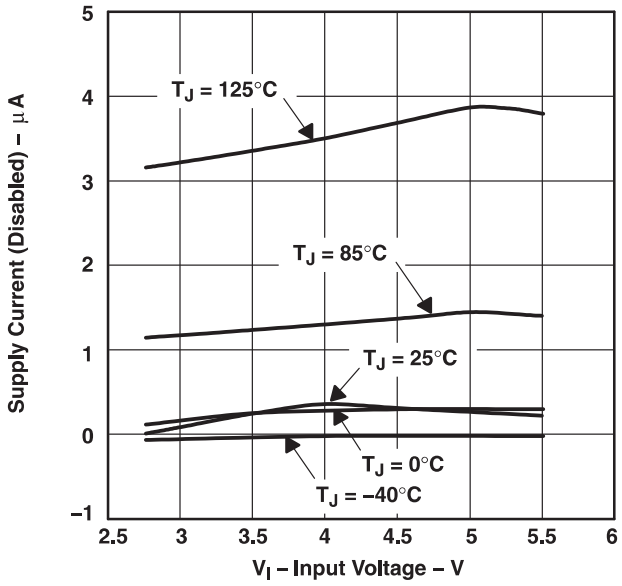


Figure 27.

SHORT-CIRCUIT CURRENT LIMIT
vs
INPUT VOLTAGE

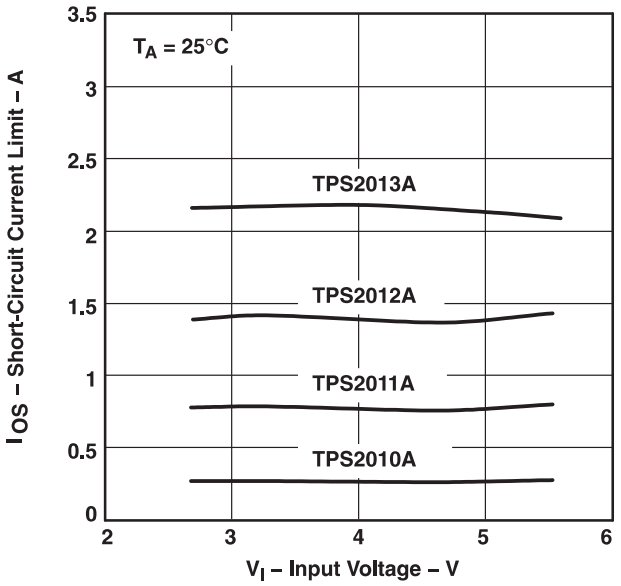


Figure 28.

SHORT-CIRCUIT CURRENT LIMIT
vs
JUNCTION TEMPERATURE

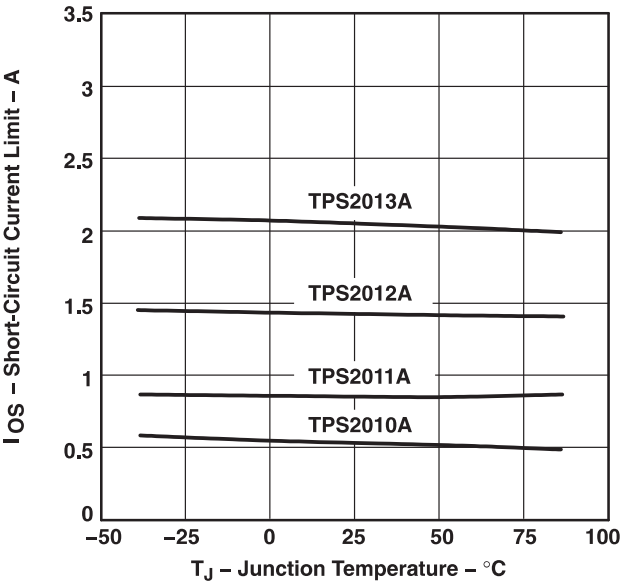


Figure 29.

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs INPUT VOLTAGE

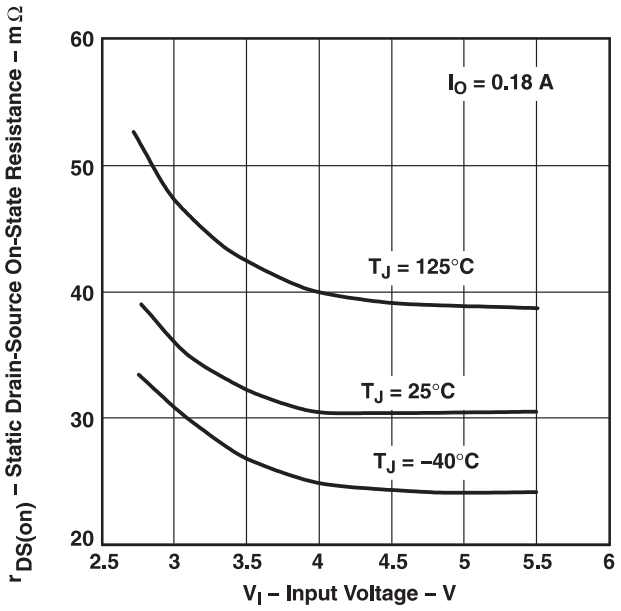


Figure 30.

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

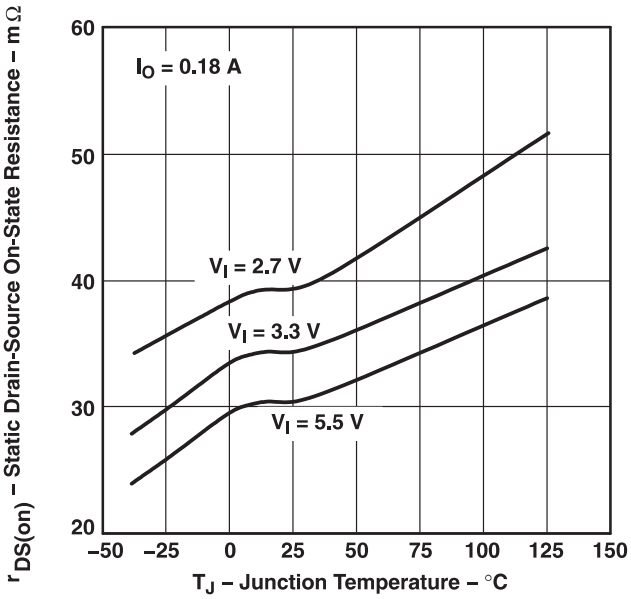


Figure 31.

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs INPUT VOLTAGE

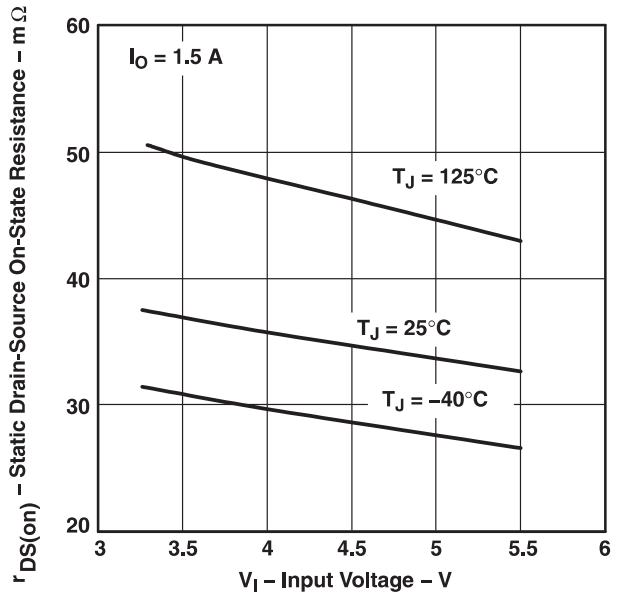


Figure 32.

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

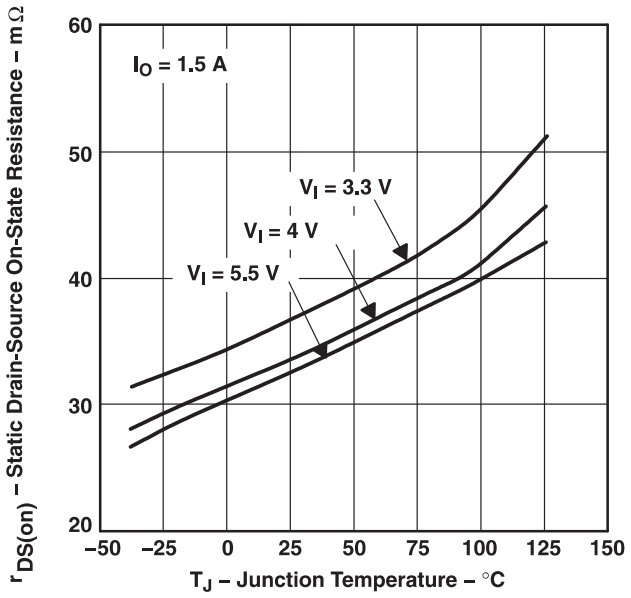


Figure 33.

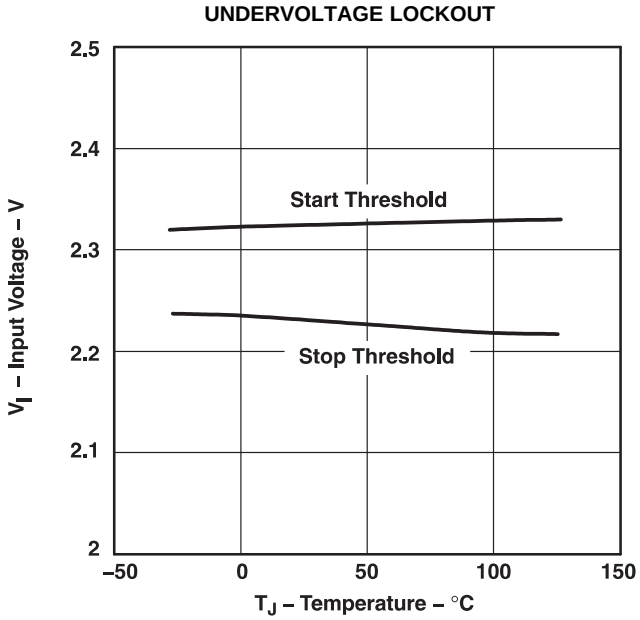

UNDERVOLTAGE LOCKOUT
2.5
2.4
2.3
2.2
2.1
2
Start Threshold
Stop Threshold
VI – Input Voltage – V
–50
0
50
100
150
TJ – Temperature – °C

Figure 34.

APPLICATION INFORMATION

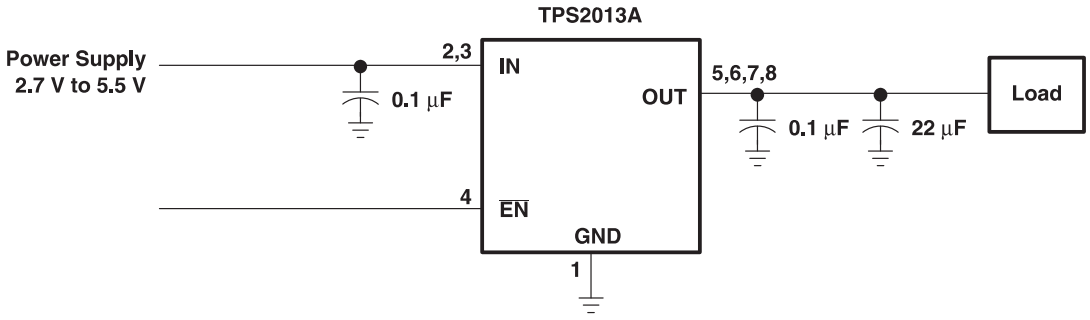


Figure 35. Typical Application

POWER-SUPPLY CONSIDERATIONS

A 0.01-µF to 0.1-µF ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output and input pins is recommended when the output load is heavy. This precaution reduces power supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-µF to 0.1-µF ceramic capacitor improves the immunity of the device to short-circuit transients.

OVERCURRENT

A sense FET checks for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 6). The TPS201xA senses the short and immediately switches into a constant-current output.

In the second condition, the excessive load occurs while the device is enabled. At the instant the excessive load occurs, very high currents may flow for a short time before the current-limit circuit can react (see Figure 12–Figure 19). After the current-limit circuit has tripped (reached the overcurrent trip threshold) the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figures Figure 77–Figure 10). The TPS201xA is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

POWER DISSIPATION AND JUNCTION TEMPERATURE

The low on-resistance on the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistance of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find $r_{DS(on)}$ at the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from SLVS1892074Figure 30–Figure 33 . Next, calculate the power dissipation using:

$$P_D = r_{DS(on)} \times I^2 \quad (1)$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A \quad (2)$$

Where:

T_A = Ambient Temperature °C

$R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get an acceptable answer.

THERMAL PROTECTION

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS201xA into constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels. The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

UNDERVOLTAGE LOCKOUT (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch will be quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO will also keep the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. Upon reinsertion, the power switch will be turned on, with a controlled rise time to reduce EMI and voltage overshoots.

GENERIC HOT-PLUG APPLICATIONS (see Figure 36)

In many applications it may be necessary to remove modules or p-c boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Because of the controlled rise times and fall times of the TPS201xA series, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS201xA also ensures the switch will be off after the card has been removed, and the switch will be off during the next insertion. The UVLO feature guarantees a soft start with a controlled rise time for every insertion of the card or module.

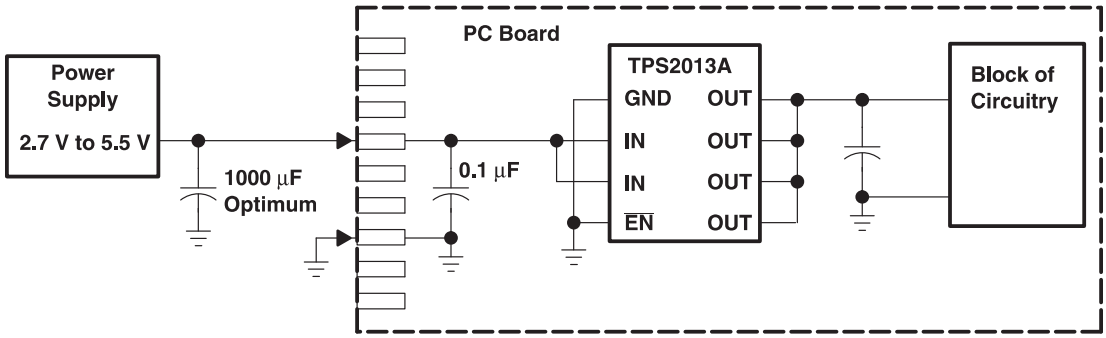


Figure 36. Typical Hot-Plug Implementation

By placing the TPS201xA between the V_{CC} input and the rest of the circuitry, the input power will reach this device first after insertion. The typical rise time of the switch is approximately 9 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2010AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2010A	Samples
TPS2010ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2010A	Samples
TPS2010ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2010A	Samples
TPS2010ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2010A	Samples
TPS2011AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2011A	Samples
TPS2011ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2011A	Samples
TPS2011ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2011A	Samples
TPS2011ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2011A	Samples
TPS2011APWP	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		2011A	Samples
TPS2012AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2012A	Samples
TPS2012ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2012A	Samples
TPS2012ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2012A	Samples
TPS2012ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2012A	Samples
TPS2013AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2013A	Samples
TPS2013ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2013A	Samples
TPS2013ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2013A	Samples
TPS2013ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2013A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2013APWP	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		2013A	Samples
TPS2013APWPR	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		2013A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

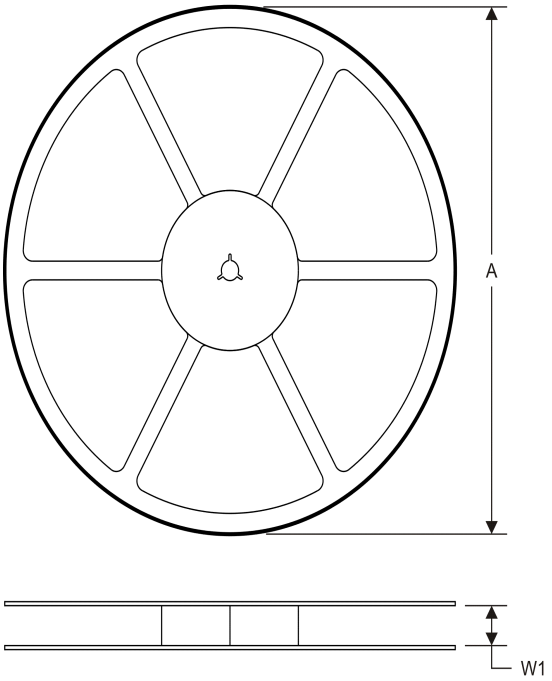
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

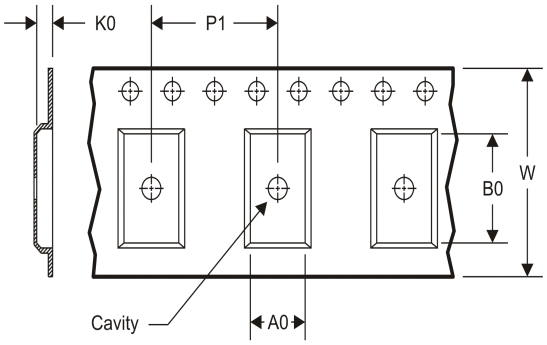
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



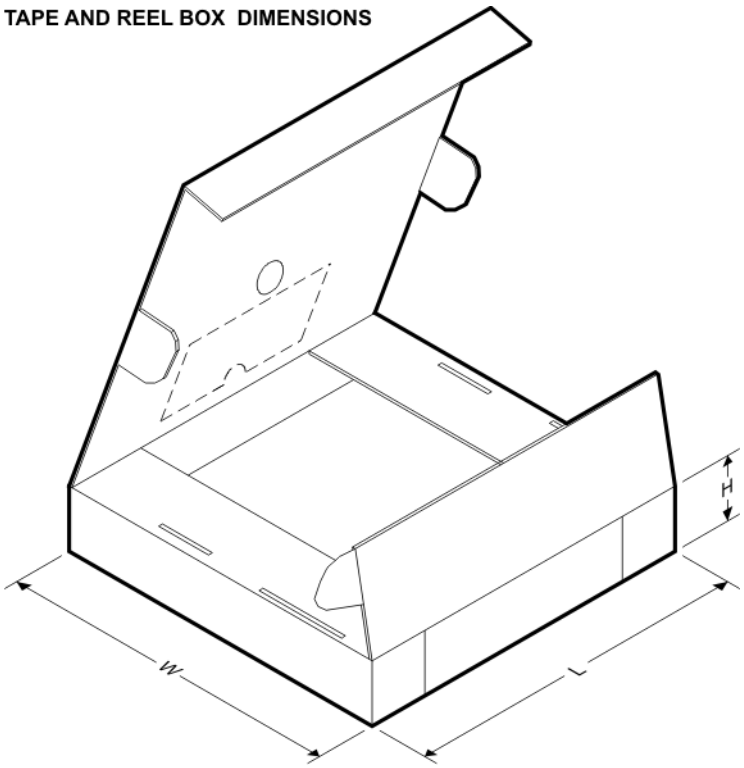
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2010ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2011ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2012ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2013ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2013APWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

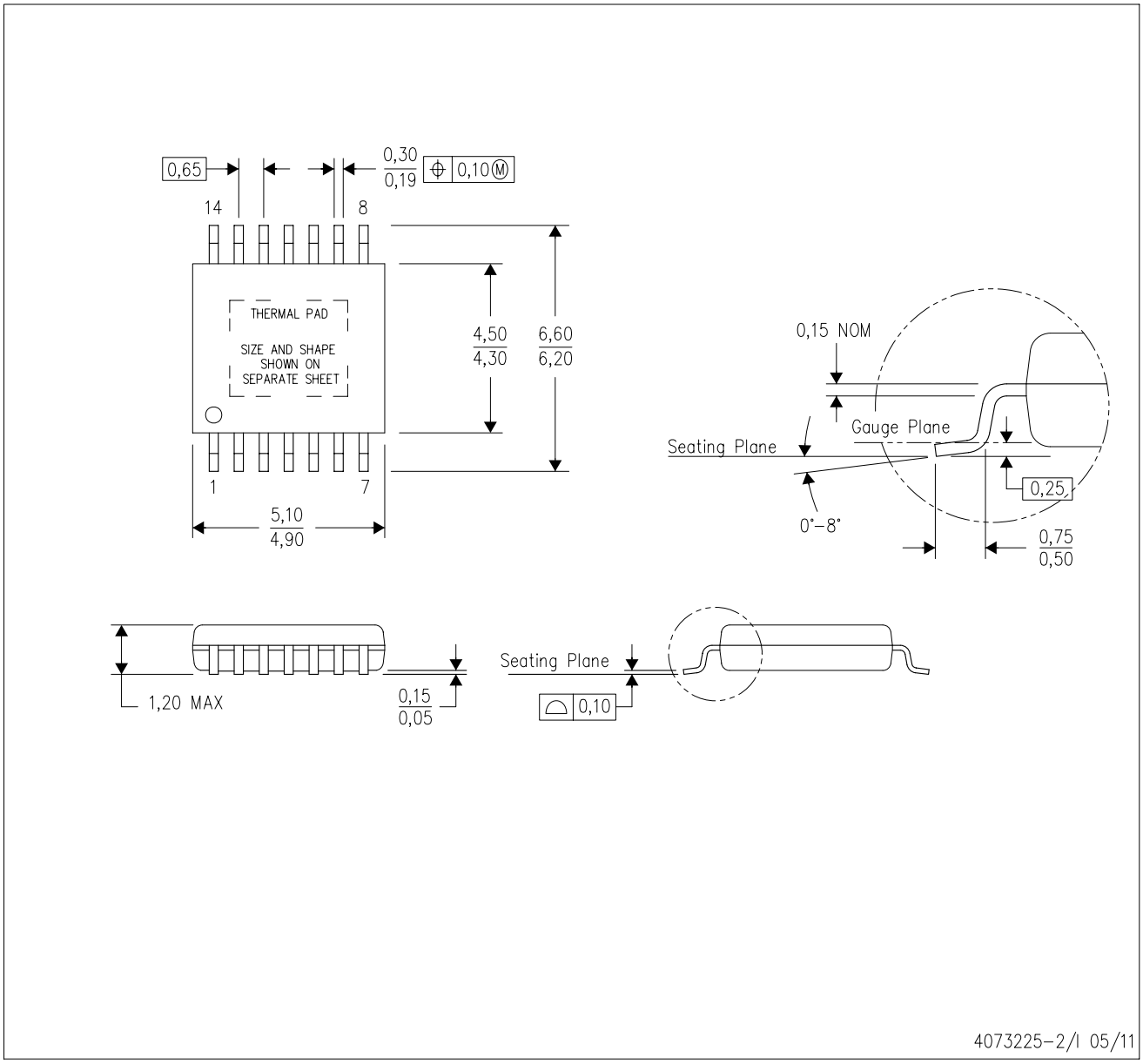
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2010ADR	SOIC	D	8	2500	340.5	338.1	20.6
TPS2011ADR	SOIC	D	8	2500	340.5	338.1	20.6
TPS2012ADR	SOIC	D	8	2500	340.5	338.1	20.6
TPS2013ADR	SOIC	D	8	2500	340.5	338.1	20.6
TPS2013APWPR	HTSSOP	PWP	14	2000	367.0	367.0	35.0

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

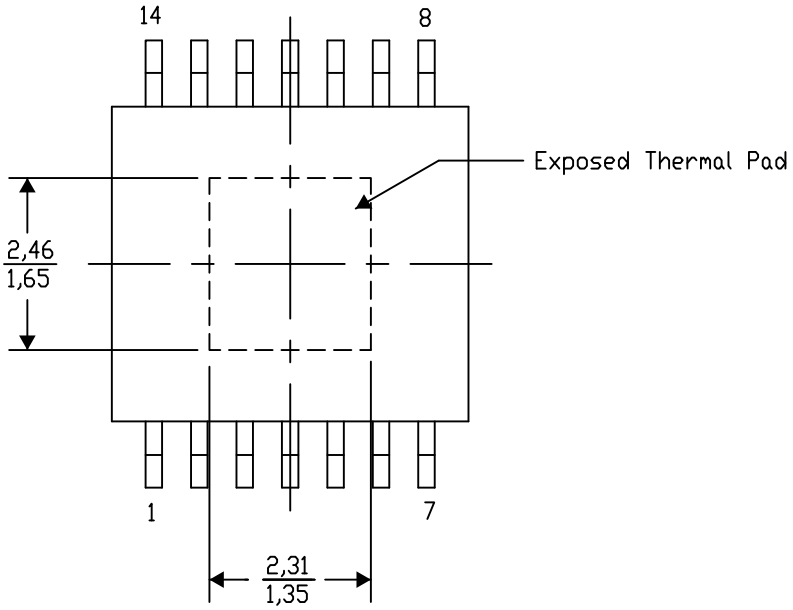
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

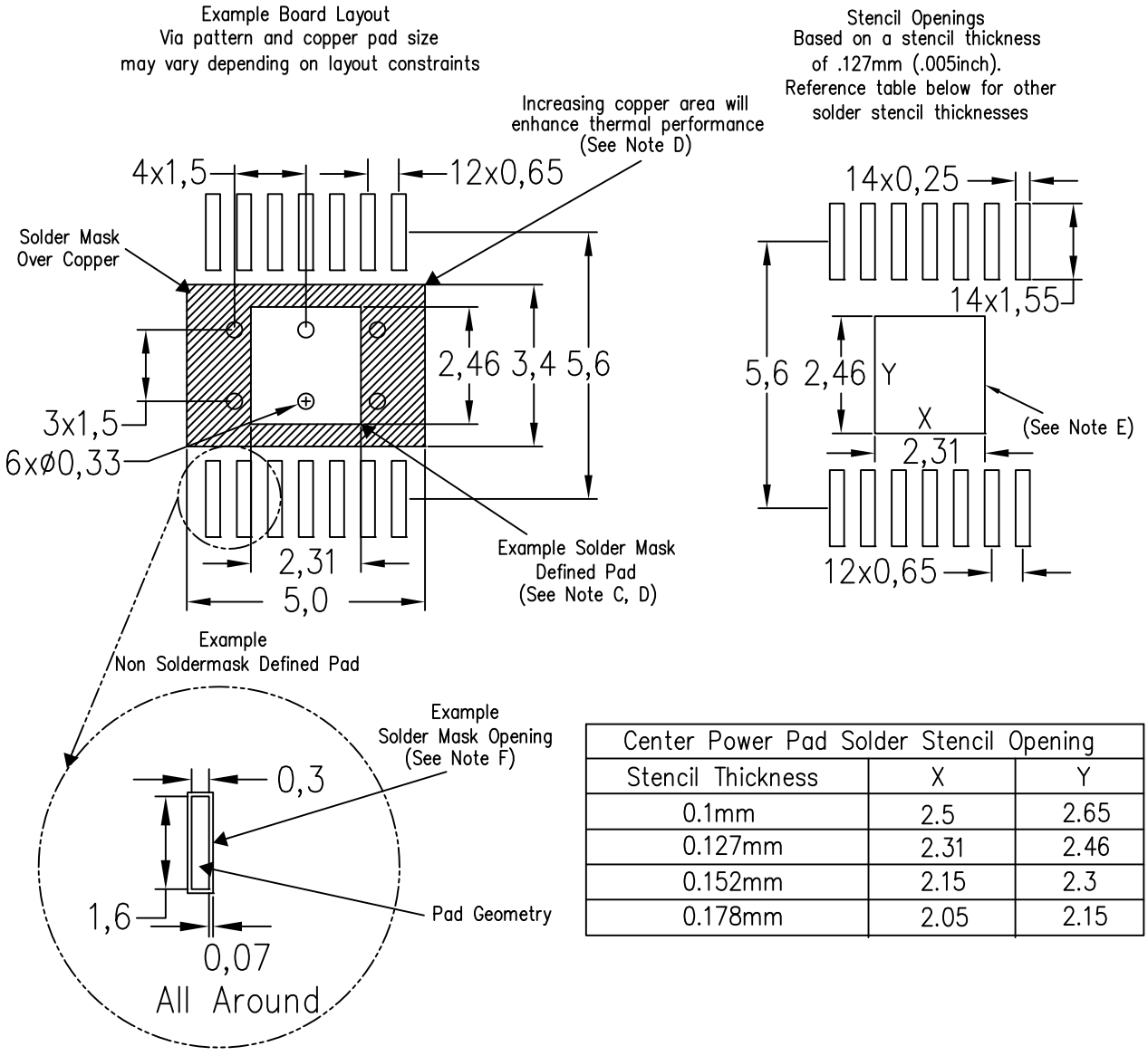
Exposed Thermal Pad Dimensions

4206332–2/AH 11/13

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE

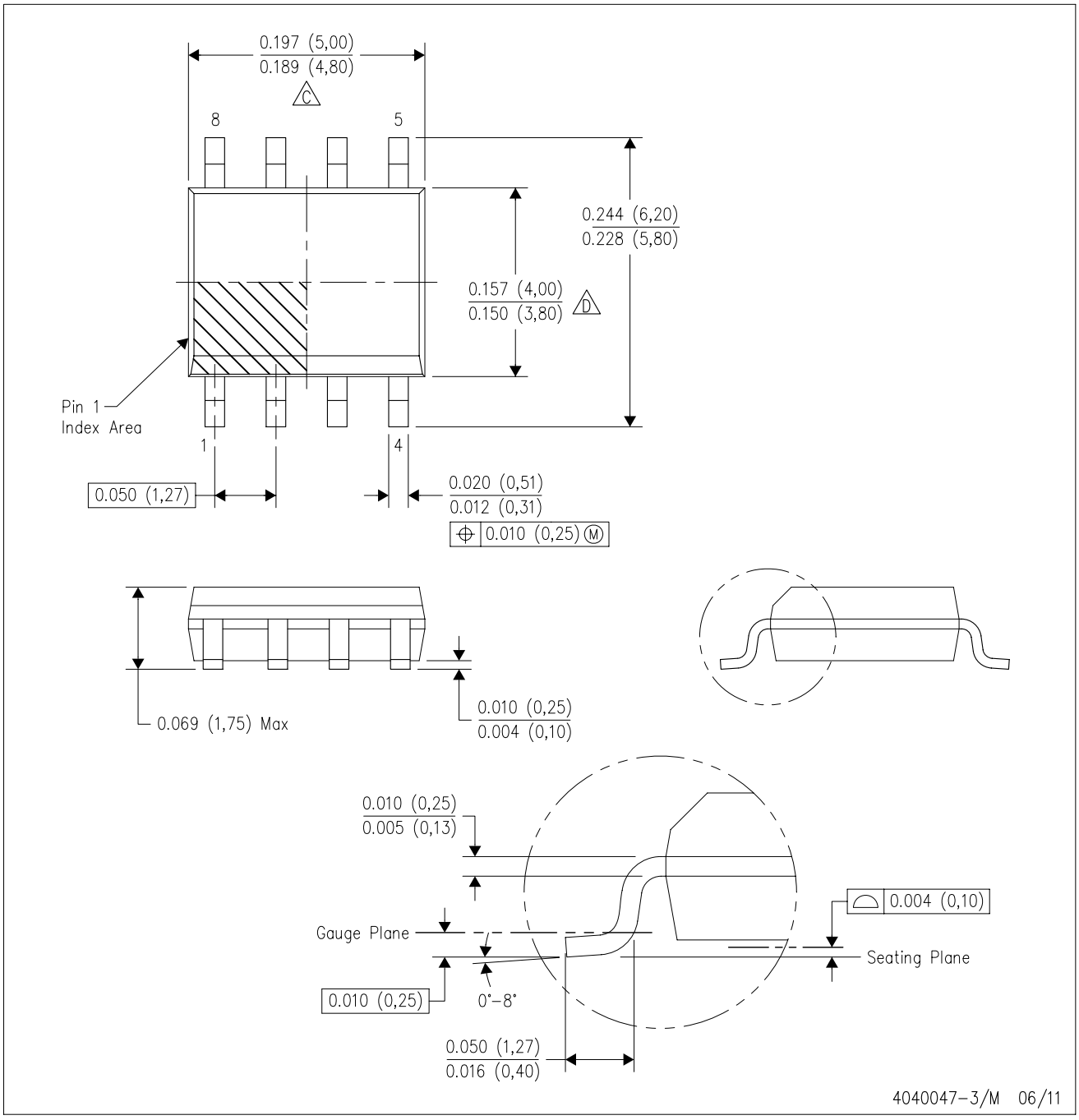


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/T 08/13

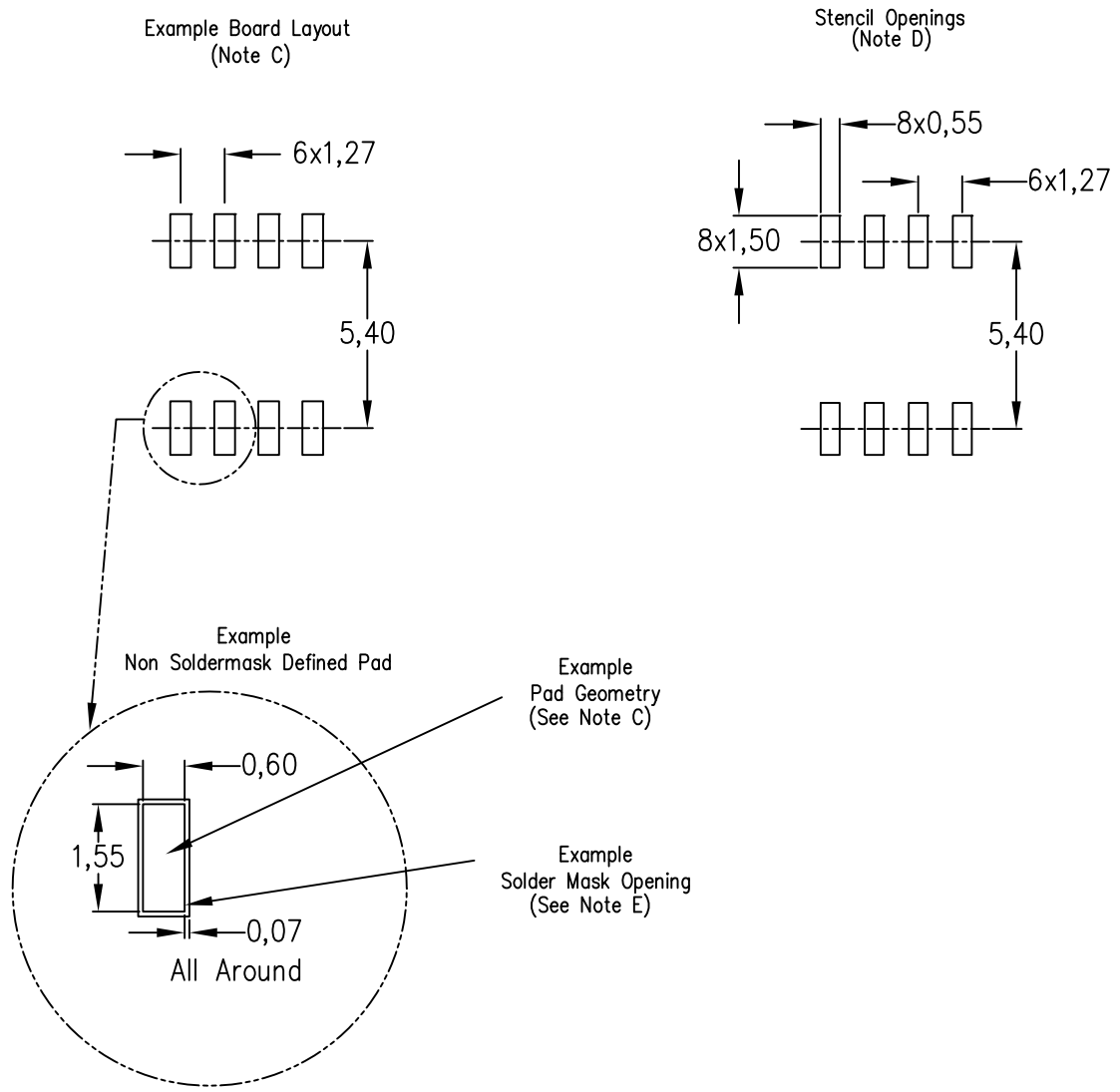
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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