

General Description

- Latest Trench Power AlphaMOS (αMOS LV) technology
- Integrated Schottky Diode (SRFET) on Low-Side
- Very Low $R_{DS(on)}$ at 4.5V V_{GS}
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

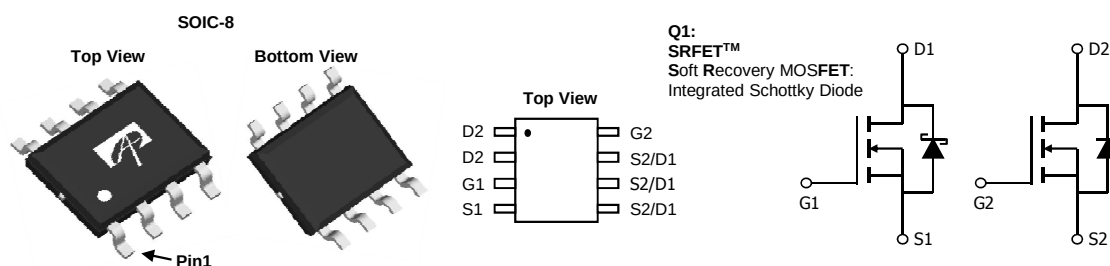
Application

- DC/DC Converters in Computing, Servers, and POL
- Isolated DC/DC Converters in Telecom and Industrial

Product Summary

	<u>Q1</u>	<u>Q2</u>
V_{DS}	30V	30V
I_D (at $V_{GS}=10V$)	11A	11A
$R_{DS(on)}$ (at $V_{GS}=10V$)	<10.5mΩ	<11.5mΩ
$R_{DS(on)}$ (at $V_{GS}=4.5V$)	<15.5mΩ	<16.5mΩ

100% UIS Tested
100% Rg Tested



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter		Symbol	Max Q1	Max Q2	Units
Drain-Source Voltage		V _{DS}	30		V
Gate-Source Voltage		V _{GS}	±20	±20	V
Continuous Drain Current	T _A =25°C	I _D	11	11	A
	T _A =70°C		9	9	
Pulsed Drain Current ^C		I _{DM}	75	74	
Avalanche Current ^C		I _{AS}	18	15	A
Avalanche Energy L=0.1mH ^C		E _{AS}	16	11	mJ
V _{DS} Spike	100ns	V _{SPIKE}	36	36	V
Power Dissipation ^B	T _C =25°C	P _D	2	2	W
	T _C =70°C		1.3	1.3	
Junction and Storage Temperature Range		T _J , T _{STG}	-55 to 150		°C

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	48	62.5	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{A, D}		74	90	$^\circ\text{C/W}$
Maximum Junction-to-Case	$R_{\theta JL}$	32	40	$^\circ\text{C/W}$

Q1 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =10mA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			0.5 100	mA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.4	1.8	2.5	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =11A T _J =125°C		8.3 11.8	10.5 15	mΩ
		V _{GS} =4.5V, I _D =9A		12.2	15.5	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =11A		52		S
V _{SD}	Diode Forward Voltage	I _S =0.2A, V _{GS} =0V		0.45	0.65	V
I _S	Maximum Body-Diode Continuous Current				2.5	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		605		pF
C _{oss}	Output Capacitance			275		pF
C _{rss}	Reverse Transfer Capacitance			37		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	1	2	3	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =11A		10.2	15	nC
Q _g (4.5V)	Total Gate Charge			4.9	8	nC
Q _{gs}	Gate Source Charge			2		nC
Q _{gd}	Gate Drain Charge			2.3		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =1.36Ω, R _{GEN} =3Ω		5		ns
t _r	Turn-On Rise Time			3		ns
t _{D(off)}	Turn-Off DelayTime			17.5		ns
t _f	Turn-Off Fall Time			3		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =11A, dI/dt=500A/μs		11		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =11A, dI/dt=500A/μs		12.5		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. The maximum current limited by package.

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Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

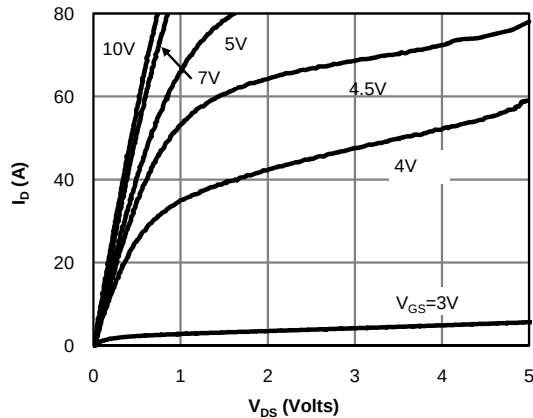


Fig 1: On-Region Characteristics (Note E)

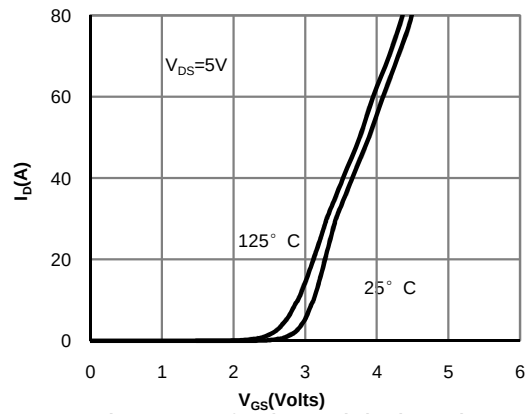


Figure 2: Transfer Characteristics (Note E)

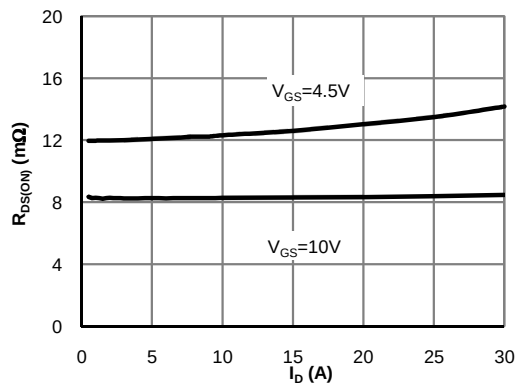


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

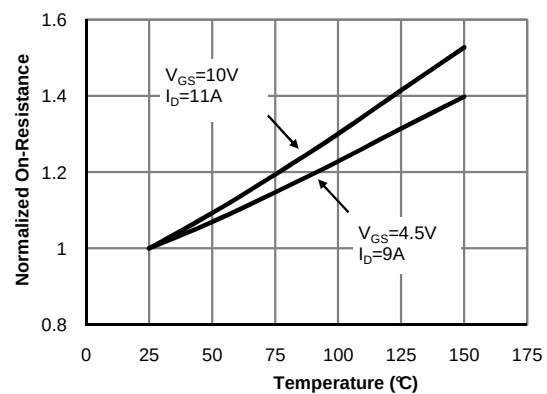


Figure 4: On-Resistance vs. Junction Temperature (Note E)

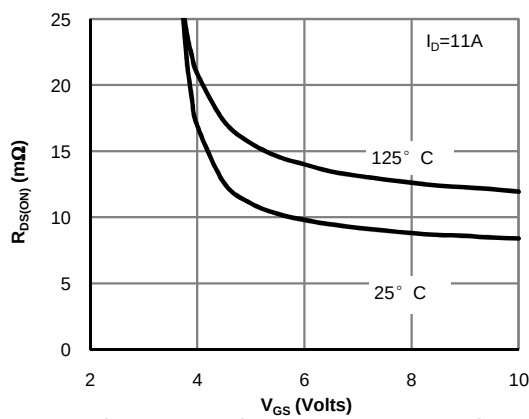


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

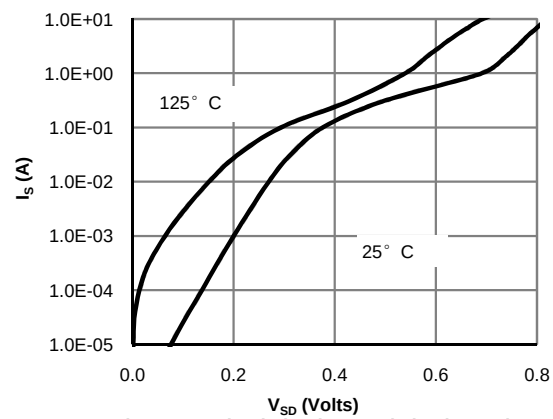
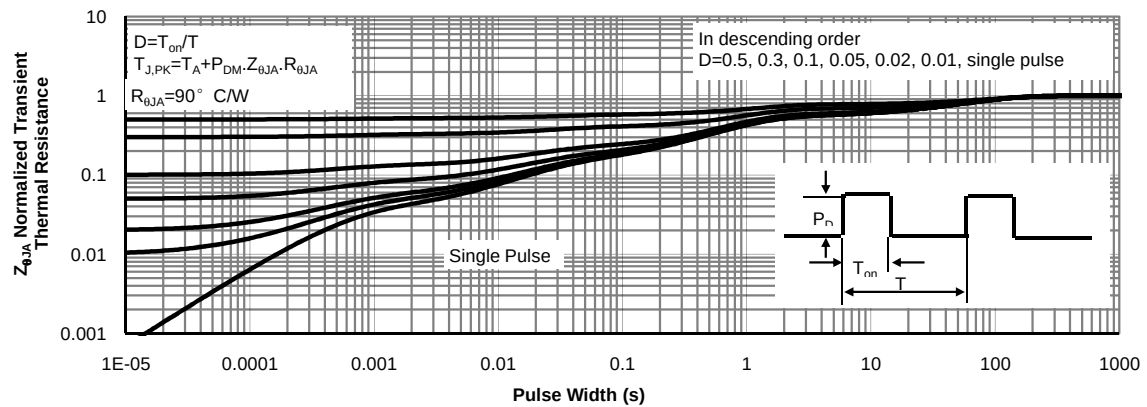
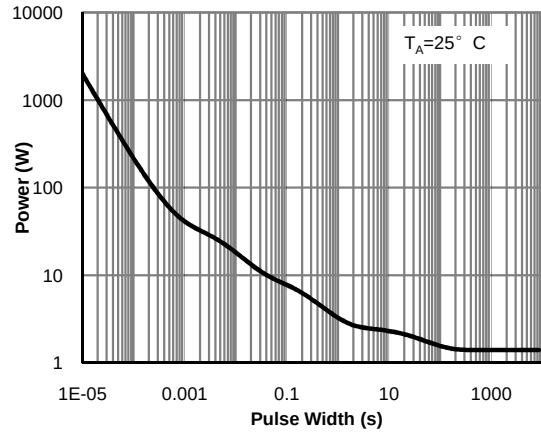
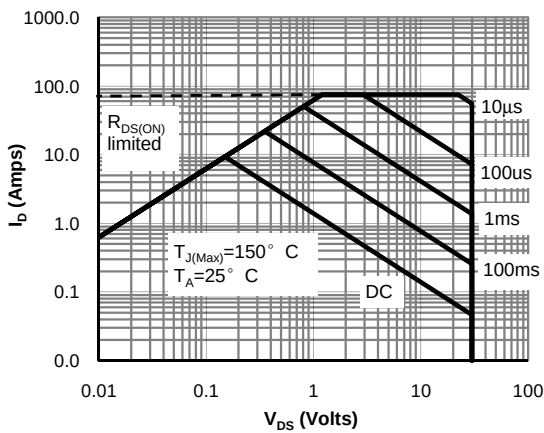
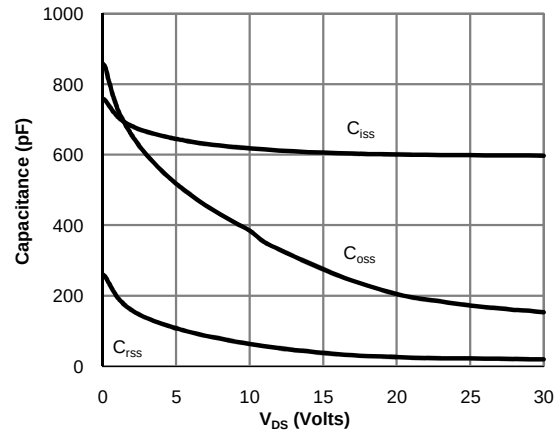
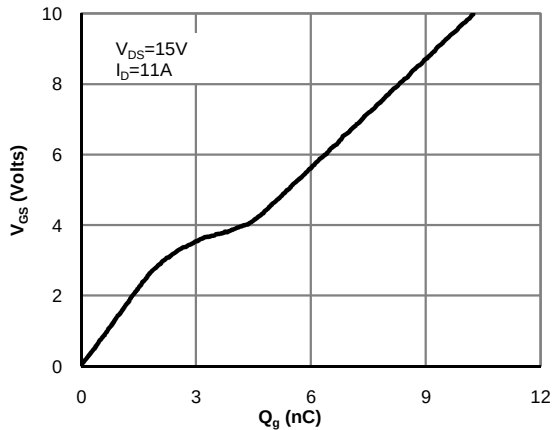


Figure 6: Body-Diode Characteristics (Note E)

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



Q2 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.4	1.8	2.2	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =11A T _J =125°C		9 12.4	11.5 15.8	mΩ
		V _{GS} =4.5V, I _D =9A		12.8	16.5	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =11A		40		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.72	1	V
I _S	Maximum Body-Diode Continuous Current				2.5	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		542		pF
C _{oss}	Output Capacitance			233		pF
C _{rss}	Reverse Transfer Capacitance			31		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	1	2	3	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =11A		9	12.5	nC
Q _g (4.5V)	Total Gate Charge			4.3	6	nC
Q _{gs}	Gate Source Charge			2.2		nC
Q _{gd}	Gate Drain Charge			1.7		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =1.36Ω, R _{GEN} =3Ω		4		ns
t _r	Turn-On Rise Time			3.5		ns
t _{D(off)}	Turn-Off DelayTime			18		ns
t _f	Turn-Off Fall Time			3		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =11A, dI/dt=500A/μs		9.7		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =11A, dI/dt=500A/μs		11.5		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

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Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

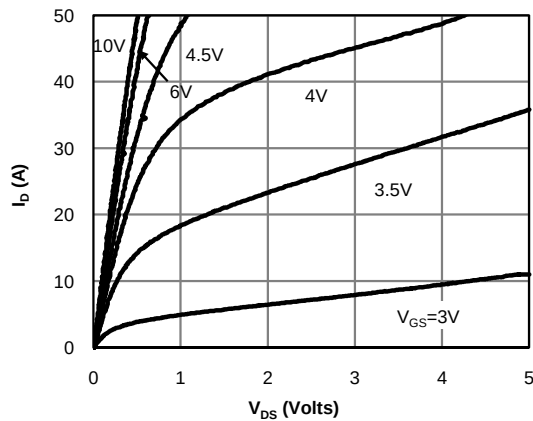


Fig 1: On-Region Characteristics (Note E)

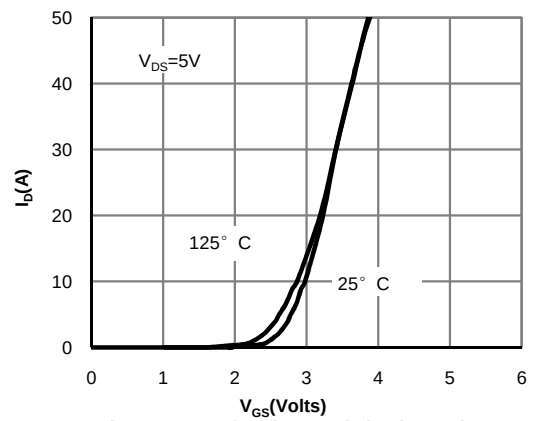


Figure 2: Transfer Characteristics (Note E)

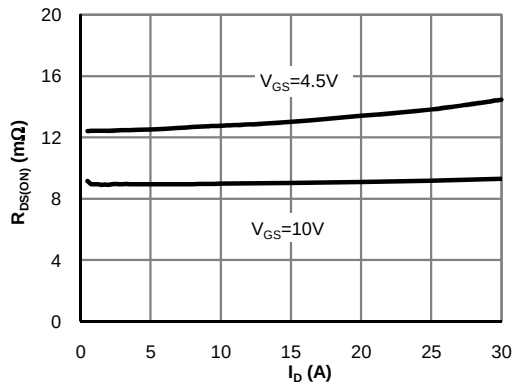


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

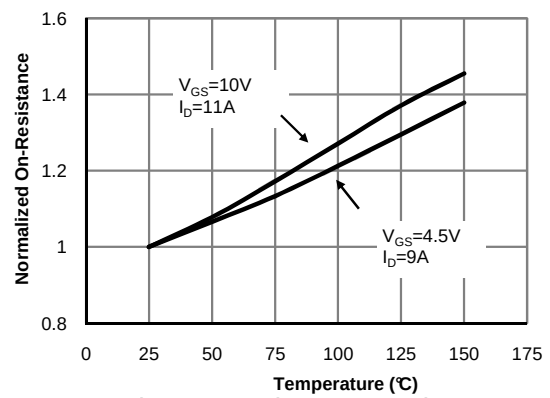


Figure 4: On-Resistance vs. Junction Temperature (Note E)

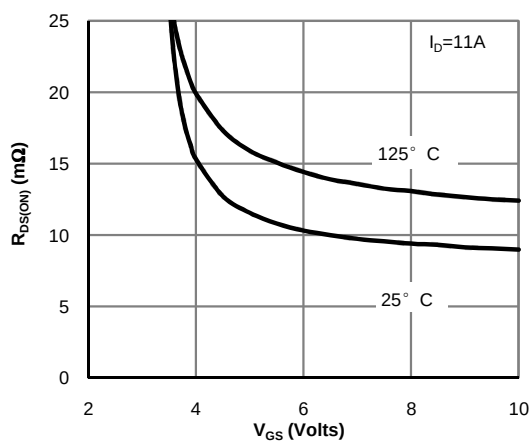


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

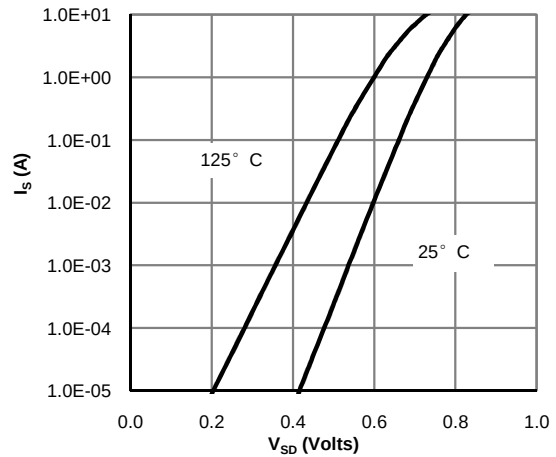


Figure 6: Body-Diode Characteristics (Note E)

Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

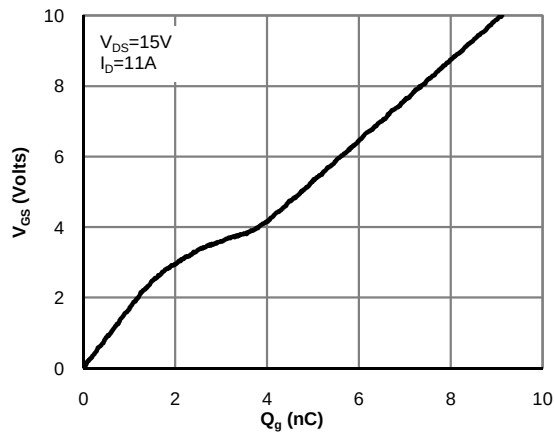


Figure 7: Gate-Charge Characteristics

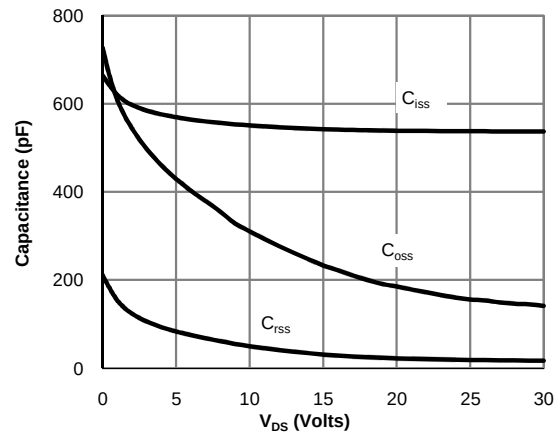


Figure 8: Capacitance Characteristics

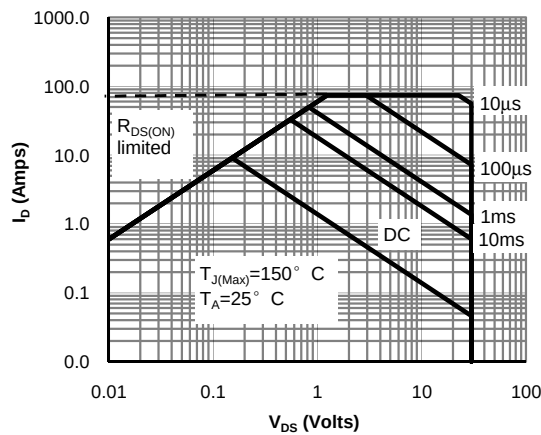


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

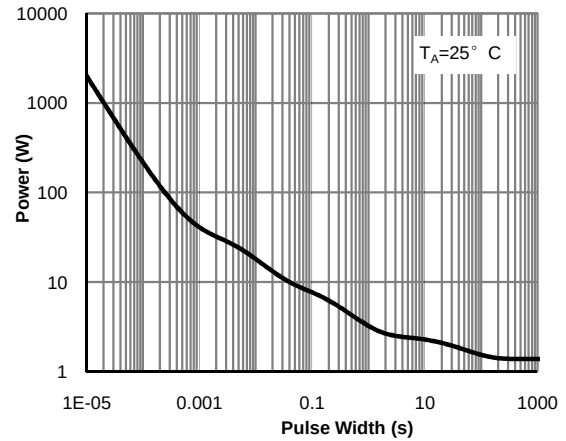


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note H)

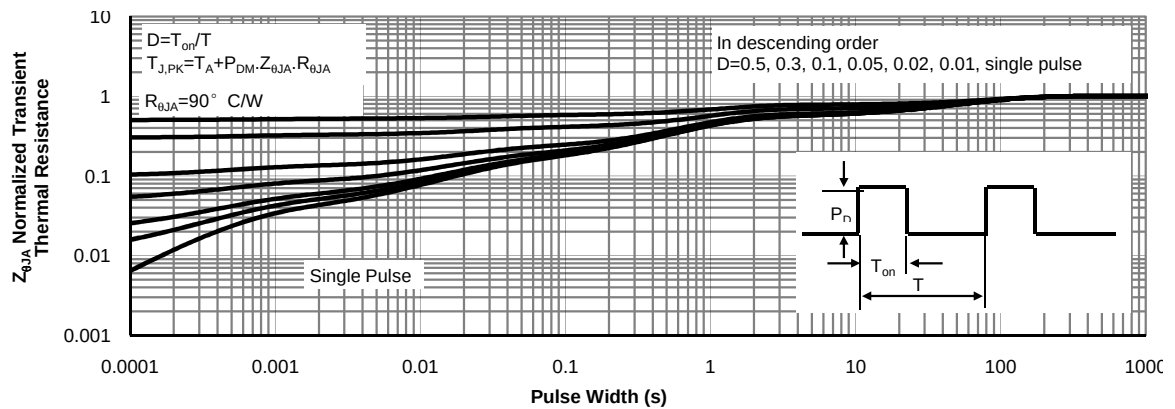
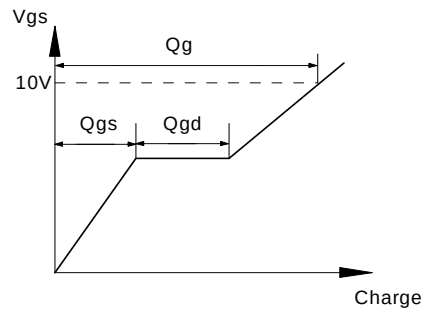
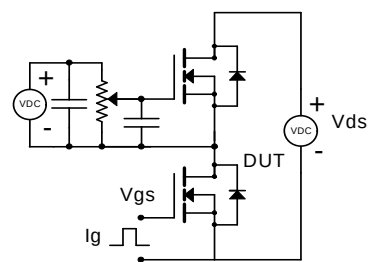
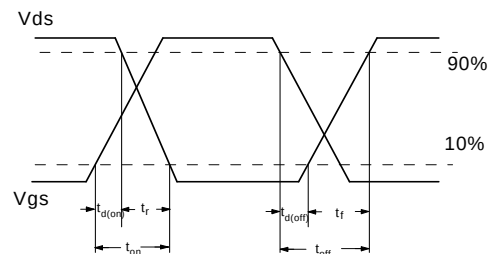
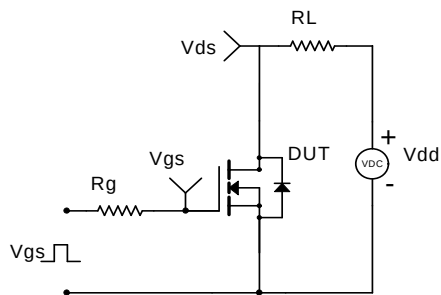


Figure 11: Normalized Maximum Transient Thermal Impedance (Note H)

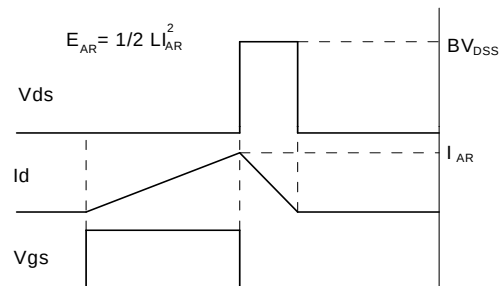
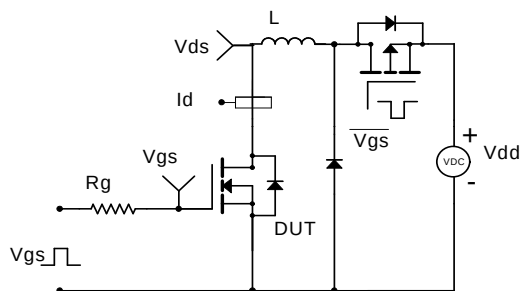
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

