



TDA6500; TDA6501

5 V mixer/oscillator and synthesizer for PAL and NTSC standards

Rev. 02 — 14 June 2005

Product data sheet

1. General description

TDA6500TT and TDA6501TT are programmable 2-mixer, 3-oscillator and synthesizer MOPLLs intended for pure 3-band tuner concepts.

The device includes two double balanced mixers for the low and mid/high bands and three oscillators for the low, mid and high bands, respectively. Other functions are an IF amplifier, a wide-band AGC detector and a PLL synthesizer. Two pins are available between the mixer output and the IF amplifier input to enable IF filtering for improved signal handling.

The device can be controlled according to the I²C-bus format.

2. Features

- Single-chip, 5 V mixer/oscillator and synthesizer for TV and VCR tuners
- I²C-bus protocol compatible with 3.3 V and 5 V microcontrollers:
 - ◆ Address + 6 data bytes transmission
 - ◆ Address + 1 status byte (I²C-bus read mode)
 - ◆ Four independent I²C-bus addresses
- Two PMOS open-drain ports with 5 mA source capability to switch high band and FM sound trap (P2 and P3)
- One PMOS open-drain port P1 with 20 mA source capability to switch the mid band
- One PMOS open-drain port P0 with 10 mA source capability to switch the low band
- Five step, 3-bit Analog-to-Digital Converter (ADC) and NPN open-collector general purpose port P6 with 5 mA sinking capability
- NPN open-collector general purpose port P4 with 5 mA sinking capability
- Internal AGC flag
- In-lock flag
- 33 V tuning voltage output
- 15-bit programmable divider
- Programmable reference divider ratio: 64, 80 or 128
- Programmable charge pump current: 60 µA or 280 µA
- Varicap drive disable
- Balanced mixer with a common emitter input for the low band (single input)
- Balanced mixer with a common base input for the mid and high bands (balanced input)
- 2-pin asymmetrical oscillator for the low band
- 2-pin asymmetrical oscillator for the mid band
- 4-pin symmetrical oscillator for the high band

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- IF preamplifier with asymmetrical 75 Ω output impedance to drive a SAW filter (500 Ω /40 pF)
- Wide-band AGC detector for internal tuner AGC:
 - ◆ Five programmable take-over points
 - ◆ Two programmable time constants

3. Applications

- TV and VCR tuners
- Specially suited for switched concepts, all systems
- Specially suited for strong off-air reception

4. Ordering information

Table 1: Ordering information

| Type number | Package | | |
|-------------|---------|--|----------|
| | Name | Description | Version |
| TDA6500TT | TSSOP32 | plastic thin shrink small outline package; 32 leads; body width 6.1 mm; lead pitch 0.65 mm | SOT487-1 |
| TDA6501TT | | | |

5. Block diagram

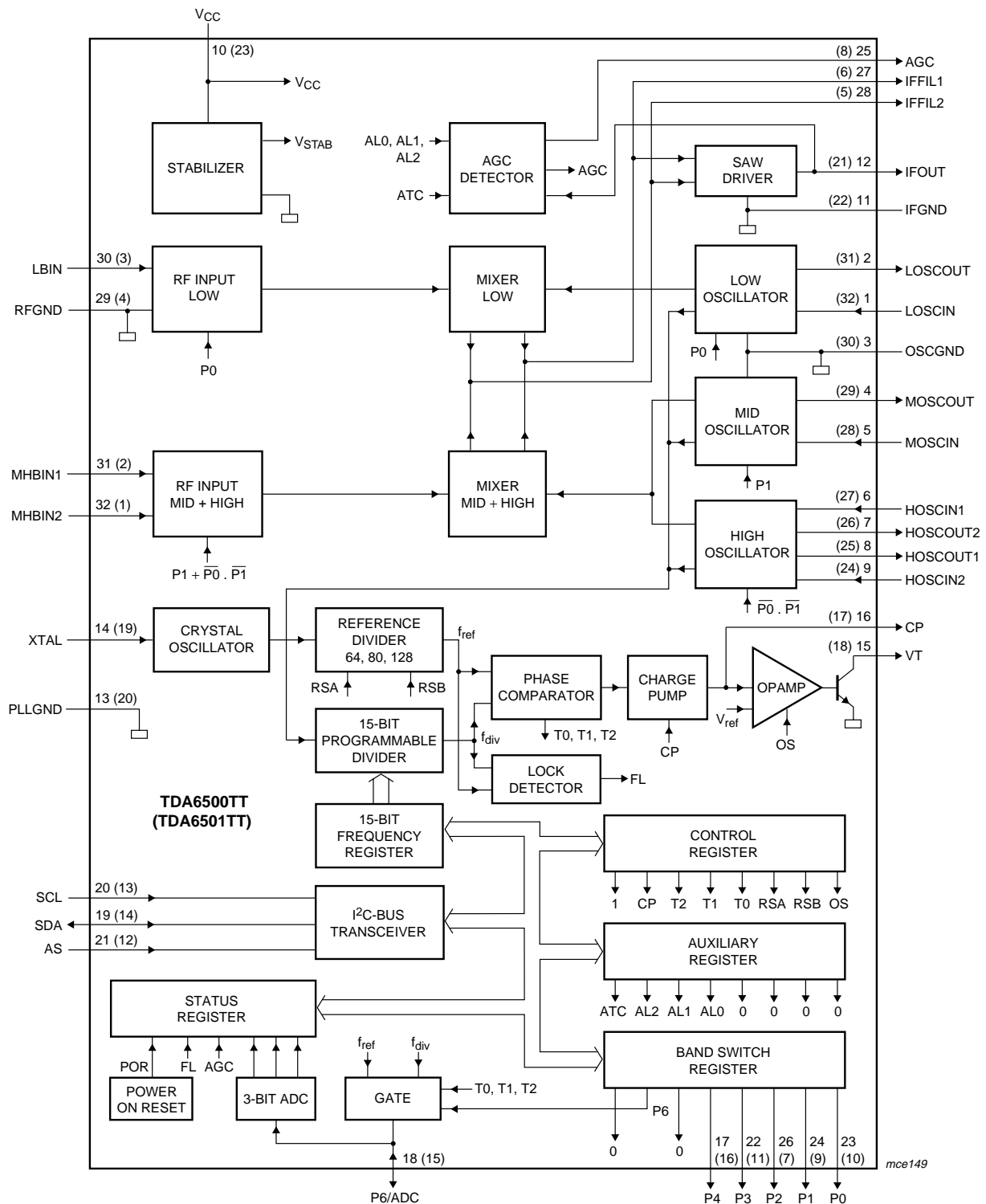
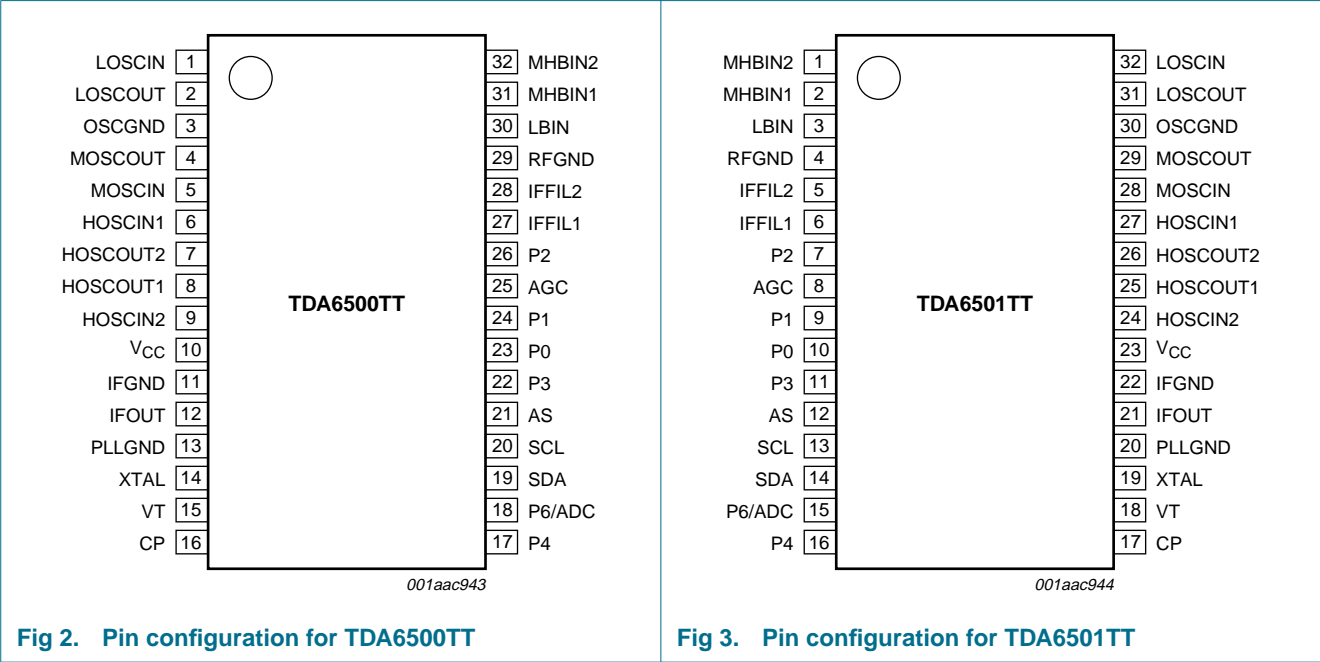


Fig 1. Block diagram

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 2: Pin description

| Symbol | Pin | | Description |
|----------|-----------|-----------|-------------------------------|
| | TDA6500TT | TDA6501TT | |
| AGC | 25 | 8 | AGC output |
| AS | 21 | 12 | address selection input |
| CP | 16 | 17 | charge pump output |
| HOSCIN1 | 6 | 27 | high band oscillator input 1 |
| HOSCIN2 | 9 | 24 | high band oscillator input 2 |
| HOSCOUT1 | 8 | 25 | high band oscillator output 1 |
| HOSCOUT2 | 7 | 26 | high band oscillator output 2 |
| IFFIL1 | 27 | 6 | IF filter output 1 |
| IFFIL2 | 28 | 5 | IF filter output 2 |
| IFGND | 11 | 22 | IF ground |
| IFOUT | 12 | 21 | IF output |
| LBIN | 30 | 3 | low band RF input |
| LOSCIN | 1 | 32 | low band oscillator input |
| LOSCOUT | 2 | 31 | low band oscillator output |
| MHBIN1 | 31 | 2 | mid and high band RF input 1 |
| MHBIN2 | 32 | 1 | mid and high band RF input 2 |
| MOSCIN | 5 | 28 | mid band oscillator input |

Table 2: Pin description ...continued

| Symbol | Pin | | Description |
|-----------------|-----------|-----------|--|
| | TDA6500TT | TDA6501TT | |
| MOSCOUT | 4 | 29 | mid band oscillator output |
| OSCGND | 3 | 30 | oscillator ground |
| P0 | 23 | 10 | PMOS open-drain port 0 to select low band operation |
| P1 | 24 | 9 | PMOS open-drain port 1 to select mid band operation |
| P2 | 26 | 7 | PMOS open-drain general purpose port 2 |
| P3 | 22 | 11 | PMOS open-drain general purpose port 3 |
| P4 | 17 | 16 | NPN open-collector general purpose port 4 |
| P6/ADC | 18 | 15 | NPN open-collector general purpose port 6 or ADC input |
| PLLGND | 13 | 20 | digital ground |
| RFGND | 29 | 4 | RF ground |
| SCL | 20 | 13 | serial clock input |
| SDA | 19 | 14 | serial data input and output |
| V _{CC} | 10 | 23 | supply voltage |
| VT | 15 | 18 | tuning voltage output |
| XTAL | 14 | 19 | crystal oscillator input |

7. Functional description

7.1 General

TDA6500TT and TDA6501TT are programmable 2-mixer, 3-oscillator and synthesizer MOPLLs intended for pure 3-band tuner concepts.

The device includes two double balanced mixers for the low and mid/high bands and three oscillators for the low, mid and high bands respectively. The band limits for PAL tuners are shown in [Table 3](#).

Table 3: Low, mid and high band limits

| Band | Input f_{RFpix} (MHz) | | Oscillator f_{osc} (MHz) | |
|------|-------------------------|--------|----------------------------|--------|
| | Min | Max | Min | Max |
| Low | 45.25 | 154.25 | 84.15 | 193.15 |
| Mid | 161.25 | 439.25 | 200.15 | 478.15 |
| High | 455.25 | 855.25 | 494.15 | 894.15 |

Other functions are an IF amplifier, a wide-band AGC detector and a PLL synthesizer.

Two pins are available between the mixer output and the IF amplifier input to enable IF filtering for improved signal handling.

Bit P0 enables Port P0 and the low band mixer and oscillator (see [Table 4](#)). Bit P1 enables Port P1, the mid/high band mixer and the mid band oscillator. Bit P2 enables Port P2 and bit P3 enables Port P3. When Ports P0 and P1 are disabled, the mid/high band mixer and the high band oscillator are enabled.

Table 4: Mixer and oscillator band selection

| Bit | | Mixer band | | | Oscillator band | | |
|-----|----|------------|-----|------|-----------------|-----|------|
| P0 | P1 | low | mid | high | low | mid | high |
| 1 | 0 | x | | | x | | |
| 0 | 1 | | x | x | | x | |
| 0 | 0 | | x | x | | | x |

The AGC detector provides information about the IF amplifier level. Five AGC take-over points are available by software. Two programmable AGC time constants are available for search tuning and normal tuner operation. The synthesizer consists of a 15-bit programmable divider, a crystal oscillator and its programmable reference divider and a phase/frequency detector combined with a charge pump, which drives the tuning amplifier including 33 V output.

Depending on the reference divider ratio (64, 80 or 128) the phase comparator operates at 62.50 kHz, 50.00 kHz or 31.25 kHz with a 4 MHz crystal.

The device can be controlled according to the I²C-bus format. The lock detector bit FL is set to logic 1 when the loop is locked. The AGC bit is set to logic 1 when the internal AGC is active (level below 3 V). These two flags are read on the SDA line (status byte) during a read operation (see [Table 11](#)).

The ADC input is available on pin P6/ADC for digital AFC control. The ADC code is read during a read operation (see [Table 11](#)). In test mode, pin P6/ADC is used as a test output for $\frac{1}{2}f_{ref}$ and $\frac{1}{2}f_{div}$ (see [Table 8](#)).

A minimum of seven bytes, including address byte, is required to address the device, select the VCO frequency, program the ports, set the charge pump current, set the reference divider ratio, select the AGC take-over point and select the AGC time constant. The device has four independent I²C-bus addresses which can be selected by applying a specific voltage on input AS (see [Table 7](#)).

7.2 Device control

The device is controlled via the I²C-bus. For programming, a module address of 7 bits and the R/W bit for selecting the read or the write mode is required.

7.2.1 Write mode

Data bytes can be sent to the device after the address transmission (first byte). Seven data bytes are needed to fully program the device. The bus transceiver has an auto-increment facility, which permits the programming of the device within one single transmission (address + 6 data bytes).

The device can also be partially programmed providing that the first data byte following the address is the first divider byte DB1 or the control byte CB. The data bytes are defined in [Table 5](#) and [Table 6](#).

The first bit of the first data byte indicates whether frequency data (first bit = 0) or control, port and auxiliary data (first bit = 1) will follow. Until an I²C-bus STOP command is sent by the controller, additional data bytes can be entered without the need to re-address the device. The frequency register is loaded with data from byte DB2 after the 8th SCL clock

pulse, the control register is loaded with data from byte CB after the 8th SCL clock pulse, the band switch register is loaded with data of byte BB after the 8th SCL clock pulse and the auxiliary register is loaded with data of byte AB after the 8th SCL clock pulse.

To program the AGC take-over point setting and the AGC current to a different value than the default value, an additional byte, the auxiliary byte, has to be sent. To this end, the auxiliary byte is preceded by a control byte with the test bits T2, T1 and T0 set to logic 011 (see [Table 8](#)).

Table 5: I²C-bus data format for write mode

| Name | Byte | Bit | | | | | | | | Ack |
|-------------------------------|------|-----|-----|-----|-----|-----|-----|-----|----------------------|-----|
| | | MSB | | | | | | | LSB | |
| Address byte | ADB | 1 | 1 | 0 | 0 | 0 | MA1 | MA0 | $R/\overline{W} = 0$ | A |
| Divider byte 1 | DB1 | 0 | N14 | N13 | N12 | N11 | N10 | N9 | N8 | A |
| Divider byte 2 | DB2 | 0 | N7 | N6 | N5 | N4 | N3 | N2 | N1 | A |
| Control byte | CB | 1 | CP | T2 | T1 | T0 | RSA | RSB | OS | A |
| Band switch byte | BB | 0 | P6 | 0 | P4 | P3 | P2 | P1 | P0 | A |
| Auxiliary byte ^[1] | AB | ATC | AL2 | AL1 | AL0 | 0 | 0 | 0 | 0 | A |

[1] Auxiliary byte AB replaces band switch byte BB when bit T2 = 0, T1 = 1 and T0 = 1.

Table 6: Description of bits shown in [Table 5](#)

| Symbol | Description |
|------------------|--|
| A | acknowledge |
| MA1 and MA0 | programmable address bits; see Table 7 |
| R/\overline{W} | logic 0 for write mode |
| N14 to N0 | programmable divider bits; $N = (N14 \times 2^{14}) + (N13 \times 2^{13}) + \dots + (N1 \times 2^1) + N0$ |
| CP | charge pump current CP = 0: the charge pump current is 60 μ A CP = 1: the charge pump current is 280 μ A (default) |
| T2, T1 and T0 | test bits; see Table 8 |
| RSA and RSB | reference divider ratio select bits; see Table 9 |
| OS | tuning amplifier control bit OS = 0: normal operation; tuning voltage is on OS = 1: tuning voltage is off; high-impedance state (default) |
| P6 and P4 | NPN port control bits Pn = 0: port n is off; high-impedance state (default) Pn = 1: buffer n is on; $V_O = V_{CE(sat)}$ |
| P3 to P0 | PMOS port control bits Pn = 0: port n is off; high-impedance state (default) Pn = 1: buffer n is on; $V_O = V_{CC} - V_{DS(sat)}$ |
| ATC | AGC time constant ATC = 0: $I_{AGC} = 220$ nA; $\Delta t = 2$ s with C = 160 nF (default) ATC = 1: $I_{AGC} = 9$ μ A; $\Delta t = 50$ ms with C = 160 nF |
| AL2, AL1 and AL0 | AGC take-over point bits; see Table 10 |

The module address contains programmable address bits (MA1 and MA0) which offer the possibility of having up to 4 synthesizers in one system by applying a specific voltage on the AS input. [Table 7](#) gives the relationship between the input voltage applied to the AS input and bits MA1 and MA0.

Table 7: I²C-bus address selection

| Voltage applied to pin AS | MA1 | MA0 |
|--|-----|-----|
| 0 V to 0.1V _{CC} | 0 | 0 |
| 0.2V _{CC} to 0.3V _{CC} or open | 0 | 1 |
| 0.4V _{CC} to 0.6V _{CC} | 1 | 0 |
| 0.9V _{CC} to V _{CC} | 1 | 1 |

Table 8: Test modes

| T2 | T1 | T0 | Test modes |
|----|----|----|--|
| 0 | 0 | 0 | normal mode |
| 0 | 0 | 1 | normal mode; default mode at power-on reset |
| 0 | 1 | 0 | charge pump is off |
| 0 | 1 | 1 | control byte is followed by auxiliary byte AB instead of the band switch byte BB |
| 1 | 1 | 0 | charge pump is sinking current |
| 1 | 1 | 1 | charge pump is sourcing current |
| 1 | 0 | 0 | $\frac{1}{2}f_{ref}$ is available on pin P6/ADC [1] |
| 1 | 0 | 1 | $\frac{1}{2}f_{div}$ is available on pin P6/ADC [1] |

[1] The ADC input cannot be used when these test modes are active; see [Section 7.2.2](#) for more information.

Table 9: Reference divider ratio select

| RSA | RSB | Reference divider ratio |
|-----|-----|-------------------------|
| 0 | 0 | 80 |
| 0 | 1 | 128 |
| 1 | 1 | 64 |
| 1 | 0 | forbidden |

Table 10: AGC take-over point

| AL2 | AL1 | AL0 | Asymmetrical mode |
|-----|-----|-----|---|
| 0 | 0 | 0 | 115 dB μ V |
| 0 | 0 | 1 | 115 dB μ V |
| 0 | 1 | 0 | 112 dB μ V; default mode at power-on reset |
| 0 | 1 | 1 | 109 dB μ V |
| 1 | 0 | 0 | 106 dB μ V |
| 1 | 0 | 1 | 103 dB μ V |
| 1 | 1 | 0 | I _{AGC} = 0 mA; external AGC [1] |
| 1 | 1 | 1 | 3.5 V; disabled [1] |

[1] The AGC detector is disabled. Both the sinking and sourcing currents from the IC are disabled. The AGC output goes into a high-impedance state and an external AGC source can be connected in parallel.

[2] The AGC detector is disabled and the fast mode current source is enabled.

7.2.2 Read mode

Data can be read from the device by setting the R/\overline{W} bit to logic 1. The data read format is shown in [Table 11](#). After the slave address has been recognized, the device generates an acknowledge pulse and the first data byte (status byte) is transferred on the SDA line with the MSB first. Data is valid on the SDA line during a HIGH-level of the SCL clock signal.

A second data byte can be read from the device if the microcontroller generates an acknowledge on the SDA line (master acknowledge). End of transmission will occur if no master acknowledge occurs. The device will then release the data line to allow the microcontroller to generate a STOP condition.

The POR flag is set to logic 1 at power-on. The flag is reset when an end-of-data is detected by the device (end of a read sequence).

Control of the loop is made possible with the in-lock flag (FL) which indicates when the loop is locked (FL = 1).

The internal AGC status is available from the AGC bit. AGC = 1 indicates when the selected take-over point is reached.

A built-in ADC is available on the P6/ADC pin. The ADC can be used to apply AFC information to the microcontroller from the IF section of the tuner. The relationship between the voltage applied to the ADC input and the A2, A1 and A0 bits is given in [Table 13](#).

Table 11: Read data format

| Name | Byte | Bit | | | | | | | | Ack |
|--------------|------|---------|----|---|---|-----|-----|-----|----------------------|-----|
| | | MSB [1] | | | | | | | LSB | |
| Address byte | ADB | 1 | 1 | 0 | 0 | 0 | MA1 | MA0 | $R/\overline{W} = 1$ | A |
| Status byte | SB | POR | FL | 1 | 1 | AGC | A2 | A1 | A0 | - |

[1] MSB is transmitted first.

Table 12: Description of bits shown in [Table 11](#)

| Symbol | Description |
|------------------|---|
| A | acknowledge |
| MA1 and MA0 | programmable address bits; see Table 7 |
| R/\overline{W} | logic 1 for read mode |
| POR | power-on reset flag POR = 0, normal operation POR = 1, power-on state |
| FL | in-lock flag FL = 0, not locked FL = 1, the PLL is locked |
| AGC | internal AGC flag AGC = 0, internal AGC not active AGC = 1, internal AGC is active; level below 3 V |
| A2, A1 and A0 | digital output of the 5-level ADC; see Table 13 |

Table 13: ADC levels

| Voltage applied to ADC input ^[1] | A2 | A1 | A0 |
|---|----|----|----|
| 0.60V _{CC} to V _{CC} | 1 | 0 | 0 |
| 0.45V _{CC} to 0.60V _{CC} | 0 | 1 | 1 |
| 0.30V _{CC} to 0.45V _{CC} | 0 | 1 | 0 |
| 0.15V _{CC} to 0.30V _{CC} | 0 | 0 | 1 |
| 0 V to 0.15V _{CC} | 0 | 0 | 0 |

[1] Accuracy is $\pm 0.03V_{CC}$.

7.2.3 Power-on reset

The power-on detection threshold voltage is set to $V_{POR} = 3.5$ V at room temperature. Below this threshold, the device is reset to the power-on state.

In the power-on state, the charge pump current is set to 280 μ A, the tuning voltage output is disabled, the test bits T2 = 0, T1 = 0 and T0 = 1, the AGC take-over point is set to 112 dB μ V and the AGC current is set to the slow mode. The high band is selected by default.

Table 14: Default bits at power-on reset

| Name | Byte | Bit | | | | | | | |
|------------------|------|-----|---|---|---|---|-----|-----|---|
| | | MSB | | | | | | LSB | |
| Address byte | ADB | 1 | 1 | 0 | 0 | 0 | MA1 | MA0 | X |
| Divider byte 1 | DB1 | 0 | X | X | X | X | X | X | X |
| Divider byte 2 | DB2 | X | X | X | X | X | X | X | X |
| Control byte | CB | 1 | 1 | 0 | 0 | 1 | X | X | 1 |
| Band switch byte | BB | - | 0 | - | 0 | 0 | 0 | 0 | 0 |
| Auxiliary byte | AB | 0 | 0 | 1 | 0 | - | - | - | - |

8. Internal circuitry

Table 15: Internal circuits

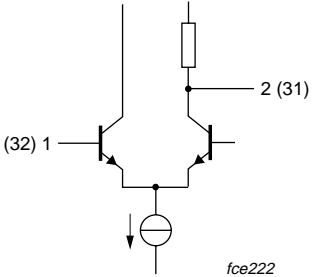
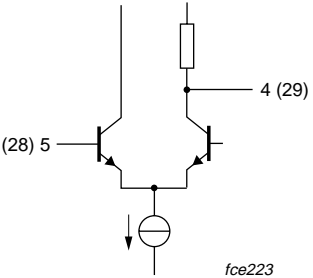
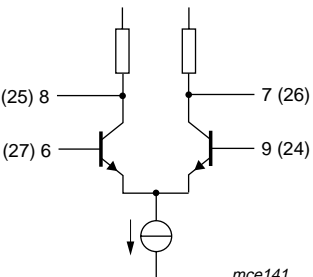
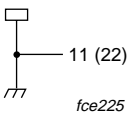
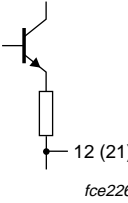
| Symbol | Pin | | Average DC voltage versus band selection | | | Equivalent circuit ^[1] |
|-----------------|-----------|-----------|--|------|------|---|
| | TDA6500TT | TDA6501TT | Low | Mid | High | |
| LOSCIN | 1 | 32 | 1.7 | 1.4 | 1.4 |  fce222 |
| LOSCOUT | 2 | 31 | 2.9 | 3.5 | 3.5 | |
| OSCGND | 3 | 30 | - | - | - | - |
| MOSCOU2 | 4 | 29 | 3.5 | 3.02 | 3.5 |  fce223 |
| MOSCIN | 5 | 28 | 1.4 | 1.7 | 1.4 | |
| HOSCIN1 | 6 | 27 | 2.2 | 2.2 | 1.8 |  mce141 |
| HOSCOU2 | 7 | 26 | 5 | 5 | 2.5 | |
| HOSCOU1 | 8 | 25 | 5 | 5 | 2.5 | |
| HOSCIN2 | 9 | 24 | 2.2 | 2.2 | 1.8 | |
| V _{CC} | 10 | 23 | 5.0 | 5.0 | 5.0 | - |
| IFGND | 11 | 22 | - | - | - |  fce225 |
| IFOUT | 12 | 21 | 2.1 | 2.1 | 2.1 |  fce226 |

Table 15: Internal circuits ...continued

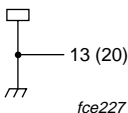
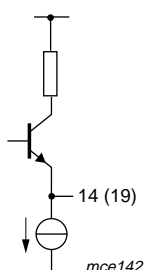
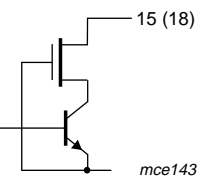
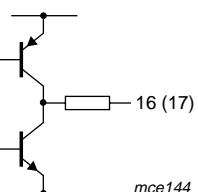
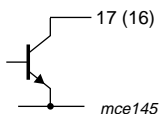
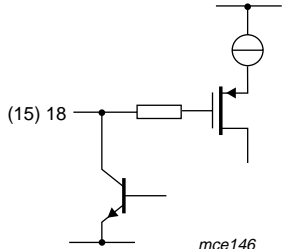
| Symbol | Pin | | Average DC voltage versus band selection | | | Equivalent circuit ^[1] |
|---------|-----------|-----------|--|----------------------------|----------------------------|---|
| | TDA6500TT | TDA6501TT | Low | Mid | High | |
| PLL GND | 13 | 20 | - | - | - |  fce227 |
| XTAL | 14 | 19 | 0.7 | 0.7 | 0.7 |  mce142 |
| VT | 15 | 18 | V_{VT} | V_{VT} | V_{VT} |  mce143 |
| CP | 16 | 17 | 1.0 | 1.0 | 1.0 |  mce144 |
| P4 | 17 | 16 | $V_{CE(sat)}$ or High Z | $V_{CE(sat)}$ or High Z | $V_{CE(sat)}$ or High Z |  mce145 |
| P6/ADC | 18 | 15 | $V_{CE(sat)}$ or High Z | $V_{CE(sat)}$ or High Z | $V_{CE(sat)}$ or High Z |  mce146 |

Table 15: Internal circuits ...continued

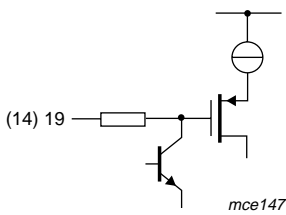
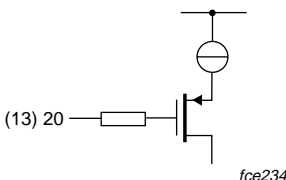
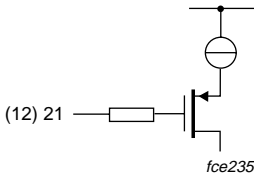
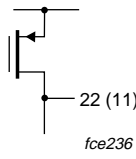
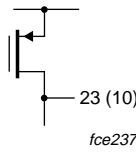
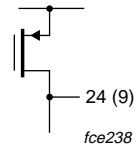
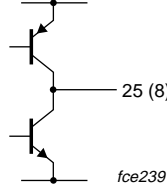
| Symbol | Pin | | Average DC voltage versus band selection | | | Equivalent circuit ^[1] |
|--------|-----------|-----------|--|-----------------------------|-----------------------------|---|
| | TDA6500TT | TDA6501TT | Low | Mid | High | |
| SDA | 19 | 14 | n.a. | n.a. | n.a. |  |
| SCL | 20 | 13 | n.a. | n.a. | n.a. |  |
| AS | 21 | 12 | 1.25 | 1.25 | 1.25 |  |
| P3 | 22 | 11 | High Z or $V_{CC} - V_{DS}$ | High Z or $V_{CC} - V_{DS}$ | High Z or $V_{CC} - V_{DS}$ |  |
| P0 | 23 | 10 | $V_{CC} - V_{DS}$ | High Z | High Z |  |
| P1 | 24 | 9 | High Z | $V_{CC} - V_{DS}$ | High Z |  |
| AGC | 25 | 8 | 0 V or 3.5 V | 0 V or 3.5 V | 0 V or 3.5 V |  |

Table 15: Internal circuits ...continued

| Symbol | Pin | | Average DC voltage versus band selection | | | Equivalent circuit ^[1] |
|--------|-----------|-----------|--|-----------------------------|-----------------------------|-----------------------------------|
| | TDA6500TT | TDA6501TT | Low | Mid | High | |
| P2 | 26 | 7 | High Z or $V_{CC} - V_{DS}$ | High Z or $V_{CC} - V_{DS}$ | High Z or $V_{CC} - V_{DS}$ | fce240 |
| IFFIL1 | 27 | 6 | 4.4 | 4.4 | 4.4 | fce241 |
| IFFIL2 | 28 | 5 | 4.4 | 4.4 | 4.4 | |
| RFGND | 29 | 4 | - | - | - | fce242 |
| LBIN | 30 | 3 | 1.8 | n.a. | n.a. | fce243 |
| MHBIN1 | 31 | 2 | n.a. | 1.0 | 1.0 | mce148 |
| MHBIN2 | 32 | 1 | n.a. | 1.0 | 1.0 | |

[1] The pin numbers in parenthesis represent the TDA6501TT.

9. Limiting values

Table 16: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). [\[1\]](#)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|--|------------|------|----------------|------|
| V_{CC} | supply voltage | | -0.3 | +6 | V |
| V_{XTAL} | crystal input voltage | | -0.3 | $V_{CC} + 0.3$ | V |
| $V_{P6/ADC}$ | NPN port input and output voltage | | -0.3 | $V_{CC} + 0.3$ | V |
| $I_{P6/ADC}$ | NPN port output current (open-collector) | | 0 | 10 | mA |
| V_{VT} | tuning voltage output | | -0.3 | +35 | V |
| V_{CP} | charge pump output voltage | | -0.3 | $V_{CC} + 0.3$ | V |
| V_{P4} | NPN port output voltage (open-collector) | | -0.3 | $V_{CC} + 0.3$ | V |
| I_{P4} | NPN port output current (open-collector) | | 0 | 10 | mA |
| V_{SDA} | serial data input/output voltage | | -0.3 | +6 | V |
| I_{SDA} | serial data output current | | -1 | +10 | mA |
| V_{SCL} | serial clock input voltage | | -0.3 | +6 | V |
| V_{AS} | address selection input voltage | | -0.3 | $V_{CC} + 0.3$ | V |
| V_{Pn} | PMOS port output voltage (open-drain) | | -0.3 | $V_{CC} + 0.3$ | V |
| I_{P1} | PMOS port output current (open-drain) | | -25 | 0 | mA |
| I_{P0} | PMOS port output current (open-drain) | | -15 | 0 | mA |
| I_{P2}, I_{P3} | PMOS port output current (open-drain) | | -10 | 0 | mA |
| T_{stg} | storage temperature | | -40 | +150 | °C |
| T_{amb} | ambient temperature | | -20 | +85 | °C |
| T_j | junction temperature | | - | 150 | °C |

[1] Maximum ratings cannot be exceeded, not even momentarily without causing irreversible IC damage. Maximum ratings cannot be accumulated.

10. Thermal characteristics

Table 17: Thermal characteristics

| Symbol | Parameter | Conditions | Typ | Unit |
|--------------------------------------|---|---|-------------------------|------|
| SOT487EC3 package (TDA6500TT) | | | | |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air; one layer printed-circuit board, JEDEC standards | [1] 110 | K/W |
| SOT487EC5 package (TDA6501TT) | | | | |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air; one layer printed-circuit board, JEDEC standards | [1] 115 | K/W |

[1] The thermal resistance is highly dependant on the printed-circuit board on which the package is mounted. The thermal resistance values are given only for customer's guidance.

11. Characteristics

Table 18: Supplies

$V_{CC} = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; values are given for an IF amplifier with $500\text{ }\Omega$ load (measured as shown in [Figure 7](#) for the PAL standard); unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|----------------|---|-----|-----|-----|------|
| Supply | | | | | | |
| V_{CC} | supply voltage | | 4.5 | 5.0 | 5.5 | V |
| I_{CC} | supply current | all PNP ports off | - | 74 | 94 | mA |
| | | one PNP port on; sourcing 20 mA | - | 96 | 116 | mA |
| | | two PNP ports on; one port sourcing 20 mA; one other port sourcing 5 mA | | 102 | 122 | mA |

Table 19: PLL

$V_{CC} = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; values are given for an IF amplifier with $500\text{ }\Omega$ load (measured as shown in [Figure 7](#) for the PAL standard); unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------|----------------------------------|---|-----|------|-------|----------|
| Functional range | | | | | | |
| V_{POR} | power-on reset supply voltage | for a voltage lower than V_{POR} , power-on reset is active | 1.5 | 3.5 | - | V |
| N | divider ratio | 15-bit frequency word | 64 | - | 32767 | |
| f_{XTAL} | crystal oscillator frequency | $R_{XTAL} = 25\text{ }\Omega$ to $300\text{ }\Omega$ | 3.2 | 4.0 | 4.48 | MHz |
| $ Z_{XTAL} $ | input impedance (absolute value) | $f_{XTAL} = 4\text{ MHz}$ | 600 | 1200 | - | Ω |

PMOS ports: P0, P1, P2 and P3

| | | | | | | |
|--|---------------------------|---|---|------|-----|---------------|
| I_{LO} | output leakage current | $V_{CC} = 5.5\text{ V}$; $V_{Pn} = 0\text{ V}$ | - | - | 10 | μA |
| $V_{DS(P0)(sat)}$ | output saturation voltage | buffer P0 is on only; sourcing 10 mA | - | 0.25 | 0.4 | V |
| $V_{DS(P1)(sat)}$ | output saturation voltage | buffer P1 is on only; sourcing 20 mA | - | 0.25 | 0.4 | V |
| $V_{DS(P2)(sat)}$, $V_{DS(P3)(sat)}$ | output saturation voltage | buffer P2 or P3 is on; sourcing 5 mA | - | 0.25 | 0.4 | V |

NPN ports: P4 and P6

| | | | | | | |
|---------------|---------------------------|---|---|------|-----|---------------|
| I_{LO} | output leakage current | $V_{CC} = 5.5\text{ V}$; $V_{Pn} = 6\text{ V}$ | - | - | 10 | μA |
| $V_{CE(sat)}$ | output saturation voltage | buffer P4 or P6 is on; sinking 5 mA | - | 0.25 | 0.4 | V |

ADC input

| | | | | | | |
|----------|--------------------------|------------------------------|-----|---|----------|---------------|
| V_i | ADC input voltage | see Table 13 | 0 | - | V_{CC} | V |
| I_{IH} | HIGH-level input current | ADC input $V_i = V_{CC}$ | - | - | 10 | μA |
| I_{IL} | LOW-level input current | ADC input $V_i = 0\text{ V}$ | -10 | - | - | μA |

AS input (address selection)

| | | | | | | |
|----------|--------------------------|-----------------------------|-----|---|----|---------------|
| I_{IH} | HIGH-level input current | AS input $V_i = V_{CC}$ | - | - | 10 | μA |
| I_{IL} | LOW-level input current | AS input $V_i = 0\text{ V}$ | -10 | - | - | μA |

SCL and SDA inputs

| | | | | | | |
|----------|--------------------------|--|-----|---|-----|---------------|
| V_{IL} | LOW-level input voltage | | 0 | - | 1.5 | V |
| V_{IH} | HIGH-level input voltage | | 2.3 | - | 5.5 | V |
| I_{IH} | HIGH-level input current | $V_{BUS} = 5.5\text{ V}$; $V_{CC} = 0\text{ V}$ | - | - | 10 | μA |
| | | $V_{BUS} = 5.5\text{ V}$; $V_{CC} = 5.5\text{ V}$ | - | - | 10 | μA |

Table 19: PLL ...continued

$V_{CC} = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; values are given for an IF amplifier with $500\text{ }\Omega$ load (measured as shown in [Figure 7](#) for the PAL standard); unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------|---|--|-----|-----|------|------|
| I _{IL} | LOW-level input current | V _{BUS} = 1.5 V; V _{CC} = 0 V | - | - | 10 | μA |
| | | V _{BUS} = 0 V; V _{CC} = 5.5 V | −10 | - | - | μA |
| SDA output | | | | | | |
| I _{LO} | leakage current | SDA output V _o = 5.5 V | - | - | 10 | μA |
| V _o | output voltage | I _{o(sink)} = 3 mA | - | - | 0.4 | V |
| Clock frequency | | | | | | |
| f _{clk} | clock frequency | | - | - | 400 | kHz |
| Charge pump output CP | | | | | | |
| I _{IH} | HIGH-level input current (absolute value) | CP = 1 | - | 280 | - | μA |
| I _{IL} | LOW-level input current (absolute value) | CP = 0 | - | 60 | - | μA |
| I _{LO(off)} | off-state leakage current | T2 = 0; T1 = 1; T0 = 0 | −15 | 0 | +15 | nA |
| Tuning voltage output VT | | | | | | |
| I _{LO(off)} | off-state leakage current | OS = 1; V _{VT} = 33 V | - | - | 10 | μA |
| V _o | output voltage when the loop is closed | OS = 0; T2 = 0; T1 = 0; T0 = 1; R _L = 27 kΩ; V _{VT} = 33 V | 0.2 | - | 32.7 | V |

Table 20: Mixer

$V_{CC} = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; values are given for an IF amplifier with $500\text{ }\Omega$ load (measured as shown in [Figure 7](#) for the PAL standard); unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|--|--|------------|------|--------|------------------|
| Low band mixer mode (P0 = 1 and P1 = 0); including IF amplifier | | | | | | |
| f_{RF} | RF frequency | picture carrier | [1] 44.25 | - | 154.25 | MHz |
| G_v | voltage gain | $f_{RF} = 44.25\text{ MHz}$; see Figure 8 | 25.0 | 27.5 | 30 | dB |
| | | $f_{RF} = 157\text{ MHz}$; see Figure 8 | 25.0 | 27.5 | 30 | dB |
| NF | noise figure | $f_{RF} = 50\text{ MHz}$; see Figure 9 and 10 | - | 8.0 | 10.0 | dB |
| $V_{o(mod)}$ | output voltage causing 0.3 % cross modulation in channel | $f_{RF} = 44.25\text{ MHz}$; see Figure 12 | 108 | 111 | - | dB μV |
| | | $f_{RF} = 157\text{ MHz}$; see Figure 12 | 108 | 111 | - | dB μV |
| $V_{o(FM)}$ | output voltage causing 1.1 kHz incidental FM | $f_{RF} = 44.25\text{ MHz}$ | [2] 108 | 111 | - | dB μV |
| | | $f_{RF} = 157\text{ MHz}$ | [2] 108 | 111 | - | dB μV |
| INT_{SO2} | channel SO2 beat | $V_{RFpix} = 115\text{ dB}\mu\text{V}$ at IF output | [3] 57 | 60 | - | dBc |
| V_i | input level without lock-out | see Figure 11 | [4] - | - | 120 | dB μV |
| g_{os} | optimum source conductance for noise figure | $f_{RF} = 50\text{ MHz}$ | - | 0.7 | - | mS |
| | | $f_{RF} = 150\text{ MHz}$ | - | 0.9 | - | mS |
| g_i | input conductance | $f_{RF} = 44.25\text{ MHz}$; see Figure 4 | - | 0.30 | - | mS |
| | | $f_{RF} = 161.25\text{ MHz}$; see Figure 4 | - | 0.33 | - | mS |
| C_i | input capacitance | $f_{RF} = 44.25\text{ to }161.25\text{ MHz}$; see Figure 4 | - | 1.29 | - | pF |
| High band mixer in mid band mode (P0 = 0 and P1 = 1); including IF amplifier | | | | | | |
| f_{RF} | RF frequency | picture carrier | [1] 161.25 | - | 439.25 | MHz |

Table 20: Mixer ...continued

$V_{CC} = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; values are given for an IF amplifier with $500\text{ }\Omega$ load (measured as shown in [Figure 7](#) for the PAL standard); unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|--|---|------------|-----|--------|------------|
| G_v | voltage gain | $f_{RF} = 157\text{ MHz}$; see Figure 13 | 35 | 38 | 41 | dB |
| | | $f_{RF} = 443\text{ MHz}$; see Figure 13 | 35 | 38 | 41 | dB |
| NF | noise figure (not corrected for image) | $f_{RF} = 157\text{ MHz}$; see Figure 14 | - | 6 | 8.0 | dB |
| | | $f_{RF} = 443\text{ MHz}$; see Figure 14 | - | 6 | 8.0 | dB |
| $V_{o(mod)}$ | output voltage causing 0.3 % cross modulation in channel | $f_{RF} = 157\text{ MHz}$; see Figure 15 | 108 | 111 | - | dB μ V |
| | | $f_{RF} = 443\text{ MHz}$; see Figure 15 | 108 | 111 | - | dB μ V |
| $V_{o(FM)}$ | output voltage causing 1.1 kHz incidental FM | $f_{RF} = 157\text{ MHz}$ | [2] 108 | 111 | - | dB μ V |
| | | $f_{RF} = 443\text{ MHz}$ | [2] 108 | 111 | - | dB μ V |
| $V_{f(N+5)-1}$ | $(N + 5) - 1\text{ MHz}$ pulling | $f_{RFwanted} = 443\text{ MHz}$; $f_{osc} = 481.9\text{ MHz}$; $f_{RFunwanted} = 482\text{ MHz}$ | [5] 72 | 80 | - | dB μ V |
| Z_i | input impedance ($R_S + jL_S\omega$) | R_S at $f_{RF} = 157\text{ MHz}$; see Figure 5 | - | 25 | - | Ω |
| | | R_S at $f_{RF} = 443\text{ MHz}$; see Figure 5 | - | 25 | - | Ω |
| | | L_S at $f_{RF} = 157\text{ MHz}$; see Figure 5 | - | 13 | - | nH |
| | | L_S at $f_{RF} = 443\text{ MHz}$; see Figure 5 | - | 13 | - | nH |
| V_i | input level without lock-out | see Figure 16 | [4] - | - | 120 | dB μ V |
| High band mixer in high band mode ($P_0 = 0$ and $P_1 = 0$); including IF amplifier | | | | | | |
| f_{RF} | RF frequency | picture carrier | [1] 455.25 | - | 855.25 | MHz |
| G_v | voltage gain | $f_{RF} = 443\text{ MHz}$; see Figure 13 | 35 | 38 | 41 | dB |
| | | $f_{RF} = 863.25\text{ MHz}$; see Figure 13 | 35 | 38 | 41 | dB |
| NF | noise figure (not corrected for image) | $f_{RF} = 443\text{ MHz}$; see Figure 14 | - | 6.0 | 8.0 | dB |
| | | $f_{RF} = 863.25\text{ MHz}$; see Figure 14 | - | 7.0 | 9.0 | dB |
| $V_{o(mod)}$ | output voltage causing 0.3 % cross modulation in channel | $f_{RF} = 443\text{ MHz}$; see Figure 15 | 108 | 111 | - | dB μ V |
| | | $f_{RF} = 863.25\text{ MHz}$; see Figure 15 | 108 | 111 | - | dB μ V |
| $V_{o(FM)}$ | output voltage causing 1.1 kHz incidental FM | $f_{RF} = 443\text{ MHz}$ | [2] 108 | 111 | - | dB μ V |
| | | $f_{RF} = 863.25\text{ MHz}$ | [2] 108 | 111 | - | dB μ V |
| $V_{f(N+5)-1}$ | $(N + 5) - 1\text{ MHz}$ pulling | $f_{RFwanted} = 863.25\text{ MHz}$; $f_{osc} = 902.15\text{ MHz}$; $f_{RFunwanted} = 902.25\text{ MHz}$ | [5] 72 | 80 | - | dB μ V |
| Z_i | input impedance ($R_S + jL_S\omega$) | R_S at $f_{RF} = 443\text{ MHz}$; see Figure 5 | - | 25 | - | Ω |
| | | R_S at $f_{RF} = 863.25\text{ MHz}$; see Figure 5 | - | 23 | - | Ω |
| | | L_S at $f_{RF} = 443\text{ MHz}$; see Figure 5 | - | 13 | - | nH |
| | | L_S at $f_{RF} = 863.25\text{ MHz}$; see Figure 5 | - | 13 | - | nH |
| V_i | input level without lock-out | see Figure 16 | [4] - | - | 120 | dB μ V |

- [1] The RF frequency range is defined by the oscillator frequency range and the Intermediate Frequency (IF).
- [2] This is the level of the RF unwanted signal, 50 % amplitude modulated with 1 kHz, that causes a 1.1 kHz FM modulation of the local oscillator and thus of the wanted signal; $V_{wanted} = 100\text{ dB}\mu\text{V}$; $f_{unwanted} = f_{wanted} + 5.5\text{ MHz}$. The FM modulation is measured at the oscillator output with a peaking coil using a modulation analyzer with a peak-to-peak detector and a post detection filter of 300 Hz up to 3 kHz.
- [3] Channel SO2 beat is the interfering product of f_{RFpix} , f_{IF} and f_{osc} of channel SO2; $f_{beat} = 37.35\text{ MHz}$. The possible mechanisms are: $f_{osc} - 2 \times f_{IF}$ or $2 \times f_{RFpix} - f_{osc}$. For the measurement $V_{o(IFOUT)} = V_{RFpix} = 115\text{ dB}\mu\text{V}$.

- [4] The IF output signal stays stable within the range of the f_{ref} step for a low level RF input up to 120 dB μ V. This should be verified for every channel in the band.
- [5] $(N + 5) - 1$ MHz pulling is the input level of channel $N + 5$, at frequency 1 MHz lower, causing FM sidebands 30 dB below the wanted carrier.

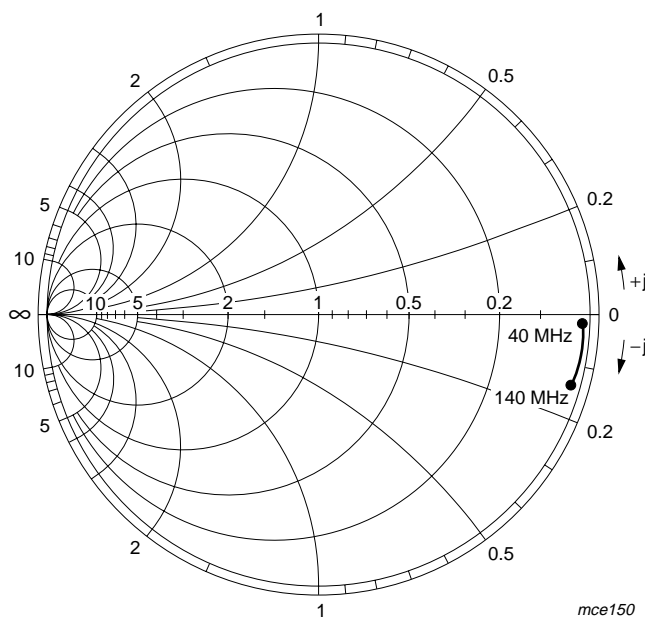


Fig 4. Input admittance (S_{11}) of the low band mixer (40 MHz to 140 MHz); $Y_o = 20 \text{ mS}$

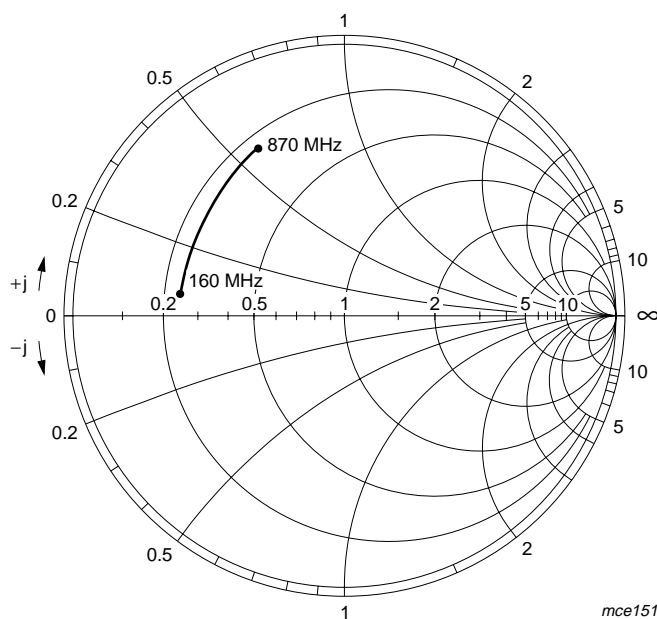


Fig 5. Input impedance (S_{11}) of the mid and high band mixer (160 MHz to 870 MHz); $Z_o = 100 \Omega$

Table 21: Oscillator

$V_{CC} = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; values are given for an IF amplifier with $500\text{ }\Omega$ load (measured as shown in [Figure 7](#) for the PAL standard); unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------------|--|--|------------|------|--------|--------|
| Low band oscillator | | | | | | |
| f_{osc} | oscillator frequency | | [1] 84.15 | - | 193.15 | MHz |
| $\Delta f_{osc(V)}$ | oscillator frequency shift with supply voltage | $\Delta V_{CC} = 5\text{ }\%$ | [2] - | 20 | 70 | kHz |
| | | $\Delta V_{CC} = 10\text{ }\%$ | [2] - | 110 | - | kHz |
| $\Delta f_{osc(T)}$ | oscillator frequency drift with temperature | $\Delta T = 25\text{ }^{\circ}\text{C}$; $V_{CC} = 5\text{ V}$ with compensation | [3] - | 800 | 1100 | kHz |
| $\Delta f_{osc(t)}$ | oscillator frequency switch-on drift | 5 s to 15 min after switching on $V_{CC} = 5\text{ V}$ | [4] - | 500 | 700 | kHz |
| Φ_{osc} | phase noise, carrier-to-noise sideband | $\pm 10\text{ kHz}$ frequency offset; worst case in the frequency range | 84 | 87 | - | dBc/Hz |
| | | $\pm 100\text{ kHz}$ frequency offset; worst case in the frequency range | 104 | 107 | - | dBc/Hz |
| RSC_{p-p} | ripple susceptibility of V_{CC} (peak-to-peak value) | $4.75\text{ V} < V_{CC} < 5.25\text{ V}$; worst case in the frequency range; ripple frequency 500 kHz | [5] 15 | 20 | - | mV |
| Mid band oscillator | | | | | | |
| f_{osc} | oscillator frequency | | [1] 200.15 | - | 478.15 | MHz |
| $\Delta f_{osc(V)}$ | oscillator frequency shift with supply voltage | $\Delta V_{CC} = 5\text{ }\%$ | [2] - | 20 | 70 | kHz |
| | | $\Delta V_{CC} = 10\text{ }\%$ | [2] - | 110 | - | kHz |
| $\Delta f_{osc(T)}$ | oscillator frequency drift with temperature | $\Delta T = 25\text{ }^{\circ}\text{C}$; $V_{CC} = 5\text{ V}$ with compensation | [3] - | 1000 | 1500 | kHz |
| $\Delta f_{osc(t)}$ | oscillator frequency drift after switch-on | 5 s to 15 min after switching on $V_{CC} = 5\text{ V}$ | [4] - | 500 | 700 | kHz |
| Φ_{osc} | phase noise, carrier-to-noise sideband | $\pm 10\text{ kHz}$ frequency offset; worst case in the frequency range | 84 | 87 | - | dBc/Hz |
| | | $\pm 100\text{ kHz}$ frequency offset; worst case in the frequency range | 104 | 107 | - | dBc/Hz |
| RSC_{p-p} | ripple susceptibility of V_{CC} (peak-to-peak value) | $4.75\text{ V} < V_{CC} < 5.25\text{ V}$; worst case in the frequency range; ripple frequency 500 kHz | [5] 15 | 20 | - | mV |
| High band oscillator | | | | | | |
| f_{osc} | oscillator frequency | | [1] 494.15 | - | 894.15 | MHz |
| $\Delta f_{osc(V)}$ | oscillator frequency shift with supply voltage | $\Delta V_{CC} = 5\text{ }\%$ | [2] - | 20 | 70 | kHz |
| | | $\Delta V_{CC} = 10\text{ }\%$ | [2] - | 300 | - | kHz |
| $\Delta f_{osc(T)}$ | oscillator frequency drift with temperature | $\Delta T = 25\text{ }^{\circ}\text{C}$; $V_{CC} = 5\text{ V}$ with compensation | [3] - | 1100 | 1500 | kHz |
| $\Delta f_{osc(t)}$ | oscillator frequency drift after switch-on | 5 s to 15 min after switching on $V_{CC} = 5\text{ V}$ | [4] - | 600 | 900 | kHz |

Table 21: Oscillator ...continued

$V_{CC} = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; values are given for an IF amplifier with $500\text{ }\Omega$ load (measured as shown in [Figure 7](#) for the PAL standard); unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------|--|---|--------|-----|-----|--------|
| Φ_{osc} | phase noise, carrier-to-noise sideband | $\pm 10\text{ kHz}$ frequency offset; worst case in the frequency range | 84 | 87 | - | dBc/Hz |
| | | $\pm 100\text{ kHz}$ frequency offset; worst case in the frequency range | 104 | 107 | - | dBc/Hz |
| RSC_{p-p} | ripple susceptibility of V_{CC} (peak-to-peak value) | $4.75\text{ V} < V_{CC} < 5.25\text{ V}$; worst case in the frequency range; ripple frequency 500 kHz | [5] 15 | 20 | - | mV |

- [1] Limits are related to the tank circuits used in [Figure 7](#) for a PAL application. The choice of different external components adapts the measurement circuit to other frequency bands or NTSC applications.
- [2] The frequency shift is defined as a change in oscillator frequency when the supply voltage varies from $V_{CC} = 5\text{ V}$ to 4.75 V (4.5 V) or from $V_{CC} = 5\text{ V}$ to 5.25 V (5.5 V). The oscillator is free running during this measurement.
- [3] The frequency drift is defined as a change in oscillator frequency when the ambient temperature varies from $T_{amb} = 25\text{ }^{\circ}\text{C}$ to $50\text{ }^{\circ}\text{C}$ or from $T_{amb} = 25\text{ }^{\circ}\text{C}$ to $0\text{ }^{\circ}\text{C}$. The oscillator is free running during this measurement.
- [4] Switch-on drift is defined as the change in oscillator frequency between 5 s and 15 min after switch on. The oscillator is free running during this measurement.
- [5] The supply ripple susceptibility is measured in the circuit according to [Figure 7](#) using a spectrum analyzer connected to the IF output. An unmodulated RF signal is applied to the test board RF input. A sinewave signal with a frequency of 500 kHz is superimposed onto the supply voltage. The amplitude of this ripple signal is adjusted to bring the 500 kHz sidebands around the IF carrier to a level of -53.5 dB with respect to the carrier.

Table 22: IF amplifier

$V_{CC} = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; values are given for an IF amplifier with $500\text{ }\Omega$ load (measured as shown in [Figure 7](#) for the PAL standard); unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|---|---|-----|------|-----|----------|
| IF amplifier | | | | | | |
| S_{22} | output reflection coefficient | magnitude; see Figure 6 | - | 38 | - | dB |
| | | phase; see Figure 6 | - | 0.36 | - | deg |
| Z_o | output impedance ($R_S + jL_S\omega$) | R_S at 36.15 MHz | - | 79 | - | Ω |
| | | C_S at 36.15 MHz | - | 9 | - | nF |
| | | R_S at 43.5 MHz | - | 80 | - | Ω |
| | | C_S at 43.5 MHz | - | 3 | - | nF |

Rejection at the IF output

| | | | | | | |
|-----------------|---|---|--------|----|----|------------|
| INT_{div} | level of divider interferences in the IF signal | worst case | [1] - | - | 23 | dB μ V |
| INT_{XTAL} | crystal oscillator interferences rejection | $V_{IF} = 100\text{ dB}\mu\text{V}$; worst case in the frequency range | [2] 60 | 66 | - | dBc |
| $INT_{f_{ref}}$ | reference frequency rejection | $V_{IF} = 100\text{ dB}\mu\text{V}$; worst case in the frequency range | [3] 60 | 66 | - | dBc |

- [1] This is the level of divider interferences close to the IF. For example channel S3: $f_{osc} = 158.15\text{ MHz}$, $\frac{1}{4}f_{osc} = 39.5375\text{ MHz}$. The LOSCIN input must be left open (i.e. not connected to any load or cable); the HOSCIN1 and HOSCIN2 inputs are connected to a hybrid.
- [2] Crystal oscillator interference means the 4 MHz sidebands caused by the crystal oscillator. The rejection has to be greater than 60 dB for an IF output signal of $100\text{ dB}\mu\text{V}$.
- [3] The reference frequency rejection is the level of reference frequency sidebands (e.g. 62.5 kHz) related to the carrier. The rejection has to be greater than 60 dB for an IF output signal of $100\text{ dB}\mu\text{V}$.

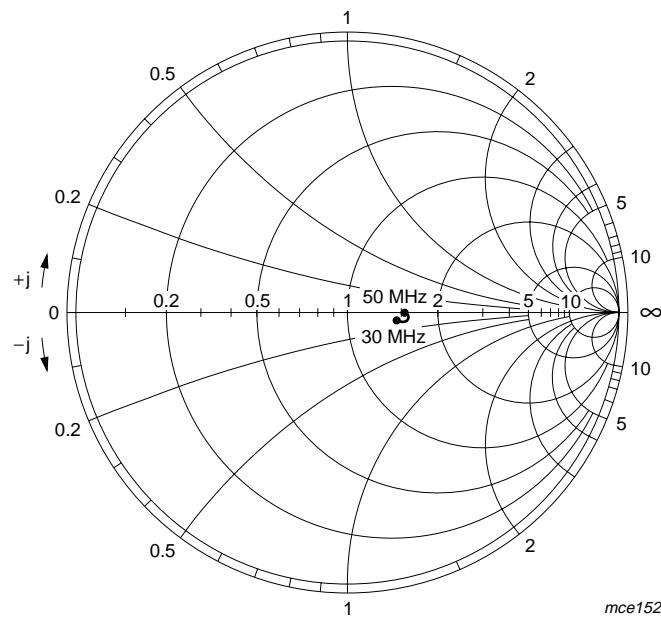


Fig 6. Output impedance (S_{22}) of the IF amplifier (30 MHz to 50 MHz); $Z_o = 50 \Omega$

Table 23: AGC output

$V_{CC} = 5 \text{ V}$; $T_{amb} = 25^\circ \text{C}$; values are given for an IF amplifier with 500Ω load (measured as shown in Figure 7 for the PAL standard); unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------|---|---|-------|-------|-------|------------------------|
| AGC_{TOP} | AGC take-over point | $AL2 = 0$; $AL1 = 1$; $AL0 = 0$ | 110.5 | 112 | 113.5 | $\text{dB}\mu\text{V}$ |
| $I_{source(fast)}$ | source current 1 | | 8.0 | 9.5 | 11.0 | μA |
| $I_{source(slow)}$ | source current 2 | | 210.0 | 245.0 | 280.0 | nA |
| $I_{sink(peak)}$ | peak sink current to ground | | 80 | 100 | 120 | μA |
| V_{max} | AGC maximum output voltage | | 3.45 | 3.5 | 4.0 | V |
| V_{min} | AGC minimum output voltage | | 0 | - | 0.1 | V |
| $V_{RF(slip)}$ | RF voltage range to switch the AGC from active to not active mode | | - | - | 0.5 | dB |
| $V_{RM(L)}$ | AGC output voltage | AGC bit = 1 or AGC active | 0 | - | 2.9 | V |
| $V_{RM(H)}$ | AGC output voltage | AGC bit = 0 or AGC not active | 3 | 3.5 | 4.0 | V |
| I_{LO} | AGC leakage current | $AL2 = 1$; $AL1 = 1$; $AL0 = 0$; $0 \text{ V} < V_{AGC} < V_{CC}$ | -50 | - | +50 | nA |
| $V_{O(off)}$ | AGC output voltage with AGC disabled | $AL2 = 1$; $AL1 = 1$; $AL0 = 1$ | 3.45 | 3.5 | 4.0 | V |

12. Application information

12.1 Tuning amplifier

The tuning amplifier is capable of driving the varicap voltage without an external transistor. The tuning voltage output must be connected to an external load of 27 k Ω which is connected to the tuning voltage supply rail. The loop filter design depends on the oscillator characteristics and the selected reference frequency.

12.2 Crystal oscillator

The crystal oscillator uses a 4 MHz crystal connected in series with an 18 pF capacitor thereby operating in the series resonance mode. Connecting the crystal to the ground is preferred, but it can also be connected to the supply voltage.

12.3 Examples of I²C-bus control

Conditions:

$$f_{\text{osc}} = 100 \text{ MHz}$$

P0 = on (to switch on low band)

P3 = on

$$I_{\text{CP}} = 280 \text{ } \mu\text{A}$$

$$f_{\text{step}} = 62.5 \text{ kHz}$$

$$N = 1600$$

$$f_{\text{XTAL}} = 4 \text{ MHz}$$

$$I_{\text{AGC}} = 245 \text{ nA}$$

AGC take-over point = set to 112 dB μ V asymmetrical

12.3.1 Write sequence

[Table 24](#) to [29](#) show various write sequences where:

S = START

A = acknowledge

P = STOP

For the complete sequence see [Table 24](#) (sequence 1) or [Table 25](#) (sequence 2).

Other I²C-bus addresses may be selected by applying an appropriate voltage to pin AS.

Table 24: Complete sequence 1

| Start | Address byte | Divider byte 1 | Divider byte 2 | Control byte | Band switch byte | Control byte | Auxiliary byte | Stop |
|-------|--------------|----------------|----------------|--------------|------------------|--------------|----------------|------|
| S | C2 A | 06 A | 40 A | CE A | 09 A | DE A | 20 A | P |

Table 25: Complete sequence 2

| Start | Address byte | Control byte | Auxiliary byte | Control byte | Band switch byte | Divider byte 1 | Divider byte 2 | Stop |
|-------|--------------|--------------|----------------|--------------|------------------|----------------|----------------|------|
| S | C2 A | DE A | 20 A | CE A | 09 A | 06 A | 40 A | P |

Table 26: Divider bytes only sequence

| Start | Address byte | | Divider byte 1 | | Divider byte 2 | | Stop |
|-------|--------------|---|----------------|---|----------------|---|------|
| S | C2 | A | 06 | A | 40 | A | P |

Table 27: Control and band switch bytes only sequence

| Start | Address byte | | Control byte | | Band switch byte | | Stop |
|-------|--------------|---|--------------|---|------------------|---|------|
| S | C2 | A | CE | A | 09 | A | P |

Table 28: Control and auxiliary bytes only sequence

| Start | Address byte | | Control byte | | Auxiliary byte | | Stop |
|-------|--------------|---|--------------|---|----------------|---|------|
| S | C2 | A | DE | A | 20 | A | P |

Table 29: Control byte only sequence

| Start | Address byte | | Control byte | | | | Stop |
|-------|--------------|---|--------------|---|--|--|------|
| S | C2 | A | DE | A | | | P |

12.3.2 Read sequence

[Table 30](#) and [31](#) show read sequences where:

S = START

A = acknowledge

XX = read status byte

X = no acknowledge from the master means end of sequence

P = STOP

Table 30: Status byte acquisition

| Start | Address byte | | Status byte | | Stop |
|-------|--------------|---|-------------|---|------|
| S | C3 | A | XX | X | P |

Table 31: Two status bytes acquisition

| Start | Address byte | | Status byte 1 | | Status byte 2 | | Stop |
|-------|--------------|---|---------------|---|---------------|---|------|
| S | C3 | A | XX | A | XX | X | P |

13. Test information

13.1 Measurement circuit

The measurement circuit for PAL on a test jig is given in [Figure 7](#) and the components are given in [Table 32](#).



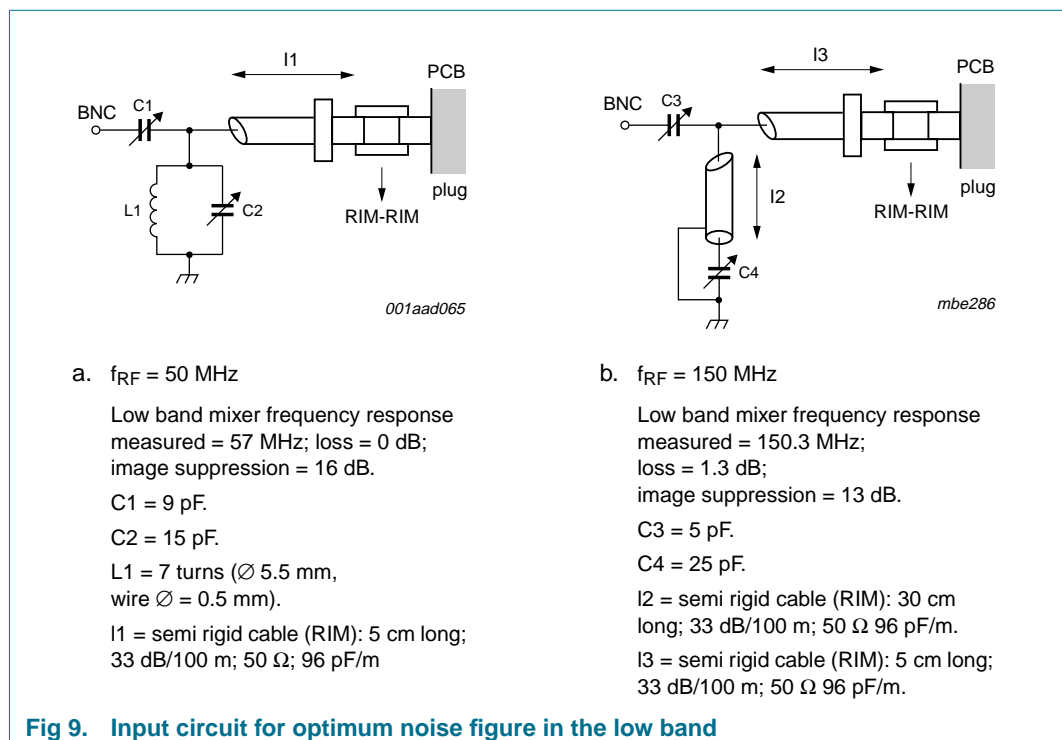
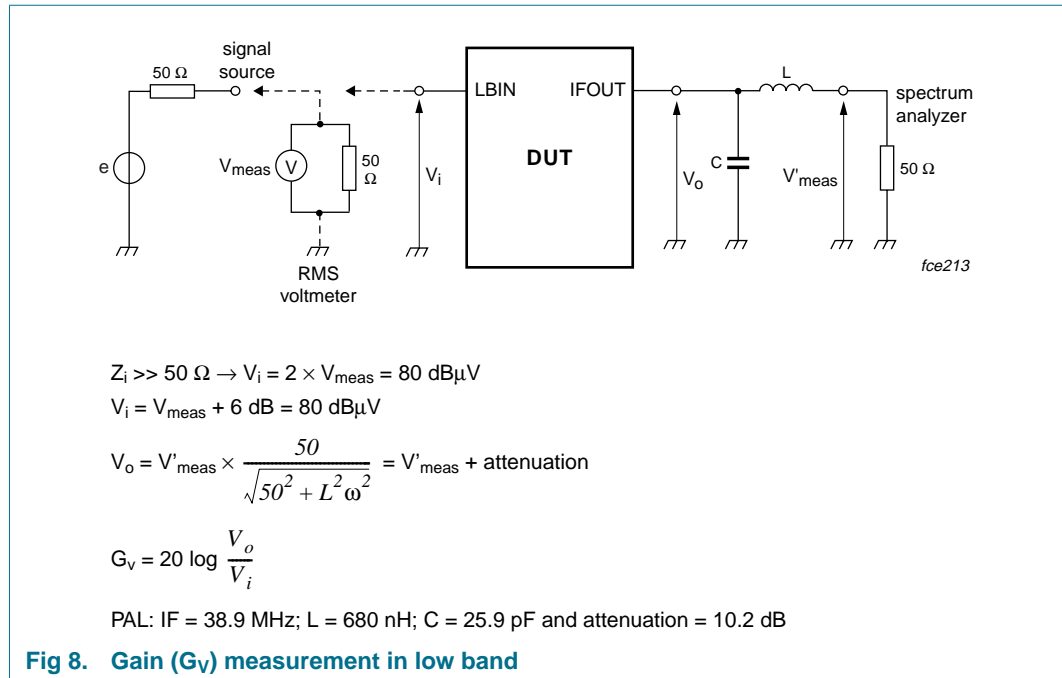
The pin numbers in parenthesis represent the TDA6501TT.

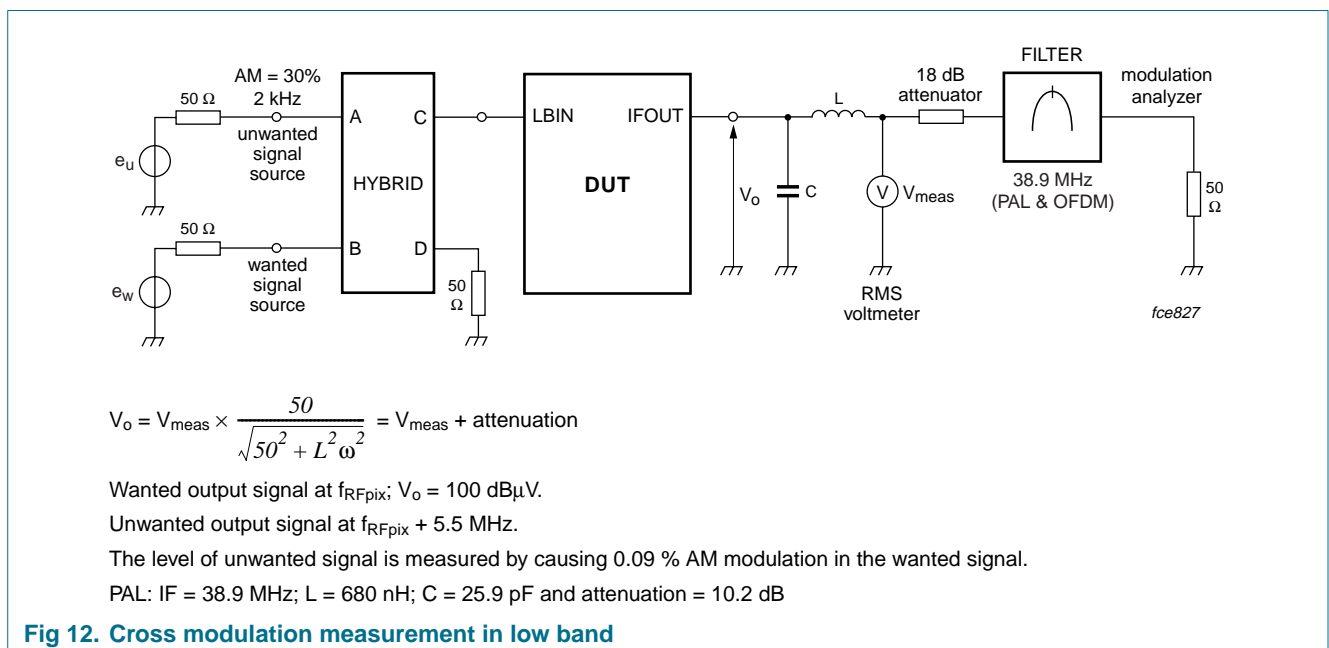
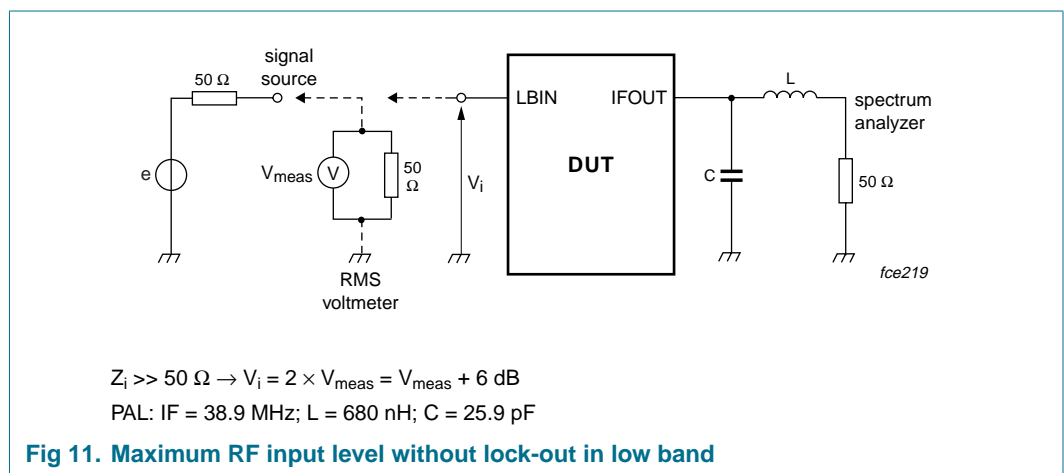
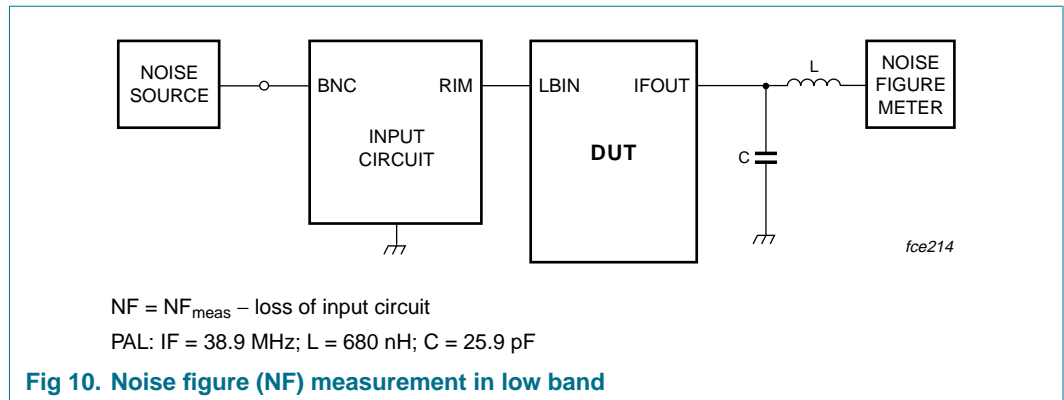
Fig 7. Measurement circuit for PAL on test jig

Table 32: Components for measurement circuit

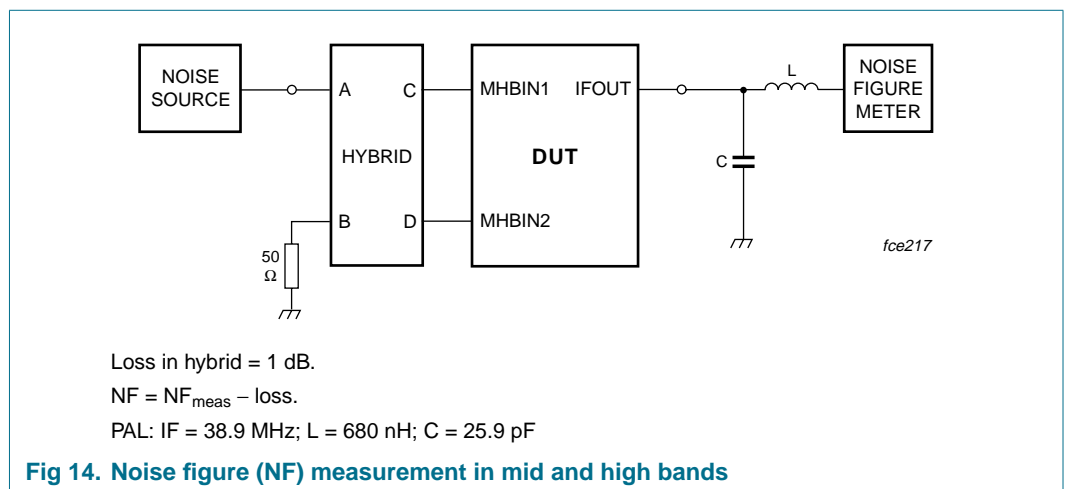
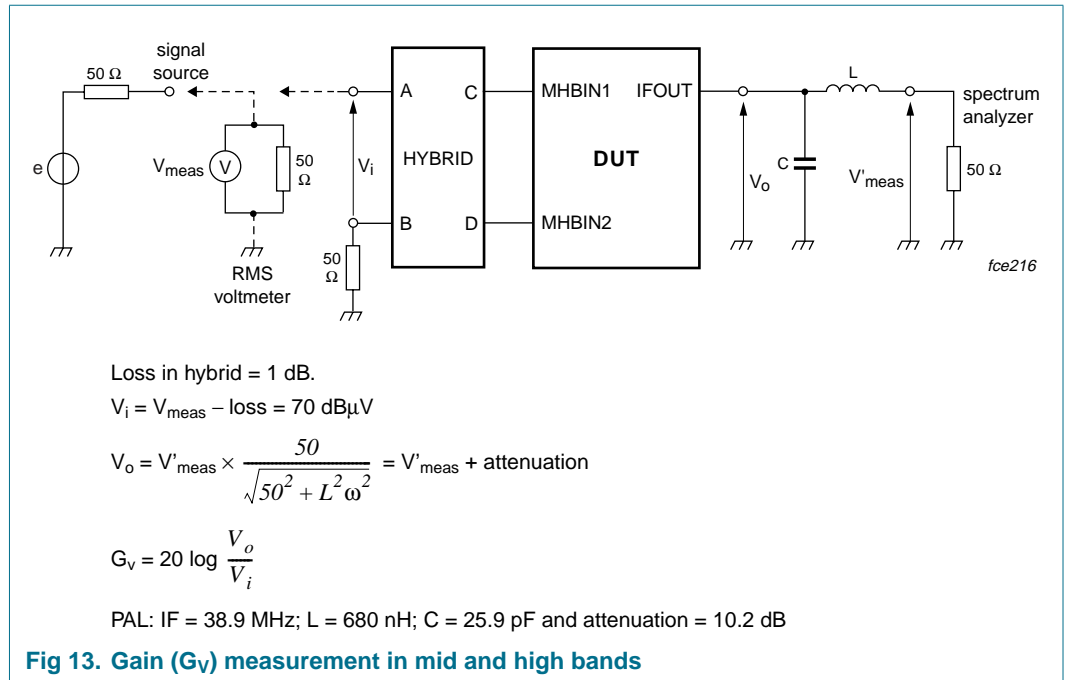
| Component | Value | Component | Value |
|--|----------------------|-----------|--|
| Capacitors; all SMD and NP0, unless otherwise stated | | | |
| C1 | 1.8 pF (N750) | C15 | 100 nF |
| C2 | 1.5 pF (N750) | C16 | 820 pF |
| C3 | 82 pF (N750) | C17 | 4.7 nF |
| C4 | 1 pF (N750) | C18 | 4.7 nF |
| C5 | 1.5 pF (N750) | C19 | 4.7 nF |
| C6 | 100 pF (N750) | C20 | 12 pF |
| C7 | 1.2 pF (N750) | C21 | 12 pF |
| C8 | 1.2 pF (N750) | C22 | 160 nF |
| C9 | 1.2 pF (N750) | C23 | 10 nF |
| C10 | 1.2 pF (N750) | C25 | 10 μF (16 V; electrolytic) |
| C11 | 27 pF (N750) | C26 | 10 μF (16 V; electrolytic) |
| C12 | 4.7 nF | C27 | 22 pF |
| C13 | 4.7 nF | C28 | 3.9 pF |
| C14 | 18 pF | | |
| Resistors; all SMD | | | |
| R1 | 12 Ω | R12 | 220 Ω |
| R2 | 5.6 Ω | R13 | 470 Ω |
| R3 | 27 Ω | R14 | 1 kΩ |
| R4 | 5.6 kΩ | R15 | 2.2 kΩ |
| R5 | 22 kΩ | R16 | 0 Ω |
| R6 | 22 kΩ | R17 | 330 Ω |
| R7 | 5.6 kΩ | R18 | 330 Ω |
| R10 | 27 kΩ | R19 | 18 kΩ |
| R11 | 1 kΩ | R20 | 4.7 kΩ |
| Diodes and LEDs | | | |
| D1 | BB182 | D4 | 3 mm |
| D2 | BB178 | D5 | 3 mm |
| D3 | BB179 | D6 | 3 mm |
| | | D7 | 3 mm |
| Coils; including IF coil; wire size 0.4 mm | | | |
| L1 | 6 t; Ø 4 mm | L4 | 2 x 6 t; coil type: TOKO 7kN; material: 113 kN; screw core: 03-0093; pot core: 04-0026 |
| L2 | 3 t; Ø 2 mm | | |
| L3 | 3 t; Ø 2 mm | | |
| L5 | 680 nH | | |
| IC, transistor and crystal | | | |
| IC | TDA6500TT; TDA6501TT | X1 | 4 MHz |
| Q1 | BC847 | | |

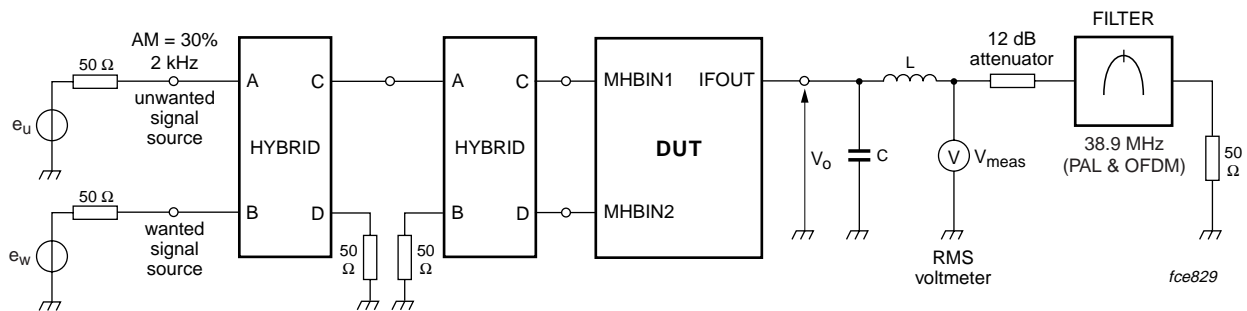
13.2 Test circuit for low band measurements





13.3 Test circuit for mid and high band measurements





$$V_o = V_{\text{meas}} \times \frac{50}{\sqrt{50^2 + L^2 \omega^2}} = V_{\text{meas}} + \text{attenuation}$$

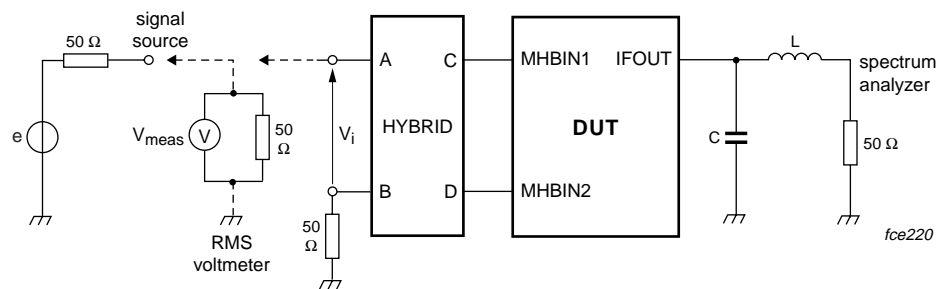
Wanted output signal at f_{RFpix} ; $V_o = 100 \text{ dB}\mu\text{V}$.

Unwanted output signal at $f_{\text{RFpix}} + 5.5 \text{ MHz}$.

The level of unwanted signal is measured by causing 0.09 % AM modulation in the wanted signal.

PAL: IF = 38.9 MHz; L = 680 nH; C = 25.9 pF and attenuation = 10.2 dB

Fig 15. Cross modulation measurement in mid and high bands



Loss in hybrid = 1 dB.

$V_i = V_{\text{meas}} - \text{loss}$.

PAL: IF = 38.9 MHz; L = 680 nH; C = 25.9 pF

Fig 16. Maximum RF input level without lock-out in mid and high bands

14. Package outline

TSSOP32: plastic thin shrink small outline package; 32 leads; body width 6.1 mm; lead pitch 0.65 mm

SOT487-1

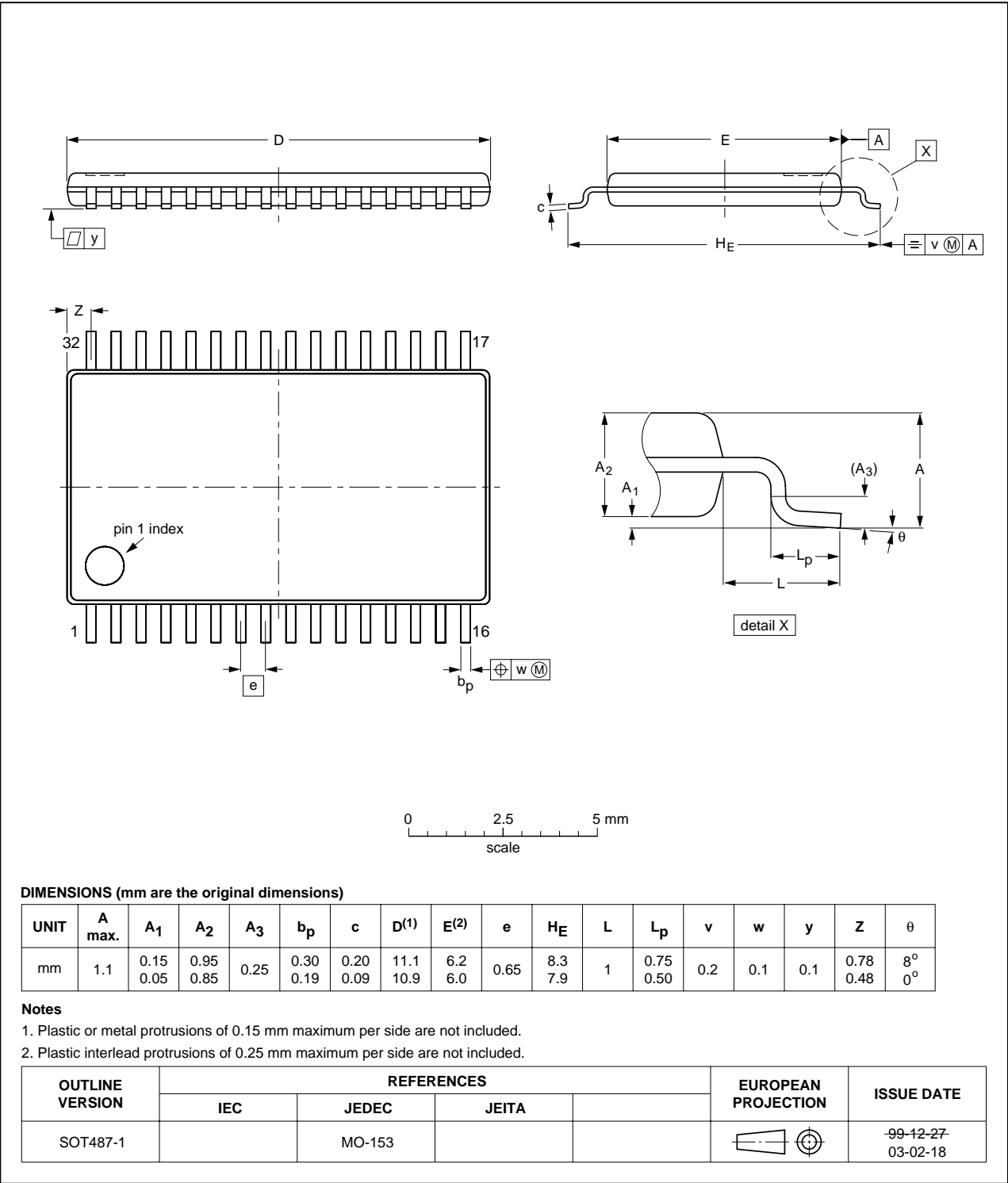


Fig 17. Package outline SOT487-1 (TSSOP32)

15. Soldering

15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
 - for all BGA, HTSSON..T and SSOP..T packages
 - for packages with a thickness ≥ 2.5 mm
 - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm³ so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm³ so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

- smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

15.5 Package related soldering information

Table 33: Suitability of surface mount IC packages for wave and reflow soldering methods

| Package ^[1] | Soldering method | |
|--|---|-----------------------|
| | Wave | Reflow ^[2] |
| BGA, HTSSON..T ^[3] , LBGA, LFBGA, SQFP, SSOP..T ^[3] , TFBGA, VFBGA, XSON | not suitable | suitable |
| DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS | not suitable ^[4] | suitable |
| PLCC ^[5] , SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended ^[5] ^[6] | suitable |
| SSOP, TSSOP, VSO, VSSOP | not recommended ^[7] | suitable |
| CWQCCN..L ^[8] , PMFP ^[9] , WQCCN..L ^[8] | not suitable | not suitable |

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

- [4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- [5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- [6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- [7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
- [8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
- [9] Hot bar soldering or manual soldering is suitable for PMFP packages.

16. Revision history

Table 34: Revision history

| Document ID | Release date | Data sheet status | Change notice | Doc. number | Supersedes |
|--|--------------|-----------------------|---------------|----------------|-------------------|
| TDA6500_TDA6501_2 | 20050614 | Product data sheet | - | 9397 750 15057 | TDA6500_TDA6501_1 |
| Modifications: | | | | | |
| <ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors.Table 23 "AGC output": maximum values of V_{max}, $V_{RM(H)}$ and $V_{O(off)}$ changed from 3.6 V to 4.0 V. | | | | | |
| TDA6500_TDA6501_1 | 20030605 | Product specification | - | 9397 750 10109 | - |

17. Data sheet status

| Level | Data sheet status ^[1] | Product status ^{[2] [3]} | Definition |
|-------|----------------------------------|-----------------------------------|--|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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