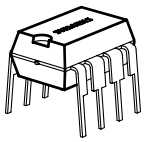
Power Factor Controller IC for High Power Factor and low THD

Boost Controller



P-DIP-8-4

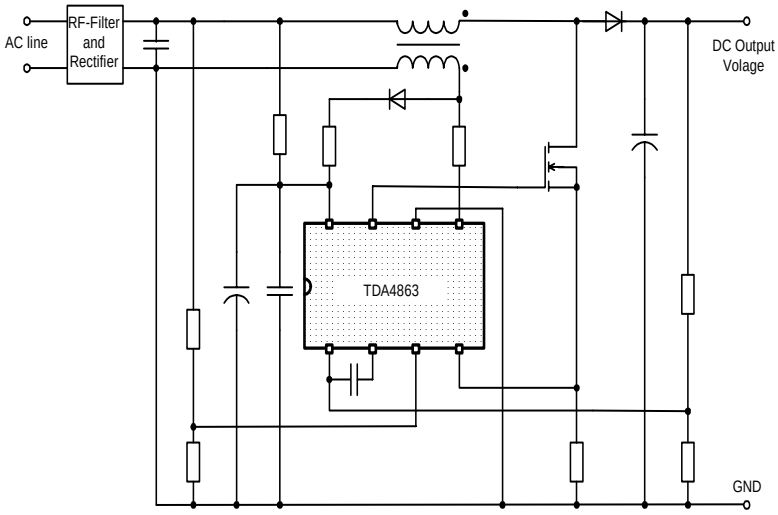
P-DSO-8-3

- IC for sinusoidal line-current consumption
- Power factor achieves nearly 1
- Controls boost converter as active harmonic filter for low THD
- Start up with low current consumption
- Zero current detector for discontinuous operation mode
- Output overvoltage protection
- Output undervoltage lockout
- Internal start up timer
- Totem pole output with active shut down
- Internal leading edge blanking LEB

Improvements referred to TDA 4862

- Suitable for universal input applications with low THD at low load conditions
- Very low start up current
- Accurate OVR and $V_{ISENSEmax}$ threshold
- Competiton compatibel VCC thresholds
- Enable threshold referred to V_{VSENSE}

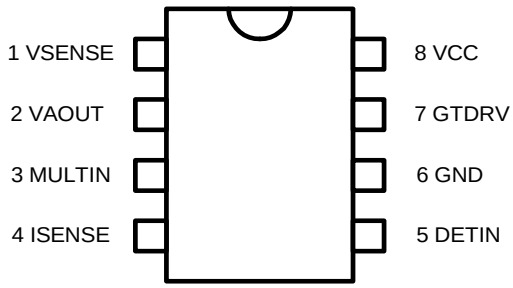
The TDA4863 IC controls a boost converter in a way that sinusoidal current is taken from the single phase line supply and stabilized DC voltage is available at the output. This active harmonic filter limits the harmonic currents resulting from the capacitor pulsed charge currents during rectification. The power factor which descibes the ratio between active and apparent power is almost one. Line voltage fluctuations can be compensated very efficiently



Type	Ordering Code	Package
TDA 4863	Q67040-S4452	P-DIP-8-4
TDA 4863G	Q67040-S4451	P-DSO-8-3

Pin Connections

Pin	Symbol	Function
1	VSENSE	Voltage amplifier inverting input
2	VAOUT	Voltage amplifier output
3	MULTIN	Multiplier input
4	ISENSE	Current sense input
5	DETIN	Zero current detector input
6	GND	Ground
7	GTDRV	Gate driver output
8	VCC	Positive voltage supply



Pin Description

Pin1 VSENSE (voltage amplifier inverting input)
VSENSE is connected via a resistive divider to the boost converter output. With a capacitor connected to VAOUT the internal error amplifier acts as an integrator.

Pin2 VAOUT (voltage amplifier output)
VAOUT is connected internally to the first multiplier input. To prevent overshoot the input voltage will be clamped internally at 5V. Input voltage less then 2.2V inhibits the gate driver.If the current flowing into this pin is exceeding an internal threshold the multiplier output voltage is rdeuced to prevent the MOSFET from overvoltage damage.

Pin 3 MULTIN (multipier input)
MULTIN is the second multiplier input and is connected via a resistive divider to the rectifier output voltage.

Pin 4 ISENSE (current sense input)
ISENSE is connected to a sense resistor controlling the MOSFET source current. The input is internally clamped at -0.3V to prevent negative input voltage interaction. A leading edge blanking circuitry suppresses voltage spiks when turning the MOSFET on.

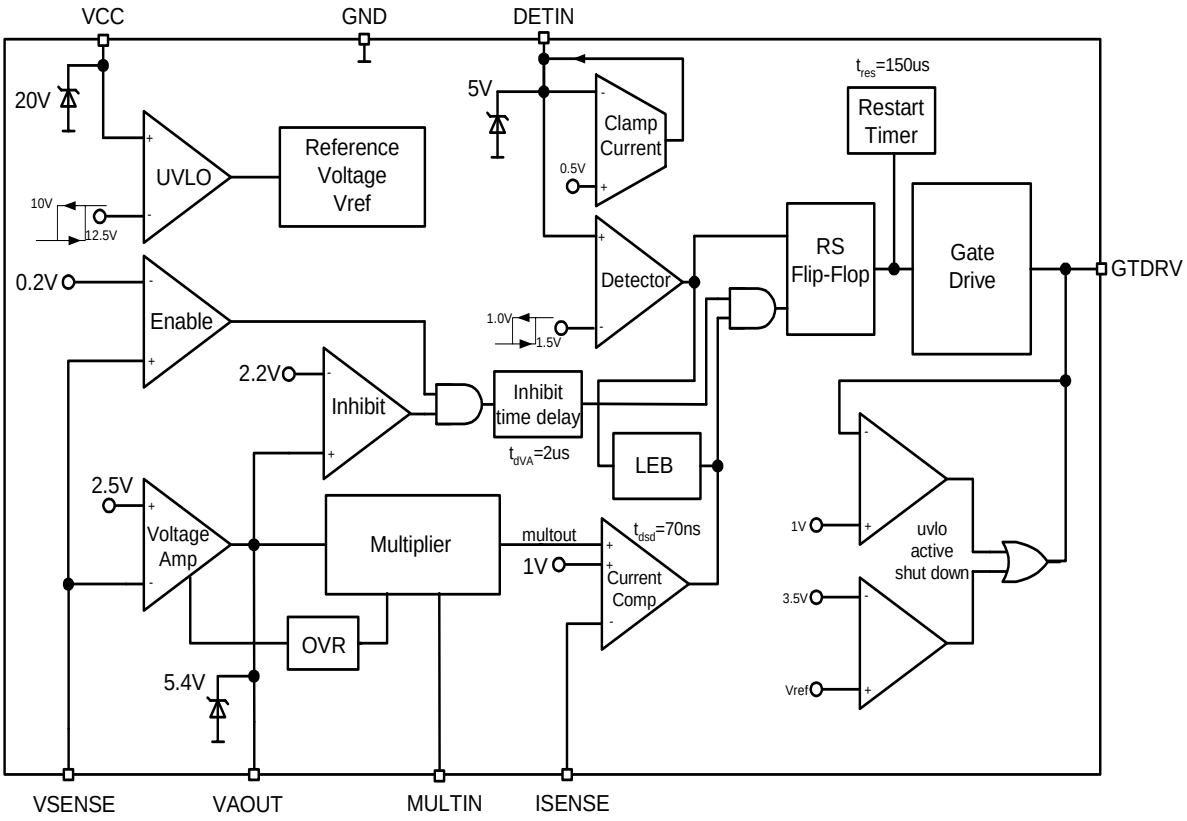
Pin 5 DETIN (Zero current detector input)
DETIN is connected to an auxiliary winding monitoring the zero crossing of the inductor current.

Pin 6 GND (Ground)

Pin 7 GTDRV (Gate driver output)
GTDRV is the output of a totem-pole circuitry for direct driving a MOSFET. An active shutdown circuitry ensures that GTDRV is low if the IC is switched off.

Pin 8 Vcc (Positive voltage supply)
If Vcc exceeds the turn-on threshold the IC is switched on. When Vcc falls below the turn-off threshold it is switched off and power consumption is very low. An auxilliary winding is charging a capacitor which provides the supply current. A second 100nF ceramic capacitor should be added to Vcc to absorbe supply current spikes required to charge the MOSFET gate capacitance.

Block Diagram



Functional Description

Introduction

Conventional electronic ballasts and switching power supplies are designed with a bridge rectifier and a bulk capacitor. Their disadvantage is that the circuit draws power from the line when the instantaneous AC voltage exceeds the capacitors voltage. This occurs near the line voltage peak and causes a high charge current spike with following characteristics: The apparent power is higher than the real power that means low power factor condition, the current spikes are non sinusoidal with a high content of harmonics causing line noise, the rectified voltage depends on load condition and requires a large bulk capacitor, special efforts in noise suppression are necessary.

With the TDA4863 preconverter a sinusoidal current is achieved which varies in direct instantaneous proportional to the input voltage half sine wave and so provides a power factor near 1. This is due to the appearence of almost any complex load like a resistive one at the AC line. The harmonic distortions are reduced and comply with the IEC555 standard requirements.

IC Description

The TDA4863 contains a wide bandwidth voltage amplifier used in a feedback loop, an overvoltage regulator, an one quadrant multiplier with a wide linear operating range, a current sense comparator, a zero current detector, a PWM and logic circuitry, a totem-pole MOSFET driver, an internal trimmed voltage reference, a restart timer and an undervoltage lockout circuitry.

Voltage Amplifier

With an external capacitor between VSENSE and VAOUT the voltage amplifier forms an integrator. The integrator monitors the average output voltage over several line cycles. Typically the integrators bandwidth is set below 20 Hz in order to suppress the 100 Hz ripple of the rectified line voltage. The voltage amplifier is internally compensated and has a gain bandwidth of 3 MHz and a phase margin of 80 degrees. The non-inverting input is biased internally at 2.5V. The output is directly connected to the multiplier input.

The gate drive is disabled when VSENSE voltage is less than 0.2 V or VVAOUT voltage is less than 2.2 V.

If the MOSFET is placed nearby the controller switching inteferences have to be taken into account. The output of the voltage amplifier is designed in a way to minimize these inteferences.

Overvoltage Regulator

Because of the integrators low bandwidth fast changes of the output voltage can’t be regulated whithin an adequate time. Fast output changes occure during initial start-up, sudden load removal, or output arcing. While the integrators differential input voltage remains zero during this fast changes a peak current is flowing through the external capacitor into pin VAOUT. If this current exceeds an internal defined margin the overvoltage regulator circuitry reduces the multiplier output voltage. As a result the on time of the MOSFET is reduced.

Multiplier

The one quadrant multiplier regulates the gate driver with respect of the DC output voltage and the AC half wave rectified input voltage. Both inputs are designed to achieve good linearity over a wide dynamic range to represent an AC line free from distortion. Special efforts are made to assure universal line applications with respect to a 90 to 270 V AC range.

The multiplier output is internally clamped at 1.3V. So the MOSFET is protected against critical operating during start up.

Current sense comparator, LEB and RS Flip-Flop

An external sense resistor transferes the source current of the MOSFET into a sense voltage.The multiplier output voltage is compared with this sense voltage.

To protect the current comparator input from negative pulses a current source is inserted which sends current out of the ISENSE pin every time when ISENSE is falling below ground potential.. The switch-on current peak of the MOSFET is blanked out via an leading edge blanking circuit with a blanking time of tyically 200ns.

The RS Flip-Flop ensures that only one single switch-on and switch-off pulse appears at the gate drive output during a given cycle (double pulse suppression).

Zero Current Detector

The zero current detector senses the inductor current via an auxiliary winding and ensures that the next on-time of the MOSFET is initiated immediately when the inductor current has reached zero. This diminishes the revers recovery losses of the boost converter diode. The MOSFET is switched off when the voltage drop of the shunt resistor reaches the voltage level of the multipler output. So the boost current waveform has a triangular shape and there are no deadtime gaps between the cycles. This leads to a continuous AC line current limiting the peak current to twice of the average current.

To prevent false tripping the zero current detector is designed as a Schmitt-Trigger with a hysteresis of 0.5V. An internal 5V clamp protects the input from overvoltage breadkdown, a 0.6V clamp prevents substrate injection. An external resistor has to be used in series with the auxiliary winding to limit the current through the clamps.

Restart Timer

The restart timer function eliminates the need of an oscillator when. The timer starts or restarts the TDA4863 when the driver output has been off for more than 150us after the inductor current reaches zero.

Undervoltage Lockout

An undervoltage lockout circuitry switches the IC on when Vcc reaches the upper threshold V_{CCH} and switches the IC off when Vcc is falling below the lower threshold V_{CCL}. During start up the supply current is less then 100uA.

An internal voltage clamp has been added to protect the IC from Vcc overvoltage condition. When using this clamp special care must be taken on power dissipation.

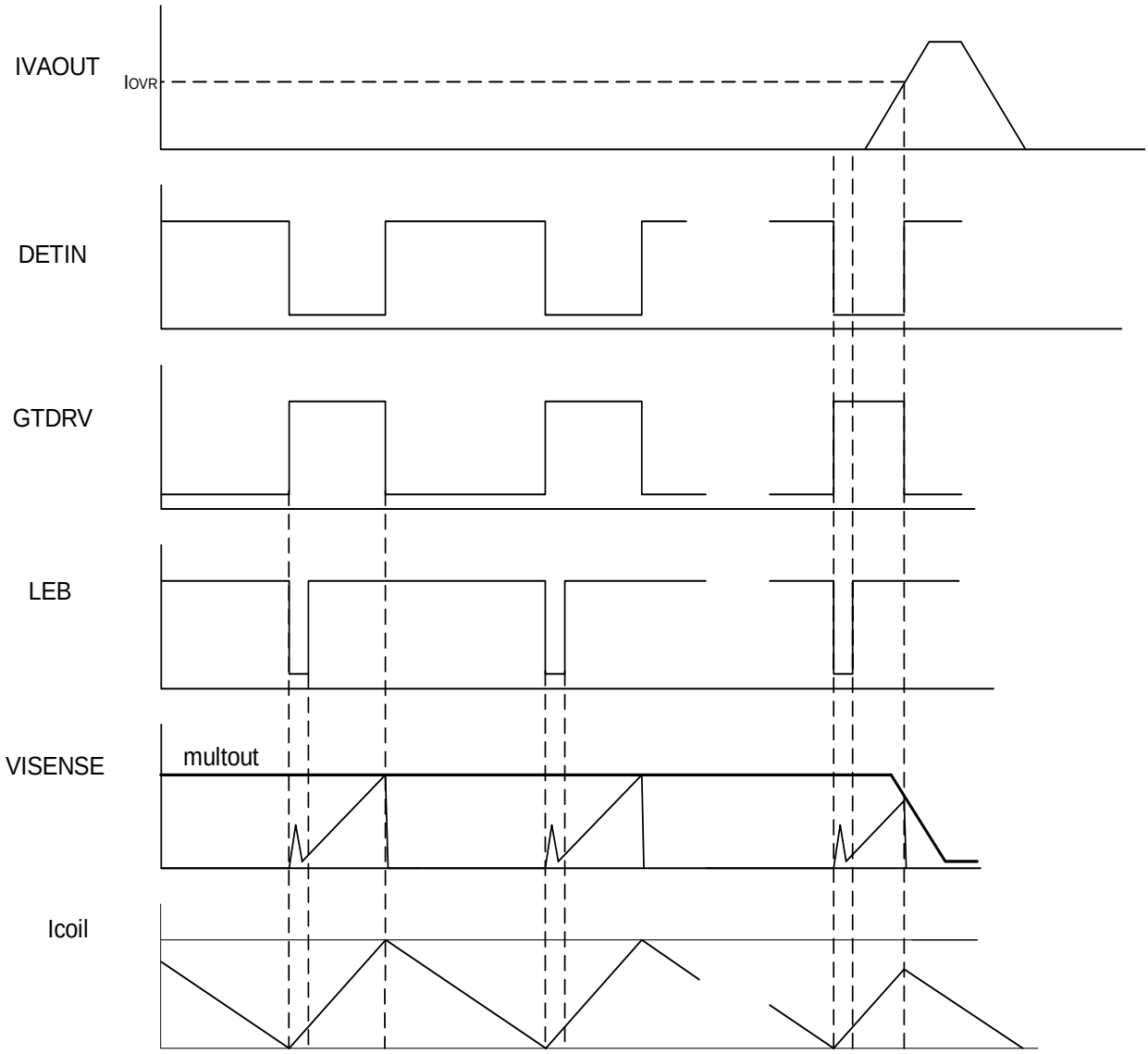
Start up current is provided by an external start up resistor which is connected from the AC line to the input supply voltage Vcc and a storage capacitor which is connected from Vcc to ground. Be aware that this capacitor is discharged befor the IC is plugged into the application board. Otherwise the IC can be destroyed due to the high capacitor voltage.

Bootstrap power supply is created with the previous mentioned auxiliary winding and a diode (see application circuit).

Gate Drive

The TDA4863 totem pole output stage is MOSFET compatible. An internal protection ciruitry is activated when Vcc is within the start up phase and ensures that the MOSFET is turned off. The totem pole output has been optimized to minimize cross conduction current during high speed operation.

Signal Diagrams



Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit	Remark
Supply + Zener Current	I_{CCH}+Iz	-	20	mA	
Supply Voltage	V_{CC}	-0.3	Vz	V	Vz=Zener Voltage Icc+Iz=20mA
Voltage at Pin 1,3,4		-0.3	6.5	V	
Current into Pin 2	IVAOUT	 -10	30	mA mA	VAOUT=4V,VSENSE=2.8V VAOUT=0V,VSENSE=2.3V t<1ms
Current into Pin 5	IDETIN	 -10	10	mA mA	DETIN > 6V DETIN< 0.4V t<1ms
Current into Pin 7	IGTDRV	-500	500	mA	t<1ms
ESD Protection			2000	V	MIL STD 883C method 3015.6, 100pF,1500Ω
Storage Temperature	T_{stg}	-50	150	°C	
Operating Junction Temperature	T_J	-40	150	°C	
Thermal Resistance Junction-Ambient	R_{thJA}		100 180	K/W K/W	P-DIP-8 P-DSO-8

Characteristics

Unless otherwise stated, -40°C<T_j <150 °C, V_{CC} = 14.5V

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
Start-Up circuit						
Zener Voltage	Vz	18	20	22	V	Icc+Iz=20mA
Start-up supply current	I_{CCL}		20	100	uA	Vcc=V_{CCON} - 0.5V
Operating supply current	I_{CCH}		4	6	mA	Output low
Vcc Turn-ON threshold	V_{CCON}	12	12.5	13	V	
Vcc Turn-OFF threshold	V_{CCOFF}	9.5	10	10. 5	V	
Vcc Hysteresis	V_{CCHY}		2.5			
Voltage Amplifier						
Voltage feedback Input Threshold	V_{FB}	2.45	2.5	2.55	V	
Line regulation	V_{FBLR}			5	mV	V_{CC}=12V to 16V
Open Loop Voltage Gain[1])	G_V		100		dB	
Unity Gain Bandwidth[1])	B_W		5		MHz	
Phase Margin[1)]	M		80		Degr	
Bias current VSENSE	$I_{BVSENSE}$	-1.0	-0.3		uA	
Enable Threshold	V_{VSENSE}		0.2		V	
Inhibit Threshold Voltage	V_{VAOUTI}		2.2		V	V_{ISENSE}= -0.1V
Inhibit Time Delay	t_{dVA}		3		us	V_{ISENSE}= -0.1V
Output Current Source	I_{VAOUTH}		-6		mA	VAOUT=0V VSENSE=2.3V, t<1ms
Output Current Sink	I_{VAOUTL}		30		mA	VAOUT=4V VSENSE=2.8V,t<1ms
Upper Clamp Voltage	V_{VAOUTH}		5.4		V	VSENSE=2.3V, I= -0.2mA
Lower Clamp Voltage	V_{VAOUTL}		1.1		V	VSENSE=2.8V, I=0.5mA
Overvoltage Regulator						
Threshold Current	I_{OVR}	35	40	45	uA	Tj=25°C
1) guaranteed by design, not tested						

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
Current Comparator						
Input Bias Current	$I_{BISENSE}$	-1	-0.2	1	uA	V_{ISENSE}=0V
Input Offset Voltage	$V_{ISENSEO}$		25		mV	V_{AOUT}=2.7V
Max Threshold Voltage	$V_{ISENSEM}$	0.95	1.0	1.05	V	
Threshold at OVR	$V_{ISENOVR}$		0.05		V	I_{OVR}=50uA
Leading Edge Blanking	t_{LEB}		200		ns	
Shut Down Delay	t_{dISG}		80		ns	
Detector						
Upper threshold voltage	V_{DETINU}		1.5		V	
Lower threshold voltage	V_{DETINL}		1		V	
Hysteresis	$V_{DETINHY}$		0.5		V	
Input current	I_{BDETIN}	-1	-0.2	1	uA	V_{DETIN}=2V
Input clamp voltage High state Low state	 $V_{DETINHC}$ $V_{DETINLC}$		 5 0.5			 I_{DETIN}=5mA I_{DETIN}=-5mA
Multiplier						
Input bias current	$I_{BMULTIN}$	-1	-0.2	1	uA	V_{MULTIN}=0V
Dynamic voltage range MULTIN	V_{MULTIN}		0 to 4		V	V_{VAOUT}=2.75V
Dynamic voltage range VAOUT	V_{VAOUT}		V_{FB} to V_{FB}+1.5			V_{MULTIN}=1V
Multiplier Gain	K_{low} K_{high}		0.3 0.7			V_{VAOUT}<3V, V_{MULTIN}=1V V_{VAOUT}>3.5V,V_{MULTIN}=1V
K=delta $V_{VISENSE}$/deltaV_{VAOUT} at V_{MULTIN}=constant						
Restart Timer						
restart time	t_{RES}	100	160	250	us	

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
Gate Drive						
Output voltage low state Output voltage low state Output voltage low state	V_{GTL} V_{GTL} V_{GTL}		1.0 1.7 2.2		V V V	I_{GT}= 2mA I_{GT}= 20mA I_{GT}=200mA
Output voltage high state Output voltage high state Output voltage high state	V_{GTH} V_{GTH} V_{GTH}		10.9 10.7 9.6		V V V	I_{GT}=-20mA I_{GT}=-200mA I_{GT}=-2mA, V_{CC}=11V see Diagram 14
Output voltage active shut down	V_{GTSD}		1		V	I_{GT}=20mA, V_{CC}=9V
Rise time Fall time	t_{rise} t_{fall}		80 55	180 120	ns ns	C_{GT}= 4.7nF Vout=2...8V C_{GT}= 4.7nF Vout=2...8V

Electrical Diagrams

Diagram 1: Icc versus Vcc

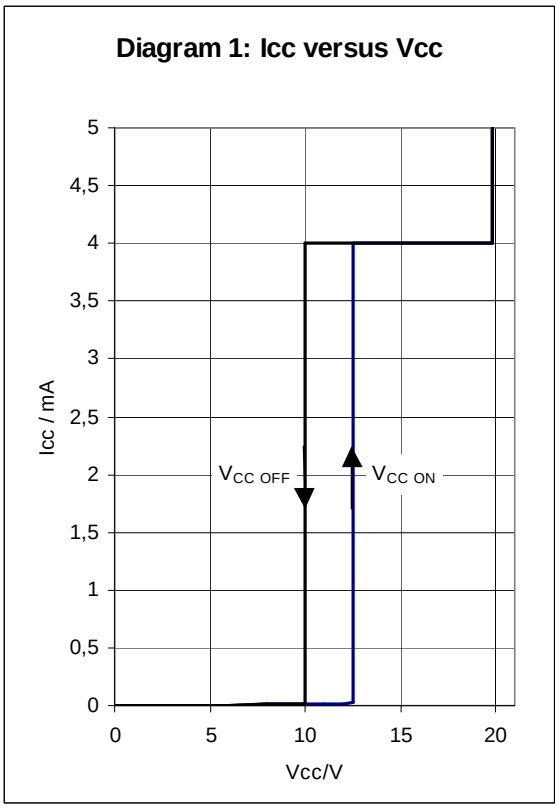


Diagram 2: $V_{CCON/OFF}$ versus Temperature

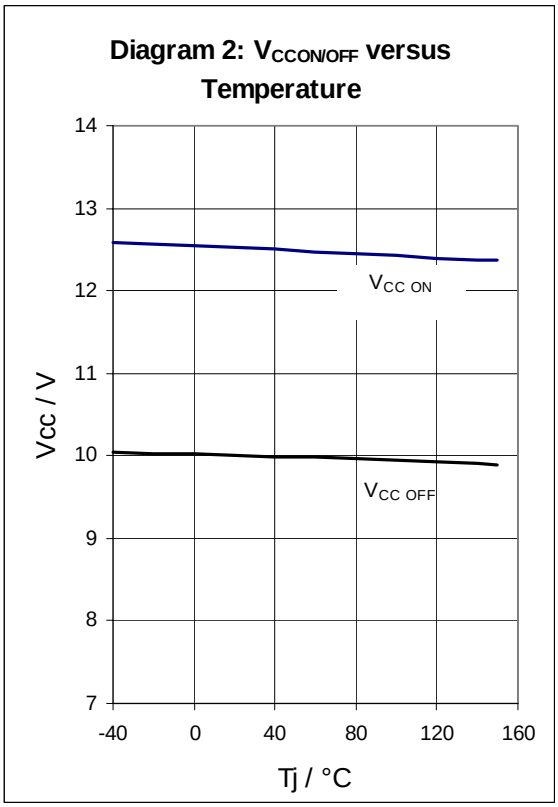


Diagram 3: Iccl versus Vcc

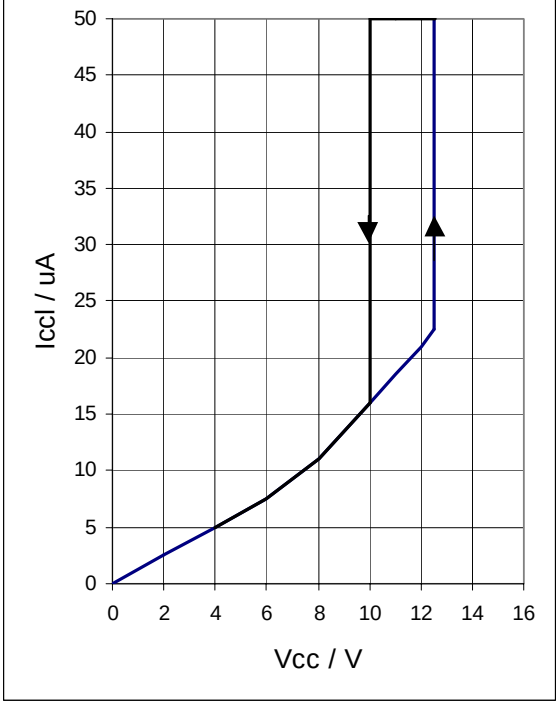


Diagram 4: I_{CCL} versus Temperature, V_{CC}=10V

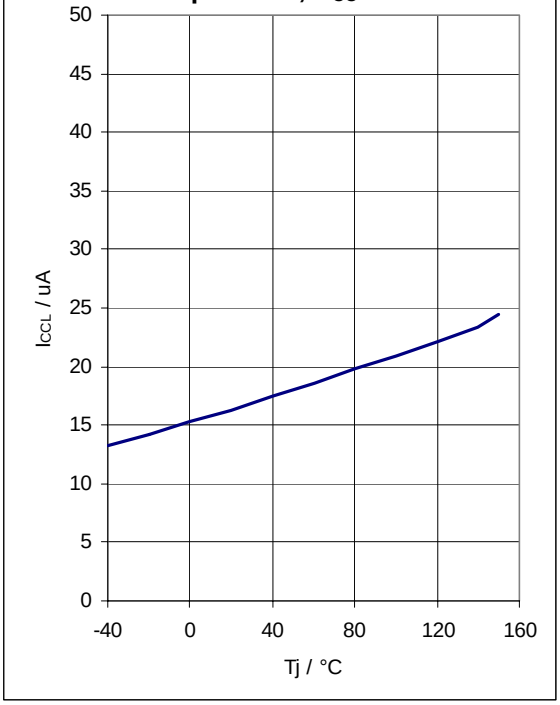


Diagram 5: V_{FB} vers. Temperature
(pin1 connected to pin2)

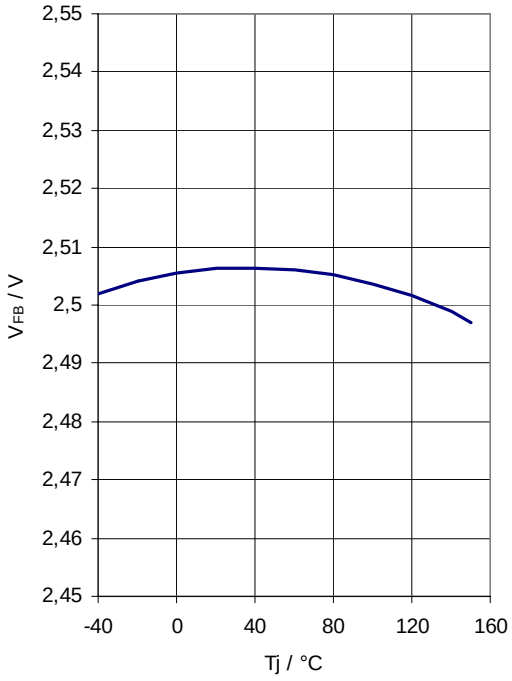


Diagram 6: Open loop gain and Phase versus frequency

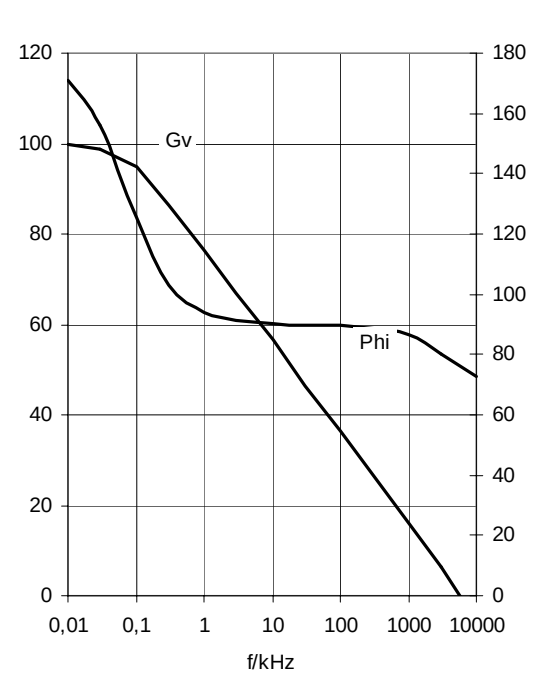


Diagram 7: Overvoltage Regulator V_{ISENSE} vers. Threshold Voltage

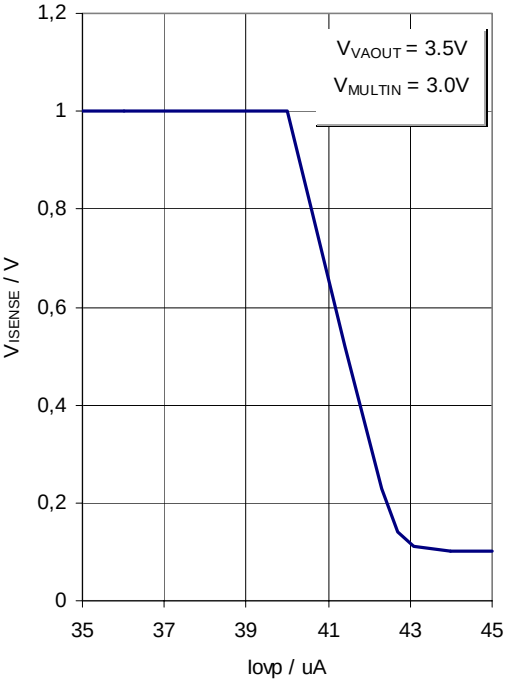


Diagram 8: Leading edge blanking vers. Temp.

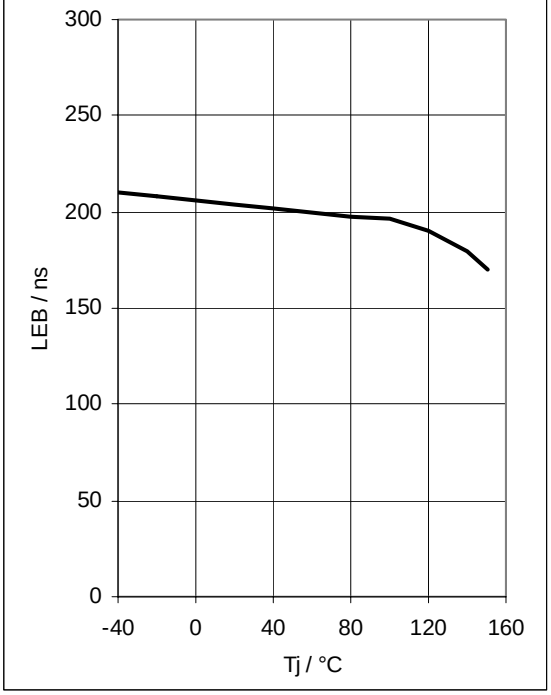


Diagram 9: Current Sense Threshold V_{ISENSE} versus V_{MULTIN}

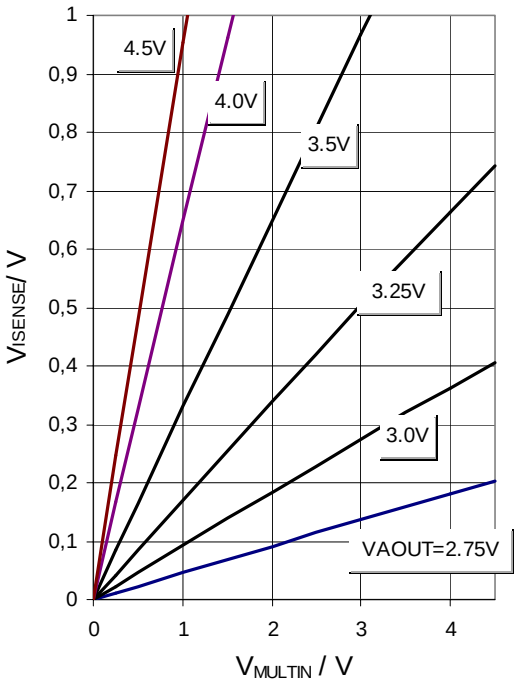


Diagram 10: Current sense threshold V_{ISENSE} versus V_{VAOUT}

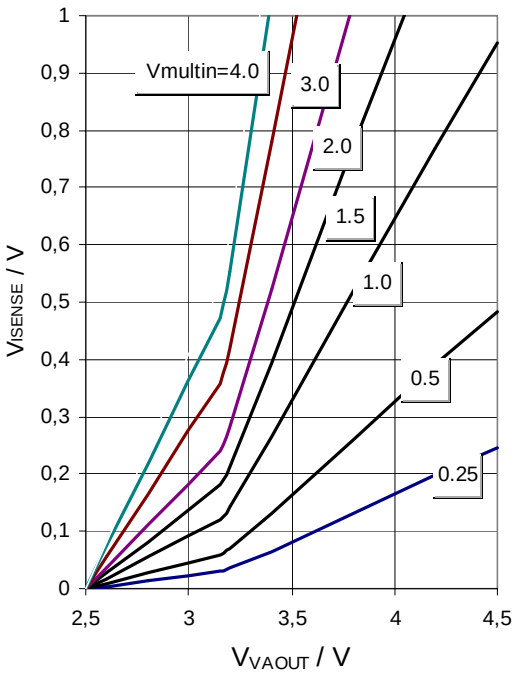


Diagram 11: Restart time versus temperature

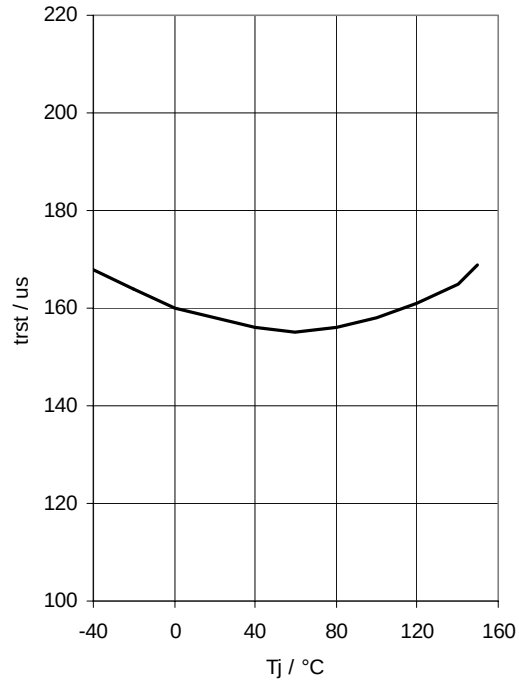


Diagram 12: Gate Drive Rise Time and Fall Time vers. temperature

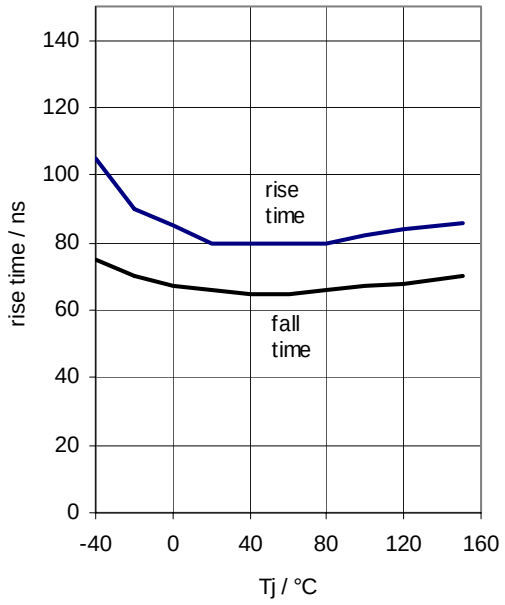
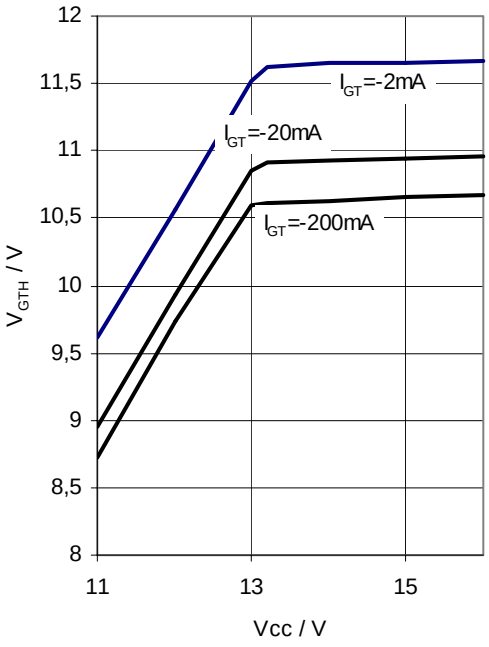
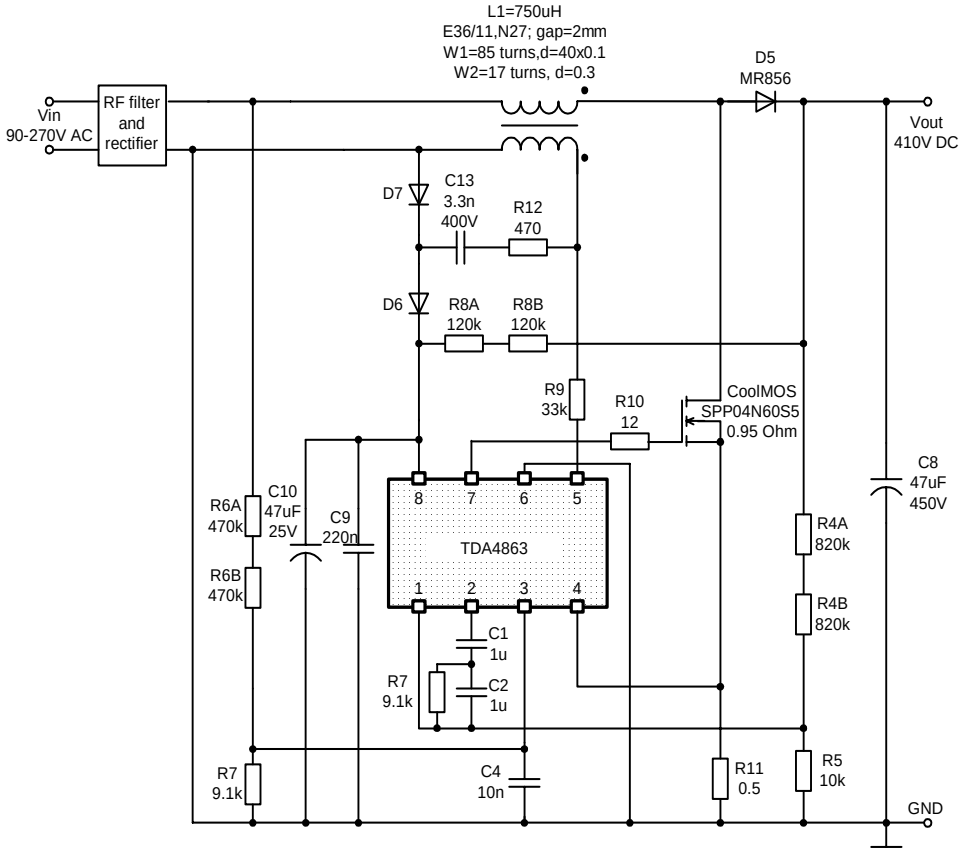


Diagram 13: Gate drive voltage high state versus Vcc



Application circuit: Pout=110W, universal Input Vin=90-270V AC



Results of THD measurements with application board Pout=110W

Diagram:THD Class C: Pmax=110W, Vinac=90V, Iout=250mA, Vout=420, PF=0.998

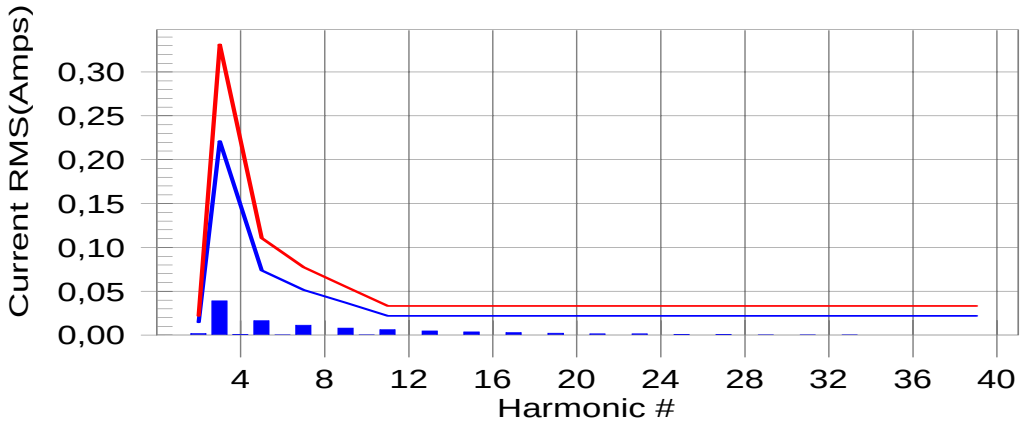


Diagramm: THD ClassC: Pmax=110W, Vinac=220V, Iout=250mA, Vaout=420V, PF=0.992

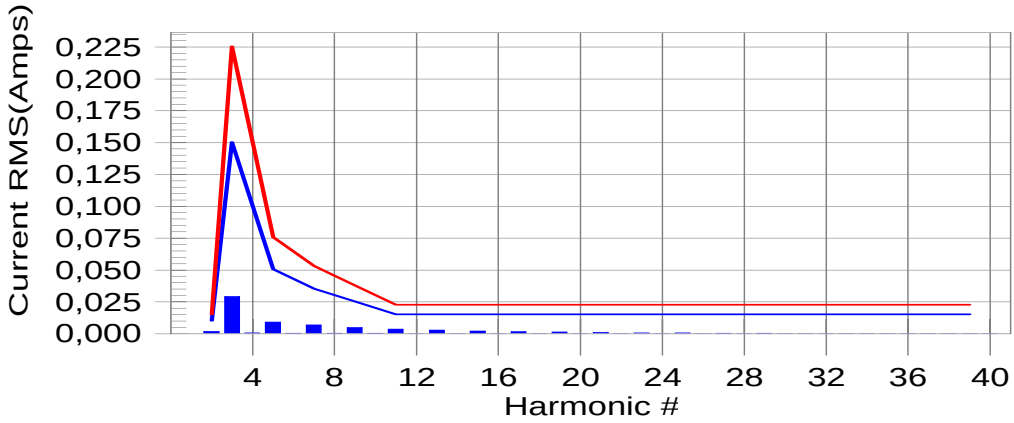


Diagramm: THD ClassC: Pmax=110W, Vinac=270V, Iout=250mA, Vaout=420V, PF=0.978

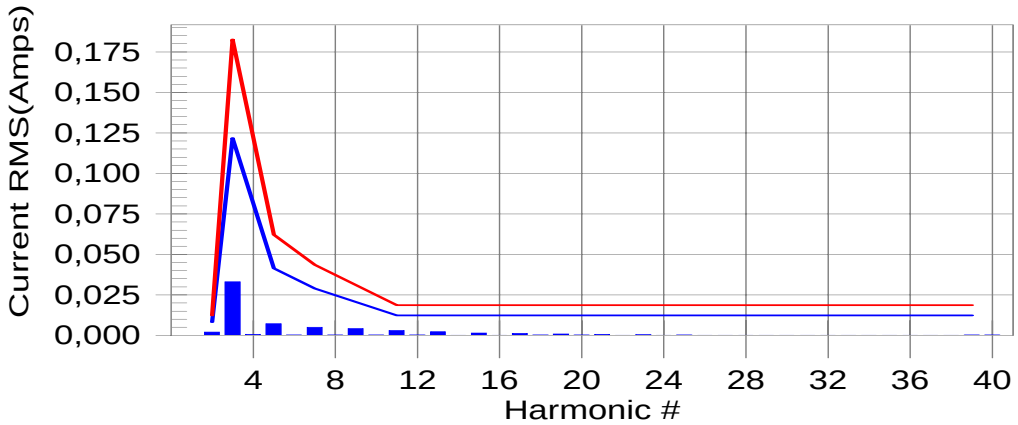


Diagramm: THD ClassC: Pmax=110W, Vinac=90V, Iout=140mA, Vaout=420V, PF=0.999

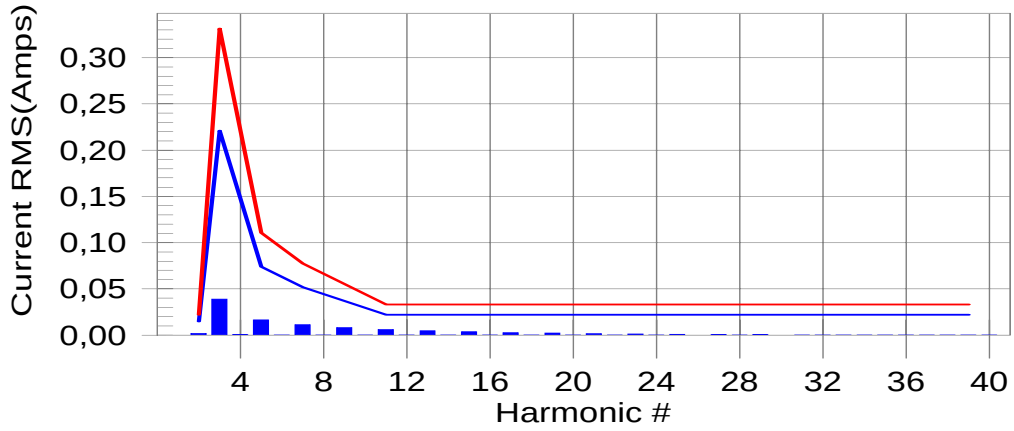


Diagramm: THD ClassC: Pmax=110W, Vinac=270V, Iout=140mA, Vaout=420V, PF=0.975

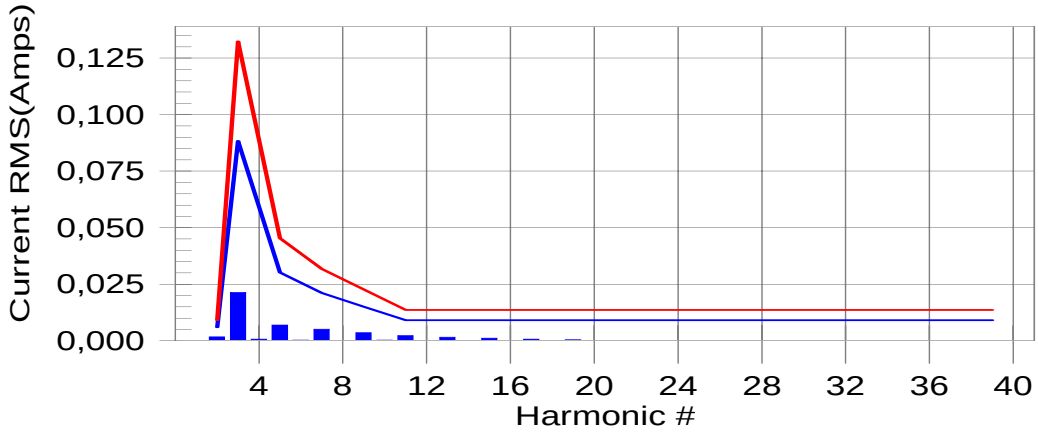


Diagramm: THD ClassC: Pmax=110W, Vinac=270V, Iout=140mA, Vaout=420V, PF=0.883