

PAD SERIES

PICO AMPERE DIODES

FEATURES

DIRECT REPLACEMENT FOR SILICONIX PAD SERIES

REVERSE BREAKDOWN VOLTAGE $BV_R \geq -30V$

REVERSE CAPACITANCE $C_{RSS} \leq 2.0pF$

ABSOLUTE MAXIMUM RATINGS¹

@ 25 °C (unless otherwise stated)

Maximum Temperatures

Storage Temperature -65 to +150 °C

Operating Junction Temperature -55 to +135 °C

Maximum Power Dissipation

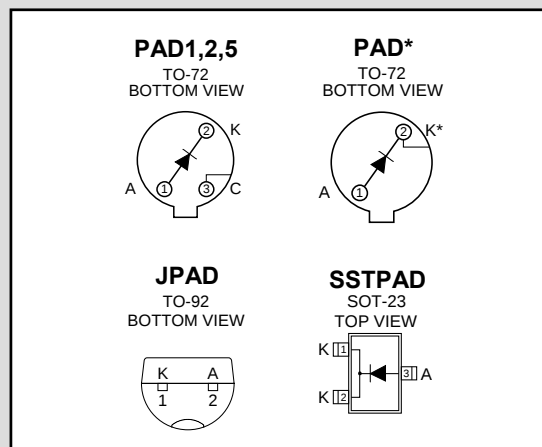
Continuous Power Dissipation (PAD) 300mW

Continuous Power Dissipation (J/SSTPAD) 350mW

Maximum Currents

Forward Current (PAD) 50mA

Forward Current (J/SSTPAD) 10mA



* Cathode tied to Case

COMMON ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_R	Reverse Breakdown Voltage	ALL PAD	-45		V	$I_R = -1\mu A$
		ALL SSTPAD	-30			
		ALL JPAD	-35			
V_F	Forward Voltage		0.8	1.5		$I_F = 5mA$
C_{RSS}	Total Reverse Capacitance	PAD1,5	0.5	0.8	pF	$V_R = -5V, f = 1MHz$
		All Others	1.5	2		

SPECIFIC ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

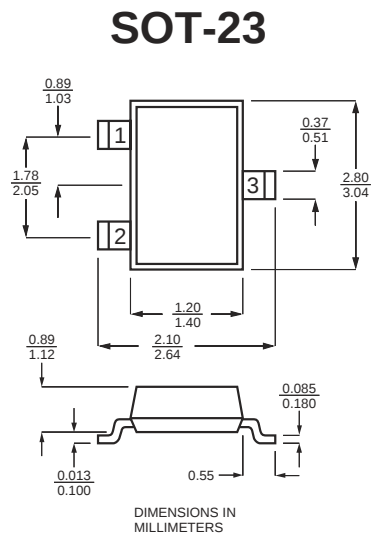
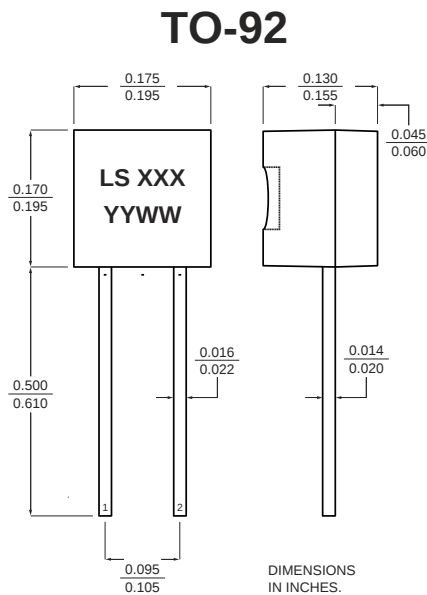
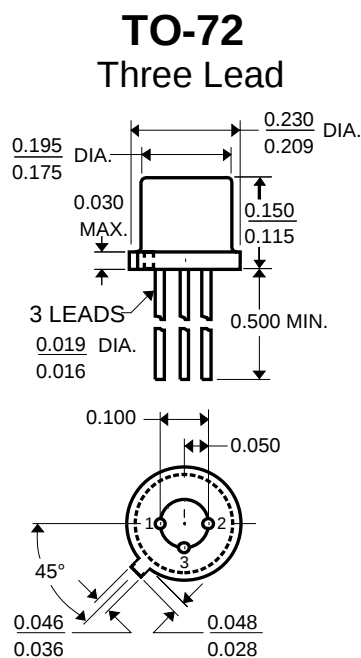
SYMBOL	CHARACTERISTIC	PAD ²	JPAD ²	SSTPAD ²	UNITS	CONDITIONS
I_R	Maximum Reverse Leakage Current ²	(SST/J)PAD1	-1		pA	$V_R = -20V$
		(SST/J)PAD2	-2			
		(SST/J)PAD5	-5	-5		
		(SST/J)PAD10	-10	-10		
		(SST/J)PAD20	-20	-20		
		(SST/J)PAD50	-50	-50		
		(SST/J)PAD100	-100			
		(SST/J)PAD200	-200			
		(SST/J)PAD500	-500			

Input Differential Voltage limited to 0.8V (typ) by JPADs D₁ and D₂. Common Mode Input voltage limited by JPADs D₃ and D₄ to ± 15 V.

Typical Sample and Hold circuit with clipping. JPAD diodes reduce offset voltages fed capacitively from the JFET switch gate.

The diagram shows a differential amplifier circuit. Two input lines, labeled +15V and -15V, are connected to four diodes: D1 and D2 on the top line, and D3 and D4 on the bottom line. D1 and D3 are oriented with their cathodes to the input lines, while D2 and D4 have their anodes to the input lines. The outputs of the diodes are connected to the non-inverting (+) and inverting (-) inputs of an OP-27 operational amplifier. The output of the OP-27 is connected to a common output terminal.

The circuit diagram illustrates a precision rectifier. The input signal e_{in} is connected to the non-inverting input of the first op-amp. The output of the first op-amp is connected to the gate of a 2N4393 JFET, which acts as a buffer. The JFET's source is grounded, and its drain is connected to the inverting input of the second op-amp. The inverting input of the second op-amp is also connected to the anode of diode D1 (JPAD5) and the cathode of diode D2 (JPAD5). The cathode of D1 is connected to the positive supply $+V$, and the anode of D2 is connected to the negative supply $-V$. The output of the second op-amp is connected to the collector of a 2N4117A BJT. The emitter of the BJT is connected to ground, and the base is connected to the output of the first op-amp. A feedback capacitor C is connected between the output of the second op-amp and its inverting input. A load resistor R is connected between the output of the second op-amp and ground. The output voltage is V_{OUT} .



1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. The PAD type number denotes its maximum reverse current value in pico amperes. Devices with I_R values intermediate to those shown are available upon request.

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