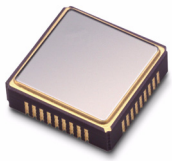
M2006-02

VCSO BASED FEC CLOCK PLL

GENERAL DESCRIPTION



The M2006-02 is a VCSO (Voltage Controlled SAW Oscillator) based clock generator PLL designed for clock frequency translation and jitter attenuation. The device supports both forward and inverse FEC (Forward Error Correction) clock multiplication ratios. Multiplication ratios are pin-selected from pre-programming look-up tables.

FEATURES

- **Pin-selectable PLL divider ratios support forward and inverse FEC ratio translation, including:**
  - 255/238 (OTU1) Mapping and 238/255 De-mapping
  - 255/237 (OTU2) Mapping and 237/255 De-mapping
  - 255/236 (OTU3) Mapping and 236/255 De-mapping
- **Supports input reference and VCSO frequencies up to 700MHz, supports loop timing modes (Specify VCSO frequency at time of order)**
- **Low phase jitter < 0.5 ps rms typical (12kHz to 20MHz or 50kHz to 80MHz)**
- **Supports active switching between inverse-FEC and non-FEC clock ratios (same VCSO center frequency)**
- **Ideal for complex ratio FEC ratio translation* and for use with an unstable reference** *(i.e., similar to the M2006-12 - and pin-compatible - but without the Hitless Switching and Phase Build-out functions)*
- **Commercial and Industrial temperature grades**
- **Single 3.3V power supply**
- **Small 9 x 9 mm SMT (surface mount) package**

Note *: Complex ratio FEC ratio translation typically results in low phase detector frequencies.
Note **: An unstable reference which results in phase detector jitter beyond 2 ns under normal operating conditions

PIN ASSIGNMENT (9 x 9 mm SMT)

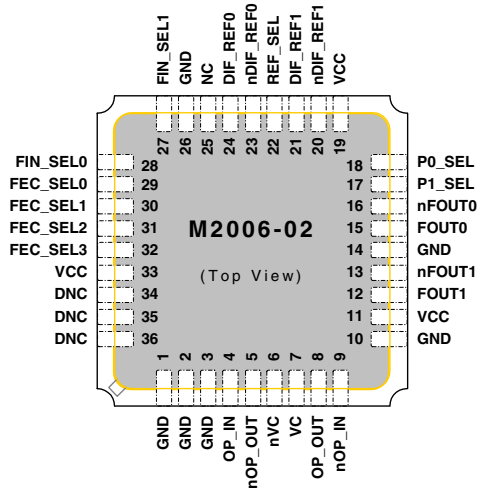


Figure 1: Pin Assignment

Example I/O Clock Frequency Combinations Using M2006-02-622.0800 and Inverse FEC Ratios

FEC PLL Ratio Mfec / Rfec	Base Input Rate [1] (MHz)	Output Clock (either output) MHz
1/1	622.0800	622.08 or 155.52
238/255	666.5143	
237/255	669.3266	
236/255	672.1627	

Table 1: Example I/O Clock Frequency Combinations

Note 1: Input reference clock can be the base frequency shown divided by "Mfin" (as shown in Table 3 on pg. 3).

SIMPLIFIED BLOCK DIAGRAM

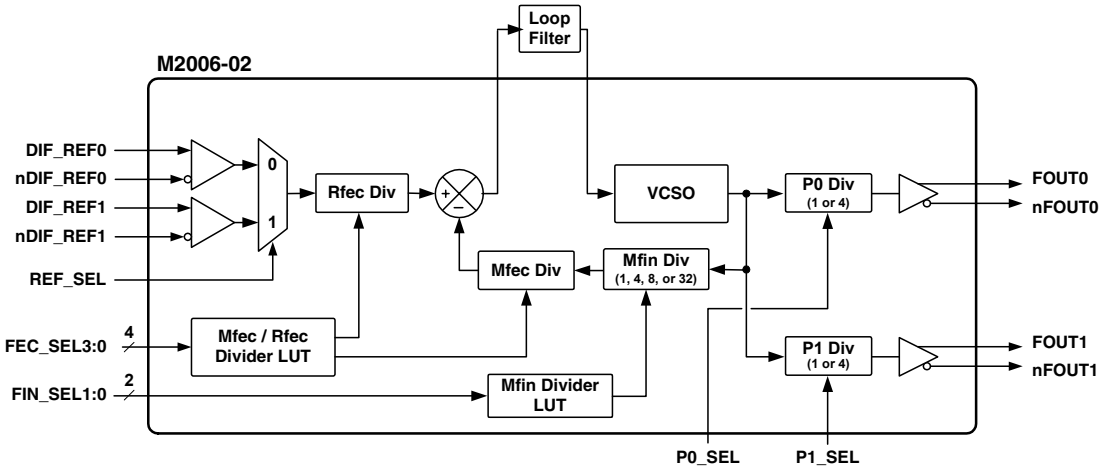


Figure 2: Simplified Block Diagram

DETAILED BLOCK DIAGRAM

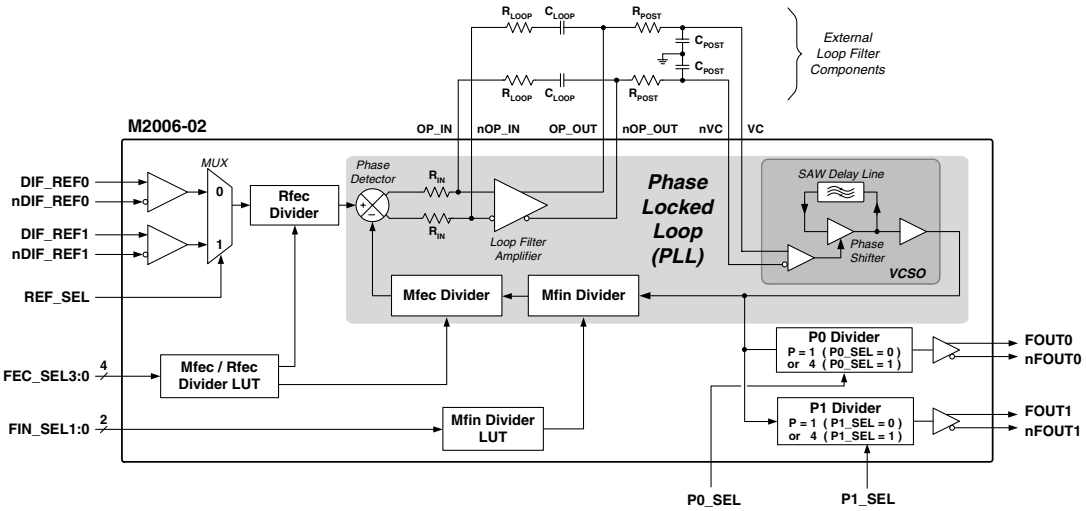


Figure 3: Detailed Block Diagram

PIN DESCRIPTIONS

Number	Name	I/O	Configuration	Description
1, 2, 3, 10, 14, 26	GND	Ground		Power supply ground connections.
4 9	OP_IN nOP_IN	Input		External loop filter connections. See Figure 4.
5 8	nOP_OUT OP_OUT	Output		
6 7	nVC VC	Input		
11, 19, 33	VCC	Power		Power supply connection, connect to +3.3V.
12, 13 15, 16	FOUT1, nFOUT1 FOUT0, nFOUT0	Output	No internal terminator	Clock output pairs. Differential LVPECL.
17 18	P1_SEL P0_SEL	Input	Internal pull-down resistor[1]	P Divider controls. LVCMOS/LVTTL. (For P0_SEL, P1_SEL, see Table 5 on pg. 3.
20 21	nDIF_REF1 DIF_REF1	Input	Internal pull-UP resistor[1] Internal pull-down resistor[1]	Reference clock input pair 1. Differential LVPECL or LVDS.
22	REF_SEL	Input	Internal pull-down resistor[1]	Reference clock input selection. LVCMOS/LVTTL: Logic 1 selects DIF_REF1, nDIF_REF1. Logic 0 selects DIF_REF0, nDIF_REF0.
23 24	nDIF_REF0 DIF_REF0	Input	Internal pull-UP resistor[1] Internal pull-down resistor[1]	Reference clock input pair 0. Differential LVPECL or LVDS.
25	NC			No internal connection.
27 28	FIN_SEL1 FIN_SEL0	Input	Internal pull-down resistor[1]	Input clock frequency selection. LVCMOS/LVTTL. (For FIN_SEL1:0, see Table 3 on pg. 3.
29 30 31 32	FEC_SEL0 FEC_SEL1 FEC_SEL2 FEC_SEL3	Input	Internal pull-UP resistor[1]	FEC PLL divider ratio selection. LVCMOS/ LVTTL. (For FEC_SEL3:0, see Table 4 on pg. 3.)
34, 35, 36	DNC		Do Not Connect.	Internal nodes. Connection to these pins can cause erratic device operation.

Table 2: Pin Descriptions

PLL DIVIDER LOOK-UP TABLES

Mfin (Frequency Input) Divider Look-Up Table (LUT)

The FIN_SEL1:0 pins select the feedback divider value ("Mfin").

FIN_SEL1:0	Mfin Value	M2006-02-622.0800 Sample Ref. Freq. (MHz) [1]
1 1	1	622.08 [2]
1 0	4	155.52
0 1	8	77.76
0 0	32	19.44

Table 3: Mfin (Frequency Input) Divider Look-Up Table (LUT)

Note 1: Example with M2006-02-622.0800 and "Non-FEC ratio" selection made from Table 4 (FEC_SEL2=1).
Note 2: Do not use with FEC_SEL3:0=1100 or 1101.

FEC PLL Ratio Dividers Look-up Table (LUT)

The FEC_SEL3:0 pins select the FEC feedback and reference divider values Mfec and Rfec.

FEC_SEL3:0	Mfec	Rfec[1]	Description
0 0 0 0	236	255	Inverse FEC ratio
0 0 0 1	79	85	Inverse FEC ratio, equivalent to 237/255
0 0 1 0	14	15	Inverse FEC ratio, equivalent to 238/255
0 0 1 1	239	255	Inverse FEC ratio
0 1 0 0	236	236	Non-FEC ratio, complements 0000 or 1000 [2]
0 1 0 1	79	79	Non-FEC ratio, complements 0001 or 1001 [2]
0 1 1 0	14	14	Non-FEC ratio, complements 0010 or 1010 [2]
0 1 1 1	239	239	Non-FEC ratio, complements 0011 or 1011 [2]
1 0 0 0	255	236	FEC ratio (OTU3)
1 0 0 1	85	79	FEC ratio, equivalent to 255/237 (OTU2)
1 0 1 0	15	14	FEC ratio, equivalent to 255/238 (OTU1)
1 0 1 1	255	239	FEC ratio
1 1 0 0	1	1	Non-FEC ratio [3] *Do not use these two settings with FIN_SEL1:0=11*
1 1 0 1	2	2	
1 1 1 0	4	4	Non-FEC ratio [3]
1 1 1 1	8	8	

Table 4: FEC PLL Ratio Dividers Look-up Table (LUT)

Note 1: The phase detector frequency (Fpd, which is calculated as Fref/Rfec) should be above 1.5 MHz to prevent spurs on the output clock. To ensure the PLL remains locked when using a recovered clock (such as in loop timing mode), the phase detector frequency should ideally be about 20MHz, or at least less than 50 MHz.
Note 2: These table selections use the same or similar Mfec divider values as the complementary selections noted. This allows the use of the same loop filter component values and resulting PLL loop bandwidth and damping factor values for complementary selections. Complementary selections can be actively switched in a given application.
Note 3: In non-FEC applications, these settings can be used optimize phase detector frequency or to actively change PLL loop bandwidth.

Post-PLL Dividers

The M2006-02 also features two post-PLL dividers, one for each output pair. The "P1" divider is for FOUT1 and nFOUT1; the "P0" divider is for FOUT0 and nFOUT0.

Each divides the VCSO frequency to produce one of two output frequencies (1/4 or 1/1 of the VCSO frequency). The P1_SEL and P0_SEL pins each select the value for their corresponding divider.

P1_SEL, P0_SEL	P Value	M2006-02-622.0800 Output Frequency (MHz)
1	4	155.52
0	1	622.08

Table 5: P Divider Selector, Values, and Frequencies

FUNCTIONAL DESCRIPTION

The M2006-02 is a PLL (Phase Locked Loop) based clock generator that generates output clocks synchronized to one of two selectable input reference clocks.

An internal high "Q" SAW filter provides low jitter signal performance and controls the output frequency of the VCSO (Voltage Controlled SAW Oscillator).

Configurable FEC feedback and reference dividers (the "Mfec Divider" and "Rfec Divider") provide the multiplication ratios necessary to accomodate clock translation for both forward and inverse Forward Error Correction.

In addition, a configurable feedback divider (labeled "Mfin Divider") provides the broader division options needed to accomodate various reference clock frequencies.

For example, the **M2006-02-622.0800** *(see "Ordering Information"* on pg. 8*)* has a 622.08MHz VCSO frequency:

- The inverse FEC PLL ratios (at top of Table 4) enable the **M2006-02-622.0800** to accept "base" input reference frequencies of: 663.7255, 666.5143, 669.3266, 672.1627, and 622.08MHz.
- The Mfin feedback divider enables the actual input reference clock to be the "base" input frequency divided by 1, 4, 8, or 32. Therefore, for the base input frequency of 622.08MHz, the actual input reference clock frequencies can be: 622.08, 155.52, 77.76, and 19.44MHz. (See Table 3 on pg. 3.)

The PLL

The PLL uses a phase detector and configurable dividers to synchronize the output of the VCSO with selected reference clock.

The “Mfin Divider” and “Mfec Divider” divide the VCSO frequency, feeding the result into the phase detector.

The selected input reference clock is divided by the “Rfec Divider”. The result is fed into the other input of the phase detector.

The phase detector compares its two inputs. It then outputs pulses to the loop filter as needed to increase or decrease the VCSO frequency and thereby match and lock the divider output’s frequency and phase to those of the input reference clock.

Due to the narrow tuning range of the VCSO (±200ppm), appropriate selection of all of the following are required for the PLL be able to lock: VCSO center frequency, input frequency, and divider selections.

Maintaining PLL Lock:
The narrow tuning range of the VCSO requires that the input reference frequency must remain suitable for the current look-up table selection. For example, when switching between “Inverse FEC ratio” and “Non-FEC ratio” look-up table selections (see Table 4 on pg. 3), the input reference frequency must change accordingly in order for the PLL to lock.

An out-of-lock condition due to an inappropriate configuration will typically result in the VCSO operating at its lower or upper frequency rail, which is approximately 200ppm above or below the nominal VCSO center frequency.

Relationship Among Frequencies and Dividers

The VCSO center frequency must be specified at time of order. The relationship between the VCSO (Fvcso) frequency, the Mfin divider, the Mfec divider, the Rfec divider, and the input reference frequency (Fin) is:

$$Fvcso = Fin \times Mfin \times \frac{Mfec}{Rfec}$$

As an example, for the **M2006-02-622.0800**, the non-FEC and inverse-FEC PLL ratios in Table 4 enable use with these corresponding input reference frequencies:

M2006-02-622.0800 VCSO Clock Frequency (MHz) ÷	FEC Ratio	M2006-02-622.0800 Base Input Ref. = Frequency (MHz) [1]
622.08	1 / 1	622.0800
	238 / 255	666.5143
	237 / 255	669.3266
	236 / 255	672.1627

Table 6: Example FEC PLL Rations and Input Reference Frequencies
Note 1: Input reference clock (“Fin”) can be the base frequency shown divided by “Mfin” (as shown in Table 3 on pg. 3).

Outputs

The M2006-02 provides a total of two differential LVPECL output pairs: FOUT1 and FOUT0. Because each output pair has its own P divider, the FOUT1 pair and the FOUT0 can output the two different frequencies at the same time. For example, FOUT1 can output 155.52MHz while FOUT0 outputs 622.08MHz.

Any unused output should be left unconnected (floating) in the system application. This will minimize output switching current and therefore minimize noise modulation of the VCSO.

External Loop Filter

To provide stable PLL operation, and thereby a low jitter output clock, the M2006-02 requires the use of an external loop filter. This is provided via the provided filter pins (see Figure 4).

Due to the differential signal path design, the implementation requires two identical complementary RC filters as shown here.

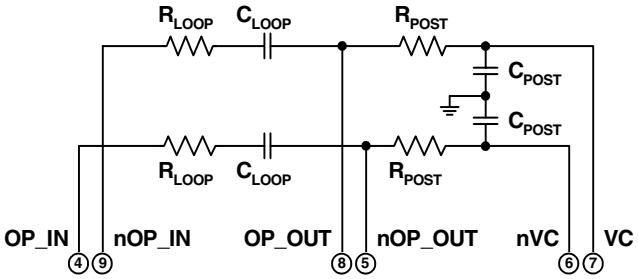


Figure 4: External Loop Filter

PLL bandwidth is affected by the "Mfec" value and the "Mfin" value, as well as the VCSO frequency.

The various "Non-FEC ratio" settings can be used to actively change PLL loop bandwidth in a given application. See "FEC PLL Ratio Dividers Look-up Table (LUT)" on pg. 3.

Consult factory for external loop filter component values.

PLL Simulator Tool Available

A free PC software utility is available on the ICS website (www.icst.com). The M2000 Timing Modules PLL Simulator is a downloadable application that simulates PLL jitter and wander transfer characteristics. This enables the user to set appropriate external loop component values in a given application.

Go to the SAW PLL Simulator Software web page at www.icst.com/products/calculators/m2000filterSWdesc.htm

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Rating	Unit
V_I	Inputs	-0.5 to V_{CC} +0.5	V
V_O	Outputs	-0.5 to V_{CC} +0.5	V
V_{CC}	Power Supply Voltage	4.6	V
T_S	Storage Temperature	-45 to +100	°C

Table 7: Absolute Maximum Ratings

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in Recommended Conditions of Operation, DC Characteristics, or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

RECOMMENDED CONDITIONS OF OPERATION

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
T_A	Ambient Operating Temperature	Commercial	0		+70	°C
		Industrial	-40		+85	°C

Table 8: Recommended Conditions of Operation

ELECTRICAL SPECIFICATIONS

DC Characteristics

Unless stated otherwise, V_{CC} = 3.3V ±5%, T_A = 0 °C to +70 °C (commercial), T_A = -40 °C to +85 °C (industrial), F_{VCSO} = F_{OUT} = 622-675MHz, LVPECL outputs terminated with 50Ω to V_{CC} - 2V

	Symbol	Parameter		Min	Typ	Max	Unit	Conditions
Power Supply	V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V	
	I_{CC}	Power Supply Current			175	225	mA	
All Differential Inputs	V_{P-P}	Peak to Peak Input Voltage	DIF_REF0, nDIF_REF0, DIF_REF1, nDIF_REF1	0.15			V	
	V_{CMR}	Common Mode Input		0.5		V_{CC} - .85	V	
	C_{IN}	Input Capacitance				4	pF	
Differential Inputs with Pull-down	I_{IH}	Input High Current (Pull-down)	DIF_REF0, DIF_REF1			150	µA	V_{CC} = V_{IN} = 3.456V
	I_{IL}	Input Low Current (Pull-down)		-5			µA	
	$R_{pulldown}$	Internal Pull-down Resistance			50		kΩ	
Differential Inputs with Pull-up	I_{IH}	Input High Current (Pull-up)	nDIF_REF0, nDIF_REF1			5	µA	V_{IN} = 0 to 3.456V
	I_{IL}	Input Low Current (Pull-up)		-150			µA	
	R_{pullup}	Internal Pull-up Resistance			50		kΩ	
All LVCMOS / LVTTL Inputs	V_{IH}	Input High Voltage	REF_SEL, FIN_SEL1, FIN_SEL0, FEC_SEL3, FEC_SEL2, FEC_SEL1, FEC_SEL0, P1_SEL, P0_SEL	2		V_{CC} + 0.3	V	
	V_{IL}	Input Low Voltage		-0.3		0.8	V	
	C_{IN}	Input Capacitance				4	pF	
LVCMOS / LVTTL Inputs with Pull-down	I_{IH}	Input High Current (Pull-down)	REF_SEL, FIN_SEL1, FIN_SEL0, P1_SEL, P0_SEL			150	µA	V_{CC} = V_{IN} = 3.456V
	I_{IL}	Input Low Current (Pull-down)		-5			µA	
	$R_{pulldown}$	Internal Pull-down Resistance			50		kΩ	
LVCMOS / LVTTL Inputs with Pull-up	I_{IH}	Input High Current (Pull-up)	FEC_SEL3, FEC_SEL2, FEC_SEL1, FEC_SEL0			5	µA	V_{CC} = 3.456V V_{IN} = 0 V
	I_{IL}	Input Low Current (Pull-up)		-150			µA	
	R_{pullup}	Internal Pull-up Resistance			50		kΩ	
Differential Outputs	V_{OH}	Output High Voltage	FOUT0, nFOUT0, FOUT1, nFOUT1	V_{CC} - 1.4		V_{CC} - 1.0	V	
	V_{OL}	Output Low Voltage		V_{CC} - 2.0		V_{CC} - 1.7	V	
	V_{P-P}	Peak to Peak Output Voltage [1]		0.4		0.85	V	

Note 1: Single-ended measurement. See Figure 5, Output Rise and Fall Time, on pg. 7.

Table 9: DC Characteristics

ELECTRICAL SPECIFICATIONS (CONTINUED)

AC Characteristics

Unless stated otherwise, V_{CC} = 3.3V ±5%, T_A = 0 °C to +70 °C (commercial), T_A = -40 °C to +85 °C (industrial), $F_{VCSO} = F_{OUT}$ = 622-675MHz, LVPECL outputs terminated with 50Ω to V_{CC} - 2V

	Symbol	Parameter		Min	Typ	Max	Unit	Test Conditions
Input Frequency Range	F_{IN}	Input Frequency	DIF_REF0, nDIF_REF0, DIF_REF1, nDIF_REF1	10		700	MHz	
Output Frequency	F_{FOUT}	Output Frequency Range	FOUT0, nFOUT0, FOUT1, nFOUT1	100		700	MHz	
	APR	VCSO Pull-Range	Commercial	±120	±200		ppm	
			Industrial	±50	±150		ppm	
PLL Loop Constants [1]	K_{VCO}	VCO Gain			800		kHz/V	
	R_{IN}	Internal Loop Resistor			50		kΩ	
	BW_{VCSO}	VCSO Bandwidth			700		kHz	
Phase Noise and Jitter	Φn	Single Side Band Phase Noise @622.08MHz	1kHz Offset		-72		dBc/Hz	Fin=19.44 MHz Mfin=32, Mfec=1, Rfec=1
			10kHz Offset		-94		dBc/Hz	
			100kHz Offset		-123		dBc/Hz	
	J(t)	Jitter (rms) @622.08MHz	12kHz to 20MHz		0.5		ps rms	
			50kHz to 80MHz		0.5		ps rms	
	t_{PW}	Output Duty Cycle [2] FOUT0, nFOUT0, FOUT1, nFOUT1	P0, P1 = 1	40	50	60	%	
			P0, P1 = 4	45	50	55	%	
	t_R	Output Rise Time [2]	FOUT0, nFOUT0, FOUT1, nFOUT1	200	450	500	ps	20% to 80%
	t_F	Output Fall Time [2]		200	450	500	ps	20% to 80%

Table 10: AC Characteristics

Note 1: Parameters needed for PLL Simulator software; see PLL Simulator Tool Available on pg. 5.
Note 2: See Parameter Measurement Information on pg. 7.

PARAMETER MEASUREMENT INFORMATION

Output Rise and Fall Time

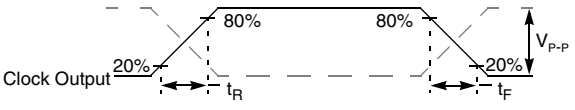


Figure 5: Output Rise and Fall Time

Output Duty Cycle

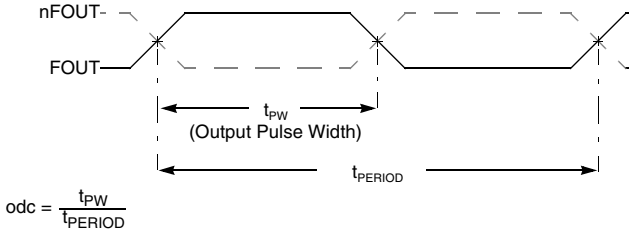
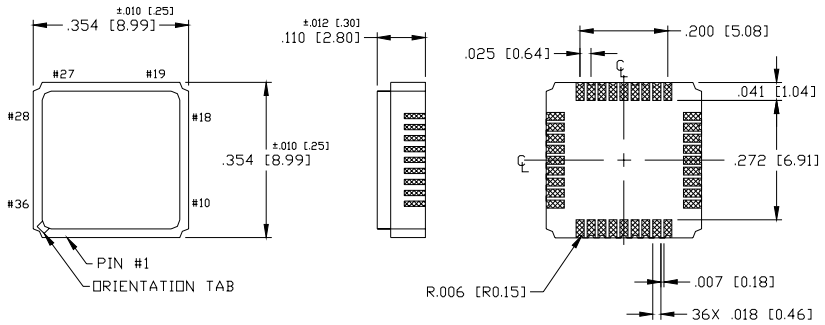


Figure 6: Output Duty Cycle

DEVICE PACKAGE - 9 x 9mm CERAMIC LEADLESS CHIP CARRIER

Mechanical Dimensions:



Refer to the M2006-02 product web page at www.icst.com/products/summary/m2006-02.htm for application notes, including recommended PCB footprint, solder mask, and furnace profile.

NOTES:
1. DIMENSIONS ARE IN INCHES, DIMENSIONS IN [ ] ARE MM.
2. UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE ±.005 [.13]

Figure 7: Device Package - 9 x 9mm Ceramic Leadless Chip Carrier

ORDERING INFORMATION

Part Numbering Scheme

Part Number: **M2006-02-xxx.xxxx**

Device Number

Temperature
"-" = 0 to +70 °C (commercial)
I = - 40 to +85 °C (industrial)

VCSO Frequency (MHz)
See Table 11, right. Consult ICS for other frequencies.

Figure 8: Part Numbering Scheme

Standard VCSO Output Frequencies (MHz)*

Consult ICS for the availablity of other VCSO frequencies

622.0800	669.3120
625.0000	669.3266
627.3296	669.6429
644.5313	670.8386
666.5143	672.1600
669.1281	690.5692

Table 11: Standard VCSO Output Frequencies (MHz)

Note *: Fout can equal Fvcso divided by: 1 or 4

Consult ICS for the availability of other PLL frequencies.

Example Part Numbers

PLL Frequency (MHz)	Temperature	Order Part Number
622.08	commercial	**M2006-02-622.0800**
	industrial	**M2006-02I-622.0800**
625.00	commercial	**M2006-02-625.0000**
	industrial	**M2006-02I-625.0000**
669.3266	commercial	**M2006-02-669.3266**
	industrial	**M2006-02I-669.3266**
669.6429	commercial	**M2006-02-669.6429**
	industrial	**M2006-02I-669.6429**

Table 12: Example Part Numbers