T-52-33-90

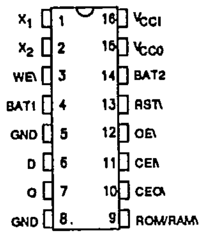
DALLAS SEMICONDUCTOR

DS1215/S
Phantom Time Chip

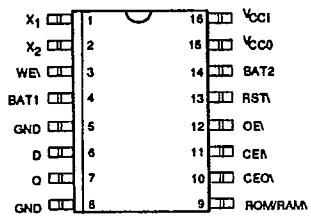
FEATURES

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Adjusts for months with fewer than 31 days
- Leap year automatically corrected
- No address space required
- Provides nonvolatile controller functions for battery backup of RAM
- Supports redundant batteries for high-rel applications
- Uses a 32.768 KHz watch crystal
- Full ±10% operating range
- Operating temperature range 0°C to 70°C
- Space-saving, 16-pin DIP package and SOIC

PIN DESCRIPTION



16 Pin DIP (300 mil)



16 Pin SOIC (300 mil)

PIN NAMES (\ Denotes Condition Low)

Pins 1&2	- X_1, X_2	- 32.768 KHz Crystal Connections
Pin 3	- WE\	- Write Enable
Pin 4	- BAT_1	- Battery 1 Input
Pins 5&8	- GND	- Ground
Pin 6	- D	- Data In
Pin 7	- Q	- Data Out
Pin 9	- ROM/ RAM\	- ROM-RAM Select
Pin 10	- CEO\	- Chip Enable Out
Pin 11	- CEI\	- Chip Enable Input
Pin 12	- OE\	- Output Enable
Pin 13	- RST\	- Reset
Pin 14	- BAT_2	- Battery 2 Input
Pin 15	- V_{CCO}	-Switched Supply Output
Pin 16	- V_{CCI}	- +5V DC Input

NOTE: Both pins 5 and 8 must be grounded.

DESCRIPTION

The DS1215 Phantom Time Chip is a combination of a CMOS timekeeper and a nonvolatile memory controller. In the absence of power, an external battery maintains the timekeeping operation and provides power for a CMOS static RAM. The watch keeps track of hundredths of seconds, seconds, minutes, hours, day, date, month, and year information, while the nonvolatile controller supplies all the necessary support circuitry to convert a CMOS RAM to a nonvolatile memory. The DS1215 can be interfaced with either RAM or ROM without leaving gaps in memory.

The last day of the month is automatically adjusted for months with less than 31 days, including correction for leap year every four years. The watch operates in one of two formats: a 12-hour mode with an AM/PM indicator or a 24-hour mode.

NONVOLATILE CONTROLLER OPERATION

The operation of the nonvolatile controller circuits within the Time Chip is determined by the level of the ROM/RAM\ select pin. When ROM/RAM\ is connected to ground, the controller is set in the RAM mode and performs the circuit functions required to make static CMOS RAM and the timekeeping function nonvolatile. A switch is provided to direct power from the battery inputs or V_{CCI} to V_{CCO} with a maximum voltage drop of 0.3 volts. The V_{CCO} output pin is used to supply uninterrupted power to CMOS SRAM. The DS1215 also performs redundant battery control for high reliability. On power-fail, the battery with the highest voltage is automatically switched to V_{CCO}. If only one battery is used in the system, the unused battery input should be connected to ground.

The DS1215 safeguards the Time Chip and RAM data by power-fail detection and write protection. Power-fail detection occurs when V_{CCI} falls below VTP, which is equal to 1.26 x V_{BAT}. The DS1215 constantly monitors the V_{CCI} supply pin. When V_{CCI} is less than VTP, a comparator outputs a power-fail signal to the control logic. The power-fail signal forces the chip enable output (CEO\) to V_{CCI} or V_{BAT}-0.2 volts for external RAM write protection. During nominal supply conditions, CEO\ will track CEI\ with a maximum propagation delay of 20ns. Internally, the DS1215 aborts any data transfer in progress without changing any of the Time Chip registers and prevents future access until V_{CCI} exceeds VTP. A typical RAM/Time Chip interface is illustrated in Figure 4.

When the ROM/RAM\ pin is connected to V_{CCO}, the controller is set in the ROM mode. Since ROM is a read-only device that retains data in the absence of power, battery backup and write protection is not required. As a result, the chip enable logic will not force CEO\ high when power fails. However, the Time Chip does retain the same internal nonvolatility and write protection as described in the RAM mode. In addition, the chip enable output is set at a low level on power-fail as V_{CCI} falls below the level of V_{BAT}. A typical ROM/Time Chip interface is illustrated in Figure 5.

TIME CHIP COMPARISON REGISTER DEFINITION Figure 1

	7	6	5	4	3	2	1	0	HEX VALUE
Byte 0	1	1	0	0	0	1	0	1	C5
Byte 1	0	0	1	1	1	0	1	0	3A
Byte 2	1	0	1	0	0	0	1	1	A3
Byte 3	0	1	0	1	1	1	0	0	5C
Byte 4	1	1	0	0	0	1	0	1	C5
Byte 5	0	0	1	1	1	0	1	0	3A
Byte 6	1	0	1	0	0	0	1	1	A3
Byte 7	0	1	0	1	1	1	0	0	5C

NOTE:
The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the Time Chip are less than 1 in 10^{19}.

TIME CHIP REGISTER INFORMATION

Time Chip information is contained in 8 registers of 8 bits, each of which is sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the Time Chip registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the Time Chip registers is not binary coded decimal format (BCD) in the12-hour mode. Reading and writing the registers is always accomplished by stepping though all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

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TIME CHIP REGISTER DEFINITION Figure 2

REGISTER	7	6	5	4	3	2	1	0	RANGE (BCD)
0	0.1 SEC				0.01 SEC				00-99
1	0	10 SEC			SECONDS				00-59
2	0	10 MIN			MINUTES				00-59
3	12/24	0	10 A/P	HR	HOUR				01-12 00-23
4	0	0	OSC\	RST\	0	DAY			01-07
5	0	0	10 DATE		DATE				01-31
6	0	0	0	10 MONTH	MONTH				01-12
7	10 YEAR				YEAR				00-99

AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the reset and oscillator functions. Bit 4 controls the reset pin (Pin 13). When the reset bit is set to logic 1, the reset input pin is ignored. When the reset bit is set to logic 0, a low input on the reset pin will cause the Time Chip to abort data transfer without changing data in the time-keeping registers. Reset operates independently of all other inputs. Bit 5 controls the oscillator. When set to logic 0, the oscillator turns on and the watch becomes operational.

ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits that will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

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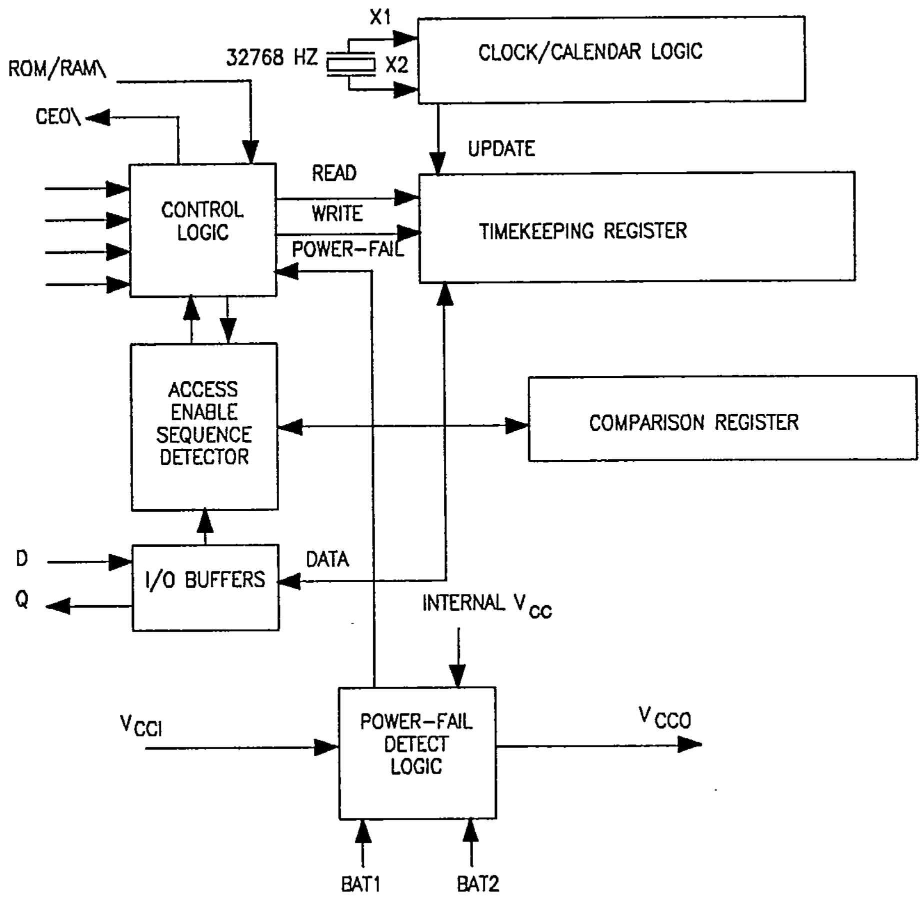
TIMING BLOCK DIAGRAM Figure 3



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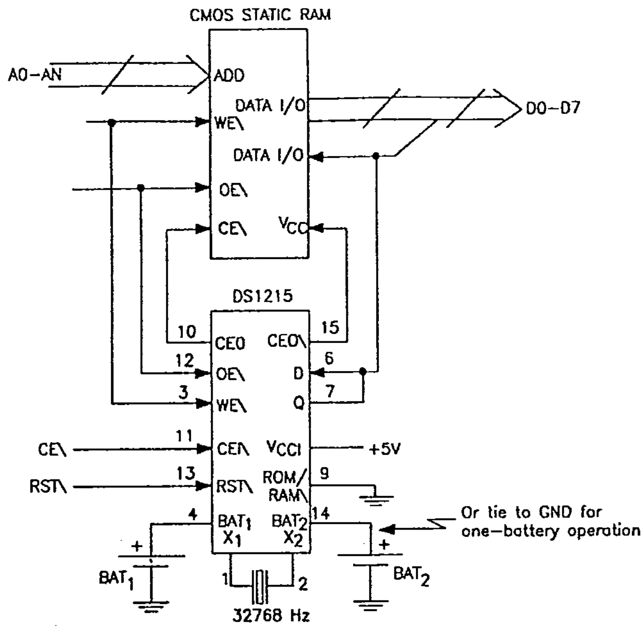
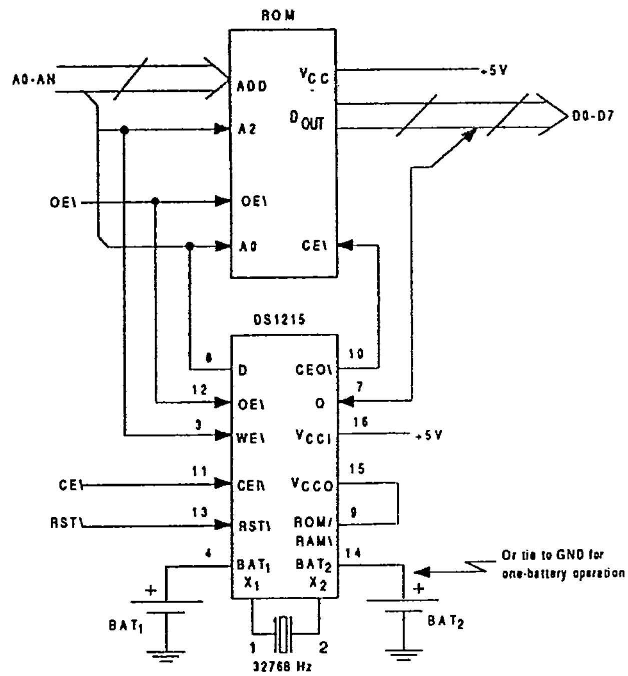
RAM/TIME CHIP INTERFACE Figure 4



ROM/TIME CHIP INTERFACE Figure 5



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ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.2		V_{CC}+0.3 V		1
Logic 0	V_{IL}	-0.3		+0.8	V	1
V_{BAT1} or V_{BAT2} Battery Voltage	V_{BAT}	2.5		3.7	V	7

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CCI}			5	mA	6
Supply Current $V_{CCO}=V_{CCI}-0.3$	I_{CCO1}			80	mA	8
Input Leakage	I_{IL}	-1.0		+1.0	uA	
Output Leakage	I_{LO}	-1.0		+1.0	uA	
Output @ 2.4V	I_{OH}	-1.0			mA	2
Output @ 0.4V	I_{OL}			4.0	mA	2

(0°C to 70°C, V_{CC} < 4.5V)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
CEO\ Output	V_{OH1}	V_{CCI} or V_{BAT}-0.2		V	9
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}		1	uA	6
Battery Backup Current @ $V_{CCO}=V_{BAT}-0.2V$	I_{CCO2}		10	uA	10

AC ELECTRICAL CHARACTERISTICS ROM/RAM\=GND(0°C to 70°C, V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
CE\ Access Time	t_{CO}			200	ns	
OE\ Access Time	t_{OE}			100	ns	
CE\ to Output Low Z	t_{COE}	10			ns	
OE\ to Output Low Z	t_{OEE}	10			ns	
CE\ to Output High Z	t_{OD}			100	ns	
OE\ to Output High Z	t_{ODO}			100	ns	
Read Recovery	t_{RR}	50			ns	
Write Cycle	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	170			ns	
Write Recovery	t_{WR}	50			ns	4
Data Setup	t_{DS}	100			ns	5
Data Hold Time	t_{DH}	10			ns	5
CE\ Pulse Width	t_{CW}	170			ns	
RST\ Pulse Width	t_{RST}	200			ns	
CE\ Propagation Delay	t_{PD}	5	10	20	ns	2, 3
CE\ High to Power-Fail	t_{PF}			0	ns	

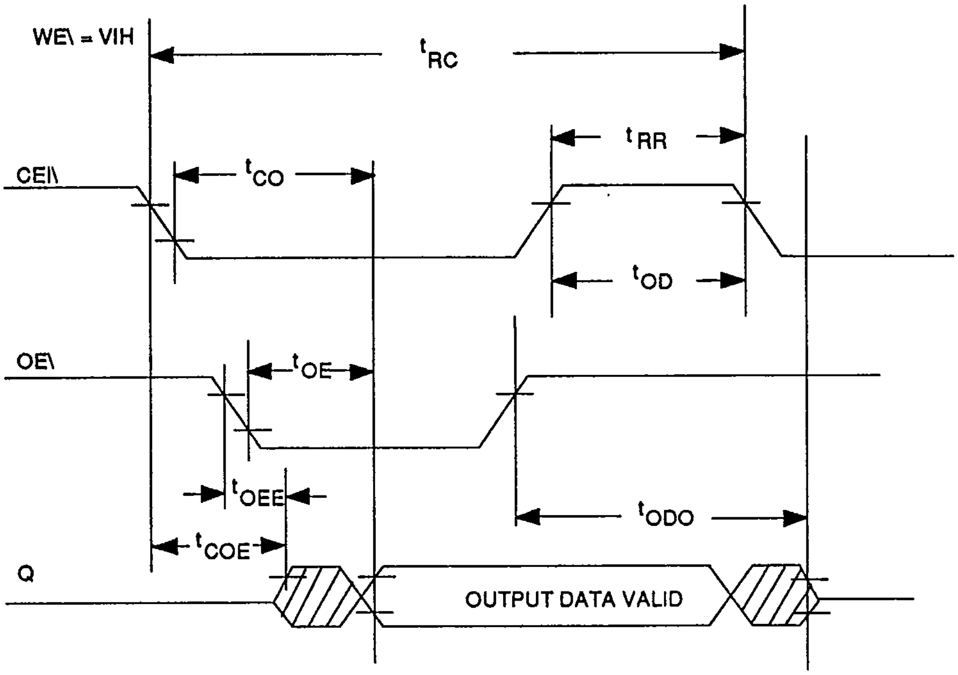
(0°C to 70°C, V_{CC} < 4.5V)

Recovery at Power-Up	t_{REC}			2	ms	
V_{CC} Slew Rate 4.5 - 3.0V	t_F	0			ms	

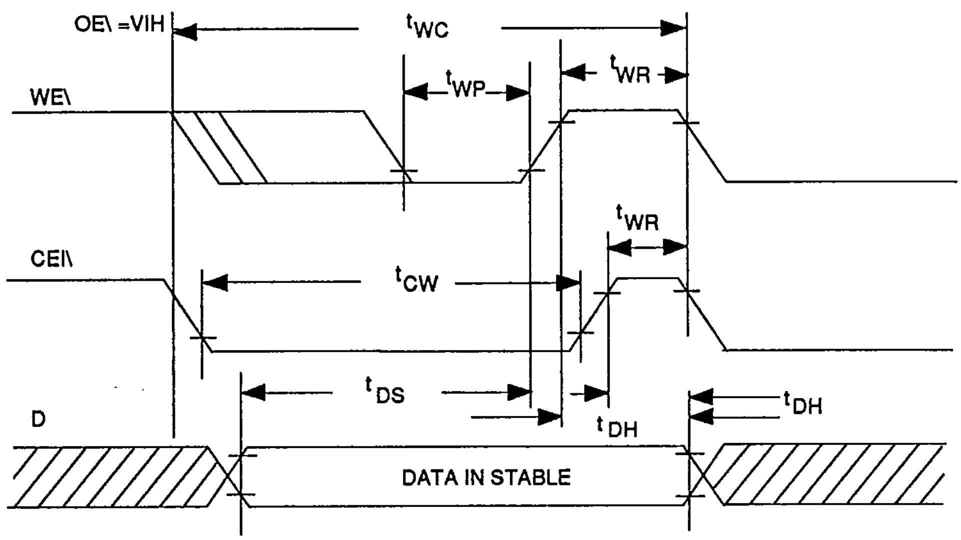
CAPACITANCE (t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5			pF	
Output Capacitance	C_{OUT}	7			pF	

TIMING DIAGRAM-READ CYCLE TO TIME CHIP ROM/RAM\=GND



TIMING DIAGRAM-WRITE CYCLE TO TIME CHIP ROM/RAM\=GND



AC ELECTRICAL CHARACTERISTICS ROM/RAM\=V_{CCO} (0°C to 70°C; V_{CC} = 5V ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
CE\ Access Time	t_{CO}			200	ns	
OE\ Access Time	t_{OE}			200	ns	
CE\ to Output in Low Z	t_{COE}	10			ns	
OE\ to Output in Low Z	t_{OEE}	10			ns	
CE\ to Output in High Z	t_{OD}			100	ns	
OE\ to Output in High Z	t_{ODO}			100	ns	
Address Setup Time	t_{AS}	20			ns	
Address Hold Time	t_{AH}			10	ns	
Read Recovery	t_{RR}	50			ns	
Write Cycle Time	t_{WC}	250			ns	
CE\ Pulse Width	t_{CW}	170			ns	
OE\ Pulse Width	t_{OW}	170			ns	
Write Recovery	t_{WR}	50			ns	4
Data Setup Time	t_{DS}	100			ns	5
Data Hold Time	t_{DH}	10			ns	5
RST\ Pulse Width	t_{RST}	200			ns	
CE\ Propagation Delay	t_{PD}	5	10	20	ns	2, 3
CE\ High to Power Fail	t_{PF}			0	ns	

(0°C to 70°C, V_{CC} < 4.5V)

Recovery at Power-Up	t_{REC}			2	ms	
V_{CC} Slew Rate 4.5 - 3.0V	t_F	0			ms	

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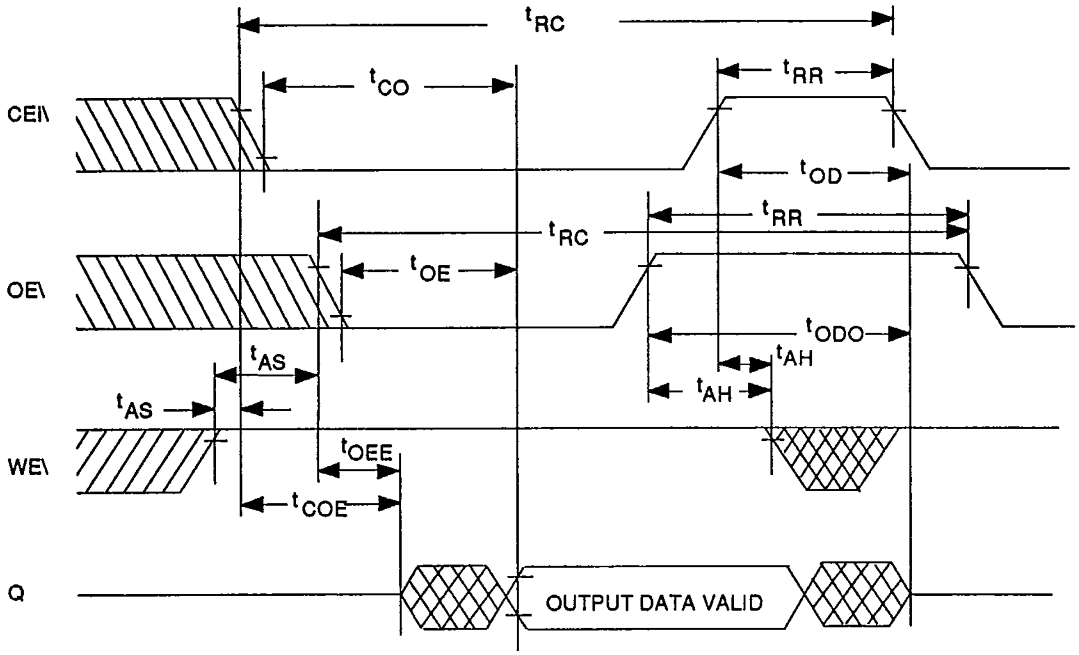
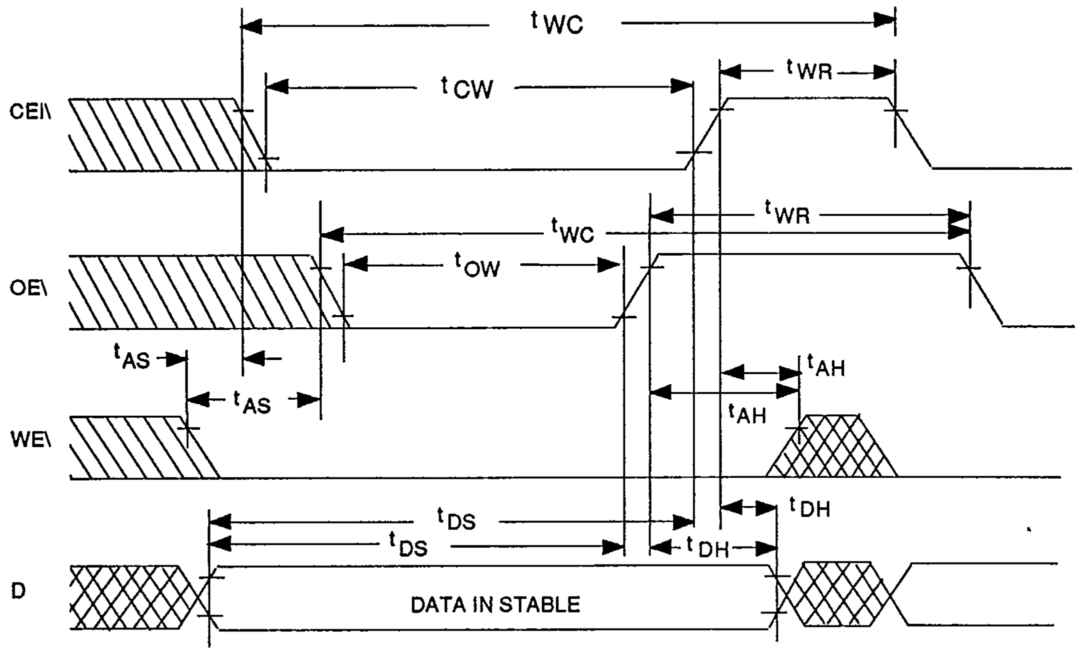
TIMING DIAGRAM-READ CYCLE ROM/RAM\=V_{CCO}



TIMING DIAGRAM-WRITE CYCLE ROM/RAM\=V_{CCO}



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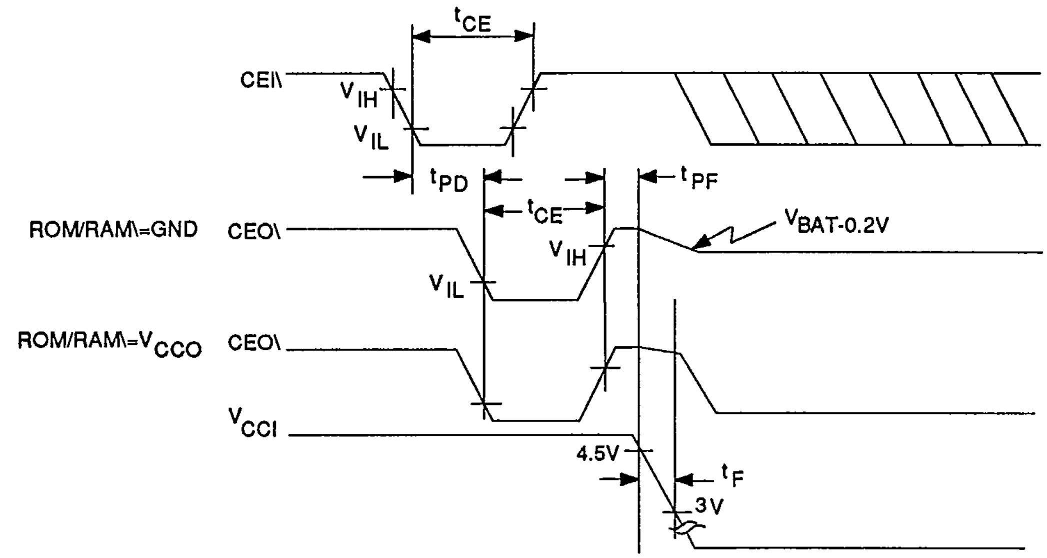
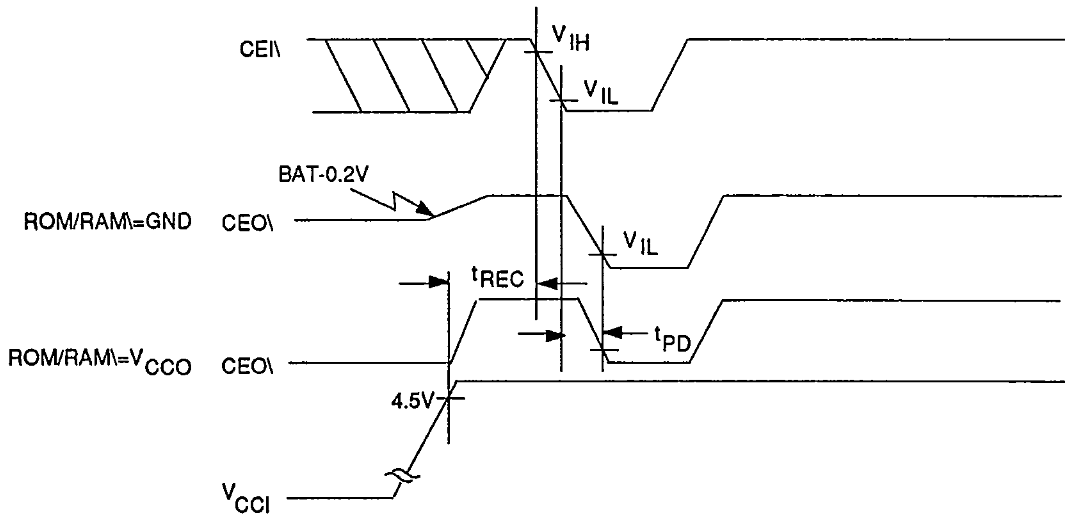
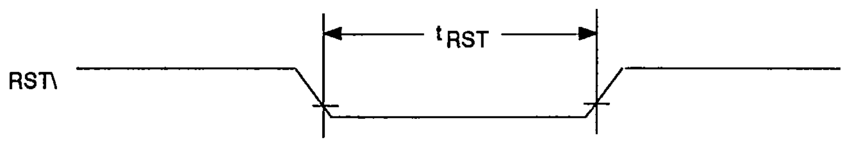
TIMING DIAGRAM--POWER-DOWN



TIMING DIAGRAM--POWER-UP



TIMING DIAGRAM--RESET FOR TIME CHIP



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NOTES

1. All voltages are referenced to ground.
2. Measured with load shown in Figure 6.
3. Input pulse rise and fall times equal 10ns.
4. t_{WR} is a function of the latter occurring edge of WE\ or CE\ in RAM mode, or OE\ or CE\ in ROM mode.
5. t_{DH} and t_{DS} are functions of the first occurring edge of WE\ or CE\ in RAM mode, or OE\ or CE\ in ROM mode.
6. Measured without RAM connected.
7. Trip point voltage for power-fail detect. $V_{TP} = 1.26 \times V_{BAT}$. For 10% V_{CC}= 5V ± 10% operation V_{BAT} = 3.5V max.; for 5% operation V_{BAT} = 3.7V max.
8. I_{CC01} is the maximum average load current the DS1215 can supply to memory.
9. Applies to CEO\ with the ROM/RAM\ pin grounded. When the ROM/RAM\ pin is connected to V_{CCO}, CEO\ will go to a low level as V_{CCI} falls below V_{BAT}.
10. I_{CC02} is the maximum average load current that the DS1215 can supply to memory in the battery backup mode.
11. Applies to all input pins except RST\. RST\ is pulled internally to V_{CCI}.

OUTPUT LOAD Figure 6