

To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M62367GP

3V TYPE 8-BIT 8CH D-A CONVERTER WITH BUFFER AMPLIFIERS

DESCRIPTION

The M62367GP is a CMOS semiconductor IC has 8 channels of 8-bit D-A converter. It is operable with a low supply voltage between 2.7~3.6V, and is easy to use due to serial data input, and 3-pin (DI, CLK, LD) connection with microcomputer.

The IC also contains Do pin terminal, enabling cascade connection, and therefore is suitable for automatic control in combination with a microcomputer.

FEATURES

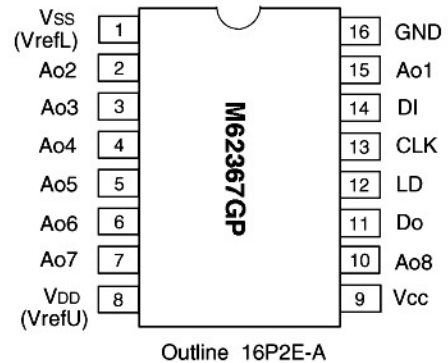
- Operable with a low voltage between 2.7~3.6V
- 12-bit serial data input (connected via 3 pins: DI, CLK, LD)
- 8 channels of R-2R and segment type high-performance 8-bit D-A converters
- 8 buffer operational amplifiers with full swing of output voltage between Vcc and GND.
- High oscillation stability against the capacitive load of buffer operational amplifiers.

APPLICATION

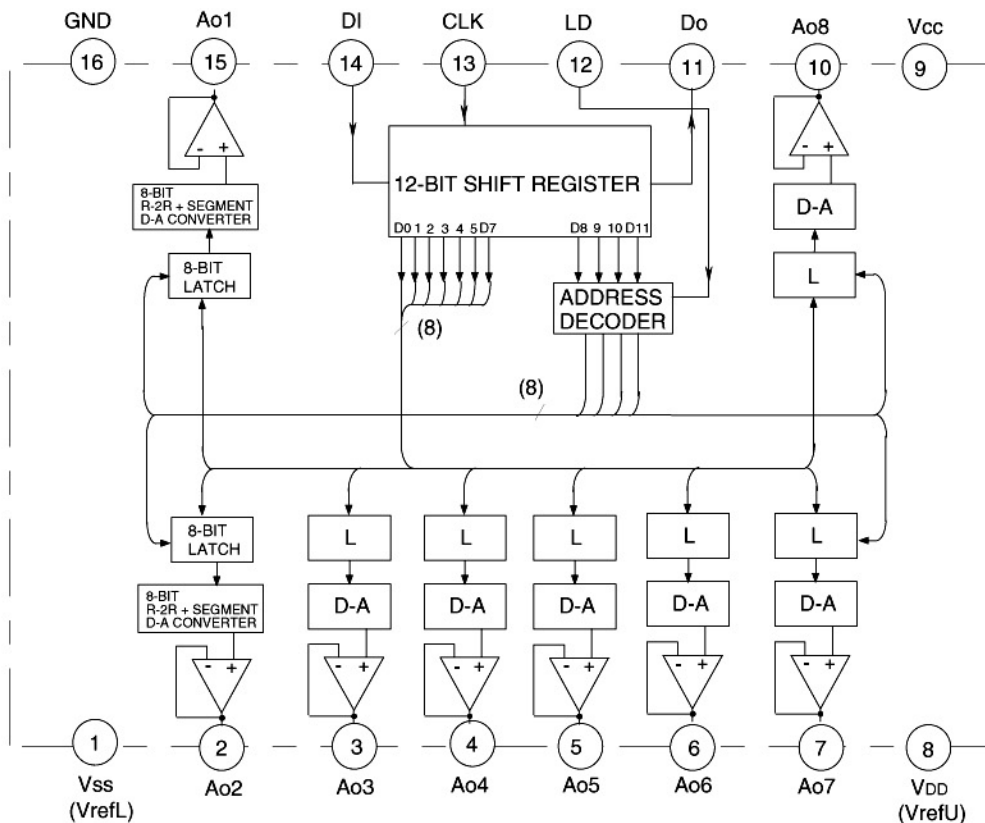
Digital-analog conversion in industrial or home-use electronic equipment.

Automatic control in combination with EEPROM and microcomputer (Substitute for conventional semi-fixed resistor)

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM



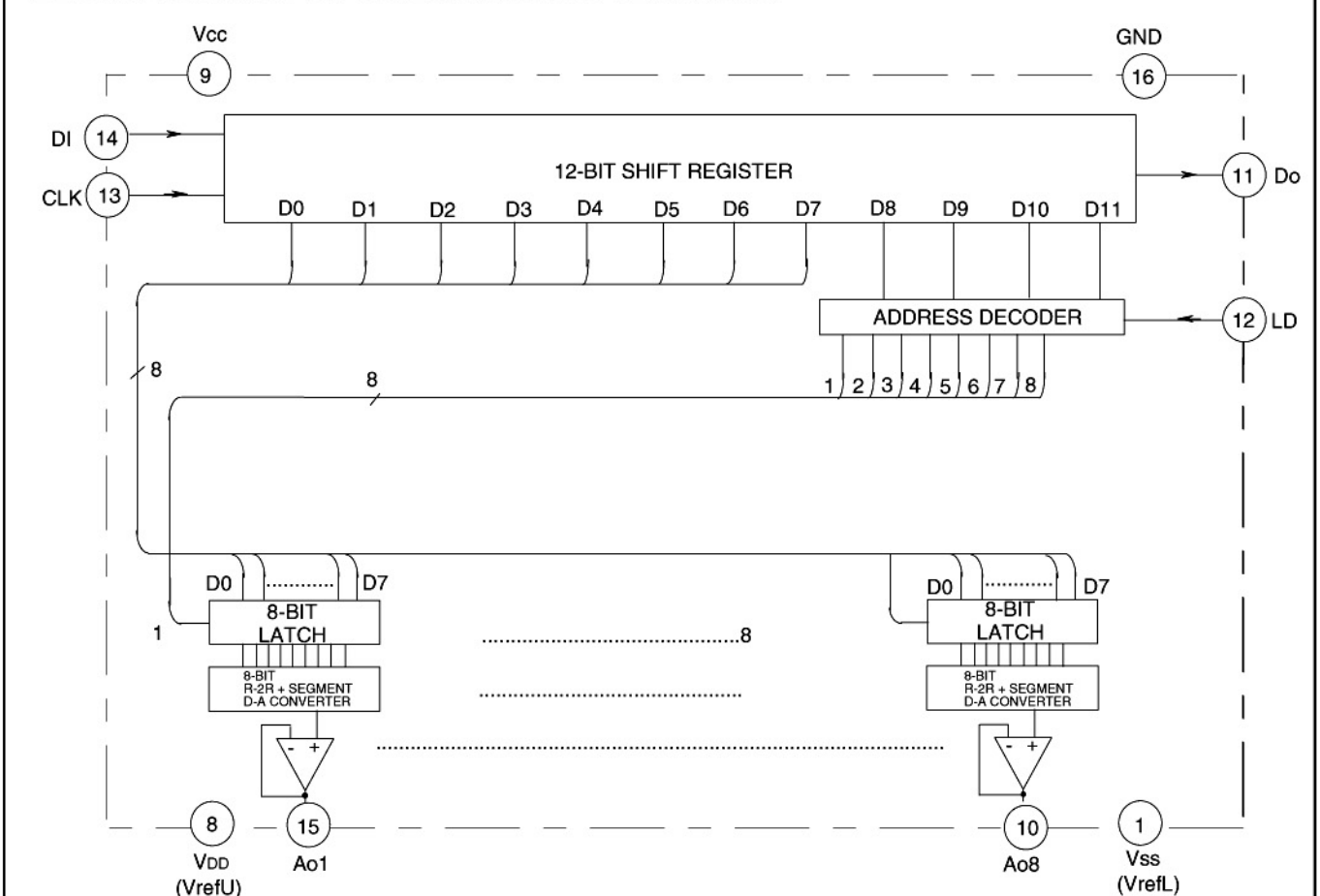
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EXPLANATION OF TERMINALS

Pin No.	Symbol	Function
⑭	DI	Serial data input terminal to input 12-bit long serial data
⑪	Do	Terminal to output MSB data of 12-bit shift register
⑬	CLK	Shift clock input terminal. Input signal at DI pin is input to 12-bit shift register at rise of shift clock pulse
⑫	LD	When H-level signal is input to this terminal. The value stored in 12-bit shift register is loaded in decoder and D-A converter output register
⑮	Ao1	8-bit D-A converter output terminal
②	Ao2	
③	Ao3	
④	Ao4	
⑤	Ao5	
⑥	Ao6	
⑦	Ao7	
⑩	Ao8	
⑨	Vcc	Power supply terminal
⑯	GND	GND terminal
⑧	VDD	D-A converter upper reference voltage input terminal
①	VSS	D-A converter lower reference voltage input terminal

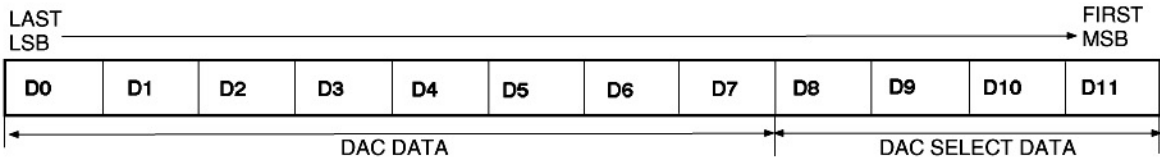
BLOCK DIAGRAM FOR EXPLANATION OF TERMINALS



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DIGITAL DATA FORMAT

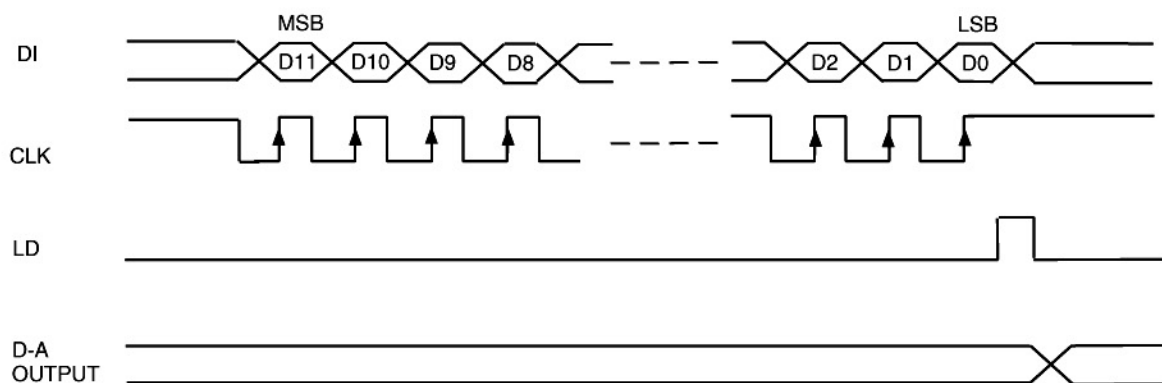


D0	D1	D2	D3	D4	D5	D6	D7	D-A output
0	0	0	0	0	0	0	0	$(V_{refU}-V_{refL}) / 256 \times 1 + V_{refL}$
1	0	0	0	0	0	0	0	$(V_{refU}-V_{refL}) / 256 \times 2 + V_{refL}$
0	1	0	0	0	0	0	0	$(V_{refU}-V_{refL}) / 256 \times 3 + V_{refL}$
1	1	0	0	0	0	0	0	$(V_{refU}-V_{refL}) / 256 \times 4 + V_{refL}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	1	1	$(V_{refU}-V_{refL}) / 256 \times 255 + V_{refL}$
1	1	1	1	1	1	1	1	V_{refU}

D8	D9	D10	D11	DAC selection
0	0	0	0	Don't care
0	0	0	1	Ao1 selection
0	0	1	0	Ao2
0	0	1	1	Ao3
0	1	0	0	Ao4
0	1	0	1	Ao5
0	1	1	0	Ao6
0	1	1	1	Ao7
1	0	0	0	Ao8
1	0	0	1	Don't care
1	0	1	0	Don't care
1	0	1	1	Don't care
1	1	0	0	Don't care
1	1	0	1	Don't care
1	1	1	0	Don't care
1	1	1	1	Don't care

* $V_{refU}=V_{DD}$
 $V_{refL}=V_{SS}$

TIMING CHART (MODEL)



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.3~+7.0	V
V _{DD}	Upper reference voltage of D-A converter		-0.3~+7.0	V
V _{IN}	Input voltage		-0.3~V _{CC} +0.3	V
V _O	Output voltage		-0.3~V _{CC} +0.3	V
P _d	Power dissipation		150	mW
T _{opr}	Operating temperature		-20~+85	°C
T _{stg}	Storage temperature		-40~+125	°C

ELECTRICAL CHARACTERISTICS

Digital part(V_{CC},V_{refU}=+3V±10%, V_{CC}≥V_{refU},GND,V_{refL}=0V,T_a=-20 ~ +85°C,unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V _{CC}	Supply voltage		2.7	3.0	3.6	V
I _{CC}	Circuit current	CLK=1MHz operation,V _{CC} =3V,I _{AO} =0μA			3.5	mA
I _{ILK}	Input leak current	V _{IN} =0~V _{CC}	-10		10	μA
V _{IL}	Input low voltage				0.2V _{CC}	V
V _{IH}	Input high voltage		0.8V _{CC}			V
V _{OL}	Output low voltage	I _{OL} =2.5mA			0.4	V
V _{OH}	Output high voltage	I _{OH} =-400μA	V _{CC} -0.4			V

Analog part(V_{CC},V_{refU}=+3V±10%, V_{CC}≥V_{refU},GND,V_{refL}=0V,T_a=-20 ~ +85°C,unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I _{refU}	Current dissipation	V _{refU} =3V,V _{refL} =0V Data condition:maximum current		1.4	2.5	mA
V _{refU}	D-A converter upper reference voltage range	Reference voltage can not always be set to any value in this range,because it is restricted to the buffer amplifier output voltage range	0.7V _{CC}		V _{CC}	V
V _{refL}	D-A converter lower reference voltage range		GND		0.3V _{CC}	V
V _{AO}	Buffer amplifier output driver voltage range	I _{AO} =±100μA	0.1		V _{CC} -0.1	V
		I _{AO} =+500μA -200μA	0.2		V _{CC} -0.2	V
I _{AO}	Buffer amplifier output voltage range	Upper saturation voltage=0.4V Lower saturation voltage=0.4V	-0.3		1	mA
SDL	Differential nonlinearity error	V _{CC} =2.760V	-1.0		1.0	LSB
SL	Nonlinearity error	V _{refU} =2.610V	-1.5		1.5	LSB
S _{ZERO}	Zero code error	V _{refL} =0.050V(10mV/LSB)	-2		2	LSB
S _{FULL}	Full scale error	Without load(I _{AO} =±0)	-2		2	LSB
C _O	Output capacitive load				0.1	μF
R _O	Buffer amplifier output impedance			5		Ω

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AC CHARACTERISTICS($V_{CC}, V_{refU}=+3V\pm 10\%$, $V_{CC}\geq V_{refU}, GND, V_{refL}=0V, T_a=-20\sim +85^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
tCKL	Clock "L" pulse width		200			ns
tCKH	Clock "H" pulse width		200			ns
tCR	Clock rise time				200	ns
tCF	Clock fall time				200	ns
tDCH	Data set up time		30			ns
tCHD	Data hold time		60			ns
tCHL	LD set up time		200			ns
tLDC	LD hold time		100			ns
tLDH	LD "H" pulse duration		100			ns
tDo	Data output delay time	$C_L=100pF$	70		350	ns
tLDD	D-A output setting time	$C_L\geq 100pF, V_{AO}: 0.1\sim 2.6V$ The time until the output becomes the final value of 1/2 LSB			300	μs

TIMING CHART

