

# HD74LS373 ● Octal D-type Transparent Latches (with three-state outputs)

The HD74LS373, 8-bit register features totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide this register with the capacity of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

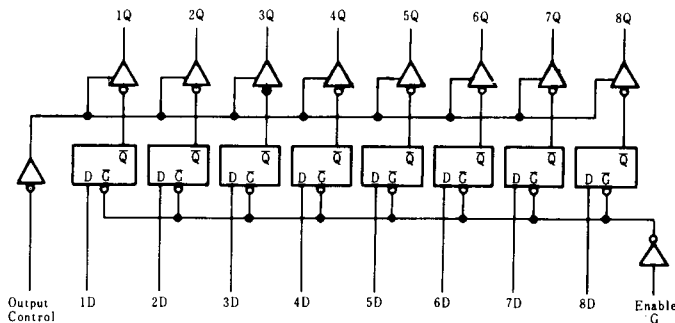
The eight latches are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was setup.

## ■ FUNCTION TABLE

| Inputs         |          |   | Output |
|----------------|----------|---|--------|
| Output control | Enable G | D | Q      |
| L              | H        | H | H      |
| L              | H        | L | L      |
| L              | L        | X | $Q_0$  |
| H              | X        | X | Z      |

Notes: H = high level, L = low level,  
X = irrelevant  
 $Q_0$  = level of Q before the indicated steady-state input conditions were established.  
Z = off (high-impedance) state of a three-state output

## ■ BLOCK DIAGRAM

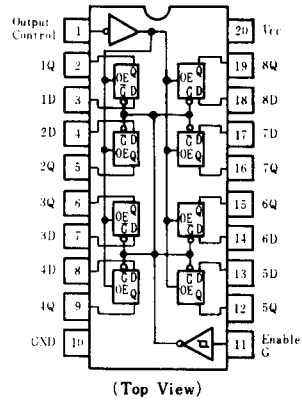


## ■ RECOMMENDED OPERATING CONDITIONS

| Item               | Symbol    | min   | typ  | max  | Unit |
|--------------------|-----------|-------|------|------|------|
| Supply voltage     | $V_{CC}$  | 4.75  | 5.00 | 5.25 | V    |
| Output voltage     | $V_{OH}$  | —     | —    | 5.5  | V    |
| Output current     | $I_{OH}$  | —     | —    | -2.6 | mA   |
|                    | $I_{OL}$  | —     | —    | 24   | mA   |
| Enable pulse width | "H" level | $t_w$ | 15   | —    | ns   |
|                    | "L" level | $t_w$ | 15   | —    | ns   |
| Data setup time    | $t_{su}$  | 5 ↓   | —    | —    | ns   |
| Data hold time     | $t_h$     | 25 ↓  | —    | —    | ns   |

Note) ↓ : The arrow indicates the falling edge of clock pulse.

## ■ PIN ARRANGEMENT



# HD74LS373

### ■ ELECTRICAL CHARACTERISTICS ( $T_a = -20 \sim +75^\circ\text{C}$ )

| Item                         | Symbol    | Test Conditions                                                      |               | min | typ* | max  | Unit    |    |
|------------------------------|-----------|----------------------------------------------------------------------|---------------|-----|------|------|---------|----|
| Input voltage                | $V_{IH}$  |                                                                      |               | 2.0 | --   | —    | V       |    |
|                              | $V_{IL}$  | Data inputs                                                          |               | —   | --   | 0.7  | V       |    |
|                              |           | G, Output control inputs                                             |               | —   | --   | 0.8  |         |    |
| Output voltage               | $V_{OH}$  | $V_{CC}=4.75V$ , $V_{IH}=2V$ , $V_{IL}=V_{IL\max}$ , $I_{OH}=-2.6mA$ |               | 2.4 | —    | —    | V       |    |
|                              | $V_{OL}$  | $V_{CC}=4.75V$ , $V_{IH}=2V$ ,<br>$V_{IL}=V_{IL\max}$                | $I_{OL}=12mA$ | —   | —    | 0.4  | V       |    |
|                              |           |                                                                      | $I_{OL}=24mA$ | —   | —    | 0.5  |         |    |
|                              |           |                                                                      |               |     |      |      |         |    |
| Off-state output current     | $I_{OZH}$ | $V_{CC}=5.25V$ , $V_{IH}=2V$                                         | $V_O=2.7V$    | —   | —    | 20   | $\mu A$ |    |
|                              | $I_{OZL}$ |                                                                      | $V_O=0.4V$    | —   | —    | -20  |         |    |
|                              |           |                                                                      |               |     |      |      |         |    |
| Input current                | $I_{IH}$  | $V_{CC}=5.25V$ , $V_I=2.7V$                                          |               | —   | —    | 20   | $\mu A$ |    |
|                              | $I_{IL}$  | $V_{CC}=5.25V$ , $V_I=0.4V$                                          |               | —   | —    | -0.4 | mA      |    |
|                              | $I_I$     | $V_{CC}=5.25V$ , $V_I=7V$                                            | —             | —   | 0.1  | mA   |         |    |
|                              |           |                                                                      | —             | —   |      |      |         |    |
| Short-circuit output current | $I_{OS}$  | $V_{CC}=5.25V$                                                       |               | -30 | —    | -130 | mA      |    |
| Supply current               | $I_{CC}$  | $V_{CC}=5.25V$ , $V_I=4.5V$ (Output control)                         |               |     | —    | 24   | 40      | mA |
| Input clamp voltage          | $V_{IK}$  | $V_{CC}=4.75V$ , $I_{IN}=-18mA$                                      |               |     | —    | —    | -1.5    | V  |

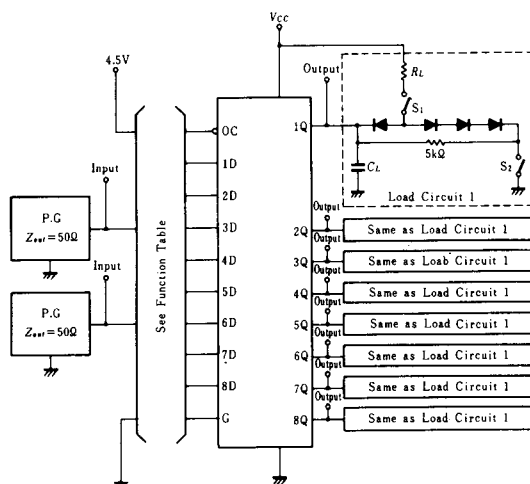
\*  $V_{CC}=5V, T_a=25^{\circ}C$

### ■ SWITCHING CHARACTERISTICS ( $V_{CC}=5V$ , $T_a=25^{\circ}C$ )

| Item                   | Symbol    | Input | Output | Test Conditions                                | min | typ | max | Unit |
|------------------------|-----------|-------|--------|------------------------------------------------|-----|-----|-----|------|
| Propagation delay time | $t_{PLH}$ | D     | Q      | $C_L = 45\text{pF}$<br>$R_L \approx 667\Omega$ | —   | 12  | 18  | ns   |
|                        | $t_{PHL}$ |       |        |                                                | —   | 12  | 18  |      |
|                        | $t_{PLH}$ | G     | Q      |                                                | —   | 20  | 30  |      |
|                        | $t_{PHL}$ |       |        |                                                | —   | 18  | 30  |      |
| Output enable time     | $t_{ZH}$  | OC    | Q      |                                                | —   | 15  | 28  |      |
|                        | $t_{ZL}$  |       |        |                                                | —   | 25  | 36  |      |
| Output disable time    | $t_{HZ}$  | OC    | Q      | $C_L = 5\text{pF}$                             | —   | 12  | 20  |      |
|                        | $t_{LZ}$  |       |        | $R_L = 667\Omega$                              | —   | 15  | 25  |      |

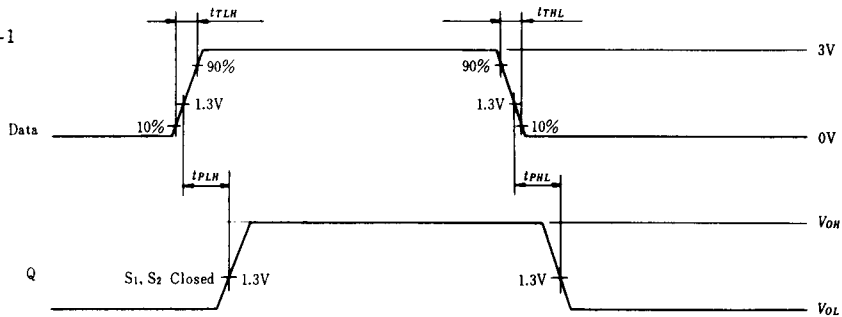
## ■ TESTING METHOD

### Test Circuit



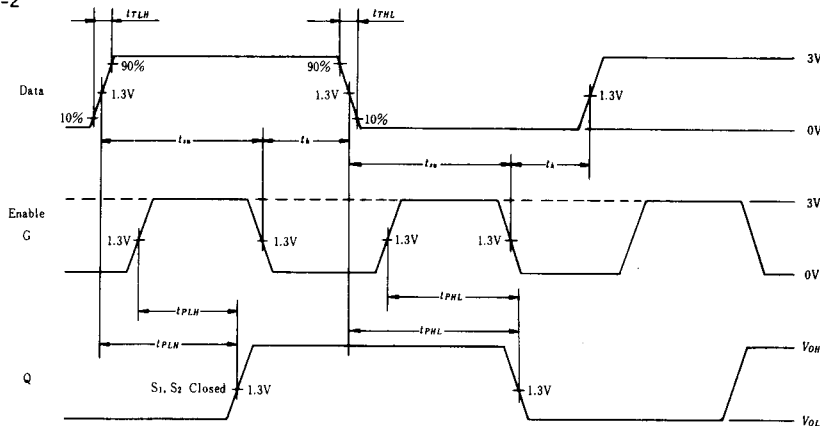
Notes: 1.  $C_L$  includes probe jig capacitance.  
2. All diodes are 1S2074 (H).

Waveform-1



Notes: Input pulse;  $t_{TLH} \leq 15\text{ns}$ ,  $t_{THL} \leq 6\text{ns}$ ,  $PRR = 1\text{MHz}$ , duty cycle 50%

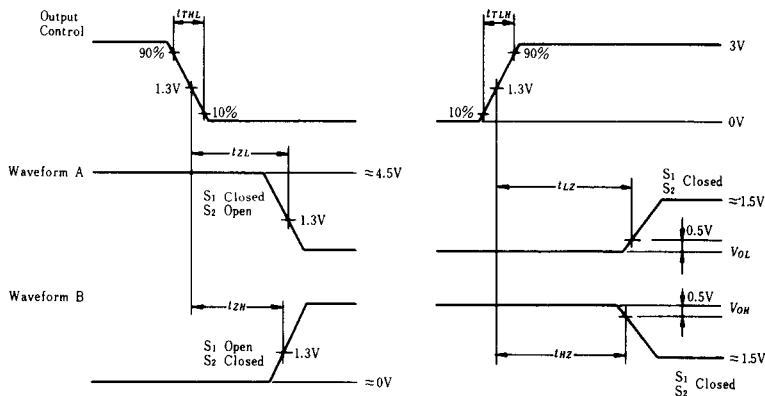
Waveform-2



Note: Enable input pulse;  $t_{TLH} \leq 15\text{ns}$ ,  $t_{THL} \leq 6\text{ns}$ ,  $PRR = 1\text{MHz}$

Data input pulse;  $t_{TLH} \leq 15\text{ns}$ ,  $t_{THL} \leq 6\text{ns}$ ,  $PRR = 1\text{MHz}$ , G input is high.

Waveform-3



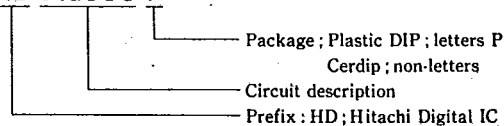
- Notes:
1. Input pulse;  $t_{TLH} \leq 15\text{ns}$ ,  $t_{THL} \leq 6\text{ns}$ ,  $PRR = 1\text{MHz}$ , duty cycle 50%
  2. Waveform A is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform B is for an output with internal conditions such that the output is high except when disabled by the output control.

# PACKAGING INFORMATION

T-90-20

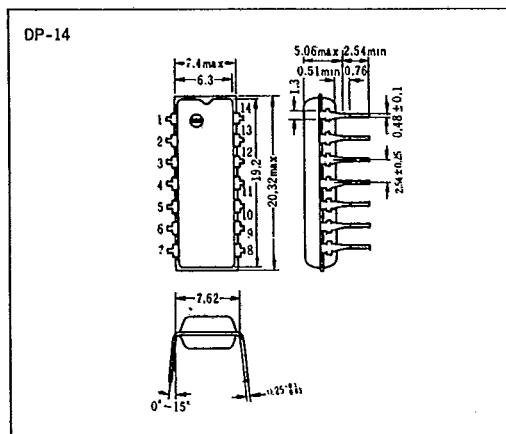
Factory orders for circuits described in this databook should include a three-part type number as explained in the following example.

## HD 74LS00 P

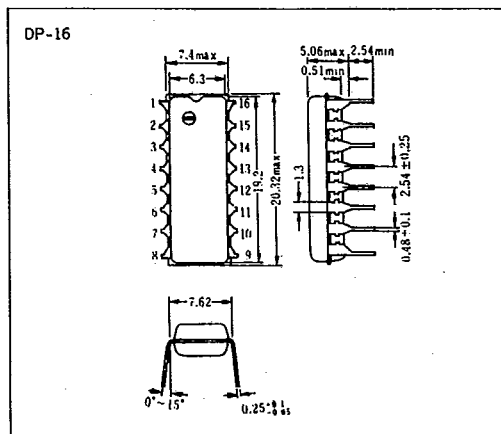


### ■ Plastic DIP

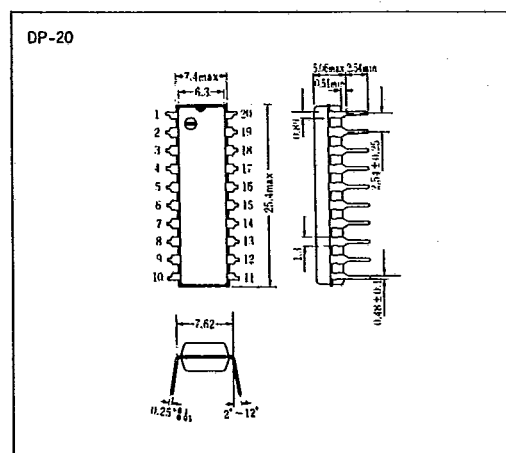
#### ● 14 Pin



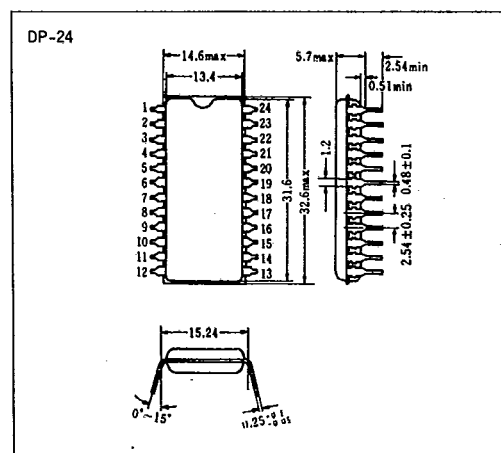
#### ● 16 Pin



#### ● 20 Pin



#### ● 24 Pin



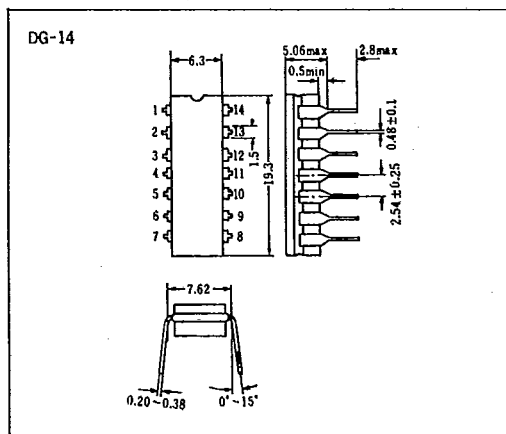
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T-90-20

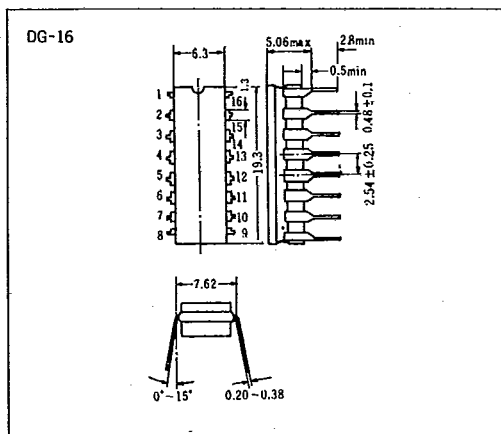
# PACKAGING INFORMATION

## ■Cerdip

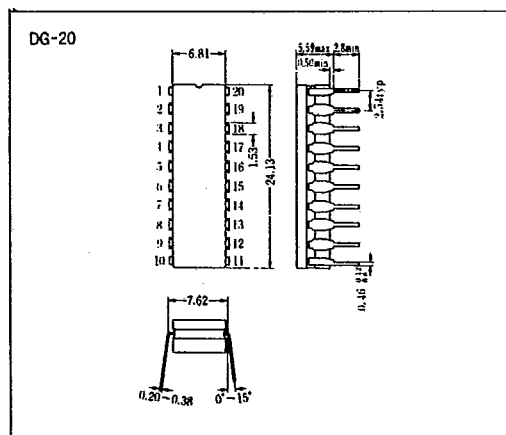
### ●14 Pin



### ●16 Pin



### ●20 Pin



### ●24 Pin

