

# THREE OUTPUTS FACTORY PROGRAMMABLE CLOCK GENERATOR

## Features

- Generates up to 3 CMOS clock outputs from 3 to 200 MHz
- Accepts crystal or reference clock input
  - 3 to 166 MHz reference clock input
  - 8 to 48 MHz crystal input
- Programmable FSEL, SSEL, SS0N, PD, and OE input functions
- Low power dissipation
- Separate voltage supply pins
  - $V_{DD} = 2.5$  to  $3.3$  V
  - $V_{DD0} = 1.8$  to  $3.3$  V ( $V_{DD0} \leq V_{DD}$ )
- 0.25% to 1.0% Spread Spectrum (Center Spread)
- Low cycle-cycle jitter
- Programmable output rise and fall times
- Ultra small 8-pin TDFN package (1.4 x 1.6 mm)

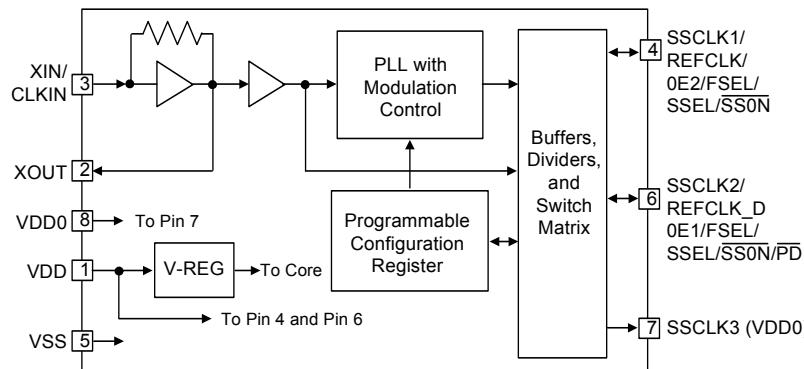
## Applications

- Crystal/XO replacement
- EMI reduction
- Portable devices
- Digital still camera
- IP phone
- Smart meter

## Description

The factory programmable Si51211 is a low power, small footprint and frequency flexible programmable clock generator targeting low power, low cost and high volume consumer and embedded applications. The device operates from a single crystal or an external clock source and generates 1 to 3 outputs up to 200 MHz. They are factory programmed to provide customized output frequencies, control inputs and ac parameter tuning like output drive strength that are optimized for customer board condition and application requirements. A separate VDD0 supply pin supports clock output at a different voltage level.

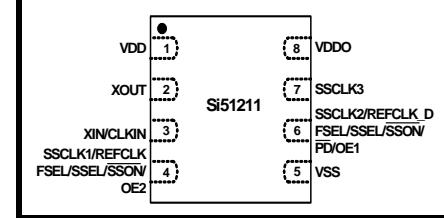
## Functional Block Diagram



### Ordering Information:

See page 9.

## Pin Assignments



Patents pending



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## 1. Electrical Specifications

**Table 1. DC Electrical Specifications**

( $V_{DD} = 2.5 \text{ V} \pm 5\%$ , or  $V_{DD} = 3.3 \text{ V} \pm 10\%$ ,  $T_A = 0 \text{ to } 70^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	$V_{DD}$	$V_{DD}=3.3 \text{ V} \pm 10\%$	2.97	3.3	3.63	V
		$V_{DD}=2.5 \text{ V} \pm 5\%$	2.375	2.5	2.625	V
	$V_{DDO}$	$V_{DDO} \leq V_{DD}$	1.71	—	3.6	V
Output High Voltage	$V_{OH}$	$I_{OH} = -4 \text{ mA}$ , $V_{DDX}=V_{DD}$ or $V_{DDO}$	$V_{DDX}-0.5$	—	—	V
Output Low Voltage	$V_{OL}$	$I_{OL} = 4 \text{ mA}$ ,	—	—	0.3	V
Input High Voltage	$V_{IH}$	CMOS level	$0.7 V_{DD}$	—	—	V
Input Low Voltage	$V_{IL}$	CMOS level	—	—	$0.3 V_{DD}$	V
Operating Supply Current	$I_{DD}$	$F_{IN}=12 \text{ MHz}$ , $SSCLK1=12 \text{ MHz}$ , $SSCLK2 =24 \text{ MHz}$ , $C_L=0$ , $V_{DD}=V_{DDO}=3.3 \text{ V}$	—	6	—	mA
Nominal Output Impedance	$Z_O$		—	30	—	$\Omega$
Internal Pull-up/Pull-down Resistor	$R_{PUP}/R_{PD}$	Pin 6	—	150k	—	$\Omega$
Input Pin Capacitance	$C_{IN}$	Input Pin Capacitance	—	3	5	pF
Load Capacitance	$C_L$	Clock outputs $< 166 \text{ MHz}$	—	—	15	pF
		Clock outputs $> 166 \text{ MHz}$	—	—	10	pF

**Table 2. AC Electrical Specifications**(V<sub>DD</sub> = 2.5 V ± 5%, or V<sub>DD</sub> = 3.3 V ± 10%, T<sub>A</sub> = 0 to 70 °C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Frequency Range	F <sub>IN1</sub>	Crystal input	8	—	48	MHz
Input Frequency Range	F <sub>IN2</sub>	Reference clock Input	3	—	166	MHz
Output Frequency Range	F <sub>OUT</sub>	SSCLK1/2/3	3	—	200	MHz
Frequency Accuracy	F <sub>ACC</sub>	Configuration dependent	—	0	—	ppm
Output Duty Cycle	DC <sub>OUT</sub>	Measured at V <sub>DD</sub> /2	45	50	55	%
Input Duty Cycle	DC <sub>IN</sub>	CLKIN, CLKOUT through PLL	30	50	70	%
Output Rise Time	t <sub>r</sub>	C <sub>L</sub> =15 pF, 20 to 80%	—	1	3.0	ns
Output Fall Time	t <sub>f</sub>	C <sub>L</sub> =15 pF, 20 to 80%	—	1	3.0	ns
Period Jitter	PJ <sub>1</sub>	SSCLK1/2/3, three clocks running, V <sub>DD</sub> =3.3 V, CL=15 pF	—	150*	—	ps
Cycle-to-Cycle Jitter	CCJ <sub>1</sub>	SSCLK1/2/3, three clocks running, V <sub>DD</sub> =3.3 V, CL=15 pF	—	100*	—	ps
Power-up Time	t <sub>PU</sub>	Time from 0.9 V <sub>DD</sub> to valid frequencies at all clock outputs	—	1.2	5.0	ms
Output Enable Time	t <sub>OE</sub>	Time from OE raising edge to active at outputs SSCLK1/2 (asynchronous)	—	15	—	ns
Output Disable Time	t <sub>OD</sub>	Time from OE falling edge to active at outputs SSCLK1/2 (asynchronous)	—	15	—	ns

**\*Note:** Jitter performance depends on configuration and programming parameters.

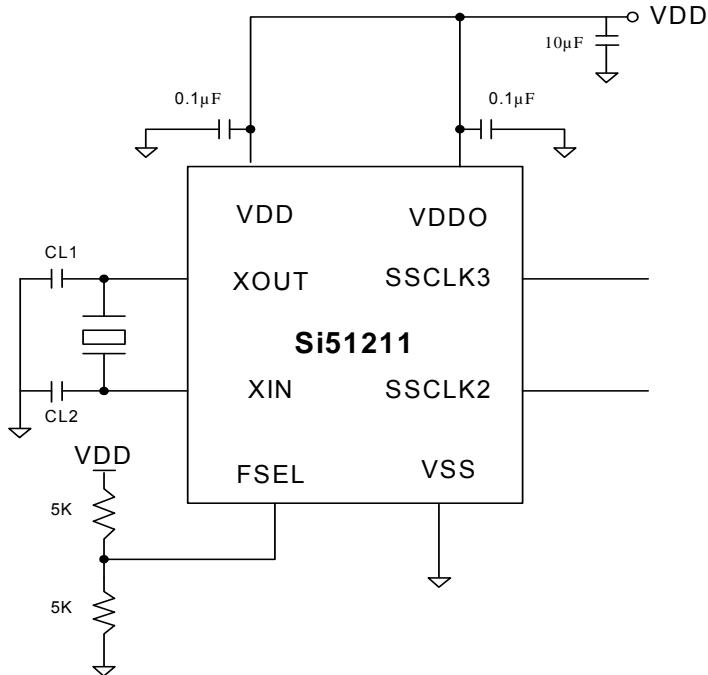
**Table 3. Absolute Maximum Conditions**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Main Supply Voltage	V <sub>DD</sub>		-0.5	—	4.2	V
Input Voltage	V <sub>IN</sub>	Relative to V <sub>SS</sub>	-0.5	—	V <sub>DD</sub> +0.5	V
Temperature, Storage	T <sub>S</sub>	Non-functional	-65	—	150	°C
Temperature, Operating Ambient	T <sub>A</sub>	Functional, C-Grade	0	—	70	°C
ESD Protection (Human Body Model)	ESD <sub>HBM</sub>	JEDEC (JESD 22-A114)	-4000	—	4000	V
ESD Protection (Charge Device Model)	ESD <sub>CDM</sub>	JEDEC (JESD 22-C101)	-1500	—	1500	V
ESD Protection (Machine Model)	ESD <sub>MM</sub>	JEDEC (JESD 22-A115)	-200	—	200	V
Moisture Sensitivity Level	MSL	JEDEC (J-STD-020)		1		

**Note:** While using multiple power supplies, the voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.

## 2. Design Considerations

### 2.1. Typical Application Schematic



### 2.2. Comments and Recommendations

**Decoupling Capacitor:** A decoupling capacitor of  $0.1 \mu\text{F}$  must be used between VDD and VSS on the pins 1 and 8. Place the capacitor on the component side of the PCB as close to the VDD pin as possible. The PCB trace to the VDD pin and to the GND via should be kept as short as possible. Do not use vias between the decoupling capacitor and the VDD pin. In addition, a  $10 \mu\text{F}$  capacitor should be placed between VDD and VSS.

**Series Termination Resistor:** A series termination resistor is recommended if the distance between the outputs (SSCLK or REFCLK pins) and the load is over  $1 \frac{1}{2}$  inch. The nominal impedance of the SSCLK output is about  $30 \Omega$ . Use  $20 \Omega$  resistor in series with the output to terminate  $50 \Omega$  trace impedance and place  $20 \Omega$  resistor as close to the SSCLK output as possible.

**Crystal and Crystal Load:** Only use a parallel resonant fundamental AT cut crystal. **Do not use higher overtone crystals.** To meet the crystal initial accuracy specification (in ppm) make sure that external crystal load capacitor is matched to crystal load specification. To determine the value of CL1 and CL2, use the following formula;

$$C1 = C2 = 2CL - (C_{pin} + C_p)$$

Where: CL is load capacitance stated by crystal manufacturer

C<sub>pin</sub> is the Si51211 pin capacitance ( $4 \text{ pF}$ ).

C<sub>p</sub> is the parasitic capacitance of the PCB traces.

**Example:** If a crystal with CL=12 pF specification is used and C<sub>p</sub>=1 pF (parasitic PCB capacitance on PCB), 19 or 20 pF external capacitors from pins XIN (pin 2) and XOUT (Pin 3) to VSS are required. Users must verify C<sub>p</sub> value.

### 3. Functional Description

#### 3.1. Input Frequency Range

The input frequency range is from 8.0 to 48.0 MHz for crystals and ceramic resonators. If an external clock is used, the input frequency range is from 8.0 to 166.0 MHz.

#### 3.2. Output Frequency Range and Outputs

Up to three outputs can be programmed as SSCLK or REFCLK. SSCLK output can be synthesized to any value from 3 to 200 MHz with spread based on valid input frequency. The spread at SSCLK pins can be stopped by the SSON input control pin. If SSON pin is high (VDD), the frequency at SSCLK pin is synthesized to the nominal value of the input frequency and there is no spread.

REFCLK is the buffered output of the oscillator and is the same frequency as the input frequency without spread. However, REFCLK\_D output is divided by output dividers from 2 to 32. By using only low cost, fundamental mode crystals, the Si51211 can synthesize output frequency up to 200 MHz, eliminating the need for higher order crystals (Xtals) and crystal oscillators (XOs). This reduces the cost while improving the system clock accuracy, performance, and reliability.

#### 3.3. Programmable Modulation Frequency

The spread spectrum clock (SSC) modulation default value is 31.5 kHz. The higher values of up to 62 kHz can also be programmed. Less than 30 kHz modulation frequency is not recommended to stay out of the range audio frequency bandwidth since this frequency could be detected as a noise by the audio receivers within the vicinity.

#### 3.4. Programmable Spread Percent (%)

The spread percent (%) value is programmable from  $\pm 0.25\%$  to  $\pm 1\%$  (center spread) for all SSCLK frequencies. It is possible to program smaller or larger non-standard values of spread percentage. Contact Silicon Labs if these non-standard spread percent values are required in the application.

#### 3.5. SSON or Frequency Select (FSEL)

The Si51211 pin 4 and 6 can be programmed as either SSON to enable or disable the programmed spread percent value or as frequency select (FSEL). If SSON is used, when this pin is pulled high (VDD), the spread is stopped and the frequency is the nominal value without spread. If low (GND), the frequency is the nominal value with the spread.

If FSEL function is used, the output pins can be programmed for different set of frequencies as selected by FSEL. SSCLK value can be any frequency from 3 to 200 MHz, but the spread % is the same percent value. REFCLK is the same frequency as the input reference clock and the REFCLK\_D input clock is divided by 2 to 32 without spread. The set of frequencies in Table 4 is given as an example, using a 48 MHz crystal.

**Table 4. Example Frequencies**

FSEL (Pin 6)	SSCLK1 (Pin 4)
0	66 MHz, $\pm 1\%$
1	33 MHz, $\pm 1\%$

#### 3.6. Power Down (PD) or Output Enable (OE)

The Si51211 pin 6 can be programmed as PD input. Pin 4 and pin 6 can be programmed as OE input. PD turns off both PLL and output buffers whereas OE only disables the output buffers to Hi-Z.

## 4. Pin Descriptions: 8-Pin TDFN

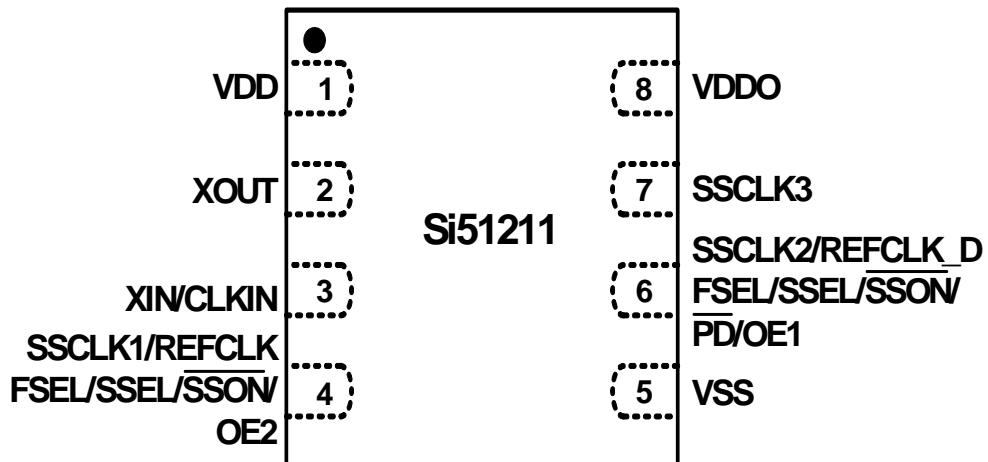
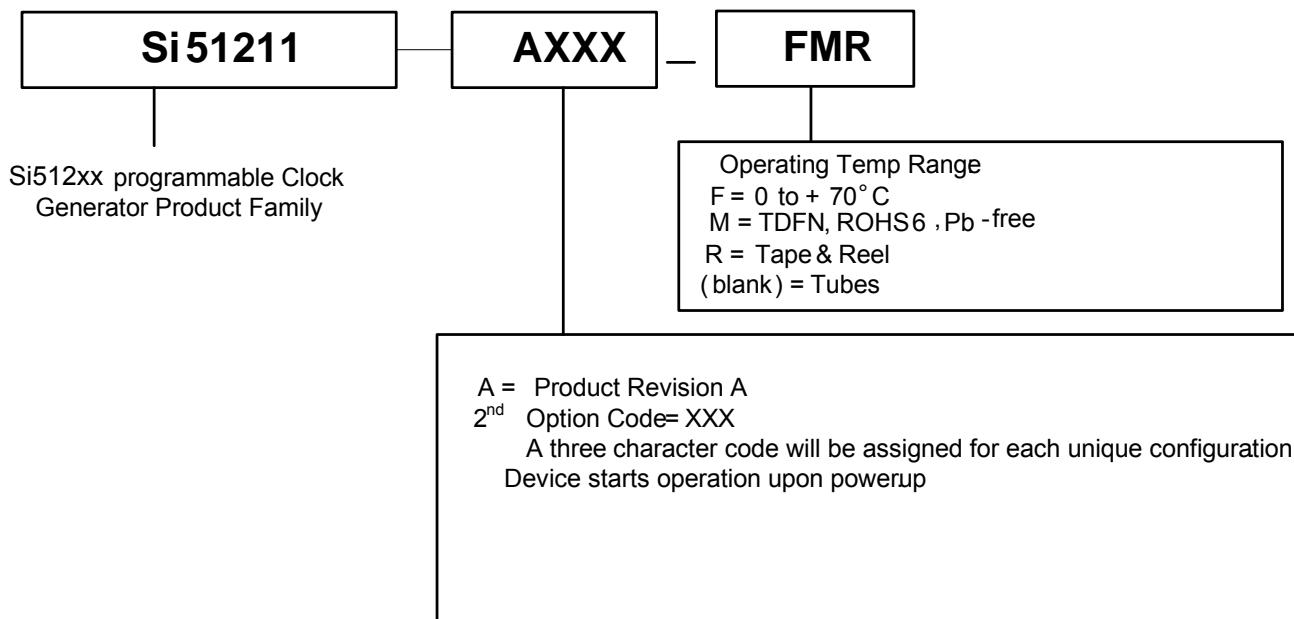


Table 5. Si51211 Pin Descriptions

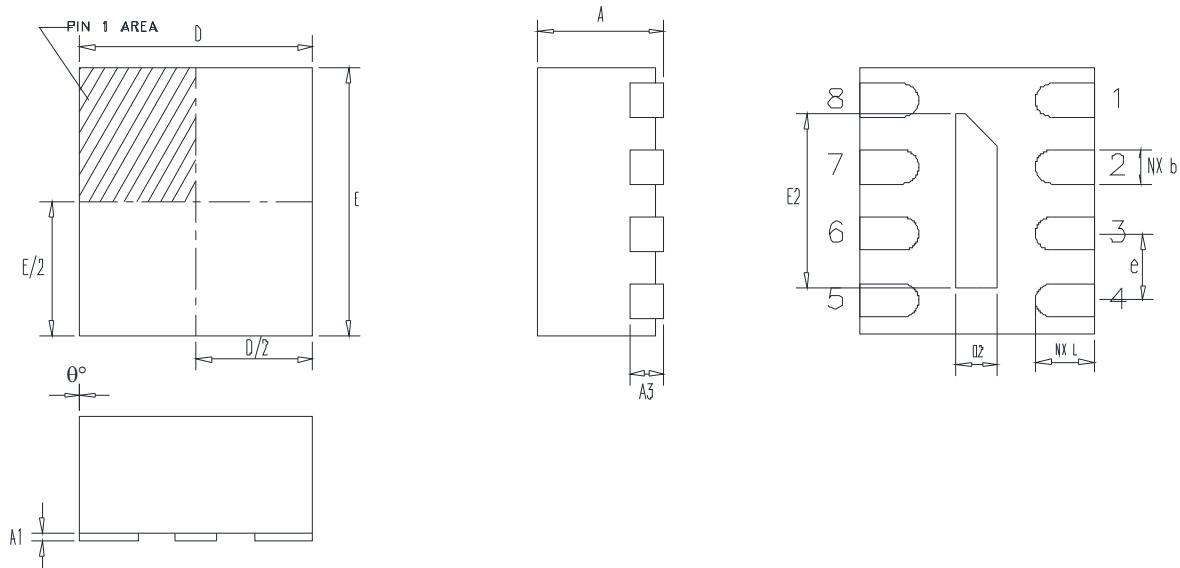
Pin #	Name	Type	Description
1	VDD	PWR	2.5 to 3.3 V power supply.
2	XOUT	O	Crystal output. Leave this pin unconnected (floating) if an external clock input is used.
3	XIN/CLKIN	I	External crystal and clock input.
4	SSCLK1/REFCLK/ FSEL/SSEL/SSON/ OE2	I/O	Programmable SSCLK1 or REFCLK output or MultiFunction control input. The frequency at this pin is synthesized by internal PLL if programmed as SSCLK1 with or without spread. If programmed as REFCLK, output clock is buffered output of crystal or reference clock input. If programmed as MultiFunction control input, it can be OE, FSEL, SSEL and SSON.
5	VSS	GND	Ground.
6	SSCLK2/REFCLK_D/ OE1/FSEL/SSEL/ SSON/PD	I/O	Programmable SSCLK2 or REFCLK_D output or MultiFunction control input. The frequency at this pin is synthesized by internal PLL if programmed as SSCLK2 with or without spread. If programmed as REFCLK_D, output clock is buffered output of crystal or reference clock input divided by 2 to 32. If programmed as MultiFunction control input, it can be OE, PD, FSEL, SSEL and SSON.
7	SSCLK3	O	Programmable SSCLK3 output. The frequency at this pin is synthesized by internal PLL with or without spread. It is power by VDDO pin (pin 8).
8	VDDO	PWR	1.8 to 3.3 V output power supply to SSCLK3 (pin 7) $V_{DDO} \leq V_{DD}$ .

## 5. Ordering Information

Part Number	Package Type	Temperature
Si51211-AxxxFM	8-pin TDFN	Commercial, 0 to 70 °C
Si51211-AxxxFMR	8-pin TDFN—Tape and Reel	Commercial, 0 to 70 °C



## 6. Package Outline: 8-pin TDFN



Dimension	mm		mils	
	Min	Max	Min	Max
A	0.70	0.80	27.56	31.50
A1	0	0.05	D	1.97
A3	0.175	0.225	6.89	8.86
D	1.3	1.5	51.18	59.06
E	1.5	1.7	59.06	66.93
D2	0.20	0.30	7.87	11.81
E2	1.0	1.1	39.37	43.31
theta	0.4	BSC	15.75	BSC
NX b	0.15	0.25	5.91	9.84
NX L	0.25	0.45	9.84	17.72
theta	0*	4*	0*	4*
ND	0			
NE	4			

### Note:

1. SPADE WIDTH, LEAD WIDTH AND LEAD THICKNESS EXCLUSIVE OF SOLDER PLATE
2. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASHES AND BURR DIMENSIONS
3. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
4. WARPAGE SHALL NOT EXCEED 0.10mm.
5. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED, THE TERMINAL#1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

**NOTES:**

## CONTACT INFORMATION

### Silicon Laboratories Inc.

400 West Cesar Chavez

Austin, TX 78701

Tel: 1+(512) 416-8500

Fax: 1+(512) 416-9669

Toll Free: 1+(877) 444-3032

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