

- 5- $\Omega$  Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Bus Hold on Data Inputs/Outputs  
Eliminates the Need for External  
Pullup/Pulldown Resistors

### description

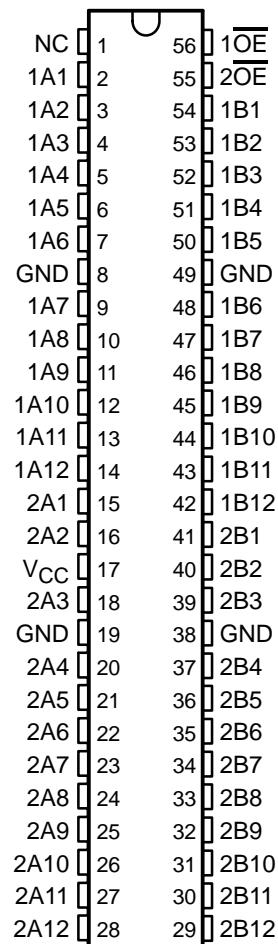
The SN74CBTH16211 provides 24 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as dual 12-bit bus switches with separate output-enable ( $\overline{OE}$ ) inputs. It can be used as two 12-bit bus switches or one 24-bit bus switch. When  $\overline{OE}$  is low, the associated 12-bit bus switch is on, and the A port is connected to the B port. When  $\overline{OE}$  is high, the switch is open, and a high-impedance state exists between the two ports.

Active bus-hold circuitry is provided to hold unused or floating A and B ports at a valid logic level.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



NC – No internal connection

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74CBTH16211DL	CBTH16211
		Tape and reel	SN74CBTH16211DLR	
	TSSOP – DGG	Tape and reel	SN74CBTH16211DGGR	CBTH16211
	TVSOP – DGV	Tape and reel	SN74CBTH16211DGVR	CYH211

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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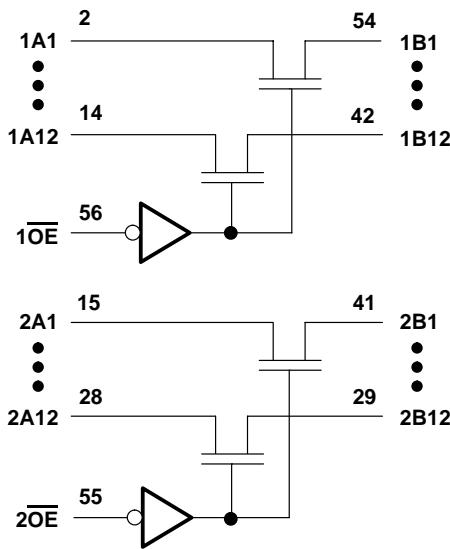
**SN74CBTH16211  
24-BIT FET BUS SWITCH  
WITH BUS HOLD**

SCDS062C – JUNE 1998 – REVISED NOVEMBER 2001

## FUNCTION TABLE (each bus switch)

INPUT <u>OE</u>	FUNCTION
L	A port = B port
H	Disconnect

## logic diagram (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Continuous channel current .....	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
DGG package .....	64°C/W
DGV package .....	48°C/W
DL package .....	56°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JEDEC 51-7.

### **recommended operating conditions (see Note 3)**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4	5.5	V
$V_{IH}$	High-level control input voltage	2		V
$V_{IL}$	Low-level control input voltage		0.8	V
$T_A$	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
$V_{IK}$		$V_{CC} = 4.5 \text{ V}$ , $ I  = -18 \text{ mA}$					-1.2	V
$I_I$	Control inputs	$V_{CC} = 0 \text{ V}$ , $V_I = 5.5 \text{ V}$					$\pm 10$	$\mu\text{A}$
	All inputs	$V_{CC} = 5.5 \text{ V}$ , $V_I = 5.5 \text{ V}$ or GND					$\pm 10$	
$I_{BHL}^{\ddagger}$		$V_{CC} = 4.5 \text{ V}$ , $V_I = 0.8 \text{ V}$			100			$\mu\text{A}$
$I_{BHH}^{\$}$		$V_{CC} = 4.5 \text{ V}$ , $V_I = 2 \text{ V}$			-100			$\mu\text{A}$
$I_{BHLO}^{\parallel}$		$V_{CC} = 5.5 \text{ V}$ , $V_I = 0$ to $5.5 \text{ V}$			500			$\mu\text{A}$
$I_{BHHO}^{\#}$		$V_{CC} = 5.5 \text{ V}$ , $V_I = 0$ to $5.5 \text{ V}$			-500			$\mu\text{A}$
$I_{CC}$		$V_{CC} = 5.5 \text{ V}$ , $I_O = 0$ , $V_I = V_{CC}$ or GND				3		$\mu\text{A}$
$\Delta I_{CC}^{\parallel}$	Control inputs	$V_{CC} = 5.5 \text{ V}$ , One input at $3.4 \text{ V}$ , Other inputs at $V_{CC}$ or GND				2.5		mA
$r_{on}^{\star}$		$V_{CC} = 4 \text{ V}$ , TYP at $V_{CC} = 4 \text{ V}$	$V_I = 2.4 \text{ V}$ , $I_I = 15 \text{ mA}$			14	20	$\Omega$
			$V_I = 0$	$I_I = 64 \text{ mA}$		5	7	
		$V_{CC} = 4.5 \text{ V}$		$I_I = 30 \text{ mA}$		5	7	
		$V_I = 2.4 \text{ V}$	$I_I = 15 \text{ mA}$		8	12		

† All typical values are at  $V_{CC} = 5 \text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

‡ The bus hold circuit can sink at least the minimum low sustaining current at  $V_{IL}$  max.  $I_{BHL}$  should be measured after lowering  $V_{IN}$  to GND and then raising it to  $V_{IL}$  max.

§ The bus hold circuit can source at least the minimum high sustaining current at  $V_{IH}$  min.  $I_{BHH}$  should be measured after raising  $V_{IN}$  to  $V_{CC}$  and then lowering it to  $V_{IH}$  min.

¶ An external driver must source at least  $I_{BHLO}$  to switch this node from low to high.

# An external driver must sink at least  $I_{BHHO}$  to switch this node from high to low.

|| This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

★ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

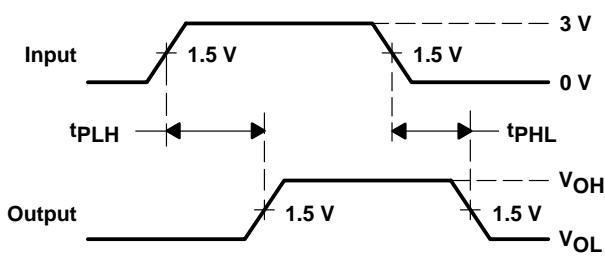
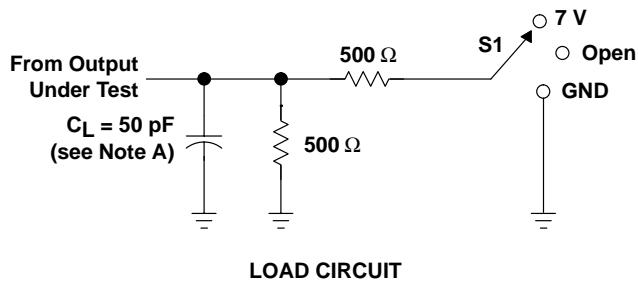
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4 \text{ V}$		$V_{CC} = 5 \text{ V}$ $\pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}^{\square}$	A or B	B or A	0.35		0.25		ns
$t_{en}$	$\overline{OE}$	A or B	9.9		1	9.6	ns
$t_{dis}$	$\overline{OE}$	A or B	9.5		1	8.3	ns

□ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

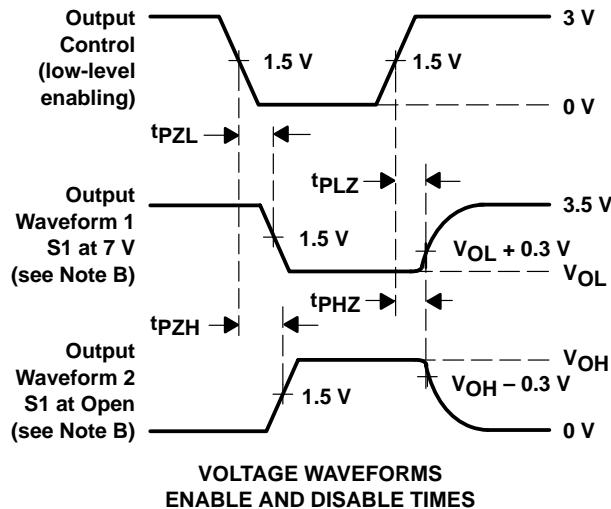
**SN74CBTH16211**  
**24-BIT FET BUS SWITCH**  
**WITH BUS HOLD**

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**PARAMETER MEASUREMENT INFORMATION**



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74CBTH16211DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBTH16211DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTH16211DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTH16211DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTH16211DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

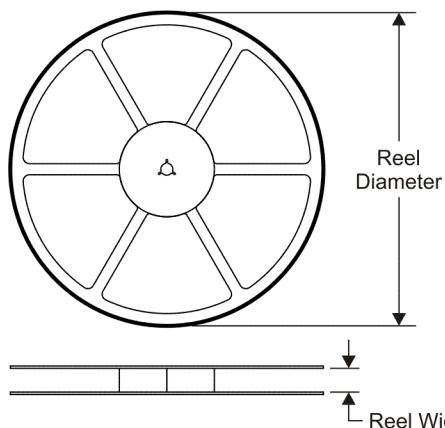
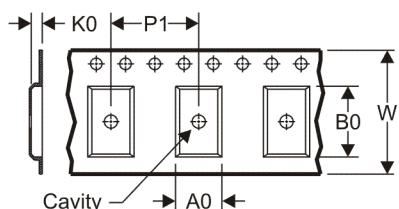
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

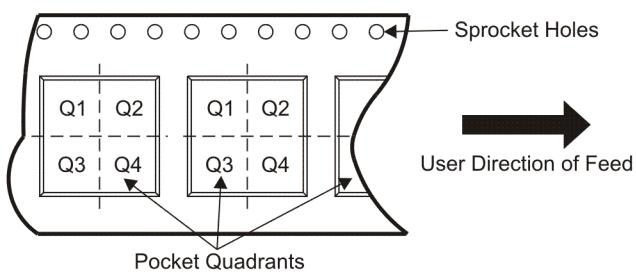
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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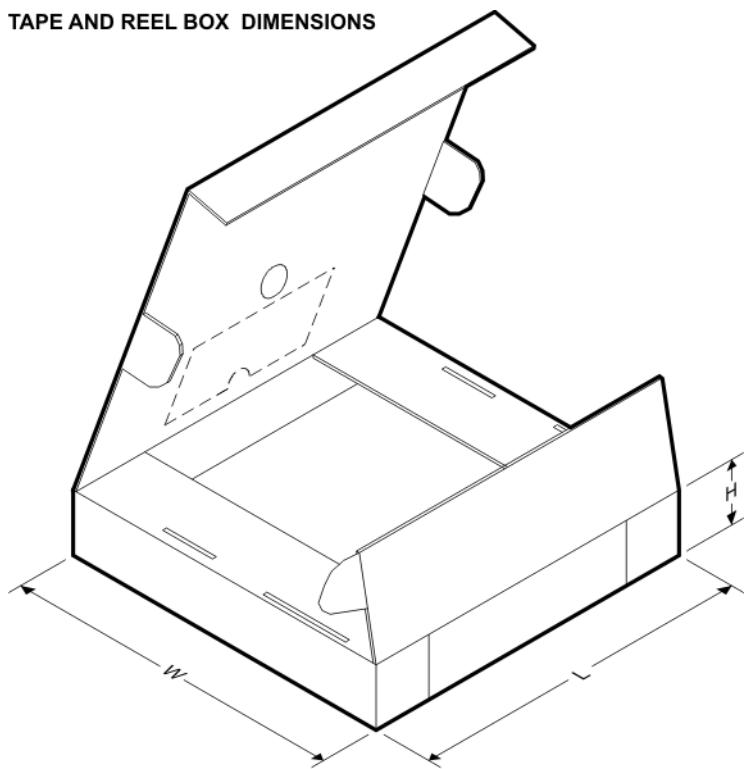
**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTH16211DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

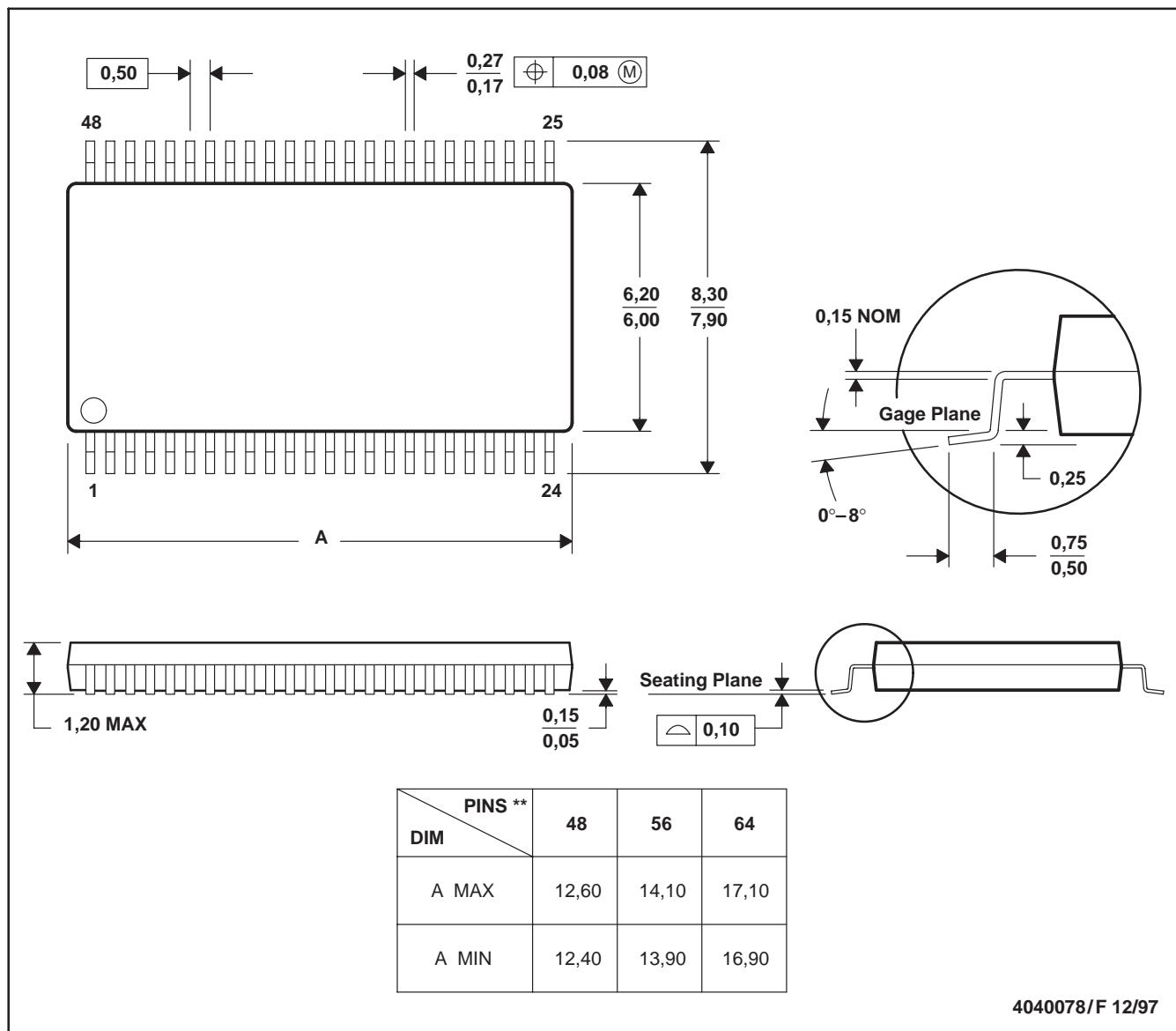
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTH16211DGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

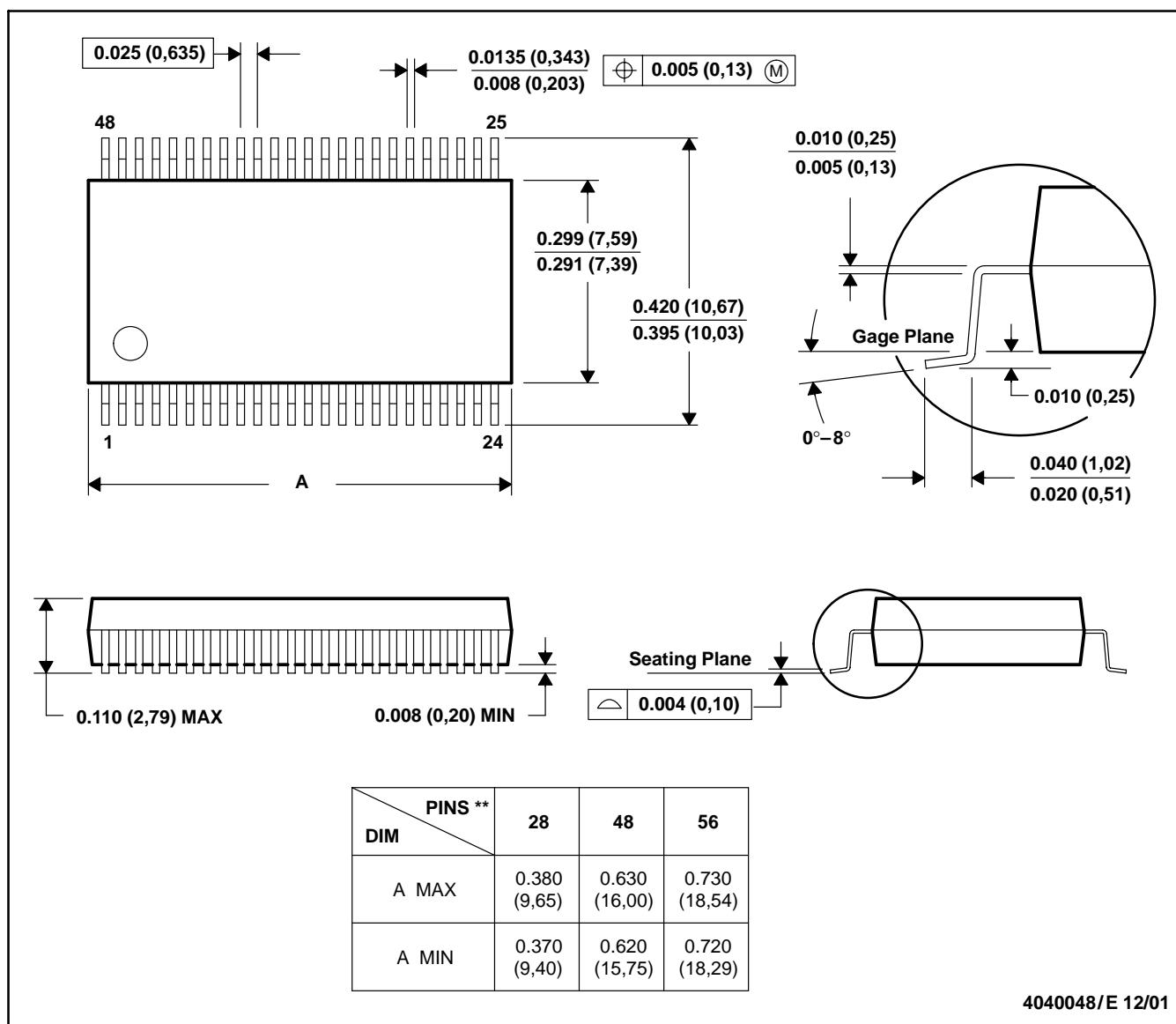


NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

## DL (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

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