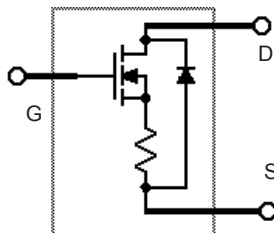


Gate Controlled Current Limiter

IXCP 01N90E
IXCY 01N90E

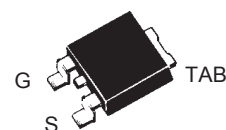
$V_{DSS} = 900 \text{ V}$
 $I_{D(limit)} = 250 \text{ mA}$
 $R_{DS(on)} = 80 \text{ } \Omega$

N-Channel, Enhancement Mode

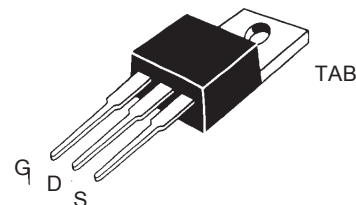


Symbol	Test Conditions	Maximum Ratings	
V _{DSS}	T _J = 25°C to 150°C	900	V
V _{DGR}	T _J = 25°C to 150°C; R _{GS} = 1 MΩ	900	V
V _{GS}	Continuous	±20	V
V _{GSM}	Transient	±30	V
P _D	T _C = 25°C	40	W
T _J		-55 ... +150	°C
T _{JM}		150	°C
T _{stg}		-55 ... +150	°C
T _L	1.6 mm (0.062 in.) from case for 10 s	300	°C
M _d	Mounting torque with 3.5mm screw (TO-220)	0.55/5 Nm/lb.in.	
Weight	TO-251/252 = 1 g, TO-220 = 4 g		

TO-252 (IXCY)



TO-220 (IXCP)



G = Gate, D = Drain,
S = Source, TAB = Drain

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
V_{DSS}	$V_{GS} = 0 \text{ V}, I_D = 25 \text{ } \mu\text{A}$	900		V
$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 25 \text{ } \mu\text{A}$	2.5		V
I_{GSS}	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0$			$\pm 50 \text{ nA}$
I_{DSS}	$V_{DS} = V_{DSS}, V_{GS} = 0 \text{ V}$			$10 \text{ } \mu\text{A}$
$R_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 50 \text{ mA}$ Pulse test, $t \leq 300 \text{ } \mu\text{s}$, duty cycle $d \leq 2 \%$			$80 \text{ } \Omega$
I_{DP}	Plateau Current; $V_{DS} = 10 \text{ V}, V_{GS} = 10 \text{ V}$ Pulse test, $t \leq 300 \text{ } \mu\text{s}$, duty cycle $d \leq 2 \%$	100		130 mA

Features

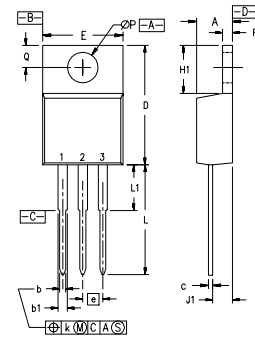
- High output resistance in the saturated mode of operation
- Rugged HDMOS™ process
- Stable peak drain current limit
- High voltage current regulator
- International standard packages

Applications

- Current regulation
- Over current and over voltage protection for sensitive loads
- Linear regulator

Symbol	Test Conditions	Characteristic Values (T _J = 25°C, unless otherwise specified)		
		min.	typ.	max.
g_{fs}	V _{DS} = 20 V; I _D = 100 mA, pulse test			40 mS
C_{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz		133	pF
C_{oss}			24	pF
C_{rss}			6.6	pF
t_{d(on)}	V _{DS} = 500 V, I _D = 50 mA V _{GS} = 10 V, R _G = 50 Ω (External)		15	ns
t_r			137	ns
t_{d(off)}			11	ns
t_f			131	ns
Q_{g(on)}	V _{GS} = 10 V, V _{DS} = 500 V, I _D = 50 mA		7.5	nC
Q_{gs}			2.2	nC
Q_{gd}			3.0	nC
ΔI_{A(P)}/ΔT	Plateau Current Shift V _{DS} = 10 V, V _{GS} = 10 V with Temperature		±50	ppm/K
ΔV_{AK}/ΔI_{A(p)}	Dynamic Resistance V _{DS} = 20 V, V _{GS} = 10 V	125		kΩ
V_F	I _F = 50mA			1.8 V
R_{thJC}				3.1 K/W
R_{thCA}	TO-220		80	K/W
	TO-251/252		100	K/W

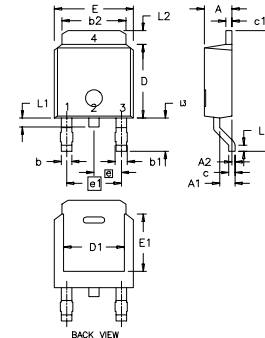
TO-220 AB Dimensions



Pins: 1 - Gate 2 - Drain
3 - Source 4 - Drain
Bottom Side

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.170	.190	4.32	4.83
b	.025	.040	0.64	1.02
b1	.045	.065	1.15	1.65
c	.014	.022	0.35	0.56
D	.580	.630	14.73	16.00
E	.390	.420	9.91	10.66
e	.100 BSC		2.54 BSC	
F	.045	.055	1.14	1.40
H1	.230	.270	5.85	6.85
J1	.090	.110	2.29	2.79
k	0	.015	0	0.38
L	.500	.550	12.70	13.97
L1	.110	.230	2.79	5.84
ØP	.139	.161	3.53	4.08
Q	.100	.125	2.54	3.18

TO-252 AA Outline



Dim.	Min.	Max.	Min.	Max.
A	2.19	2.38	0.086	0.094
A1	0.89	1.14	0.035	0.045
A2	0	0.13	0	0.005
b	0.64	0.89	0.025	0.035
b1	0.76	1.14	0.030	0.045
b2	5.21	5.46	0.205	0.215
c	0.46	0.58	0.018	0.023
c1	0.46	0.58	0.018	0.023
D	5.97	6.22	0.235	0.245
D1	4.32	5.21	0.170	0.205
E	6.35	6.73	0.250	0.265
E1	4.32	5.21	0.170	0.205
e	2.28 BSC		0.090 BSC	
e1	4.57 BSC		0.180 BSC	
H	9.40	10.42	0.370	0.410
L	0.51	1.02	0.020	0.040
L1	0.64	1.02	0.025	0.040
L2	0.89	1.27	0.035	0.050
L3	2.54	2.92	0.100	0.115

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,881,106	5,017,508	5,049,961	5,187,117	5,486,715	6,306,728B1
4,850,072	4,931,844	5,034,796	5,063,307	5,237,481	5,381,025	

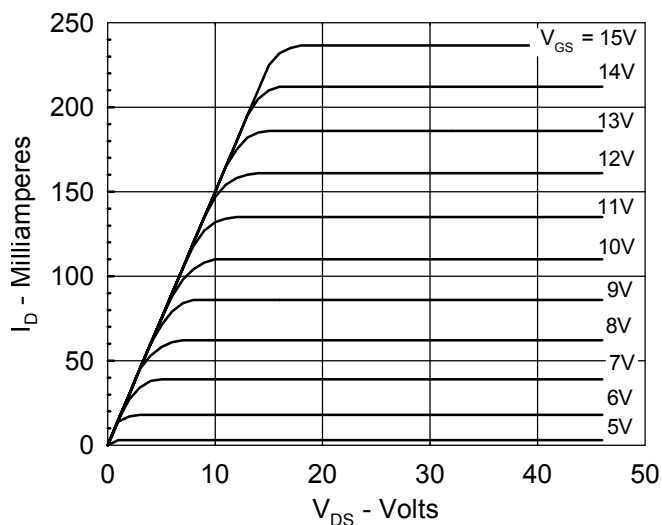


Figure 1. Output Characteristics at 25°C

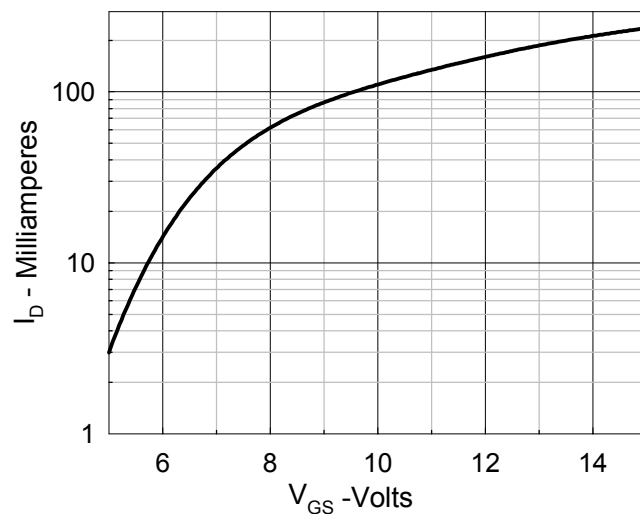


Figure 2. Drain Current vs. Gate Voltage

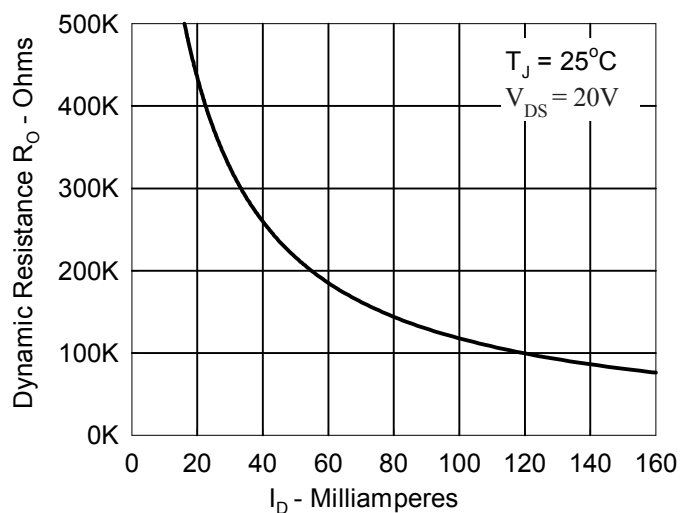


Figure 3. Dynamic Output Resistance R_O vs. Drain Current.

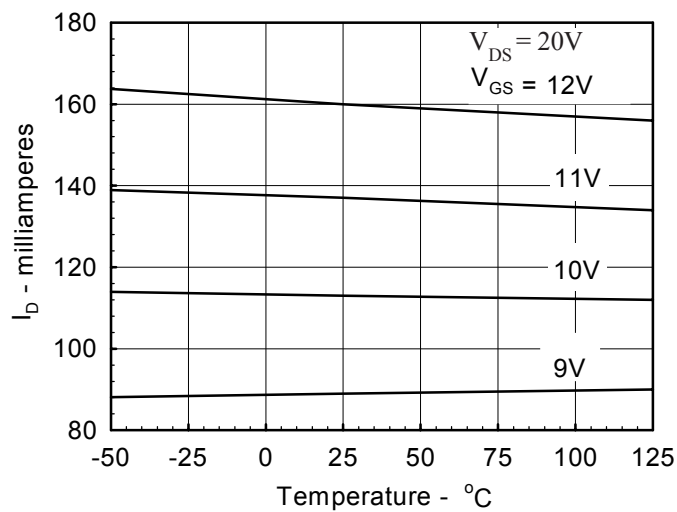


Figure 4. Drain Current vs. Temperature for a constant gate-source voltage.

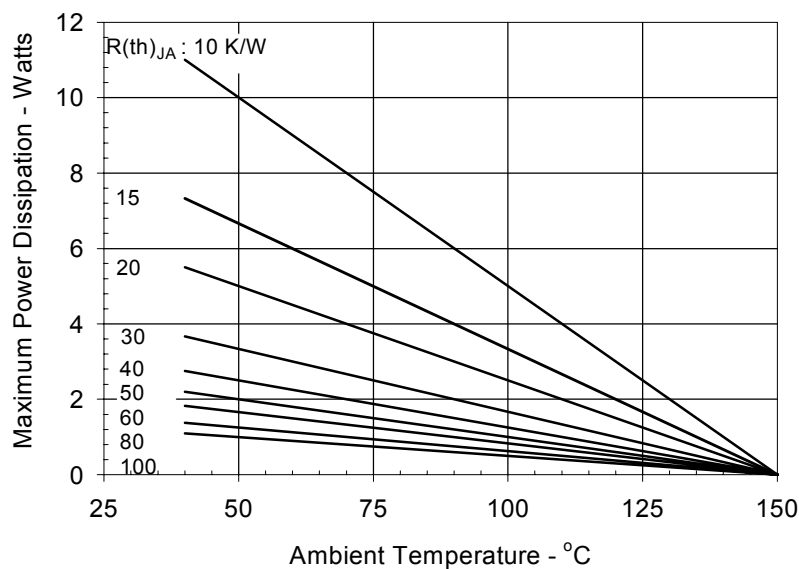


Figure 5. Allowable Power Dissipation for various heat sinking conditions. Note that the junction temperature can be derated by increasing the ambient temperature a like amount.