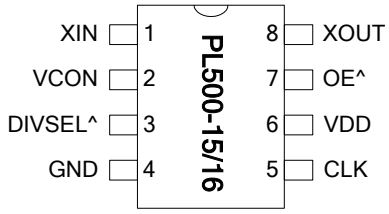
PL500-15/16

Low Phase Noise VCXO (1MHz to 18MHz)

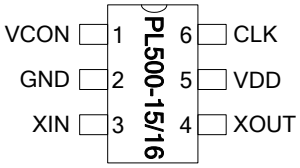
FEATURES

- VCXO with Divider Selection (DIVSEL) input pin
  - PL500-15: ÷8, ÷16
  - PL500-16: ÷2, ÷4
- VCXO output for the 1MHz to 18MHz range
- 16MHz to 36MHz fundamental crystal input.
- Low phase noise (-130 dBc @ 10kHz offset using a 35.328MHz crystal).
- LVCMOS output with OE tri-state control.
- Integrated high linearity variable capacitors.
- 12mA drive capability at TTL output.
- ± 150 ppm pull range, max 5% linearity.
- Low jitter (RMS): 2.5ps period jitter.
- 2.5V ~ 3.3V operation.
- Available in 8-Pin SOP, 6-pin SOT23 GREEN/ RoHS compliant packages, or DIE.

PIN CONFIGURATION



SOP-8L



SOT23-6L*

^: Denotes internal Pull-up
*: SOT package offers single divider option only

DESCRIPTION

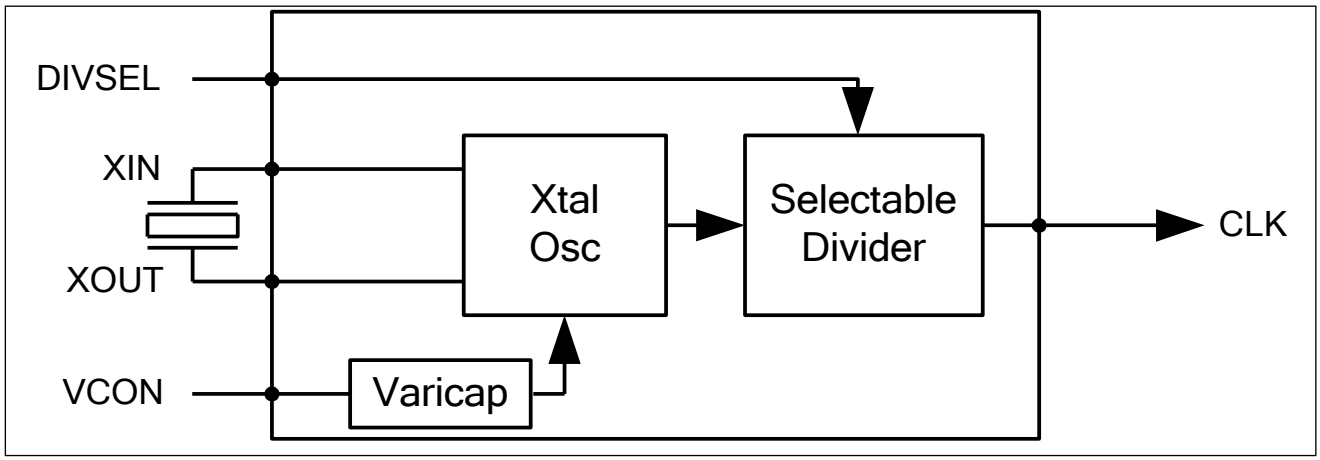
The PL500-15/16 is a low cost, high performance and low phase noise VCXO for the 1MHz to 18MHz range, providing less than -130dBc at 10kHz offset when using a 35.328MHz crystal. The very low jitter (2.5 ps RMS period jitter) makes this chip ideal for applications requiring voltage controlled frequency sources. Input crystal can range from 16MHz to 36MHz (fundamental resonant mode).

DIVIDER SELECTION LOGIC LEVELS

Part #	DivSel State	Operation
PL500-15	1 (Default)*	÷16
	0	÷8
PL500-16	1 (Default)*	÷4
	0	÷2

* Setting for SOT23 package

BLOCK DIAGRAM



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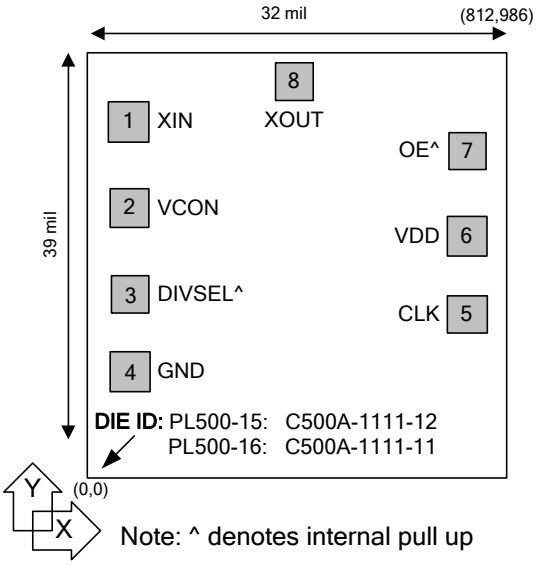
DIE PAD LAYOUT



Note: ^ denotes internal pull up

DIE SPECIFICATIONS

Name	Value
Size	39 x 32 mil
Reverse side	GND
Pad dimensions	80 micron x 80 micron
Thickness	8 mil

DIE PAD ASSIGNMENT

Name	Pin#		Die Pad Position		Type	Description
	SOP-8	SOT23-6	X (µm)	Y (µm)		
XIN	1	3	94.183	768.599	I	Crystal input pin.
VCON	2	1	94.157	605.029	P	Frequency Control Voltage input pin.
DIVSEL	3	-	94.183	331.756	I	Divider Selection input pin. Default Logic 1 for SOT23 package. See Divider Selection Logic Levels table on Page 1.
GND	4	2	94.193	140.379	P	Ground pin.
CLK	5	6	715.472	203.866	O	Output clock pin.
VDD	6	5	715.307	455.726	P	VDD power supply pin.
OE	7	-	715.472	626.716	I	Output Enable input pin. Disables the output when low. Internal pull-up enables output by default if pin is not connected to low. Default “Enabled” (Logic 1) for SOT23 package.
XOUT	8	4	476.906	888.881	I	Crystal output pin.

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

2. AC Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Crystal Frequency			16		36	MHz
Output Clock Rise/Fall Time		0.8V ~ 2.0V, 10 pF load		1.15		ns
		0.3V ~ 3.0V, 15 pF load		3.7		
Output Clock Duty Cycle		Measured @ 1.4V	45	50	55	%

3. Voltage Control Crystal Oscillator

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time *	$T_{VCXOSTB}$	From power valid			10	ms
VCXO Tuning Range		XTAL C_0/C_1 < 250 0V ≤ VCON ≤ 3.3V		300		ppm
CLK output pullability		VCON=1.65V, ±1.65V	±150			ppm
VCXO Tuning Characteristic				100		ppm/V
Pull range linearity					5	%
Power Supply Rejection	PWSRR	Frequency change with VDD varied +/- 10%	-1		+1	ppm
VCON pin input impedance			2000			kΩ
VCON modulation BW		0V ≤ VCON ≤ 3.3V, -3dB	18			kHz

Note: Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits.

4. Jitter and Phase Noise Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
RMS Period Jitter (1 sigma – 1000 samples)	With capacitive decoupling between VDD and GND.		2.5		ps
Phase Noise relative to carrier	13.5MHz @100Hz offset		-100		dBc/Hz
Phase Noise relative to carrier	13.5MHz @1kHz offset		-125		dBc/Hz
Phase Noise relative to carrier	13.5MHz @10kHz offset		-142		dBc/Hz
Phase Noise relative to carrier	13.5MHz @100kHz offset		-150		dBc/Hz
Phase Noise relative to carrier	13.5MHz @1MHz offset		-150		dBc/Hz

5. DC Specifications

PARAMETERS	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic, with Loaded Outputs	I_{DD}	F_{XIN} = 27MHz Output load of 15pF	3.3V		3.7	5	mA
			2.5V		2.4	3.5	
Operating Voltage	V_{DD}			2.25		3.63	V
Output Low Voltage at CMOS level	V_{OLC}	I_{OL} = +4mA				0.4	V
Output High Voltage at CMOS level	V_{OHC}	I_{OH} = -4mA		V_{DD} – 0.4			V
Output drive current		For V_{OL}<0.4V or V_{OH}>2.4V		8	9.5		mA
VCXO Control Voltage	VCON			0		V_{DD}	V

6. Crystal Specifications

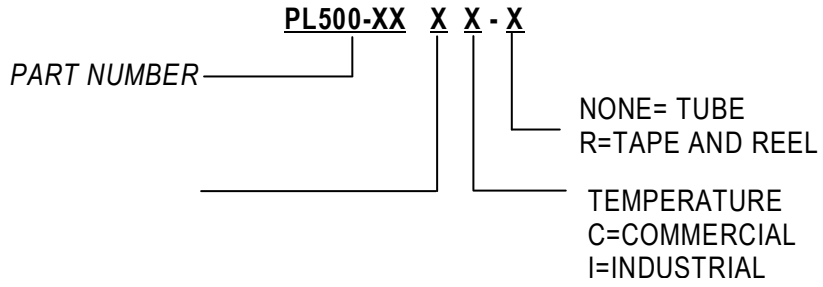
PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS
Crystal Loading Rating (VCON = 1.65V, 3.3V VDD)	$C_{L\ (xtal)}$ (see note below)		7.8		pF
Crystal Loading Rating (VCON = 1.25V, 2.5V VDD)			8.9		
Maximum Sustainable Drive Level				200	µW
Operating Drive Level			50		µW
Max C0				5	pF
C0/C1				250	-
ESR	R_S			30	Ω

Note: The crystal must be such that it oscillates (parallel resonant) at nominal frequency when presented a C Load as specified above. If the crystal requires more load to be at nominal frequency, the additional load must be added externally. This however may reduce the pull range. Note that the Cload values above are for the IC only, and do not include PCB parasitics. Crystal specifications for Cload include PC B parasitics.

ORDERING INFORMATION (GREEN PACKAGE COMPLIANT)

For part ordering, please contact our Sales Department:
2180 Fortune Drive, San Jose, CA 95131, USA
Tel: (408) 944-0800 Fax: (408) 474-1000

PART NUMBER
The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range



Part / Order Number	Marking	Package Option
PL500-15DC	N/A	Die (Waffle Pack)
PL500-15SC	P500-15 SC LLLLL	8-Pin SOP (Tube)
PL500-15SC-R		8-Pin SOP (Tape and Reel)
PL500-15TC-R	B15 LLL	6-Pin SOT23 (Tape and Reel)
PL500-16DC	N/A	Die (Waffle Pack)
PL500-16SC	P500-16 SC LLLLL	8-Pin SOP (Tube)
PL500-16SC-R		8-Pin SOP (Tape and Reel)
PL500-16TC-R	B16 LLL	6-Pin SOT23 (Tape and Reel)

Note: LLL / LLLLL designate Production Lot.