User's Guide

TPS51163 Buck Controller Evaluation Module User's Guide

ABSTRACT

The TPS51163EVM evaluation module (EVM) is a high efficiency single phase synchronous buck converter providing a fixed 1.2-V output at up to 10 A from a 12-V input bus. The EVM uses the TPS51163 synchronous buck controller with 600 kHz.

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Trademarks

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1 Introduction

The TPS51163EVM evaluation module (EVM) is a highly effective, single-phase synchronous buck controller providing a fixed 1.2-V output at up to 10 A from a 12-V input bus. The EVM uses the TPS51163 step-down buck controller.

2 Description

The TPS51163EVM is designed to use a regulated 12-V (8-V to 14-V) bus to produce a high current, regulated 1.2-V output at up to 10 A of the load current. The TPS51163EVM is designed to demonstrate the TPS51163 in a typical low-voltage application while providing a number of test points to evaluate the performance of the TPS51163.

3 Typical Applications

- Server and desktop computer subsystem power supplies
- Distributed power supplies
- General DC-DC converters

4 Features

The TPS51163EVM features include:

- 10-A DC steady state current
- Support pre-bias output voltage start-up
- 600-kHz switching frequency
- JP1 for enable function
- Convenient test points for probing critical waveforms and loop response testing
- Four-layer PCB with 2-oz. copper and all components on the top layer

5 Electrical Performance Specifications

Table 5-1 gives the EVM performance specifications.

Table 5-1. Performance Specification Summary

SPECIFICATION		TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
V_{IN}	Input voltage range		8	12	14	V
$I_{IN(max)}$	Maximum input current	V_{IN} = 8 V, I_O = 10 A			1.7	A
I_{IN}	No load input current	V_{IN} = 14 V, I_O = 0 A			35	mA
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage			1.2		V
V_{REG}	Output voltage regulation	Line regulation			0.1%	
		Load regulation			0.4%	
V_{RIPPLE}	Output voltage ripple	V_{IN} = 12 V, I_O = 10 A			20	mVpp
	Ouptut load current		0		10	A
	Output overcurrent threshold			15		A
SYSTEMS CHARACTERISTICS						
f_{SW}	Switching frequency			600		kHz
η	Peak efficiency	V_{IN} = 12 V, V_{OUT} = 1.2 V, I_O = 8 A		89.13%		
η	Full load efficiency	V_{IN} = 12 V, V_{OUT} = 1.2 V, I_O = 10 A		88.96%		
T_A	Operating ambient temperature			25		°C

6 Schematic

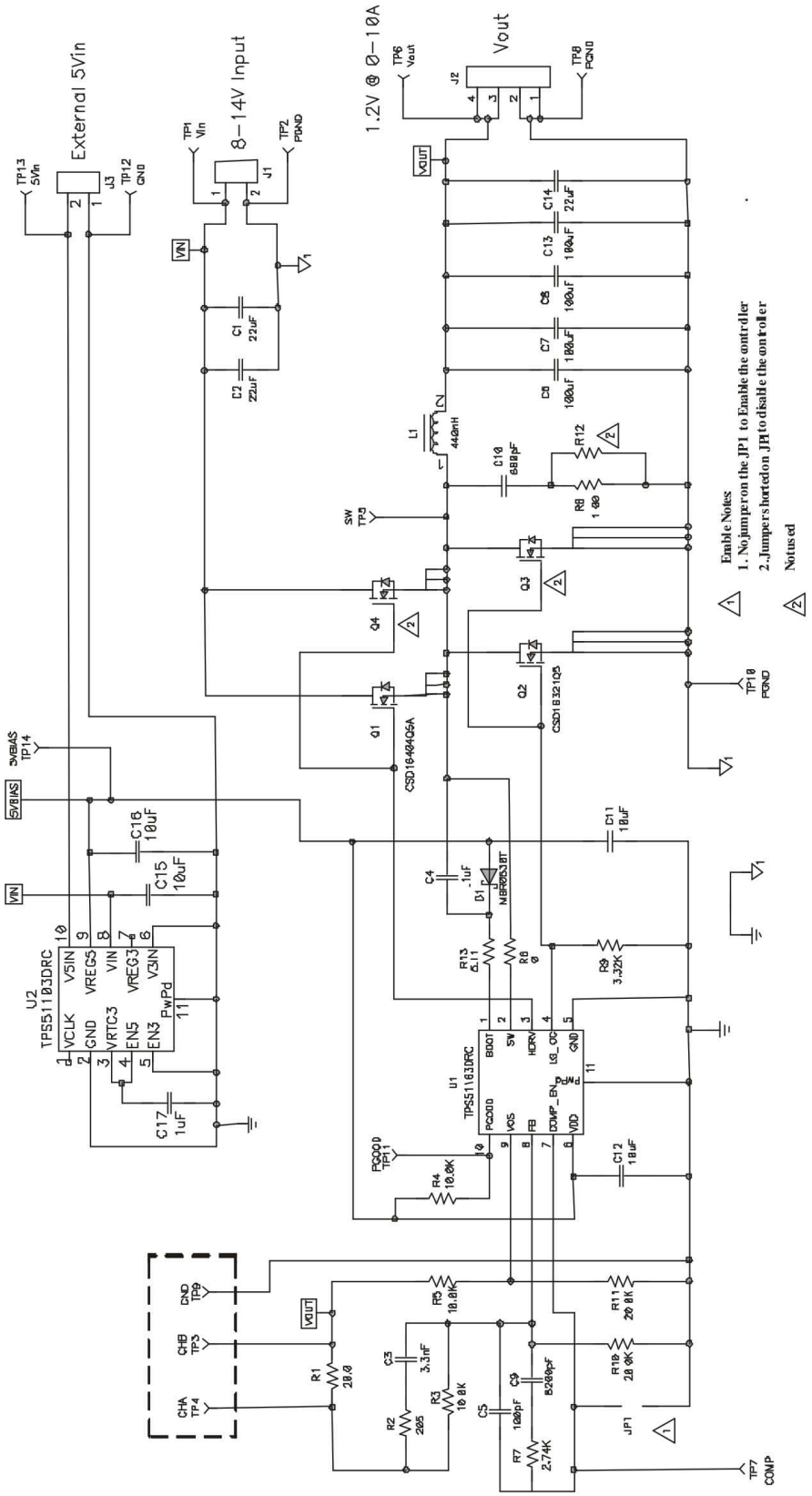


Figure 6-1. TPS51163EVM Schematic Diagram

7 Test Setup

7.1 Test Equipment

7.1.1 Voltage Source

The input voltage source V_{IN} should be a variable DC source between 0 V and 14 V, capable of supplying 10 Adc. Connect V_{IN} to J1 as shown in Figure 7-2.

7.1.2 Multimeters

A voltmeter with a range between 0 V and 14 V should be used to measure V_{IN} at TP1 (V_{IN}) and TP2 (GND). A voltmeter with a range between 0 V and 5 V for V_{OUT} measurement at TP6 (V_{OUT}) and TP8 (GND). A current meter with a range between 0 A and 10 A (A1) as shown in Figure 7-2 is used for input current measurements.

7.1.3 Output Load

The output load should be an electronic constant resistance mode load capable of between 0 Adc and 20 Adc at 1.2 V.

7.1.4 Oscilloscope

A digital or analog oscilloscope can be used to measure the output ripple. The oscilloscope should be set for the following:

- 1-MΩ impedance
- 20-MHz bandwidth
- AC coupling
- 1-µs/division horizontal resolution
- 20-mV/division vertical resolution

Test points TP6 and TP8 can be used to measure the output ripple voltage. Place the oscilloscope probe tip through TP6 and rest the ground barrel on TP8 as shown in Figure 7-1. Using a leaded ground connection can induce additional noise due to the large ground loop.

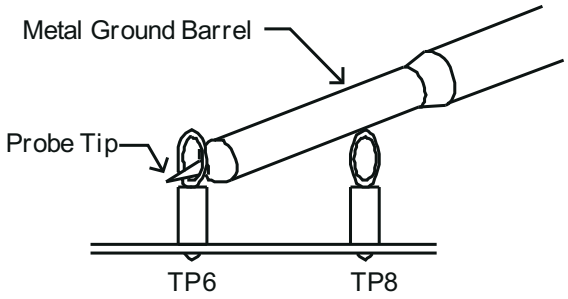


Figure 7-1. Tip and Barrel Measurement for V_{OUT} Ripple

7.1.5 Fan

Some of the components in this EVM cab approach temperatures of 60°C during operating. A small fan capable of 200–400 LFM is recommended to reduce component temperatures while the EVM is operating. The EVM should not be probed while the fan is not running.

7.1.6 Recommended Wire Gauge

For V_{IN} to J1 (12-V input) the recommended wire size is 1 × AWG #14 per input connection with the total length of wire less than four feet (2-feet input, 2-feet return). For J2 to LOAD, the minimum recommended wire size is 1 × AWG #14 with the total length of wire less than four feet (2-feet output, 2-feet return).

7.2 Recommended Test Setup

Figure 7-2 is the recommended test setup to evaluate the TPS51163EVM. Working at an ESD workstation, make sure that any wrist straps, bootstraps, or mats are connected referencing the user to earth ground before power is applied to the EVM.

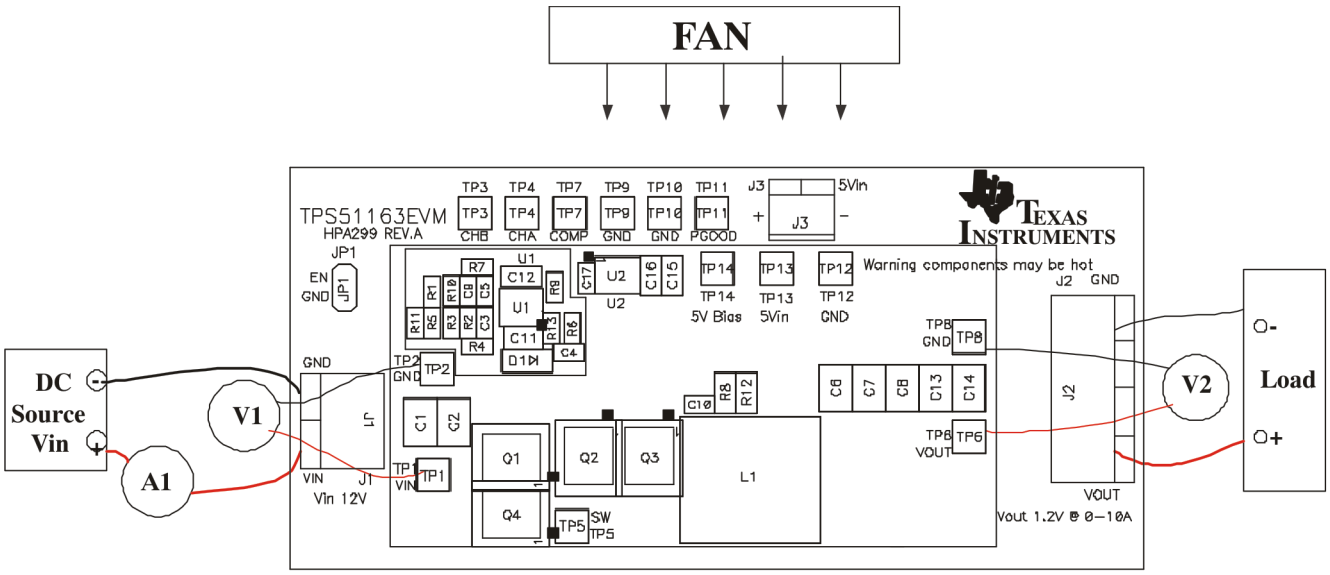


Figure 7-2. TPS51163EVM Recommended Test Setup

7.2.1 Input Connections

1. Prior to connecting the DC input source V_{IN}, it is advisable to limit the source current from V_{IN} to 10 A maximum. Make sure V_{IN} is initially set to 0 V and connected as shown in Figure 7-2.
2. Connect a voltmeter V1 at TP1 (V_{IN}) and TP2 (GND) to measure the input voltage.

7.2.2 Output Connections

1. Connect Load to J2 and set the load to constant resistance mode to sink 0 Adc before V_{IN} is applied.
2. Connect a voltmeter V2 at TP6 (V_{OUT}) and TP8 (GND) to measure the output voltage.

7.2.3 Other Connections

Place a fan as shown in Figure 7-2 and turn it on, making sure air is flowing across the EVM.

8 Test Procedure

8.1 Line/Load Regulation and Efficiency Measurement Procedure

1. Ensure that the load is set to constant resistance mode and to sink 0 Adc.
2. Ensure that the jumper provided in the EVM to short on JP1 before V_{IN} is applied.
3. Increase V_{IN} from 0 V to 12 V, using V1 to measure input voltage.
4. Remove the jumper on JP1 to enable the controller.
5. Vary load from between 0 VAdc and 10 Adc, V_{OUT} should remain in load regulation.
6. Vary V_{IN} from 8 V to 14 V. V_{OUT} should remain in line regulation.
7. Put the jumper on JP1 to disable the controller.
8. Decrease the load to 0 A.
9. Decrease V_{IN} to 0 V.

8.2 Control Loop Gain and Phase Measurement Procedure

The TPS51163EVM contains a 20-Ω series resistor in the feedback loop for loop response analysis.

1. Set up the EVM as described in Section 8.1 and Figure 7-2.
2. Connect the isolation transformer to test points marked TP4 and TP3.
3. Connect an input signal amplitude measurement probe (channel A) to TP4.
4. Connect an output signal amplitude measurement probe (channel B) to TP3.
5. Connect the ground lead of channel A and channel B to TP9 and TP10.
6. Inject approximately 40-mV or less signal through the isolation transformer.
7. Sweep the frequency from 100 Hz to 1 MHz with a 10-Hz or lower post filter. The control loop gain and phase margin can be measured.
8. Disconnect the isolation transformer from bode plot test points before making other measurements (Signal injection into feedback may interfere with accuracy of other measurements).

8.3 List of Test Points

Table 8-1. Test Point Functions

TEST POINTS	NAME	DESCRIPTION
TP1	V_{IN}+	12-V input
TP2	PGND	PGND for V_{IN}
TP3	CHB	Input B for loop injection
TP4	CHA	Input A for loop injection
TP5	SW	Monitor switch node voltage
TP6	V_{OUT}	V_{OUT}
TP7	COMP	COMP/ Enable
TP8	PGND	PGND for V_{OUT}
TP9	GND	GND for loop measurement
TP10	PGND	PGND
TP11	PGOOD	Power Good
TP12	GND	GND for External 5 V_{IN}
TP13	5Vin	External 5 V_{IN}
TP14	5Vbias	5 V bias for VDD

8.4 Equipment Shutdown Procedure

1. Shut down the load.
2. Shut down V_{IN}.
3. Shut down the fan.

9 Performance Data and Typical Characteristic Curves

Figure 9-1 through Figure 9-10 present typical performance curves for the TPS51163EVM.

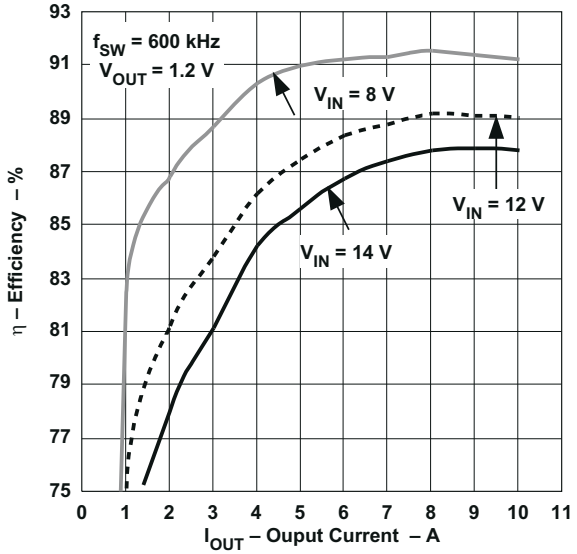


Figure 9-1. Efficiency

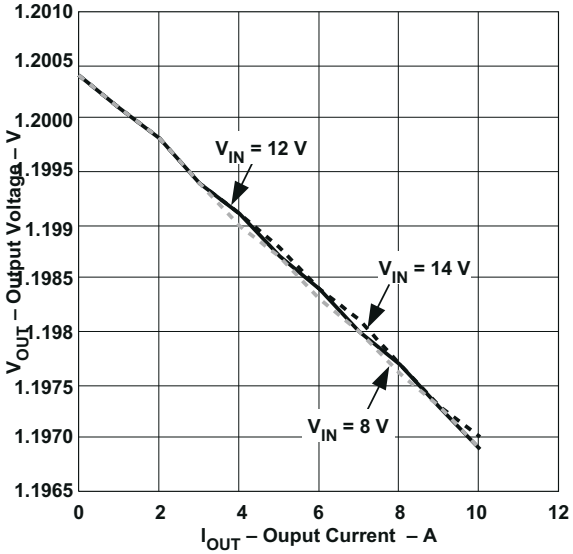


Figure 9-2. Load Regulation

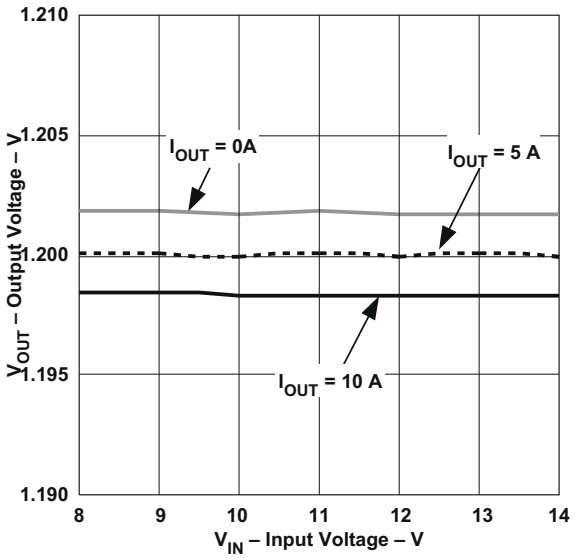


Figure 9-3. Line Regulation

In Figure 9-4, the following conditions apply:

- V_{IN} = 12 V
- V_{OUT} = 1.2 V
- I_{LOAD} = 10 A
- Crossover Frequency = 67.68 kHz
- Phase margin = 67.03°
- Gain margin = 35.83 dB

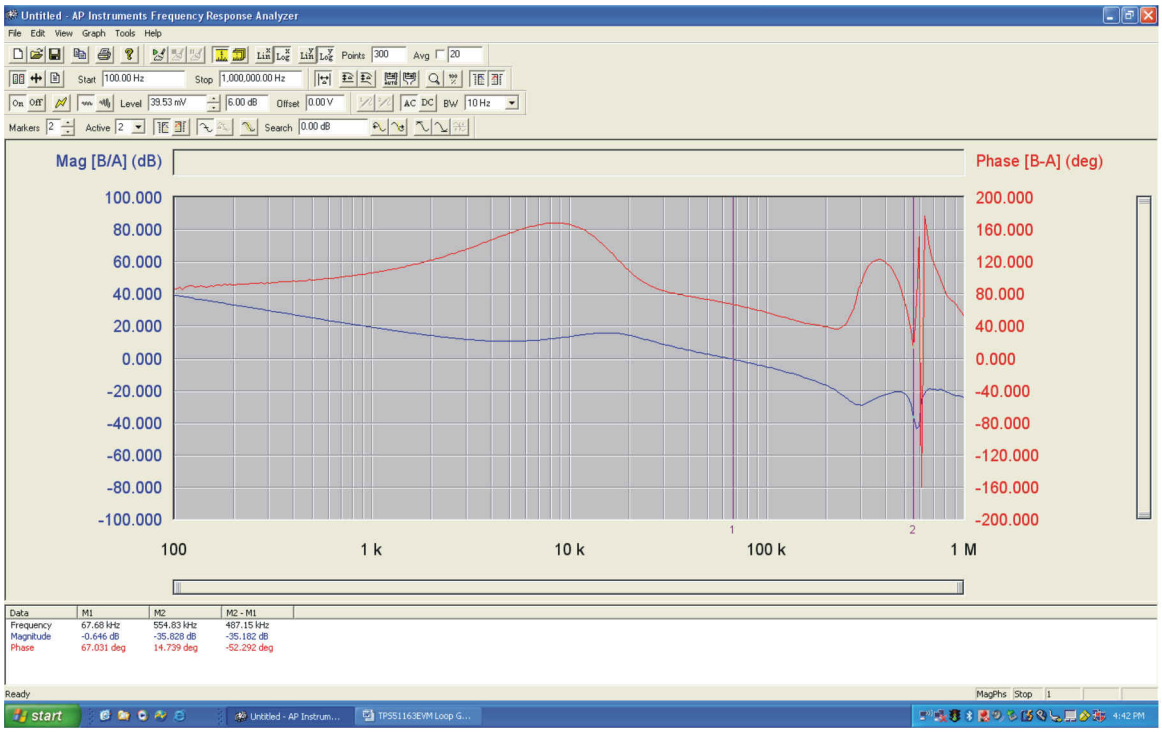
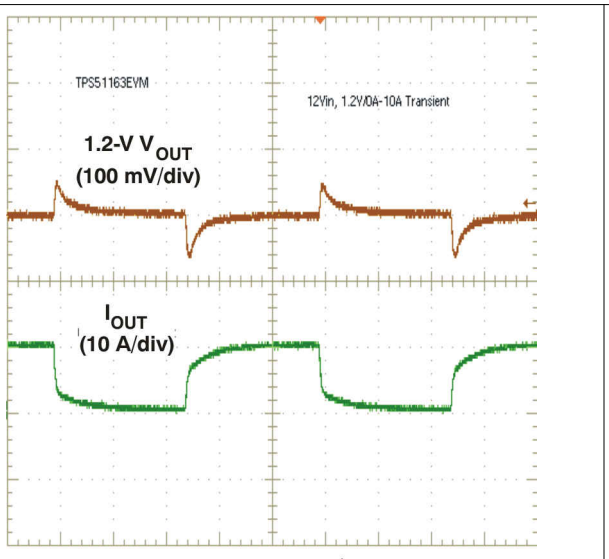
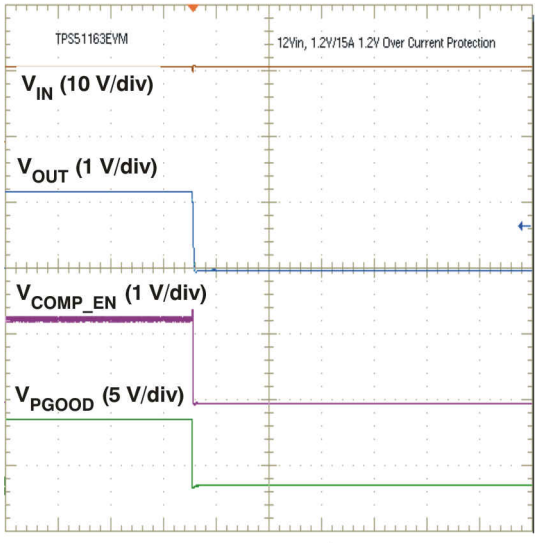


Figure 9-4. Loop Response Gain and Phase



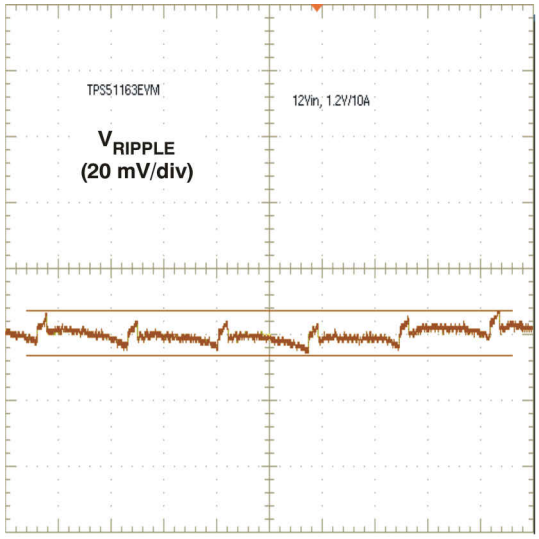
t – Time – 400 µs/div

Figure 9-5. Load Transient



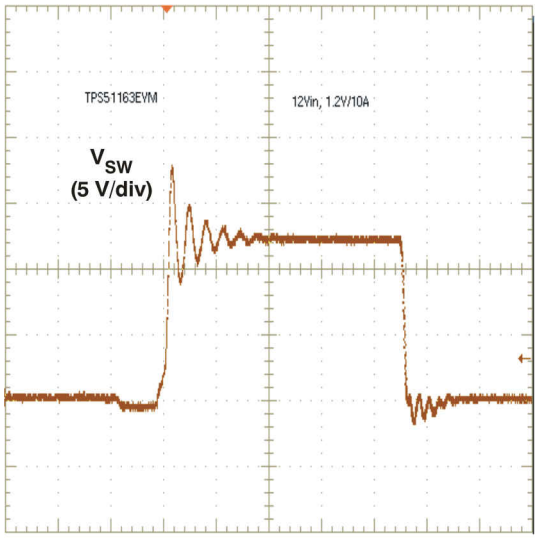
t – Time – 1 ms/div

Figure 9-6. Output Overcurrent Protection



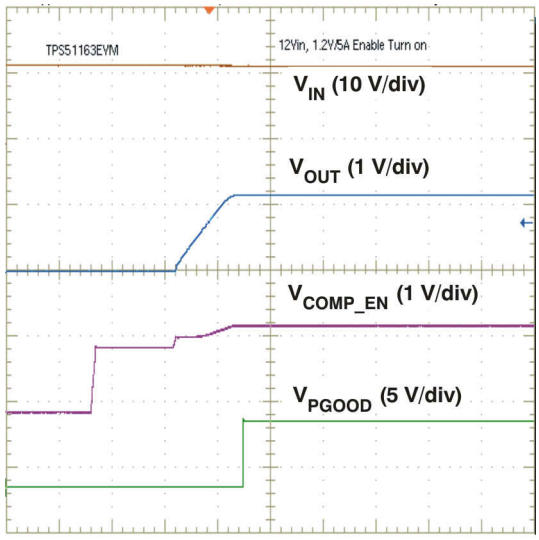
t – Time – 1 µs/div

Figure 9-7. Output Ripple



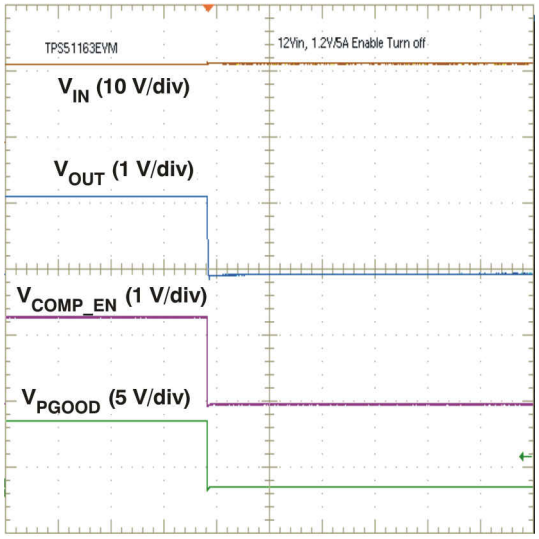
t – Time – 40 ns/div

Figure 9-8. Switch Node Waveform



t – Time – 4 ms/div

Figure 9-9. Enable Turn-On



t – Time – 4 ms/div

Figure 9-10. Enable Turn-Off

10 EVM Assembly Drawing and PCB layout

Figure 10-1 through Figure 10-6 show the design of the TPS51163EVM printed circuit board. The EVM has been designed using four layers on a 2-oz. copper circuit board.

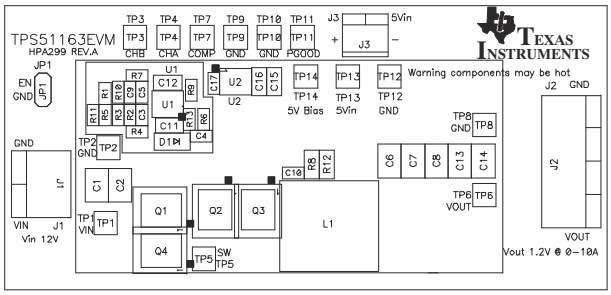


Figure 10-1. Top Layer Assembly Drawing (Top View)

Figure 10-2. Bottom Assembly Drawing (Bottom View)

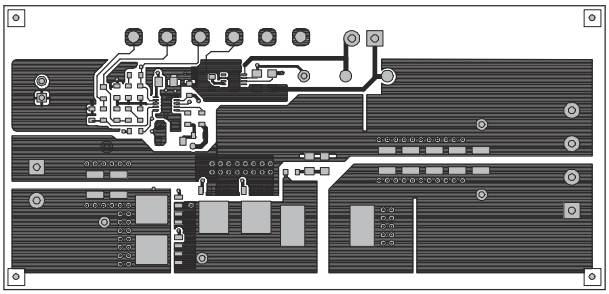


Figure 10-3. Top Copper (Top View)

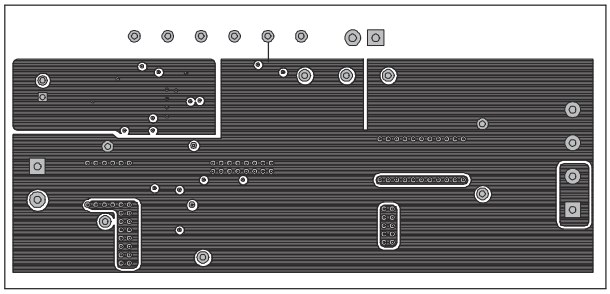


Figure 10-4. Internal Layer 1

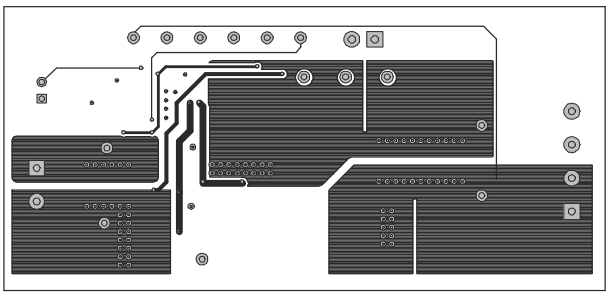


Figure 10-5. Internal Layer 2

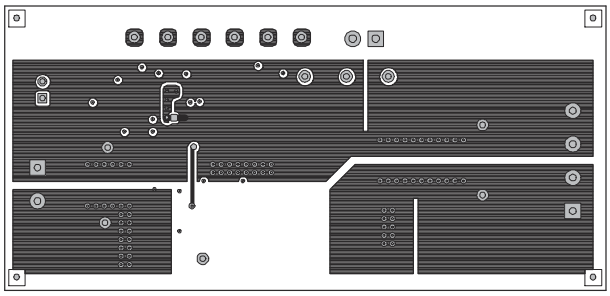


Figure 10-6. Bottom Copper (Top View)

11 List of Materials

List of materials for the TPS51163EVM.

Table 11-1. TPS51163EVM List of Materials

REFERENCE DESIGNATOR	QTY	DESCRIPTION	MFR	PART NUMBER
C1, C2, C14	3	Capacitor, Ceramic, 22 µF, 16 V, X5R, 20%, 1210	MuRata	GRM32ER61C226KE20L
C10	1	Capacitor, Ceramic, 680 pF, 25 V, X7R, 10%, 0603	STD	STD
C11, C12, C15, C16	4	Capacitor, Ceramic, 10 µF, 16 V, X5R, 10%, 0805	STD	STD
C17	1	Capacitor, Ceramic, 1 µF, 16 V, X7R, 10%, 0603	STD	STD
C3	1	Capacitor, Ceramic, 3300 pF, 25 V, X7R, 10%, 0603	STD	STD
C4	1	Capacitor, Ceramic, 0.1 µF, 25 V, X7R, 10%, 0603	STD	STD
C5	1	Capacitor, Ceramic, 100 pF, 25 V, X7R, 10%, 0603	STD	STD
C9	1	Capacitor, Ceramic, 8200 pF, 25 V, X7R, 10%, 0603	STD	STD
C6, C7, C8, C13	4	Capacitor, Ceramic, 100 µF, 6.3 V, X5R, 20%, 1210	Murata	GRM32ER60J107ME20L
L1	1	Inductor, Toroid, 440 nH, 30 A, 0.530" x 0.510"	E & E Magnetic	831-02990F
			PULSE	PA0513-441NLT
R1	1	Resistor, Chip, 20.0 Ω, 1/16 W, 1%, 0603	STD	STD
R10, R11	2	Resistor, Chip, 20.0 kΩ, 1/16 W, 1%, 0603	STD	STD
R2	1	Resistor, Chip, 205 Ω, 1/16 W, 1%, 0603	STD	STD
R13	1	Resistor, Chip, 5.11Ω, 1/16 W, 1%, 0603	STD	STD
R3, R4, R5	3	Resistor, Chip, 10.0 kΩ, 1/16 W, 1%, 0603	STD	STD
R6	1	Resistor, Chip, 0.00, 1/16 W, 1%, 0603	STD	STD
R7	1	Resistor, Chip, 2.74 kΩ, 1/16 W, 1%, 0603	STD	STD
R8	1	Resistor, Chip, 1.0 Ω, 1/8 W, 1%, 0805	STD	STD
R9	1	Resistor, Chip, 3.32 kΩ, 1/16 W, 1%, 0603	STD	STD
D1	1	Diode, Schottky, 0.5 A, 30 V	Onsemi	MBR0530T
Q1	1	MOSFET, N-channel, 25 V, 20 A, 5.8 mΩ, TDSON-8	Ciclon	CSD16404Q5A
Q2	1	MOSFET, N-channel, 25 V, 30 A, 2.1 mΩ, TDSON-8	Ciclon	CSD16321Q5
U1	1	IC, 4.5-V to 13.2-V synchronous buck controller, SON-10	TI	TPS51163DRC
U2	1	IC, integrated LDO with switchover circuit	TI	TPS51103DRC

12 References

- Texas Instruments, *TPS511x3 Synchronous Buck Controller with High-Current Gate Driver Data Sheet*
- Texas Instruments, *TPS51103 Integrated LDO with Switchover Circuit for Notebook Computers Data Sheet*

13 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2009) to Revision A (February 2022) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document. 2
- Updated the user's guide title..... 2

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