

# SN54HCT652, SN74HCT652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCLS179D – MARCH 1984 – REVISED MARCH 2003

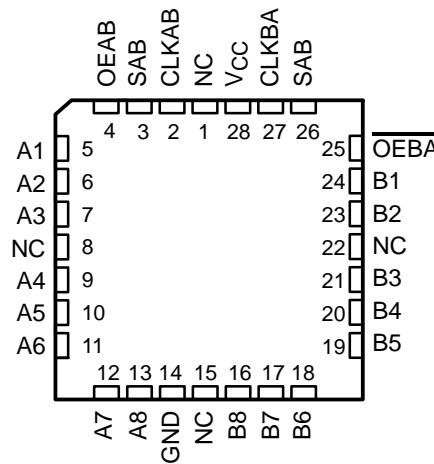
- Operating Voltage Range of 4.5 V to 5.5 V
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 12$  ns
- $\pm 6$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- Inputs Are TTL-Voltage Compatible

SN54HCT652 . . . JT OR W PACKAGE  
SN74HCT652 . . . DW OR NT PACKAGE  
(TOP VIEW)



- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- True Data Paths
- High-Current 3-State Outputs Can Drive Up To 15 LSTTL Loads

SN54HCT652 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The 'HCT652 devices consist of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output-enable (OEAB and OEBA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select real-time or stored data transfer. A low input level selects real-time data; a high input level selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with these devices.

## ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – NT	Tube	SN74HCT652NT	SN74HCT652NT
	SOIC – DW	Tube	SN74HCT652DW	HCT652
		Tape and reel	SN74HCT652DWR	
–55°C to 125°C	CDIP – JT	Tube	SNJ54HCT652JT	SNJ54HCT652JT
	CFP – W	Tube	SNJ54HCT652W	SNJ54HCT652W
	LCCC – FK	Tube	SNJ54HCT652FK	SNJ54HCT652FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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## description/ordering information (continued)

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) terminals, regardless of the select- or output-control terminals. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and  $\overline{OEBA}$ . In this configuration, each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

To ensure the high-impedance state during power up or power down,  $\overline{OEBA}$  should be tied to  $V_{CC}$  through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data-output functions can be enabled or disabled by a variety of level combinations at OEAB or OEBA. Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition on the clock inputs.

‡ Select control = L: clocks can occur simultaneously.

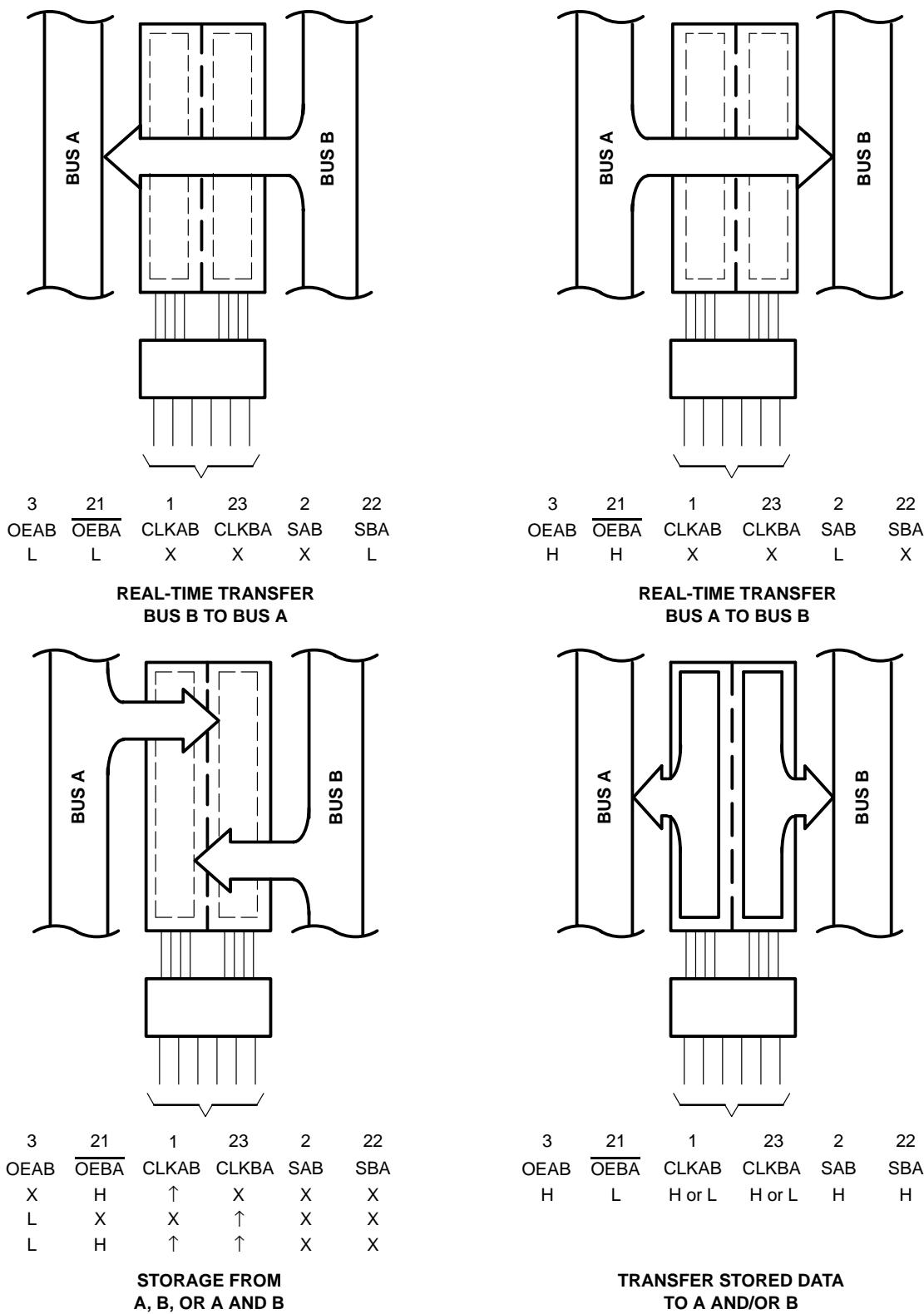
Select control = H: clocks must be staggered to load both registers.



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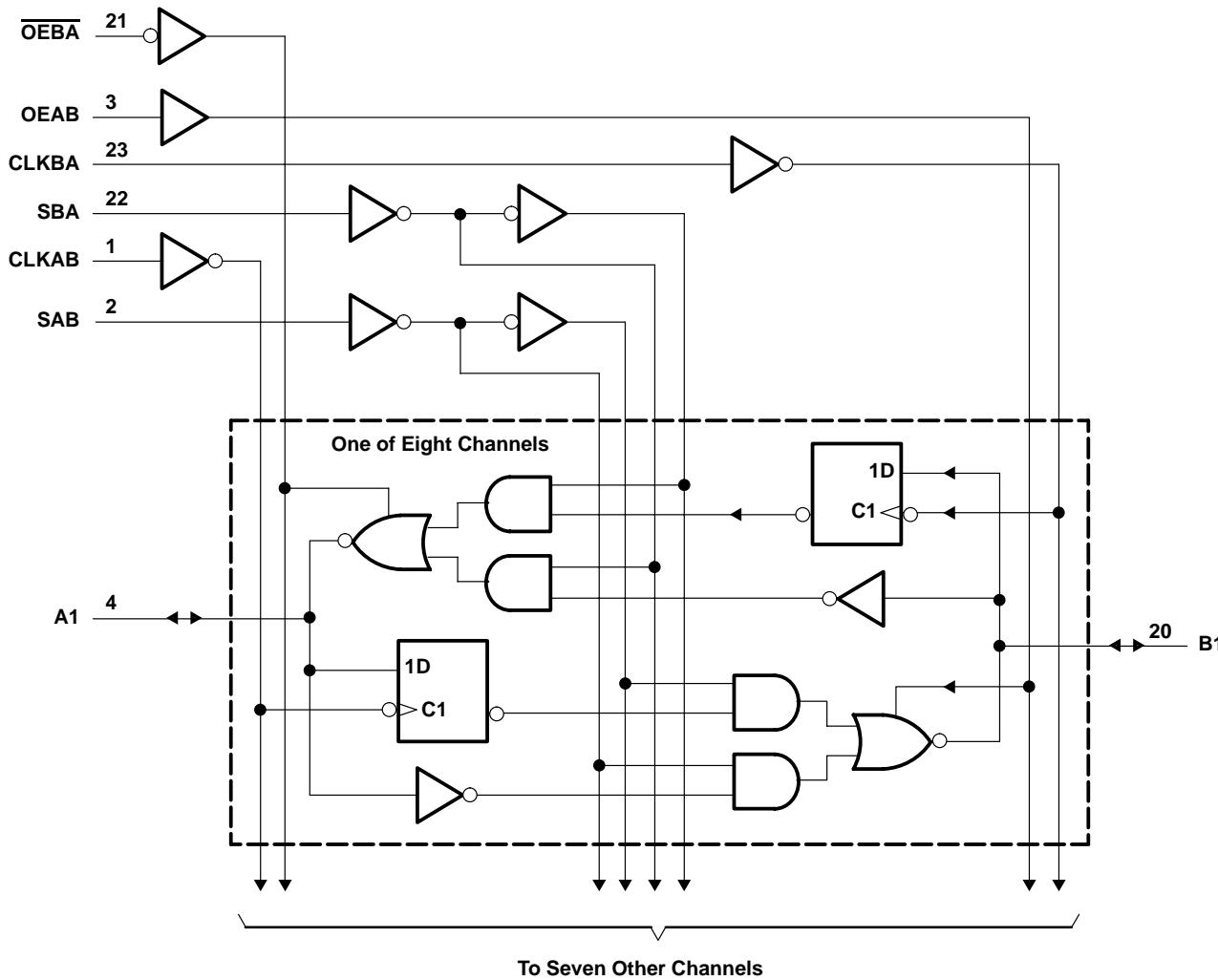
Pin numbers shown are for the DW, JT, NT, and W packages.

**Figure 1. Bus-Management Functions**

# **SN54HCT652, SN74HCT652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS**

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## logic diagram (positive logic)



Pin numbers shown are for the DW, JT, NT, and W packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

1. The input and output voltage ratings may be exceeded if the input and output current ratings are exceeded.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-3.

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**recommended operating conditions (see Note 4)**

			SN54HCT652			SN74HCT652			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2			2			V
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V			0.8			0.8	V
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
t <sub>t</sub>	Input transition (rise and fall) time				500			500	ns
T <sub>A</sub>	Operating free-air temperature		-55	125		-40		85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HCT652		SN74HCT652		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	4.5 V	4.4	4.499		4.4		4.4		V
			3.98	4.3		3.7		3.84		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	4.5 V	0.001	0.1		0.1		0.1		V
			0.17	0.26		0.4		0.33		
I <sub>I</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or 0	5.5 V	±0.1	±100	±1000		±1000		nA
I <sub>OZ</sub>	A or B	V <sub>O</sub> = V <sub>CC</sub> or 0, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , Data = V <sub>CC</sub> or 0	5.5 V	±0.01	±0.5	±10		±5		µA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	5.5 V		8	160		80		µA
ΔI <sub>CC</sub> <sup>†</sup>		One input at 0.5 V or 2.4 V, Other inputs at 0 or V <sub>CC</sub>	5.5 V	1.4	2.4	3		2.9		mA
C <sub>i</sub>	Control inputs		4.5 V to 5.5 V	3	10	10		10		pF

<sup>†</sup>This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted)**

	V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HCT652		SN74HCT652		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	4.5 V	25		17		20	MHz
		5.5 V	28		19		22	
t <sub>w</sub>	Pulse duration, CLKBA or CLKAB high or low	4.5 V	20	30		25		ns
		5.5 V	18	27		23		
t <sub>su</sub>	Setup time, A before CLKAB↑ or B before CLKBA↑	4.5 V	15	23		19		ns
		5.5 V	14	21		17		
t <sub>h</sub>	Hold time, A after CLKAB↑ or B after CLKBA↑	4.5 V	5	5		5		ns
		5.5 V	5	5		5		

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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**SN54HCT652, SN74HCT652  
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**switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HCT652	SN74HCT652	UNIT
				MIN	TYP	MAX	MIN	MAX	
f <sub>max</sub>			4.5 V	25	35		17	20	MHz
			5.5 V	28	40		19	22	
t <sub>pd</sub>	CLKBA or CLKAB	A or B	4.5 V	18	36		54	45	ns
			5.5 V	16	32		49	41	
	A or B	B or A	4.5 V	14	27		41	34	
			5.5 V	12	24		37	31	
t <sub>en</sub>	OEBA or OEAB	A or B	4.5 V	20	38		57	48	ns
			5.5 V	17	34		51	43	
	OEBA or OEAB	A or B	4.5 V	25	49		74	61	ns
			5.5 V	22	44		67	55	
t <sub>dis</sub>	OEBA or OEAB	A or B	4.5 V	25	49		74	61	ns
			5.5 V	22	44		67	55	
t <sub>t</sub>		Any	4.5 V	9	12		18	15	ns
			5.5 V	7	11		16	14	

<sup>†</sup> These parameters are measured with the internal output state of the storage register opposite that of the bus input.

**switching characteristics over recommended operating free-air temperature range,  $C_L = 150 \text{ pF}$  (unless otherwise noted) (see Figure 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HCT652	SN74HCT652	UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	CLKBA or CLKAB	A or B	4.5 V	24	53		80	66	ns
			5.5 V	22	47		72	60	
	A or B	B or A	4.5 V	22	44		70	55	
			5.5 V	20	39		60	50	
t <sub>en</sub>	OEBA or OEAB	A or B	4.5 V	26	55		83	69	ns
			5.5 V	24	49		74	62	
	OEBA or OEAB	A or B	4.5 V	33	66		100	82	ns
			5.5 V	30	59		90	74	
t <sub>t</sub>		Any	4.5 V	17	42		63	53	ns
			5.5 V	14	38		57	48	

<sup>†</sup> These parameters are measured with the internal output state of the storage register opposite that of the bus input.

**operating characteristics, T<sub>A</sub> = 25°C**

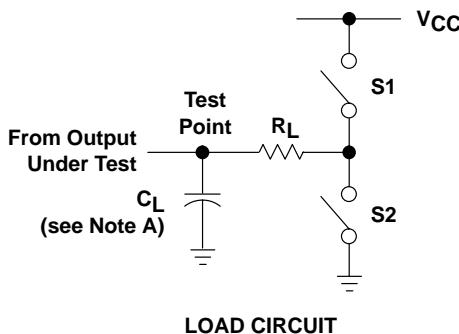
PARAMETER			TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance		No load	50	pF

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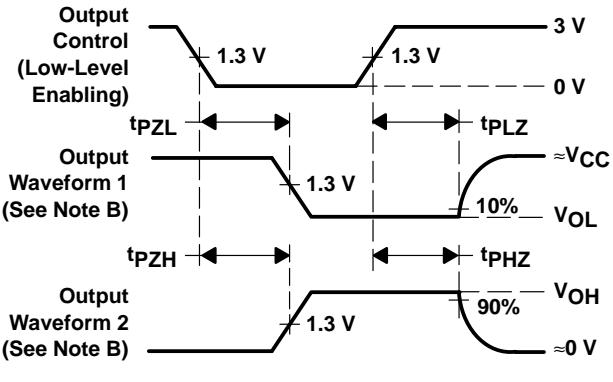
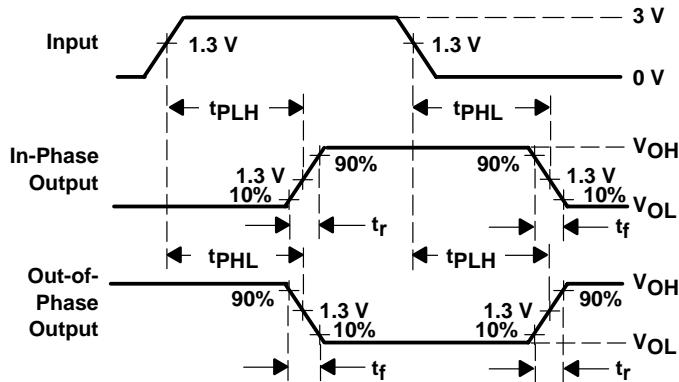
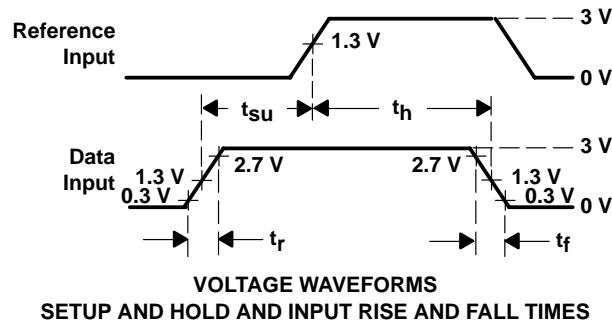
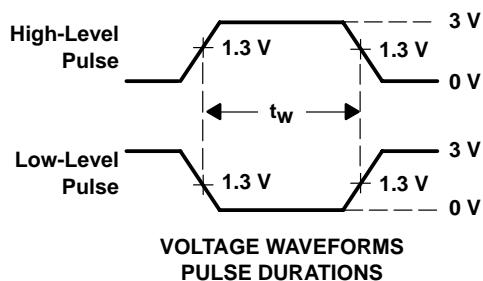


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PARAMETER MEASUREMENT INFORMATION



PARAMETER	R <sub>L</sub>	C <sub>L</sub>	S1	S2
t <sub>en</sub>	1 kΩ	50 pF	Open	Closed
		or 150 pF	Closed	Open
t <sub>dis</sub>	1 kΩ	50 pF	Open	Closed
		or 150 pF	Closed	Open
t <sub>pd</sub> or t <sub>t</sub>	—	50 pF or 150 pF	Open	Open



NOTES:

- C<sub>L</sub> includes probe and test-fixture capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> = 6 ns, t<sub>f</sub> = 6 ns.
- For clock inputs, f<sub>max</sub> is measured when the input duty cycle is 50%.
- The outputs are measured one at a time with one input transition per measurement.
- t<sub>PZL</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
- t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
- t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCT652DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT652	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HCT652DWE4	ACTIVE	SOIC	DW	24		TBD	Call TI	Call TI	-40 to 85		<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HCT652DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT652	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HCT652DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT652	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HCT652DWRE4	ACTIVE	SOIC	DW	24		TBD	Call TI	Call TI	-40 to 85		<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HCT652DWRG4	ACTIVE	SOIC	DW	24		TBD	Call TI	Call TI	-40 to 85		<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HCT652NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT652NT	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HCT652NTE4	ACTIVE	PDIP	NT	24		TBD	Call TI	Call TI	-40 to 85		<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

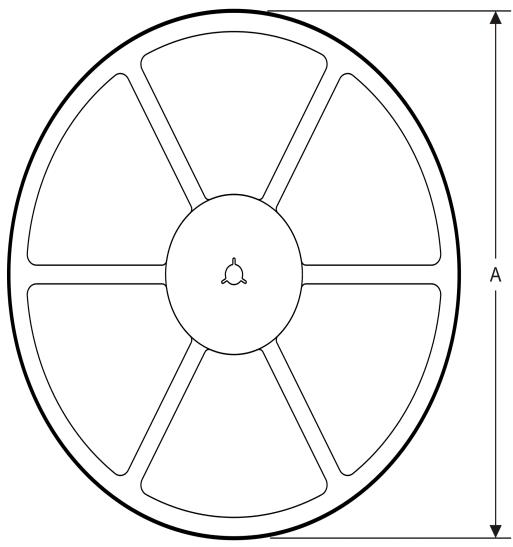
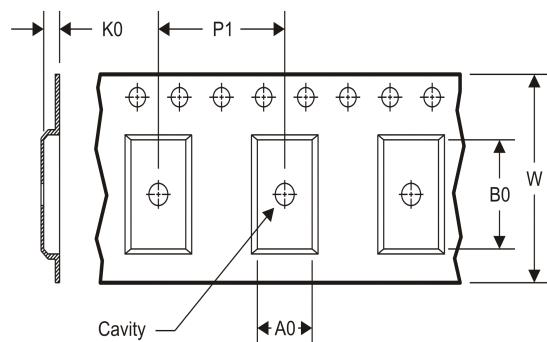
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

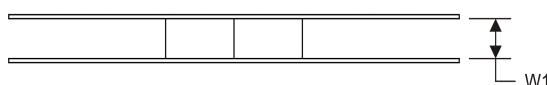
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers


**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT652DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

\*All dimensions are nominal

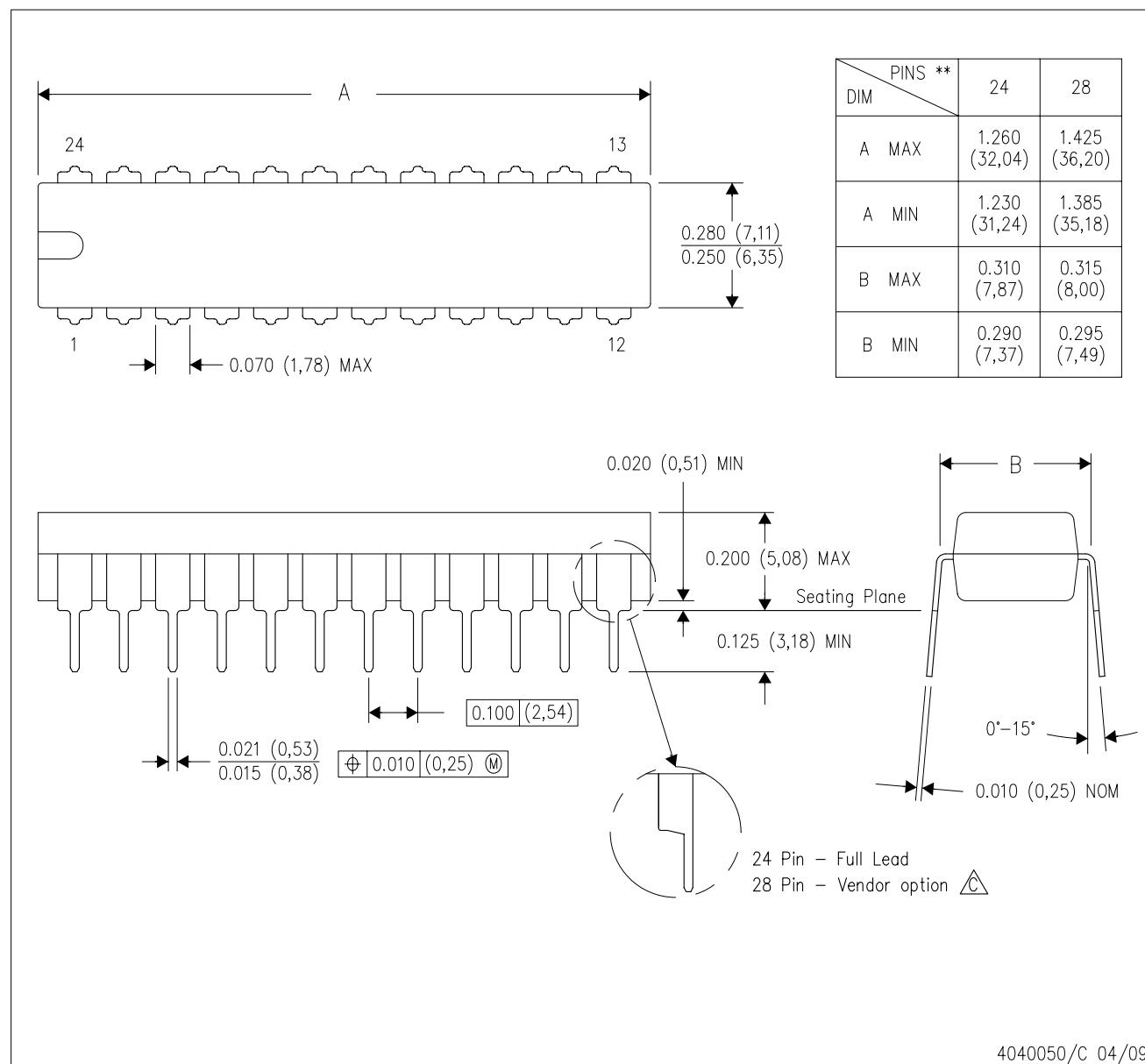
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT652DWR	SOIC	DW	24	2000	367.0	367.0	45.0

## MECHANICAL DATA

NT (R-PDIP-T\*\*)

24 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



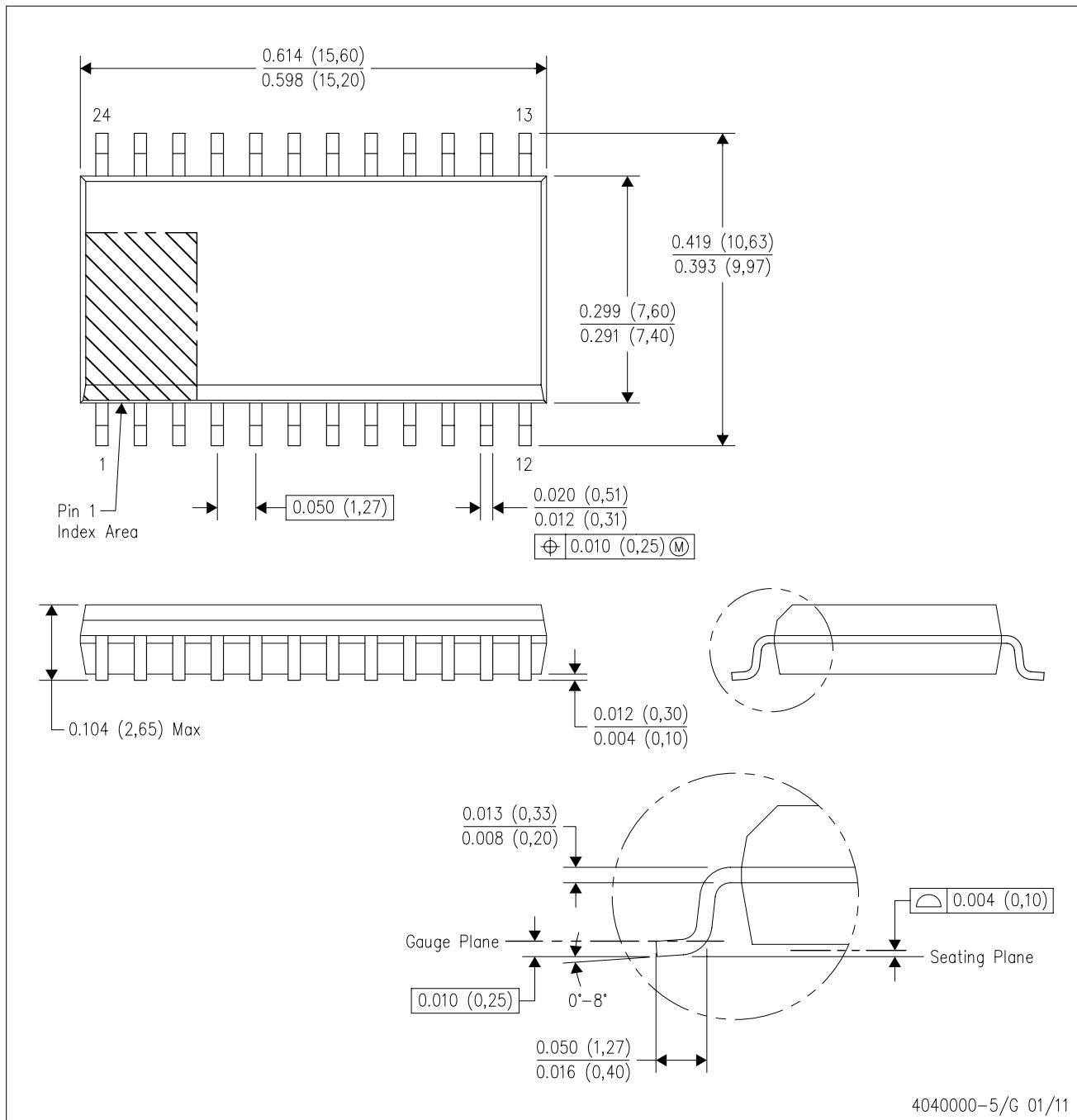
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

△ The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES:

- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AD.

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