SAA7108AE; SAA7109AE

HD-CODEC

Rev. 03 — 6 February 2007 Product data sheet

1. General description

The SAA7108AE; SAA7109AE is a new multistandard video decoder and encoder chip, offering high quality video input and TV output processing as required by PC-99 specifications. It enables hardware manufacturers to implement versatile video functions on a significantly reduced printed-circuit board area at very competitive costs.

Separate pins for supply voltages as well as for I^2C-bus control and boundary scan test have been provided for the video encoder and decoder sections to ensure both flexible handling and optimized noise behavior.

The **video encoder** is used to encode PC graphics data at maximum 1280×1024 resolution (optionally 1920×1080 interlaced) to PAL (50 Hz) or NTSC (60 Hz) video signals. A programmable scaler and anti-flicker filter (maximum 5 lines) ensures properly sized and flicker-free TV display as CVBS or S-video output.

Alternatively, the three Digital-to-Analog Converters (DACs) can output RGB signals together with a TTL composite sync to feed SCART connectors.

When the scaler/interlacer is bypassed, a second VGA monitor can be connected to the RGB outputs and separate H and V-syncs as well, thereby serving as an auxiliary monitor at maximum 1280×1024 resolution/60 Hz (PIXCLK < 85 MHz). Alternatively this port can provide Y, P_B and P_R signals for HDTV monitors.

The encoder section includes a sync/clock generator and on-chip DACs.

All inputs intended to interface to the host graphics controller are designed for low-voltage signals down to 1.1 V and up to 3.45 V.

The **video decoder**, a 9-bit video input processor, is a combination of a 2-channel analog pre-processing circuit including source selection, anti-aliasing filter and Analog-to-Digital Converter (ADC), automatic clamp and gain control, a Clock Generation Circuit (CGC), and a digital multistandard decoder (PAL BGHI, PAL M, PAL N, combination PAL N, NTSC M, NTSC-Japan, NTSC N, NTSC 4.43 and SECAM).

The decoder includes a brightness, contrast and saturation control circuit, a multistandard VBI data slicer and a 27 MHz VBI data bypass. The pure 3.3 V (5 V compatible) CMOS circuit SAA7108AE; SAA7109AE, consisting of an analog front-end and digital video decoder, a digital video encoder and analog back-end, is a highly integrated circuit especially designed for desktop video applications.

The decoder is based on the principle of line-locked clock decoding and is able to decode the color of PAL, SECAM and NTSC signals into ITU-R BT.601 compatible color component values.

The encoder can operate fully independently at its own variable pixel clock, transporting graphics input data, and at the line-locked, single crystal-stable video encoding clock.

As an option, it is possible to slave the video PAL/NTSC encoding to the video decoder clock with the encoder FIFO acting as a buffer to decouple the line-locked decoder clock from the crystal-stable encoder clock.

2. Features

2.1 Video decoder

- Six analog inputs, internal analog source selectors, e.g. 6 × CVBS or (2 × Y/C and 2 × CVBS) or (1 × Y/C and 4 × CVBS)
- Two analog preprocessing channels in differential CMOS style for best S/N performance
- Fully programmable static gain or Automatic Gain Control (AGC) for the selected CVBS or Y/C channel
- Switchable white peak control
- Two built-in analog anti-aliasing filters
- Two 9-bit video CMOS Analog-to-Digital Converters (ADCs), digitized CVBS or Y/C signals are available on the Image Port Data (IPD) port under I^2C-bus control
- On-chip clock generator
- Line-locked system clock frequencies
- Digital PLL for horizontal sync processing and clock generation, horizontal and vertical sync detection
- Requires only one crystal (either 24.576 MHz or 32.11 MHz) for all standards
- Automatic detection of 50 Hz and 60 Hz field frequency, and automatic switching between PAL and NTSC standards
- Luminance and chrominance signal processing for PAL BGHI, PAL N, combination PAL N, PAL M, NTSC M, NTSC-Japan, NTSC N, NTSC 4.43 and SECAM
- User programmable luminance peaking or aperture correction
- Cross-color reduction for NTSC by chrominance comb filtering
- PAL delay line for correcting PAL phase errors
- Brightness Contrast Saturation (BCS) and hue control on-chip
- Two multifunctional real-time output pins controlled by the I^2C-bus
- Multistandard VBI data slicer decoding World Standard Teletext (WST), North-American Broadcast Text System (NABTS), Closed Caption (CC), Wide Screen Signalling (WSS), Video Programming System (VPS), Vertical Interval Time Code (VITC) variants (EBU/SMPTE) etc.
- Standard ITU 656 Y-C_B-C_R 4 : 2 : 2 format (8-bit) on IPD output bus
- Enhanced ITU 656 output format on IPD output bus containing:
  - Active video
  - Raw CVBS data for INTERCAST applications (27 MHz data rate)
  - Decoded VBI data
- Detection of copy protected input signals according to the Macrovision standard. Can be used to prevent unauthorized recording of pay-TV or video tape signals

2.2 Video scaler

- Both up and downscaling
- Conversion to square pixel format
- NTSC to 288 lines (video phone)
- Phase accuracy better than $^{1}/_{64}$ pixel or line, horizontally or vertically
- Independent scaling definitions for odd and even fields
- Anti-alias filter for horizontal scaling
- Provides output as:
  - Scaled active video
  - Raw CVBS data for INTERCAST, WAVE-PHORE, POPCON applications or general VBI data decoding (27 MHz or sample rate converted)
- Local video output for Y-C_B-C_R 4 : 2 : 2 format (VMI, VIP and ZV)

2.3 Video encoder

- Digital PAL/NTSC encoder with integrated high quality scaler and anti-flicker filter for TV output from a PC
- Supports Intel Digital Video Out (DVO) low-voltage interfacing to graphics controller
- 27 MHz crystal-stable subcarrier generation
- Maximum graphics pixel clock 85 MHz at double edged clocking, synthesized on-chip or from external source
- Programmable assignment of clock edge to bytes (in double edged mode)
- Synthesizable pixel clock (PIXCLK) with minimized output jitter, can be used as reference clock for the VGC, as well
- PIXCLK output and bi-phase PIXCLK input (VGC clock loop-through possible)
- Hot-plug detection through dedicated interrupt pin
- Supported VGA resolutions for PAL or NTSC legacy video output up to 1280×1024 graphics data at 60 Hz or 50 Hz frame rate
- Supported VGA resolutions for HDTV output up to 1920×1080 interlaced graphics data at 60 Hz or 50 Hz frame rate
- Three Digital-to-Analog Converters (DACs) for CVBS (BLUE, C_B), VBS (GREEN, CVBS) and C (RED, C_R) at 27 MHz sample rate (signals in parenthesis are optionally selected), all at 10-bit resolution
- Non-interlaced C_B-Y-C_R or RGB input at maximum 4 : 4 : 4 sampling
- Downscaling and upscaling from 50 % to 400 %
- Optional interlaced C_B-Y-C_R input of Digital Versatile Disk (DVD) signals
- Optional non-interlaced RGB output to drive second VGA monitor (bypass mode, maximum 85 MHz)
- 3×256 bytes RGB Look-Up Table (LUT)
- Support for hardware cursor
- HDTV up to 1920×1080 interlaced and 1280×720 progressive, including 3-level sync pulses
- Programmable border color of underscan area
- Programmable 5-line anti-flicker filter
- On-chip 27 MHz crystal oscillator (3rd harmonic or fundamental 27 MHz crystal)
- Fast I^2C-bus control port (400 kHz)

- Encoder can be master or slave
- Adjustable output levels for the DACs
- Programmable horizontal and vertical input synchronization phase
- Programmable horizontal sync output phase
- Internal Color Bar Generator (CBG)
- Optional support of various Vertical Blanking Interval (VBI) data insertion
- Macrovision Pay-per-View copy protection system rev. 7.01, rev. 6.1 and rev. 1.03 (525p) as option; this applies to the SAA7108AE only.

2.4 Common features

- 5 V tolerant digital inputs and I/O ports
- I^2C-bus controlled (full read-back ability by an external controller, bit rate up to 400 kbit/s)
- Versatile Power-save modes
- Boundary scan test circuit complies with the *"IEEE Std. 1149.b1-1994"* (separate ID codes for decoder and encoder)
- LBGA156 package
- Moisture Sensitive Level (MSL): e3

3. Applications

- Notebook (low-power consumption)
- PCMCIA card application
- AGP based graphics cards
- PC editing
- Image processing
- Video phone applications
- INTERCAST and PC teletext applications
- Security applications
- Hybrid satellite set-top boxes

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDD}	digital supply voltage		3.15	3.3	3.45	V
V_{DDA}	analog supply voltage		3.15	3.3	3.45	V
T_{amb}	ambient temperature		0	-	70	°C
P_{A+D}	analog and digital power dissipation	[1]	-	-	1.7	W

[1] Power dissipation is extremely dependent on programming and selected application.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
SAA7108AE	LBGA156	plastic low profile ball grid array package; 156 balls; body 15 × 15 × 1.05 mm	SOT700-1
SAA7109AE			

6. Block diagram

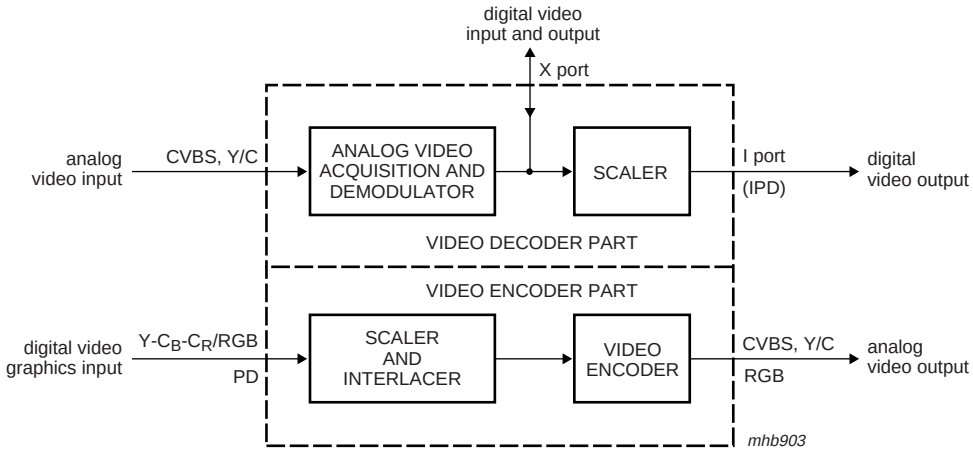


Fig 1. Simplified block diagram

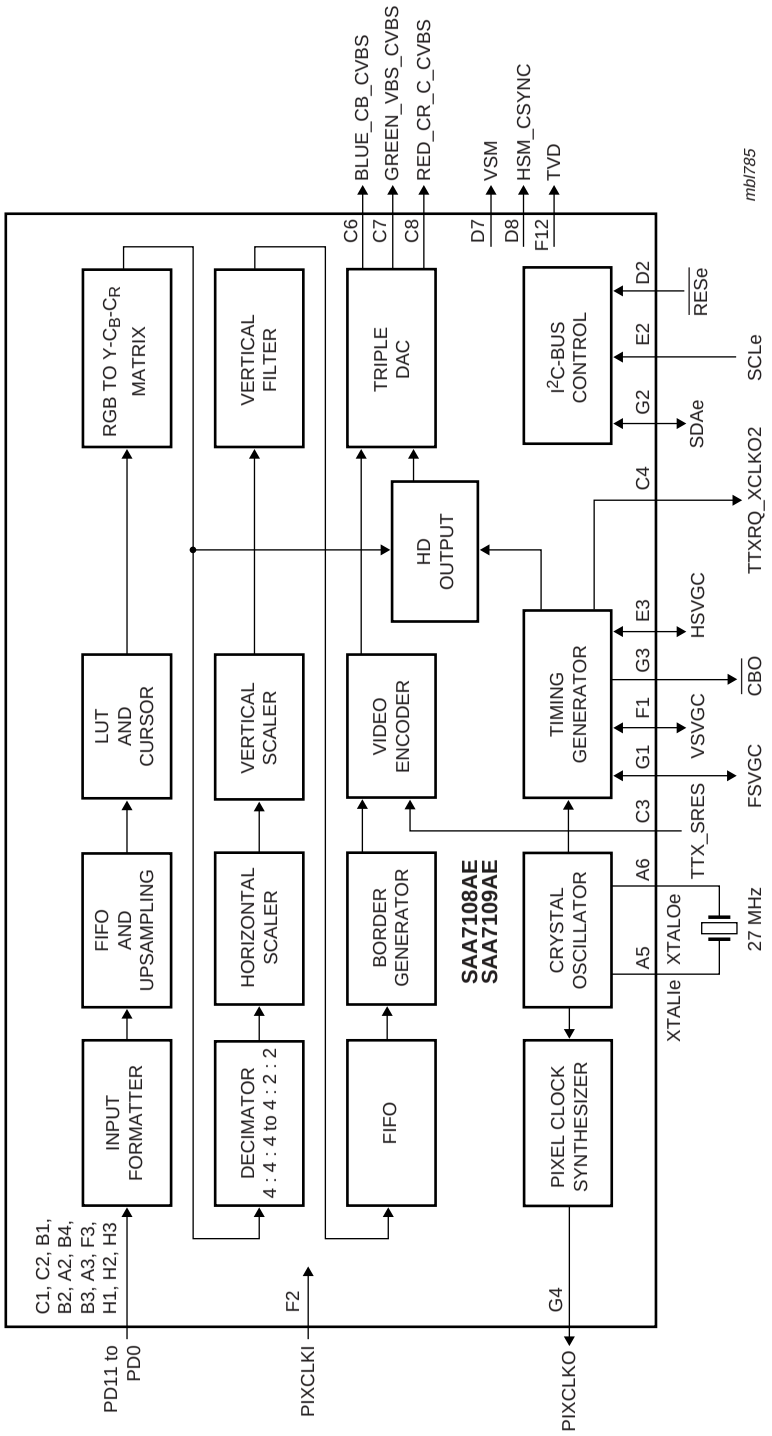
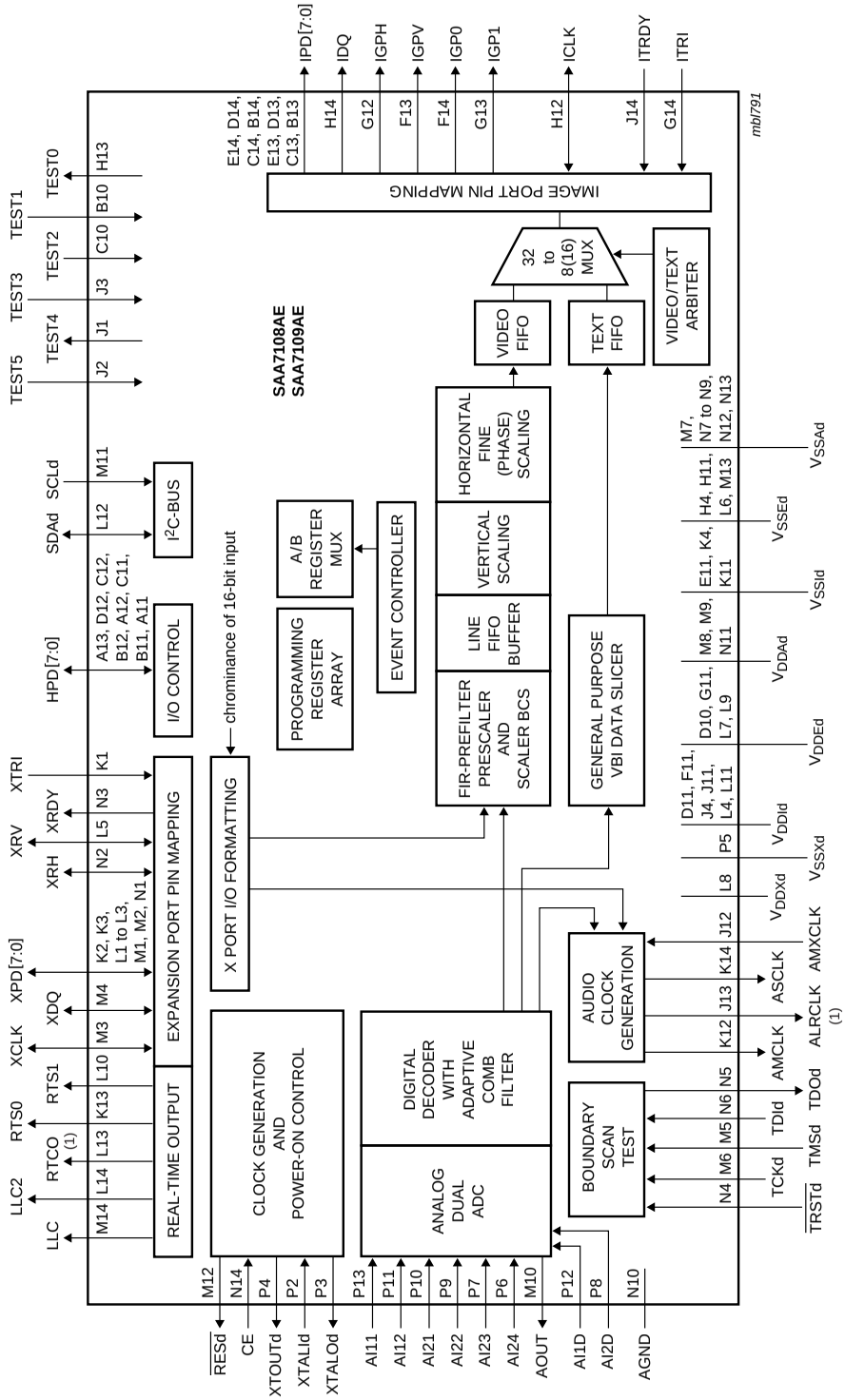


Fig 2. Block diagram (video encoder part)



(1) The pins RTCO and ALRCLK are used for configuration of the I²C-bus interface and the definition of the crystal oscillator frequency at RESET (pin strapping).

Fig 3. Block diagram (video decoder part)

7. Pinning information

7.1 Pinning

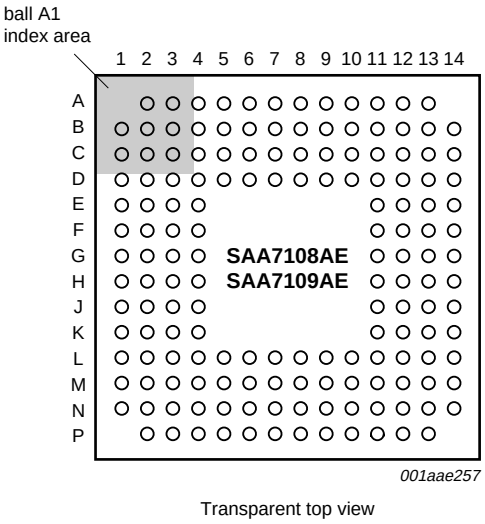


Fig 4. Pin configuration (LBGA156)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A		PD7	PD4	$\overline{\text{TRSTe}}$	XTALIe	XTALOe	DUMP	V_{SSXe}	RSET	V_{DDAe}	HPD0	HPD3	HPD7	
B	PD9	PD8	PD5	PD6	TDIe	V_{DDAe}	DUMP	V_{SSAe}	V_{DDAe}	TEST1	HPD1	HPD4	IPD0	IPD4
C	PD11	PD10	TTX_SRES	TTXRQ_XCLKO2	V_{SSIe}	BLUE_CB_CVBS	GREEN_VBS_CVBS	RED_CR_C_CVBS	V_{DDAe}	TEST2	HPD2	HPD5	IPD1	IPD5
D	TDOe	$\overline{\text{RESe}}$	TMSe	V_{DDIEe}	V_{SSIe}	V_{DDXe}	VSM	HSM_CSYNC	V_{DDAe}	V_{DDEd}	V_{DDId}	HPD6	IPD2	IPD6
E	TCKe	SCLe	HSVGC	V_{SSEe}							V_{SSId}	n.c.	IPD3	IPD7
F	VSVGC	PIXCLKI	PD3	$V_{DD(DVO)}$							V_{DDId}	TVD	IGPV	IGP0
G	FSVGC	SDAe	$\overline{\text{CBO}}$	PIXCLKO							V_{DDEd}	IGPH	IGP1	ITRI
H	PD2	PD1	PD0	V_{SSEd}							V_{SSEd}	ICLK	TEST0	IDQ
J	TEST4	TEST5	TEST3	V_{DDId}							V_{DDId}	AMXCLK	ALRCLK	ITRDY
K	XTRI	XPD7	XPD6	V_{SSId}							V_{SSId}	AMCLK	RTS0	ASCLK
L	XPD5	XPD4	XPD3	V_{DDId}	XRV	V_{SSEd}	V_{DDEd}	V_{DDXd}	V_{DDEd}	RTS1	V_{DDId}	SDAd	RTCO	LLC2
M	XPD2	XPD1	XCLK	XDQ	TMSd	TCKd	V_{SSAd}	V_{DDAd}	V_{DDAd}	AOUT	SCLd	$\overline{\text{RESd}}$	V_{SSEd}	LLC
N	XPD0	XRH	XRDY	$\overline{\text{TRSTd}}$	TDOd	TDId	V_{SSAd}	V_{SSAd}	V_{SSAd}	AGND	V_{DDAd}	V_{SSAd}	V_{SSAd}	CE
P		XTALId	XTALOd	XTOUTd	V_{SSXd}	AI24	AI23	AI2D	AI22	AI21	AI12	AI1D	AI11	

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Fig 5. Pin configuration (LBGA156 top view)

Table 3. Pin allocation table

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
A2	PD7	A3	PD4	A4	$\overline{TRSTe}$	A5	XTALIe
A6	XTALOe	A7	DUMP	A8	V_{SSXe}	A9	RSET
A10	V_{DDAe}	A11	HPD0	A12	HPD3	A13	HPD7
B1	PD9	B2	PD8	B3	PD5	B4	PD6
B5	TDIe	B6	V_{DDAe}	B7	DUMP	B8	V_{SSAe}
B9	V_{DDAe}	B10	TEST1	B11	HPD1	B12	HPD4
B13	IPD0	B14	IPD4				
C1	PD11	C2	PD10	C3	TTX_SRES	C4	TTXRQ_XCLKO2
C5	V_{SSIe}	C6	BLUE_CB_CVBS	C7	GREEN_VBS_CVBS	C8	RED_CR_C_CVBS
C9	V_{DDAe}	C10	TEST2	C11	HPD2	C12	HPD5
C13	IPD1	C14	IPD5				
D1	TDOe	D2	$\overline{RESe}$	D3	TMSe	D4	V_{DDIEe}
D5	V_{SSIe}	D6	V_{DDXe}	D7	VSM	D8	HSM_CSYNC
D9	V_{DDAe}	D10	V_{DDEd}	D11	V_{DDId}	D12	HPD6
D13	IPD2	D14	IPD6				
E1	TCKe	E2	SCLe	E3	HSVGC	E4	V_{SSEe}
E11	V_{SSId}	E12	n.c.	E13	IPD3	E14	IPD7
F1	VSVGC	F2	PIXCLKI	F3	PD3	F4	$V_{DD(DVO)}$
F11	V_{DDId}	F12	TVD	F13	IGPV	F14	IGP0
G1	FSVGC	G2	SDAe	G3	$\overline{CBO}$	G4	PIXCLKO
G11	V_{DDEd}	G12	IGPH	G13	IGP1	G14	ITRI
H1	PD2	H2	PD1	H3	PD0	H4	V_{SSEd}
H11	V_{SSEd}	H12	ICLK	H13	TEST0	H14	IDQ
J1	TEST4	J2	TEST5	J3	TEST3	J4	V_{DDId}
J11	V_{DDId}	J12	AMXCLK	J13	ALRCLK	J14	ITRDY
K1	XTRI	K2	XPD7	K3	XPD6	K4	V_{SSId}
K11	V_{SSId}	K12	AMCLK	K13	RTS0	K14	ASCLK
L1	XPD5	L2	XPD4	L3	XPD3	L4	V_{DDId}
L5	XRV	L6	V_{SSEd}	L7	V_{DDEd}	L8	V_{DDXd}
L9	V_{DDEd}	L10	RTS1	L11	V_{DDId}	L12	SDAd
L13	RTCO	L14	LLC2				
M1	XPD2	M2	XPD1	M3	XCLK	M4	XDQ
M5	TMSd	M6	TCKd	M7	V_{SSAd}	M8	V_{DDAd}
M9	V_{DDAd}	M10	AOUT	M11	SCLd	M12	$\overline{RESd}$
M13	V_{SSEd}	M14	LLC				
N1	XPD0	N2	XRH	N3	XRDY	N4	$\overline{TRSTd}$
N5	TDOd	N6	TDId	N7	V_{SSAd}	N8	V_{SSAd}
N9	V_{SSAd}	N10	AGND	N11	V_{DDAd}	N12	V_{SSAd}
N13	V_{SSAd}	N14	CE				

Table 3. Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
P2	XTALId	P3	XTALOd	P4	XTOUTd	P5	V_{SSXd}
P6	AI24	P7	AI23	P8	AI2D	P9	AI22
P10	AI21	P11	AI12	P12	AI1D	P13	AI11

7.2 Pin description

Table 4. Pin description

Symbol	Pin	Type[1]	Description
PD7	A2	I	MSB of encoder input bus with C_B-Y-C_R 4 : 2 : 2; see Table 12 to Table 18 for pin assignment
PD4	A3	I	MSB – 3 of encoder input bus with C_B-Y-C_R 4 : 2 : 2; see Table 12 to Table 18 for pin assignment
$\overline{TRSTe}$	A4	I/pu	test reset input for Boundary Scan Test (BST) (encoder); active LOW; with internal pull-up[2][3]
XTALIe	A5	I	27 MHz crystal input (encoder)
XTALOe	A6	O	27 MHz crystal output (encoder)
DUMP	A7	O	DAC reference pin (encoder); 12 Ω resistor connected to V_{SSAe}
V_{SSXe}	A8	S	ground for oscillator (encoder)
RSET	A9	O	DAC reference pin (encoder); 1 kΩ resistor connected to V_{SSAe}
V_{DDAe}	A10	S	3.3 V analog supply voltage (encoder)
HPD0	A11	I/O	MSB – 7 of Host Port Data (HPD) output bus
HPD3	A12	I/O	MSB – 4 of HPD output bus
HPD7	A13	I/O	MSB of HPD output bus
PD9	B1	I	see Table 12, Table 17 and Table 18 for pin assignment with different encoder input formats
PD8	B2	I	see Table 12, Table 17 and Table 18 for pin assignment with different encoder input formats
PD5	B3	I	MSB – 2 of encoder input bus with C_B-Y-C_R 4 : 2 : 2; see Table 12 to Table 18 for pin assignment
PD6	B4	I	MSB – 1 of encoder input bus with C_B-Y-C_R 4 : 2 : 2; see Table 12 to Table 18 for pin assignment
TDIe	B5	I/pu	test data input for BST (encoder)[4]
V_{DDAe}	B6	S	3.3 V analog supply voltage (encoder)
DUMP	B7	O	DAC reference pin (encoder); connected to A7
V_{SSAe}	B8	S	analog ground (encoder)
V_{DDAe}	B9	S	3.3 V analog supply voltage (encoder)
TEST1	B10	I	scan test input 1; do not connect
HPD1	B11	I/O	MSB – 6 of HPD output bus
HPD4	B12	I/O	MSB – 3 of HPD output bus
IPD0	B13	O	MSB – 7 of IPD output bus
IPD4	B14	O	MSB – 3 of Image Port Data (IPD) output bus
PD11	C1	I	see Table 12, Table 17 and Table 18 for pin assignment with different encoder input formats

Table 4. Pin description *...continued*

Symbol	Pin	Type[1]	Description
PD10	C2	I	see Table 12, Table 17 and Table 18 for pin assignment with different encoder input formats
TTX_SRES	C3	I	teletext input or sync reset input (encoder)
TTXRQ_XCLKO2	C4	O	teletext request output or 13.5 MHz clock output of the crystal oscillator (encoder)
V_{SSIe}	C5	S	digital ground core (encoder)
BLUE_CB_CVBS	C6	O	BLUE or C_B or CVBS output
GREEN_VBS_CVBS	C7	O	GREEN or VBS or CVBS output
RED_CR_C_CVBS	C8	O	RED or C_R or C or CVBS output
V_{DDAe}	C9	S	3.3 V analog supply voltage (encoder)
TEST2	C10	I	scan test input 2; do not connect
HPD2	C11	I/O	MSB – 5 of HPD output bus
HPD5	C12	I/O	MSB – 2 of HPD output bus
IPD1	C13	O	MSB – 6 of IPD output bus
IPD5	C14	O	MSB – 2 of IPD output bus
TDOe	D1	O	test data output for BST (encoder)[4]
$\overline{RESe}$	D2	I	reset input (encoder); active LOW
TMSe	D3	I/pu	test mode select input for BST (encoder)[4]
V_{DDIEe}	D4	S	3.3 V digital supply voltage for core and peripheral cells (encoder)
V_{SSIe}	D5	S	digital ground core (encoder)
V_{DDXe}	D6	S	3.3 V supply voltage for oscillator (encoder)
VSM	D7	O	vertical synchronization output to VGA monitor (non-interlaced)
HSM_CSYNC	D8	O	horizontal synchronization output to VGA monitor (non-interlaced) or composite sync for RGB-SCART
V_{DDAe}	D9	S	3.3 V analog supply voltage (encoder)
V_{DDEd}	D10	S	3.3 V digital supply voltage for peripheral cells (decoder)
V_{DDId}	D11	S	3.3 V digital supply voltage for core (decoder)
HPD6	D12	I/O	MSB – 1 of HPD output bus
IPD2	D13	O	MSB – 5 of IPD output bus
IPD6	D14	O	MSB – 1 of IPD output bus
TCKe	E1	I/pu	test clock input for BST (encoder)[4]
SCLe	E2	I(/O)	serial clock input (I^2C-bus encoder) with inactive output path
HSVGC	E3	I/O	horizontal synchronization output to Video Graphics Controller (VGC) (optional input)
V_{SSEe}	E4	S	digital ground peripheral cells (encoder)
V_{SSId}	E11	S	digital ground core (decoder)
n.c.	E12	-	not connected
IPD3	E13	O	MSB – 4 of IPD output bus
IPD7	E14	O	MSB of IPD output bus
VSVGC	F1	I/O	vertical synchronization output to VGC (optional input)
PIXCLKI	F2	I	pixel clock input (looped through)

Table 4. Pin description *...continued*

Symbol	Pin	Type[1]	Description
PD3	F3	I	MSB – 4 of encoder input bus with C_B-Y-C_R 4 : 2 : 2; see Table 12 to Table 18 for pin assignment
$V_{DD(DVO)}$	F4	S	digital supply voltage for DVO cells
V_{DDId}	F11	S	3.3 V digital supply voltage for core (decoder)
TVD	F12	O	TV detector; hot-plug interrupt pin; HIGH if TV is connected
IGPV	F13	O	multi-purpose vertical reference output with IPD output bus
IGP0	F14	O	general purpose output signal 0 with IPD output bus
FSVGC	G1	I/O	frame synchronization output to VGC (optional input)
SDAe	G2	I/O	serial data input/output (I^2C-bus encoder)
$\overline{CBO}$	G3	O	composite blanking output to VGC; active LOW
PIXCLKO	G4	O	pixel clock output to VGC
V_{DDEd}	G11	S	3.3 V digital supply voltage for peripheral cells (decoder)
IGPH	G12	O	multi-purpose horizontal reference output with IPD output bus
IGP1	G13	O	general purpose output signal 1 with IPD output bus
ITRI	G14	I(/O)	programmable control signals for IPD output bus
PD2	H1	I	MSB – 5 of encoder input bus with C_B-Y-C_R 4 : 2 : 2; see Table 12 to Table 18 for pin assignment
PD1	H2	I	MSB – 6 of encoder input bus with C_B-Y-C_R 4 : 2 : 2; see Table 12 to Table 18 for pin assignment
PD0	H3	I	MSB – 7 of encoder input bus with C_B-Y-C_R 4 : 2 : 2; see Table 12 to Table 18 for pin assignment
V_{SSEd}	H4	S	digital ground for peripheral cells (decoder)
V_{SSEd}	H11	S	digital ground for peripheral cells (decoder)
ICLK	H12	I/O	clock for IPD output bus (optional clock input)
TEST0	H13	O	scan test output; do not connect
IDQ	H14	O	data qualifier for IPD output bus
TEST4	J1	O	scan test output; do not connect
TEST5	J2	I	scan test input; do not connect
TEST3	J3	I	scan test input; do not connect
V_{DDId}	J4	S	3.3 V digital supply voltage for core (decoder)
V_{DDId}	J11	S	3.3 V digital supply voltage for core (decoder)
AMXCLK	J12	I	audio master external clock input
ALRCLK	J13	(I/)O	audio left/right clock output; can be strapped[5][6] to supply via a 3.3 kΩ resistor to indicate that the default 24.576 MHz crystal (pin ALRCLK = LOW; internal pull-down) has been replaced by a 32.110 MHz crystal (pin ALRCLK = HIGH)
ITRDY	J14	I	target ready input for IPD output bus
XTRI	K1	I	control signal for all X port pins
XPD7	K2	I/O	MSB of XPD bus
XPD6	K3	I/O	MSB – 1 of XPD bus
V_{SSId}	K4	S	digital ground core (decoder)
V_{SSId}	K11	S	digital ground core (decoder)
AMCLK	K12	O	audio master clock output, must be less than 50 % of crystal clock

Table 4. Pin description *...continued*

Symbol	Pin	Type[1]	Description
RTS0	K13	O	real-time status or sync information line 0
ASCLK	K14	O	audio serial clock output
XPD5	L1	I/O	MSB – 2 of XPD bus
XPD4	L2	I/O	MSB – 3 of XPD bus
XPD3	L3	I/O	MSB – 4 of XPD bus
V_{DDId}	L4	S	3.3 V digital supply voltage for core (decoder)
XRV	L5	I/O	vertical reference for XPD bus
V_{SSEd}	L6	S	digital ground for peripheral cells (decoder)
V_{DDEd}	L7	S	3.3 V digital supply voltage for peripheral cells (decoder)
V_{DDXd}	L8	S	3.3 V supply voltage for oscillator (decoder)
V_{DDEd}	L9	S	3.3 V digital supply voltage for peripheral cells (decoder)
RTS1	L10	O	real-time status or sync information line 1
V_{DDId}	L11	S	3.3 V digital supply voltage for core (decoder)
SDAd	L12	I/O	serial data input/output (I^2C-bus decoder)
RTCO	L13	(I/)O	real-time control output; contains information about actual system clock frequency, field rate, odd/even sequence, decoder status, subcarrier frequency and phase and PAL sequence (see external document *"How to use Real Time Control (RTC)"*, available on request); the RTCO pin[5][7] is enabled via I^2C-bus bit RTCE; see Table 162
LLC2	L14	O	line-locked ½ clock output (13.5 MHz nominal)
XPD2	M1	I/O	MSB – 5 of XPD bus
XPD1	M2	I/O	MSB – 6 of XPD bus
XCLK	M3	I/O	clock for XPD bus
XDQ	M4	I/O	data qualifier for XPD bus
TMSd	M5	I/pu	test mode select input for BST (decoder)[4]
TCKd	M6	I/pu	test clock input for BST (decoder)[4]
V_{SSAd}	M7	S	analog ground (decoder)
V_{DDAd}	M8	S	3.3 V analog supply voltage (decoder)
V_{DDAd}	M9	S	3.3 V analog supply voltage (decoder)
AOUT	M10	O	do not connect; analog test output
SCLd	M11	I(/O)	serial clock input (I^2C-bus decoder) with inactive output path
$\overline{RESd}$	M12	O	reset output signal; active LOW (decoder)
V_{SSEd}	M13	S	digital ground for peripheral cells (decoder)
LLC	M14	O	line-locked clock output (27 MHz nominal)
XPD0	N1	I/O	MSB – 7 of XPD bus
XRH	N2	I/O	horizontal reference for XPD bus
XRDY	N3	O	data input ready for XPD bus
$\overline{TRSTd}$	N4	I/pu	test reset input for BST (decoder); active LOW; with internal pull-up[2][3]
TDOd	N5	O	test data output for BST (decoder)[4]
TDId	N6	I/pu	test data input for BST (decoder)[4]
V_{SSAd}	N7	S	analog ground (decoder)
V_{SSAd}	N8	S	analog ground (decoder)

Table 4. Pin description *...continued*

Symbol	Pin	Type[1]	Description
V_{SSAd}	N9	S	analog ground (decoder)
AGND	N10	S	analog ground (decoder) connected to substrate
V_{DDAd}	N11	S	3.3 V analog supply voltage (decoder)
V_{SSAd}	N12	S	analog ground (decoder)
V_{SSAd}	N13	S	analog ground (decoder)
CE	N14	I	chip enable or reset input (with internal pull-up)
XTALId	P2	I	27 MHz crystal input (decoder)
XTALOd	P3	O	27 MHz crystal output (decoder)
XTOUTd	P4	O	crystal oscillator output signal (decoder); auxiliary signal
V_{SSXd}	P5	S	ground for crystal oscillator (decoder)
AI24	P6	I	analog input 24
AI23	P7	I	analog input 23
AI2D	P8	I	differential analog input for channel 2; connect to ground via a capacitor
AI22	P9	I	analog input 22
AI21	P10	I	analog input 21
AI12	P11	I	analog input 12
AI1D	P12	I	differential analog input for channel 1; connect to ground via a capacitor
AI11	P13	I	analog input 11

[1] Pin type: I = input, O = output, S = supply, pu = pull-up.

[2] For board design without boundary scan implementation connect $\overline{\text{TRSTe}}$ and $\overline{\text{TRSTd}}$ to ground.

[3] This pin provides easy initialization of the Boundary Scan Test (BST) circuit. $\overline{\text{TRSTe}}$ and $\overline{\text{TRSTd}}$ can be used to force the Test Access Port (TAP) controller to the TEST_LOGIC_RESET state (normal operation) at once.

[4] In accordance with the *"IEEE1149.1"* standard the pins TDIe (TDId), TMSe (TMSd), TCKe (TCKd) and $\overline{\text{TRSTe}}$ ($\overline{\text{TRSTd}}$) are input pins with an internal pull-up resistor and TDOe (TDOd) is a 3-state output pin.

[5] Pin strapping is done by connecting the pin to supply via a 3.3 kΩ resistor. During the power-up reset sequence the corresponding pins are switched to input mode to read the strapping level. For the default setting no strapping resistor is necessary (internal pull-down).

[6] Pin ALRCLK = LOW for 24.576 MHz crystal (default); pin ALRCLK = HIGH for 32.110 MHz crystal.

[7] Pin RTCO operates as I^2C-bus slave address pin; pin RTCO = LOW for slave address 42h/43h (default); pin RTCO = HIGH for slave address 40h/41h.

8. Functional description of digital video encoder part

The digital video encoder part encodes digital luminance and color difference signals (C_B-Y-C_R) or digital RGB signals into analog CVBS, S-video and, optionally, RGB or C_R-Y-C_B signals. NTSC M, PAL B/G and sub-standards are supported.

The SAA7108AE; SAA7109AE can be directly connected to a PC video graphics controller with a maximum resolution of 1280×1024 (progressive) or 1920×1080 (interlaced) at a 50 Hz or 60 Hz frame rate. A programmable scaler scales the computer graphics picture so that it will fit into a standard TV screen with an adjustable underscan area. Non-interlaced-to-interlaced conversion is optimized with an adjustable anti-flicker filter for a flicker-free display at a very high sharpness.

Besides the most common 16-bit 4 : 2 : 2 C_B-Y-C_R input format (using 8 pins with double edge clocking), other C_B-Y-C_R and RGB formats are also supported; see Table 12 to Table 18.

A complete 3 bytes × 256 bytes Look-Up Table (LUT), which can be used, for example, as a separate gamma corrector, is located in the RGB domain; it can be loaded either through the video input port Pixel Data (PD) or via the I^2C-bus.

The SAA7108AE; SAA7109AE supports a 32-bit × 32-bit × 2-bit hardware cursor, the pattern of which can also be loaded through the video input port or via the I^2C-bus.

It is also possible to encode interlaced 4 : 2 : 2 video signals such as PC-DVD; for that the anti-flicker filter, and in most cases the scaler, will simply be bypassed.

Besides the applications for video output, the SAA7108AE; SAA7109AE can also be used for generating a kind of auxiliary VGA output, when the RGB non-interlaced input signal is fed to the DACs. This may be of interest for example, when the graphics controller provides a second graphics window at its video output port.

The basic encoder function consists of subcarrier generation, color modulation and insertion of synchronization signals at a crystal-stable clock rate of 13.5 MHz (independent of the actual pixel clock used at the input side), corresponding to an internal 4 : 2 : 2 bandwidth in the luminance/color difference domain. Luminance and chrominance signals are filtered in accordance with the standard requirements of *'RS-170-A'* and *'ITU-R BT.470-3'*.

For ease of analog post filtering the signals are twice oversampled to 27 MHz before digital-to-analog conversion.

The total filter transfer characteristics (scaler and anti-flicker filter are not taken into account) are illustrated in Figure 6 to Figure 11. All three DACs are realized with full 10-bit resolution. The C_R-Y-C_B to RGB dematrix can be bypassed (optionally) in order to provide the upsampled C_R-Y-C_B input signals.

The 8-bit multiplexed C_B-Y-C_R formats are *'ITU-R BT.656'* (D1 format) compatible, but the SAV and EAV codes can be decoded optionally, when the device is operated in Slave mode. For assignment of the input data to the rising or falling clock edge see Table 12 to Table 18.

In order to display interlaced RGB signals through a euro-connector TV set, a separate digital composite sync signal (pin HSM_CSYNC) can be generated; it can be advanced up to 31 periods of the 27 MHz crystal clock in order to be adapted to the RGB processing of a TV set.

The SAA7108AE; SAA7109AE synthesizes all necessary internal signals, color subcarrier frequency and synchronization signals from that clock.

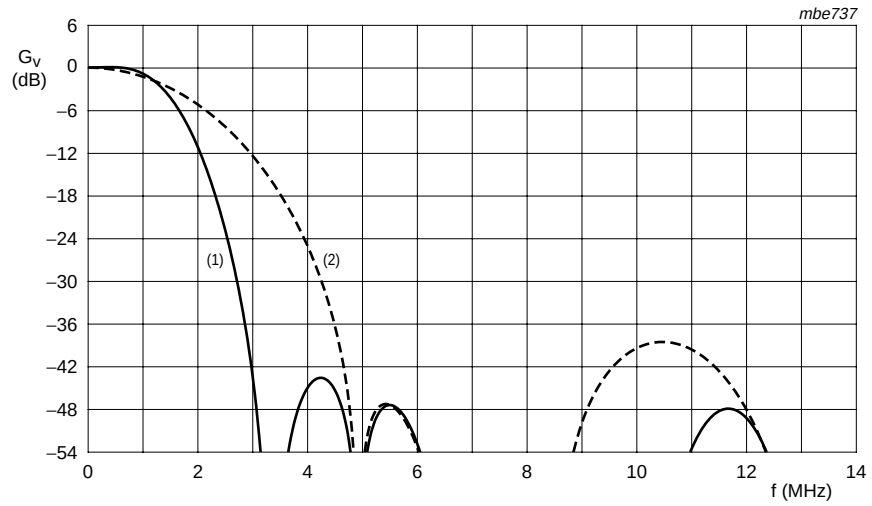
Wide screen signalling data can be loaded via the I^2C-bus and is inserted into line 23 for standards using a 50 Hz field rate.

VPS data for program dependent automatic start and stop of such featured VCRs is loadable via the I^2C-bus.

The IC also contains closed caption and extended data services encoding (line 21), and supports teletext insertion for the appropriate bit stream format at a 27 MHz clock rate (see Figure 66). It is also possible to load data for the copy generation management system into line 20 of every field (525/60 line counting).

A number of possibilities are provided for setting different video parameters such as:

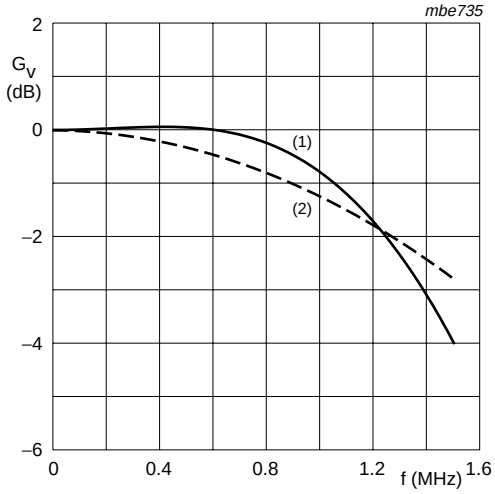
- Black and blanking level control
- Color subcarrier frequency
- Variable burst amplitude etc.



(1) SCBW = 1.

(2) SCBW = 0.

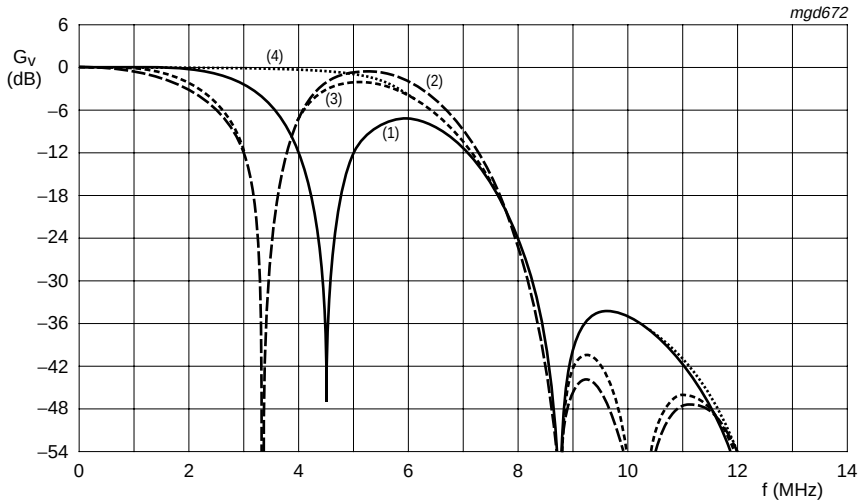
Fig 6. Chrominance transfer characteristic



(1) SCBW = 1.

(2) SCBW = 0.

Fig 7. Chrominance transfer characteristic (enlargement of Figure 6)



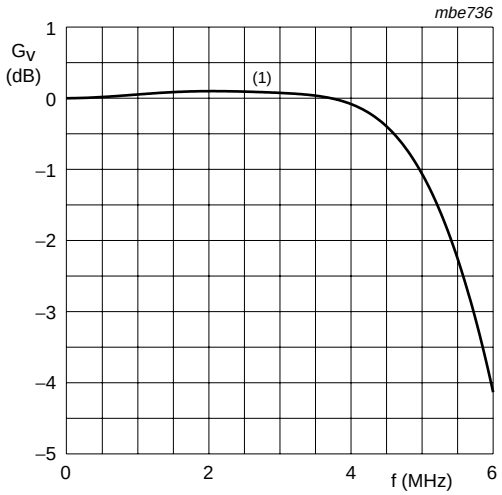
(1) CCRS[1:0] = 01.

(2) CCRS[1:0] = 10.

(3) CCRS[1:0] = 11.

(4) CCRS[1:0] = 00.

Fig 8. Luminance transfer characteristic (excluding scaler)



(1) CCRS[1:0] = 00.

Fig 9. Luminance transfer characteristic (excluding scaler) (enlargement of Figure 8)

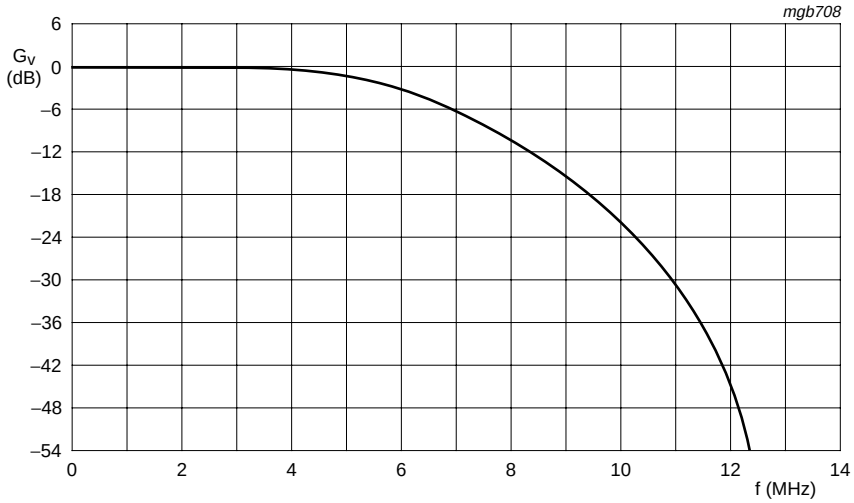


Fig 10. Luminance transfer characteristic in RGB (excluding scaler)

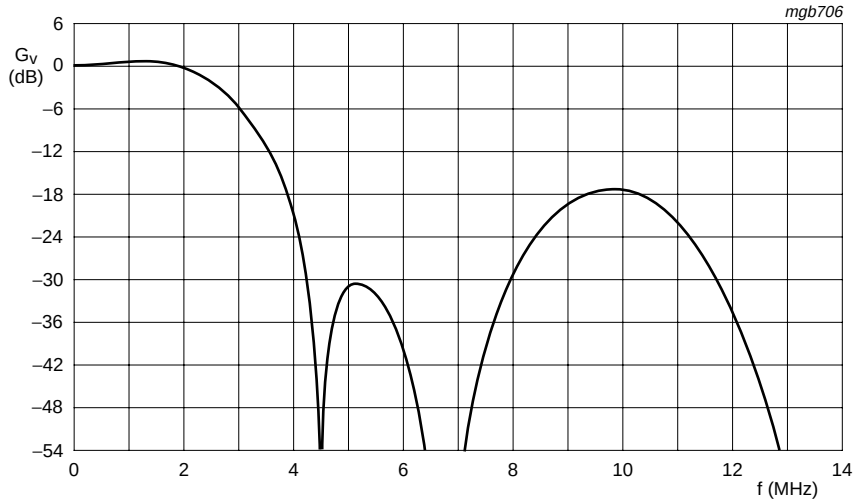


Fig 11. Color difference transfer characteristic in RGB (excluding scaler)

8.1 Reset conditions

To activate the reset, a pulse of at least 2 crystal clocks duration is required.

During reset ($\overline{\text{RESe}}$ = LOW) plus an extra 32 crystal clock periods, FSVGC, VSVGC, $\overline{\text{CBO}}$, HSVGC and TTX_SRES are set to input mode and HSM_CSYNC and VSM are set to 3-state. A reset also forces the I^2C-bus interface to abort any running bus transfer and sets it into receive condition.

After reset, the state of the I/Os and other functions is defined by the strapping pins until an I^2C-bus access redefines the corresponding registers; see Table 5.

Table 5. Strapping pins

Pin	Tied	Preset
FSVGC (pin G1)	LOW	NTSC M encoding, PIXCLK fits to 640 × 480 graphics input
	HIGH	PAL B/G encoding, PIXCLK fits to 640 × 480 graphics input
VSVGC (pin F1)	LOW	4 : 2 : 2 Y-C_B-C_R graphics input (format 0)
	HIGH	4 : 4 : 4 RGB graphics input (format 3)
$\overline{\text{CBO}}$ (pin G3)	LOW	input demultiplex phase: LSB = LOW
	HIGH	input demultiplex phase: LSB = HIGH
HSVGC (pin E3)	LOW	input demultiplex phase: MSB = LOW
	HIGH	input demultiplex phase: MSB = HIGH
TTXRQ_XCLKO2 (pin C4)	LOW	slave (FSVGC, VSVGC and HSVGC are inputs, internal color bar is active)
	HIGH	master (FSVGC, VSVGC and HSVGC are outputs)

8.2 Input formatter

The input formatter converts all accepted PD input data formats, either RGB or Y-C_B-C_R, to a common internal RGB or Y-C_B-C_R data stream.

When double-edge clocking is used, the data is internally split into portions PPD1 and PPD2. The clock edge assignment must be set according to the I^{2}C-bus control bits SLOT and EDGE for correct operation.

If Y-C_B-C_R is being applied as a 27 MB/s data stream, the output of the input formatter can be used directly to feed the video encoder block.

The horizontal upscaling is supported via the input formatter. According to the programming of the pixel clock dividers (see Section 8.10), it will sample up the data stream to 1 $\times$, 2 $\times$ or 4 $\times$ the input data rate. An optional interpolation filter is available. The clock domain transition is handled by a 4 entries wide FIFO which gets initialized every field or explicitly at request. A bypass for the FIFO is available, especially for high input data rates.

8.3 RGB LUT

The three 256-byte RAMs of this block can be addressed by three 8-bit wide signals, thus it can be used to build any transformation, e.g. a gamma correction for RGB signals. In the event that the indexed color data is applied, the RAMs are addressed in parallel.

The LUTs can either be loaded by an I^{2}C-bus write access or can be part of the pixel data input through the PD port. In the latter case, 256 bytes $\times$ 3 bytes for the R, G and B LUT are expected at the beginning of the input video line, two lines before the line that has been defined as first active line, until the middle of the line immediately preceding the first active line. The first 3 bytes represent the first RGB LUT data, and so on.

8.4 Cursor insertion

A 32 dots $\times$ 32 dots cursor can be overlaid as an option; the bit map of the cursor can be uploaded by an I^{2}C-bus write access to specific registers or in the pixel data input through the PD port. In the latter case, the 256 bytes defining the cursor bit map (2 bits per pixel) are expected immediately following the last RGB LUT data in the line preceding the first active line.

The cursor bit map is set up as follows: each pixel occupies 2 bits. The meaning of these bits depends on the CMODE I^{2}C-bus register as described in Table 8. Transparent means that the input pixels are passed through, the ‘cursor colors’ can be programmed in separate registers.

The bit map is stored with 4 pixels per byte, aligned to the least significant bit. So the first pixel is in bits 0 and 1, the next pixel in bits 3 and 4 and so on. The first index is the column, followed by the row; index 0,0 is the upper left corner.

Table 6. Layout of a byte in the cursor bit map

D7		D6		D5		D4		D3		D2		D1		D0	
pixel n + 3				pixel n + 2				pixel n + 1				pixel n			
D1		D0		D1		D0		D1		D0		D1		D0	

For each direction, there are 2 registers controlling the position of the cursor, one controls the position of the 'hot spot', the other register controls the insertion position. The hot spot is the 'tip' of the pointer arrow. It can have any position in the bit map. The actual position registers describe the co-ordinates of the hot spot. Again 0,0 is the upper left corner. While it is not possible to move the hot spot beyond the left respectively upper screen border, this is perfectly legal for the right respectively lower border. It should be noted that the cursor position is described relative to the input resolution.

Table 7. Cursor bit map

Byte	D7 D6	D5 D4	D3 D2	D1 D0
0	row 0 column 3	row 0 column 2	row 0 column 1	row 0 column 0
1	row 0 column 7	row 0 column 6	row 0 column 5	row 0 column 4
2	row 0 column 11	row 0 column 10	row 0 column 9	row 0 column 8
...	...	...	...	...
6	row 0 column 27	row 0 column 26	row 0 column 25	row 0 column 24
7	row 0 column 31	row 0 column 30	row 0 column 29	row 0 column 28
...	...	...	...	...
254	row 31 column 27	row 31 column 26	row 31 column 25	row 31 column 24
255	row 31 column 31	row 31 column 30	row 31 column 29	row 31 column 28

Table 8. Cursor modes

Cursor pattern	Cursor mode	
	CMODE = 0	CMODE = 1
00	second cursor color	second cursor color
01	first cursor color	first cursor color
10	transparent	transparent
11	inverted input	auxiliary cursor color

8.5 RGB Y-C_B-C_R matrix

RGB input signals to be encoded to PAL or NTSC are converted to the Y-C_B-C_R color space in this block. The color difference signals are fed through low-pass filters and formatted to a ITU-R BT.601 like 4 : 2 : 2 data stream for further processing.

A gain adjust option corrects the level swing of the graphics world (black-to-white as 0 to 255) to the required range of 16 to 235.

The matrix and formatting blocks can be bypassed for Y-C_B-C_R graphics input.

When the auxiliary VGA mode is selected, the output of the cursor insertion block is immediately directed to the triple DAC.

8.6 Horizontal scaler

The high quality horizontal scaler operates on the 4 : 2 : 2 data stream. Its control engines compensate the color phase offset automatically.

The scaler starts processing after a programmable horizontal offset and continues with a number of input pixels. Each input pixel is a programmable fraction of the current output pixel (XINC/4096). A special case is XINC = 0, this sets the scaling factor to 1.

If the SAA7108AE; SAA7109AE input data is in accordance with *'ITU-R BT.656'*, the scaler enters another mode. In this event, XINC needs to be set to 2048 for a scaling factor of 1. With higher values, upscaling will occur.

The phase resolution of the circuit is 12 bits, giving a maximum offset of 0.2 after 800 input pixels. Small FIFOs rearrange a 4 : 2 : 2 data stream at the scaler output.

8.7 Vertical scaler and anti-flicker filter

The functions scaling, Anti-Flicker Filter (AFF) and re-interlacing are implemented in the vertical scaler.

Besides the entire input frame, it receives the first and last lines of the border to allow anti-flicker filtering.

The circuit generates the interlaced output fields by scaling down the input frames with different offsets for odd and even fields. Increasing the YSKIP setting reduces the anti-flicker function. A YSKIP value of 4095 switches it off; see Table 107.

An additional, programmable vertical filter supports the anti-flicker function. This filter is not available at upscaling factors of more than 2.

The programming is similar to the horizontal scaler. For the re-interlacing, the resolutions of the offset registers are not sufficient, so the weighting factors for the first lines can also be adjusted. YINC = 0 sets the scaling factor to 1; YIWGTO and YIWGTE must not be 0.

Due to the re-interlacing, the circuit can perform upscaling by a maximum factor of 2. The maximum factor depends on the setting of the anti-flicker function and can be derived from the formulae given in Section 8.20.

An additional upscaling mode allows to increase the upscaling factor to maximum 4 as it is required for the old VGA modes like 320 $\times$ 240.

8.8 FIFO

The FIFO acts as a buffer to translate from the PIXCLK clock domain to the XTAL clock domain. The write clock is PIXCLK and the read clock is XTAL. An underflow or overflow condition can be detected via the I^2C-bus read access.

In order to avoid underflows and overflows, it is essential that the frequency of the synthesized PIXCLK matches to the input graphics resolution and the desired scaling factor.

8.9 Border generator

When the graphics picture is to be displayed as interlaced PAL, NTSC, S-video or RGB on a TV screen, it is desired in many cases not to lose picture information due to the inherent overscanning of a TV set. The desired amount of underscan area, which is achieved through appropriate scaling in the vertical and horizontal direction, can be filled in the border generator with an arbitrary true color tint.

8.10 Oscillator and Discrete Time Oscillator (DTO)

The master clock generation is realized as a 27 MHz crystal oscillator, which can operate with either a fundamental wave crystal or a 3rd harmonic crystal.

The crystal clock supplies the DTO of the pixel clock synthesizer, the video encoder and the I^2C-bus control block. It also usually supplies the triple DAC, with the exception of the auxiliary VGA mode, where the triple DAC is clocked by the pixel clock (PIXCLK).

The DTO can be programmed to synthesize all relevant pixel clock frequencies between circa 40 MHz and 85 MHz. Two programmable dividers provide the actual clock to be used externally and internally. The dividers can be programmed to factors of 1, 2, 4 and 8. For the internal pixel clock, a divider ratio of 8 makes no sense and is thus forbidden.

The internal clock can be switched completely to the pixel clock input. In this event, the input FIFO is useless and will be bypassed.

The entire pixel clock generation can be locked to the vertical frequency. Both pixel clock dividers get re-initialized every field. Optionally, the DTO can be cleared with each V-sync. At proper programming, this will make the pixel clock frequency a precise multiple of the vertical and horizontal frequencies. This is required for some graphic controllers.

8.11 Low-pass Clock Generation Circuit (CGC)

This block reduces the phase jitter of the synthesized pixel clock. It works as a tracking filter for all relevant synthesized pixel clock frequencies.

8.12 Encoder

8.12.1 Video path

The encoder generates luminance and color subcarrier output signals from the Y, C_B and C_R baseband signals, which are suitable for use as CVBS or separate Y and C signals.

Input to the encoder, at 27 MHz clock (e.g. DVD), is either originated from computer graphics at pixel clock, fed through the FIFO and border generator, or a ITU-R BT.656 style signal.

Luminance is modified in gain and in offset (the offset is programmable in a certain range to enable different black level set-ups). A blanking level can be set after insertion of a fixed synchronization pulse tip level, in accordance with standard composite synchronization schemes. Other manipulations used for the Macrovision anti-taping process, such as additional insertion of AGC super-white pulses (programmable in height), are supported by the SAA7108AE only.

To enable easy analog post filtering, luminance is interpolated from a 13.5 MHz data rate to a 27 MHz data rate, thereby providing luminance in a 10-bit resolution. The transfer characteristics of the luminance interpolation filter are illustrated in Figure 8 and Figure 9. Appropriate transients at start/end of active video and for synchronization pulses are ensured.

Chrominance is modified in gain (programmable separately for C_B and C_R), and a standard dependent burst is inserted, before baseband color signals are interpolated from a 6.75 MHz data rate to a 27 MHz data rate. One of the interpolation stages can be bypassed, thus providing a higher color bandwidth, which can be used for the Y and C output. The transfer characteristics of the chrominance interpolation filter are illustrated in Figure 6 and Figure 7.

The amplitude (beginning and ending) of the inserted burst, is programmable in a certain range that is suitable for standard signals and for special effects. After the succeeding quadrature modulator, color is provided on the subcarrier in 10-bit resolution.

The numeric ratio between the Y and C outputs is in accordance with the standards.

8.12.2 Teletext insertion and encoding (not simultaneously with real-time control)

Pin TTX_SRES receives a WST or NABTS teletext bitstream sampled at the crystal clock. At each rising edge of the output signal (TTXRQ) a single teletext bit has to be provided after a programmable delay at input pin TTX_SRES.

Phase variant interpolation is achieved on this bitstream in the internal teletext encoder, providing sufficient small phase jitter on the output text lines.

TTXRQ_XCLKO2 provides a fully programmable request signal to the teletext source, indicating the insertion period of bitstream at lines which can be selected independently for both fields. The internal insertion window for text is set to 360 (PAL WST), 296 (NTSC WST) or 288 (NABTS) teletext bits including clock run-in bits. The protocol and timing are illustrated in Figure 66.

Alternatively, this pin can be provided with a buffered crystal clock (XCLK) of 13.5 MHz.

8.12.3 Video Programming System (VPS) encoding

Five bytes of VPS information can be loaded via the I^2C-bus and will be encoded in the appropriate format into line 16.

8.12.4 Closed caption encoder

Using this circuit, data in accordance with the specification of closed caption or extended data service, delivered by the control interface, can be encoded (line 21). Two dedicated pairs of bytes (two bytes per field), each pair preceded by run-in clocks and framing code, are possible.

The actual line number in which data is to be encoded, can be modified in a certain range.

The data clock frequency is in accordance with the definition for NTSC M standard 32 times horizontal line frequency.

Data LOW at the output of the DACs corresponds to 0 IRE, data HIGH at the output of the DACs corresponds to approximately 50 IRE.

It is also possible to encode closed caption data for 50 Hz field frequencies at 32 times the horizontal line frequency.

8.12.5 Anti-taping (SAA7108AE only)

For more information contact your nearest NXP Semiconductors sales office.

8.13 RGB processor

This block contains a dematrix in order to produce RED, GREEN and BLUE signals to be fed to a SCART plug.

Before Y, C_B and C_R signals are de-matrixed, individual gain adjustment for Y and color difference signals and 2 times oversampling for luminance and 4 times oversampling for color difference signals is performed. The transfer curves of luminance and color difference components of RGB are illustrated in Figure 10 and Figure 11.

8.14 Triple DAC

Both Y and C signals are converted from digital-to-analog in a 10-bit resolution at the output of the video encoder. Y and C signals are also combined into a 10-bit CVBS signal.

The CVBS output signal occurs with the same processing delay as the Y, C and optional RGB or C_R-Y-C_B outputs. Absolute amplitude at the input of the DAC for CVBS is reduced by $^{15}/_{16}$ with respect to Y and C DACs to make maximum use of the conversion ranges.

RED, GREEN and BLUE signals are also converted from digital-to-analog, each providing a 10-bit resolution.

The reference currents of all three DACs can be adjusted individually in order to adapt for different output signals. In addition, all reference currents can be adjusted commonly to compensate for small tolerances of the on-chip band gap reference voltage.

Alternatively, all currents can be switched off to reduce power dissipation.

All three outputs can be used to sense for an external load (usually 75 Ω) during a pre-defined output. A flag in the I^2C-bus status byte reflects whether a load is applied or not. In addition, an automatic sense mode can be activated which indicates a 75 Ω load at any of the three outputs at the dedicated interrupt pin TVD.

If the SAA7108AE; SAA7109AE is required to drive a second (auxiliary) VGA monitor or an HDTV set, the DACs receive the signal coming from the HD data path. In this event, the DACs are clocked at the incoming PIXCLKI instead of the 27 MHz crystal clock used in the video encoder.

8.15 HD data path

This data path allows the SAA7108AE; SAA7109AE to be used with VGA or HDTV monitors. It receives its data directly from the cursor generator and supports RGB and Y-P_B-P_R output formats (RGB not with Y-P_B-P_R input formats). No scaling is done in this mode.

A gain adjustment either leads the full level swing to the digital-to-analog converters or reduces the amplitude by a factor of 0.69. This enables sync pulses to be added to the signal as it is required for display units expecting signals with sync pulses, either regular or 3-level syncs.

8.16 Timing generator

The synchronization of the SAA7108AE; SAA7109AE is able to operate in two modes; Slave mode and Master mode.

In Slave mode, the circuit accepts sync pulses on the bidirectional FSVGC (frame sync), VSVGC (vertical sync) and HSVGC (horizontal sync) pins: the polarities of the signals can be programmed. The frame sync signal is only necessary when the input signal is interlaced, in other cases it may be omitted. If the frame sync signal is present, it is possible to derive the vertical and the horizontal phase from it by setting the HFS and VFS bits. HSVGC and VSVGC are not necessary in this case, so it is possible to switch the pins to output mode.

Alternatively, the device can be triggered by auxiliary codes in a ITU-R BT.656 data stream via PD7 to PD0.

Only vertical frequencies of 50 Hz and 60 Hz are allowed with the SAA7108AE; SAA7109AE. In Slave mode, it is not possible to lock the encoders color carrier to the line frequency with the PHRES bits.

In the (more common) Master mode, the time base of the circuit is continuously free-running. The IC can output a frame sync at pin FSVGC, a vertical sync at pin VSVGC, a horizontal sync at pin HSVGC and a composite blanking signal at pin $\overline{\text{CBO}}$. All of these signals are defined in the PIXCLK domain. The duration of HSVGC and VSVGC are fixed, they are 64 clocks for HSVGC and 1 line for VSVGC. The leading slopes are in phase and the polarities can be programmed.

The input line length can be programmed. The field length is always derived from the field length of the encoder and the pixel clock frequency that is being used.

$\overline{\text{CBO}}$ acts as a data request signal. The circuit accepts input data at a programmable number of clocks after $\overline{\text{CBO}}$ goes active. This signal is programmable and it is possible to adjust the following (see Figure 64 and Figure 65):

- The horizontal offset
- The length of the active part of the line
- The distance from active start to first expected data
- The vertical offset separately for odd and even fields
- The number of lines per input field

In most cases, the vertical offsets for odd and even fields are equal. If they are not, then the even field will start later. The SAA7108AE; SAA7109AE will also request the first input lines in the even field, the total number of requested lines will increase by the difference of the offsets.

As stated above, the circuit can be programmed to accept the look-up and cursor data in the first 2 lines of each field. The timing generator provides normal data request pulses for these lines; the duration is the same as for regular lines. The additional request pulses will be suppressed with LUTL set to logic 0; see Table 132. The other vertical timings do not change in this case, so the first active line can be number 2, counted from 0.

8.17 Pattern generator for HD sync pulses

The pattern generator provides appropriate synchronization patterns for the video data path in auxiliary monitor or HDTV mode. It provides maximum flexibility in terms of raster generation for all interlaced and non-interlaced computer graphics or ATSC formats. The sync engine is capable of providing a combination of event-value pairs which can be used to insert certain values in the outgoing data stream at specified times. It can also be used to generate digital signals associated with time events. These can be used as digital horizontal and vertical synchronization signals on pins HSM_CSYNC and VSM.

The picture position is adjustable through the programmable relationship between the sync pulses and the video contents.

The generation of embedded analog sync pulses is bound to a number of events which can be defined for a line. Several of these line timing definitions can exist in parallel. For the final sync raster composition a certain sequence of lines with different sync event properties has to be defined. The sequence specifies a series of line types and the number of occurrences of this specific line type. Once the sequence has been completed, it restarts from the beginning. All pulse shapes are filtered internally in order to avoid ringing after analog post filters.

The sequence of the generated pulse stream must fit precisely to the incoming data stream in terms of the total number of pixels per line and lines per frame.

The sync engines flexibility is achieved by using a sequence of linked lists carrying the properties for the image, the lines as well as fractions of lines. Figure 12 illustrates the context between the various tables.

The first table serves as an array to hold the correct sequence of lines that compose the synchronization raster; it can contain up to 16 entries. Each entry holds a 4-bit index to the next table and a 10-bit counter value which specifies how often this particular line is invoked. If the necessary line count for a particular line exceeds the 10 bits, it has to use two table entries.

The 4-bit index in the line count array points to the line type array. It holds up to 15 entries (index 0 is not used), index 1 points to the first entry, index 2 to the second entry of the line type array etc.

Each entry of the line type array can hold up to 8 index pointers to another table. These indices point to portions of a line pulse pattern: A line could be split up e.g. into a sync, a blank, and an active portion followed by another blank portion, occupying four entries in one table line.

Each index of this table points to a particular line of the next table in the linked list. This table is called the line pattern array and each of the up to seven entries stores up to four pairs of a duration in pixel clock cycles and an index to a value table. The table entries are used to define portions of a line representing a certain value for a certain number of clock cycles.

The value specified in this table is actually another 3-bit index into a value array which can hold up to eight 8-bit values. If bit 4 (MSB) of the index is logic 1, the value is inserted into the G or Y signal only; if bit 4 = 0, the associated value is inserted into all three signals.

Two additional bits of the entries in the value array (LSBs of the second byte) determine if the associated events appear as a digital pulse on the HSM_CSYNC and/or VSM outputs.

To ease the trigger set-up for the sync generation module, a set of registers is provided to set up the screen raster which is defined as width and height. A trigger position can be specified as an x, y co-ordinate within the overall dimensions of the screen raster. If the x, y counter matches the specified co-ordinates, a trigger pulse is generated which pre-loads the tables with their initial values.

The listing in Table 9 outlines an example on how to set up the sync tables for a 1080i HD raster.

Important note: Due to a problem in the programming interface, writing to the line pattern array (address D2) might destroy the data of the line type array (address D1). A work around is to write the line pattern array data before writing the line type array. Reading of the arrays is possible but all address pointers must be initialized before the next write operation.

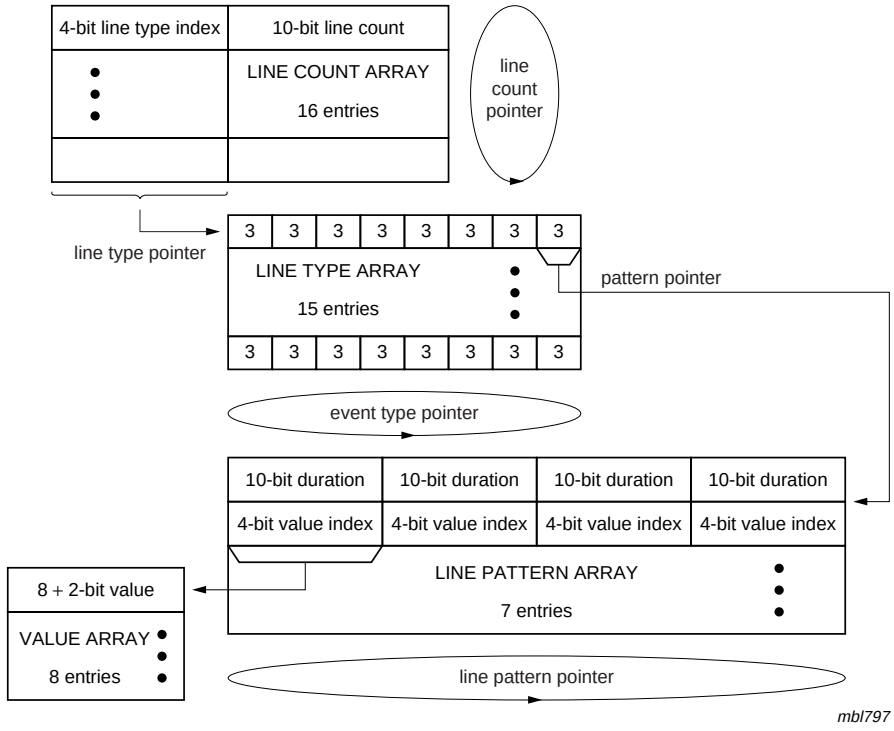


Fig 12. Context between the pattern generator tables for DH sync pulses

Table 9. Example for setup of the sync tables

Sequence (hexadecimal)	Comment
Write to subaddress D0h	
00	points to first entry of line count array (index 0)
05 20	generate 5 lines of line type index 2 (this is the second entry of the line type array); will be the first vertical raster pulse
01 40	generate 1 line of line type index 4; will be sync-black-sync-black sequence after the first vertical pulse
0E 60	generate 14 lines of line type index 6; will be the following lines with sync-black sequence

Table 9. Example for setup of the sync tables *...continued*

Sequence (hexadecimal)	Comment
1C 12	generate 540 lines of line type index 1; will be lines with sync and active video
02 60	generate 2 lines of line type index 6; will be the following lines with sync-black sequence
01 50	generate 1 line of line type index 5; will be the following line (line 563) with sync-black-sync-black-null sequence (null is equivalent to sync tip)
04 20	generate 4 lines of line type index 2; will be the second vertical raster pulse
01 30	generate 1 line of line type index 3; will be the following line with sync-null-sync-black sequence
0F 60	generate 15 lines of line type index 6; will be the following lines with sync-black sequence
1C 12	generate 540 lines of line type index 1; will be lines with sync and active video
02 60	generate 2 lines of line type index 6; will be the following lines with sync-black sequence; now, 1125 lines are defined
Write to subaddress D2h (insertion is done into all three analog output signals)	
00	points to first entry of line pattern array (index 1)
6F 33 2B 30 00 00 00 00	880 × value(3) + 44 × value(3); (subtract 1 from real duration)
6F 43 2B 30 00 00 00 00	880 × value(4) + 44 × value(3)
3B 30 BF 03 BF 03 2B 30	60 × value(3) + 960 × value(0) + 960 × value(0) + 44 × value(3)
2B 10 2B 20 57 30 00 00	44 × value(1) + 44 × value(2) + 88 × value(3)
3B 30 BF 33 BF 33 2B 30	60 × value(3) + 960 × value(3) + 960 × value(3) + 44 × value(3)
Write to subaddress D1h	
00	points to first entry of line type array (index 1)
34 00 00 00	use pattern entries 4 and 3 in this sequence (for sync and active video)
24 24 00 00	use pattern entries 4, 2, 4 and 2 in this sequence (for 2 × sync-black-null-black)
24 14 00 00	use pattern entries 4, 2, 4 and 1 in this sequence (for sync-black-null-black-null)
14 14 00 00	use pattern entries 4, 1, 4 and 1 in this sequence (for sync-black-sync-black)
14 24 00 00	use pattern entries 4, 1, 4 and 2 in this sequence (for sync-black-sync-black-null)
54 00 00 00	use pattern entries 4 and 5 in this sequence (for sync-black)
Write to subaddress D3h (no signals are directed to pins HSM_CSYNC and VSM)	
00	points to first entry of value array (index 0)
CC 00	black level, to be added during active video
80 00	sync level LOW (minimum output voltage)
0A 00	sync level HIGH (3-level sync)
CC 00	black level (needed elsewhere)

Table 9. Example for setup of the sync tables *...continued*

Sequence (hexadecimal)	Comment
80 00	null (identical to sync level LOW)
Write to subaddress DCh	
0B	insertion is active, gain for signal is adapted accordingly

8.18 I²C-bus interface

The I²C-bus interface is a standard slave transceiver, supporting 7-bit slave addresses and 400 kbit/s guaranteed transfer rate. It uses 8-bit subaddressing with an auto-increment function. All registers are write and read, except two read only status bytes.

The register bit map consists of an RGB Look-Up Table (LUT), a cursor bit map and control registers. The LUT contains three banks of 256 bytes, where each RGB triplet is assigned to one address. Thus a write access needs the LUT address and three data bytes following subaddress FFh. For further write access auto-incrementing of the LUT address is performed. The cursor bit map access is similar to the LUT access but contains only a single byte per address.

The I²C-bus slave address is defined as 88h.

8.19 Power-down modes

In order to reduce the power consumption, the SAA7108AE; SAA7109AE supports 2 Power-down modes, accessible via the I²C-bus. The analog Power-down mode (DOWNA = 1) turns off the digital-to-analog converters and the pixel clock synthesizer. The digital Power-down mode (DOWND = 1) turns off all internal clocks and sets the digital outputs to LOW except the I²C-bus interface. The IC keeps its programming and can still be accessed in this mode, however not all registers can be read from or written to. Reading or writing to the look-up tables, the cursor and the HD sync generator require a valid pixel clock. The typical supply current in full power-down is approximately 5 mA.

Because the analog Power-down mode turns off the pixel clock synthesizer, there are limitations in some applications. If there is no pixel clock, the IC is not able to set its outputs to LOW. So, in most cases, DOWNA and DOWND should be set to logic 1 simultaneously. If the EIDIV bit is logic 1, it should be set to logic 0 before power-down.

8.20 Programming the graphics acquisition scaler of the video encoder

The encoder section needs to provide a continuous data stream at its analog outputs as well as receive a continuous stream of data from its data source. Because there is no frame memory isolating the data streams, restrictions apply to the input frame timings.

Input and output processing of the encoder section are only coupled through the vertical frequencies. In Master mode, the encoder provides a vertical sync and an odd/even pulse to the input processing. In Slave mode, the encoder receives them.

The parameters of the input field are mainly given by the memory capacity of the encoder section. The rule is that the scaler and thus the input processing needs to provide the video data in the same time frames as the encoder reads them. Therefore, the vertical active video times (and the vertical frequencies) need to be the same.

The second rule is that there has to be data in the buffer FIFO when the encoder enters the active video area. Therefore, the vertical offset in the input path needs to be a bit shorter than the offset of the encoder.

The following gives the set of equations required to program the IC for the most common application: A post processor in Master mode with non-interlaced video input data.

Some variables are defined below:

- InPix: the number of active pixels per input line
- InPpl: the length of the entire input line in pixel clocks
- InLin: the number of active lines per input field/frame
- TPclk: the pixel clock period
- RiePclk: the ratio of internal to external pixel clock
- OutPix: the number of active pixels per output line
- OutLin: the number of active lines per output field
- TXclk: the encoder clock period (37.037 ns)

8.20.1 TV display window

At 60 Hz, the first visible pixel has the index 256, 710 pixels can be encoded; at 50 Hz, the index is 284, 702 pixels can be visible.

The output lines should be centred on the screen. It should be noted that the encoder has 2 clocks per pixel; see Table 76.

ADWHS = 256 + 710 – OutPix (60 Hz); ADWHS = 284 + 702 – OutPix (50 Hz);
ADWHE = ADWHS + OutPix × 2 (all frequencies)

For vertical, the procedure is the same. At 60 Hz, the first line with video information is number 19, 240 lines can be active. For 50 Hz, the numbers are 23 and 287;
see Table 84.

$$FAL = 19 + \frac{240 - OutLin}{2}$$ (60 Hz); $$FAL = 23 + \frac{287 - OutLin}{2}$$ (50 Hz);

LAL = FAL + OutLin (all frequencies)

Most TV sets use overscan, and not all pixels are visible. There is no standard for the factor, it is highly recommended to make the number of output pixels and lines adjustable. A reasonable underscan factor is 10 %, giving approximately 640 output pixels per line.

8.20.2 Input frame and pixel clock

The total number of pixel clocks per line and the input horizontal offset need to be chosen next. The only constraint is that the horizontal blanking has at least 10 clock pulses.

The required pixel clock frequency can be determined in the following way: Due to the limited internal FIFO size, the input path has to provide all pixels in the same time frame as the encoders vertical active time. The scaler also has to process the first and last border lines for the anti-flicker function. Thus:

$$TPclk = \frac{262.5 \times 1716 \times TXclk}{InPpl \times integer\left(\frac{InLin + 2}{OutLin} \times 262.5\right)}$$ (60 Hz)

$$TPclk = \frac{312.5 \times 1728 \times TXclk}{InPpl \times integer\left(\frac{InLin + 2}{OutLin} \times 312.5\right)}$$ (50 Hz) and for the pixel clock generator

$PCL = \frac{TXclk}{TPclk} \times 2^{20 + PCLE}$ (all frequencies); see Table 88 and Table 89. The divider PCLE should be set according to Table 89. PCLI may be set to a lower or the same value. Setting a lower value means that the internal pixel clock is higher and the data get sampled up. The difference may be 1 at 640 × 480 pixels resolution and 2 at resolutions with 320 pixels per line as a rule of thumb. This allows horizontal upscaling by a maximum factor of 2 respectively 4 (this is the parameter RiePclk).

$$PCLI = PCLE - \frac{log\,RiePclk}{log\,2}$$ (all frequencies)

The equations ensure that the last line of the field has the full number of clock cycles. Many graphic controllers require this. Note that the bit PCLSY needs to be set to ensure that there is not even a fraction of a clock left at the end of the field.

8.20.3 Horizontal scaler

XOFS can be chosen arbitrarily, the condition being that XOFS + XPIX ≤ HLEN is fulfilled. Values given by the VESA display timings are preferred.

HLEN = InPpl × RiePclk – 1

$$XPIX = \frac{InPix}{2} \times RiePclk$$

$$XINC = \frac{OutPix}{InPix} \times \frac{4096}{RiePclk}$$

XINC needs to be rounded up, it needs to be set to 0 for a scaling factor of 1.

8.20.4 Vertical scaler

The input vertical offset can be taken from the assumption that the scaler should just have finished writing the first line when the encoder starts reading it:

$YOFS = \frac{FAL \times 1716 \times TXclk}{InPpl \times TPclk} - 2.5$ (60 Hz) $YOFS = \frac{FAL \times 1728 \times TXclk}{InPpl \times TPclk} - 2.5$ (50 Hz)

In most cases the vertical offsets will be the same for odd and even fields. The results should be rounded down.

YPIX = InLin

YSKIP defines the anti-flicker function. 0 means maximum flicker reduction but minimum vertical bandwidth, 4095 gives no flicker reduction and maximum bandwidth. Note that the maximum value for YINC is 4095. It might be necessary to reduce the value of YSKIP to fulfil this requirement.

$$YINC = \frac{OutLin}{InLin + 2} \times \left(1 + \frac{YSKIP}{4095}\right) \times 4096$$

$$YIWGTO = \frac{YINC}{2} + 2048$$

$$YIWGTE = \frac{YINC - YSKIP}{2}$$

When YINC = 0 it sets the scaler to scaling factor 1. The initial weighting factors must not be set to 0 in this case. YIWGTE may go negative. In this event, YINC should be added and YOFSE incremented. This can be repeated as often as necessary to make YIWGTE positive.

It should be noted that these equations assume that the input is non-interlaced but the output is interlaced. If the input is interlaced, the initial weighting factors need to be adapted to obtain the proper phase offsets in the output frame.

If vertical upscaling beyond the upper capabilities is required, the parameter YUPSC may be set to logic 1. This extends the maximum vertical scaling factor by a factor of 2. Only the parameter YINC is affected, it needs to be divided by two to get the same effect.

There are restrictions in this mode:

- The vertical filter YFIL is not available in this mode; the circuit will ignore this value
- The horizontal blanking needs to be long enough to transfer an output line between 2 memory locations. This is 710 internal pixel clocks

  Or the upscaling factor needs to be limited to 1.5 and the horizontal upscaling factor is also limited to less than ~1.5. In this case a normal blanking length is sufficient

8.21 Input levels and formats

The SAA7108AE; SAA7109AE accepts digital Y, C_B, C_R or RGB data with levels (digital codes) in accordance with *'ITU-R BT.601'*. An optional gain adjustment also allows to accept data with the full level swing of 0 to 255.

For C and CVBS outputs, deviating amplitudes of the color difference signals can be compensated for by independent gain control setting, while gain for luminance is set to predefined values, distinguishable for 7.5 IRE set-up or without set-up.

The RGB, respectively C_R-Y-C_B path features an individual gain setting for luminance (GY) and color difference signals (GCD). Reference levels are measured with a color bar, 100 % white, 100 % amplitude and 100 % saturation.

The encoder section of the SAA7108AE; SAA7109AE has special input cells for the VGC port. They operate at a wider supply voltage range and have a strict input threshold at $\frac{1}{2}V_{DD(DVO)}$. To achieve full speed of these cells, the EIDIV bit needs to be set to logic 1. Note that the impedance of these cells is approximately 6 kΩ. This may cause trouble with the bootstrapping pins of some graphic chips. So the power-on reset forces the bit to logic 0, the input impedance is regular in this mode.

Table 10. *'ITU-R BT.601'* signal component levels

Color	Signals[1]					
	Y	C_B	C_R	R	G	B
White	235	128	128	235	235	235
Yellow	210	16	146	235	235	16
Cyan	170	166	16	16	235	235
Green	145	54	34	16	235	16
Magenta	106	202	222	235	16	235
Red	81	90	240	235	16	16
Blue	41	240	110	16	16	235
Black	16	128	128	16	16	16

[1] Transformation:

$R = Y + 1.3707 \times (C_R - 128)$

$G = Y - 0.3365 \times (C_B - 128) - 0.6982 \times (C_R - 128)$

$B = Y + 1.7324 \times (C_B - 128)$.

Table 11. Usage of bits SLOT and EDGE

Data slot control (example for format 0)			
SLOT	EDGE	1st data	2nd data
0	0	at rising edge G3/Y3	at falling edge R7/C_R7
0	1	at falling edge G3/Y3	at rising edge R7/C_R7
1	0	at rising edge R7/C_R7	at falling edge G3/Y3
1	1	at falling edge R7/C_R7	at rising edge G3/Y3

Table 12. Pin assignment for input format 0

8 + 8 + 8-bit 4 : 4 : 4 non-interlaced RGB/C_B-Y-C_R		
Pin	Falling clock edge	Rising clock edge
PD11	G3/Y3	R7/C_R7
PD10	G2/Y2	R6/C_R6
PD9	G1/Y1	R5/C_R5
PD8	G0/Y0	R4/C_R4
PD7	B7/C_B7	R3/C_R3
PD6	B6/C_B6	R2/C_R2
PD5	B5/C_B5	R1/C_R1
PD4	B4/C_B4	R0/C_R0
PD3	B3/C_B3	G7/Y7
PD2	B2/C_B2	G6/Y6
PD1	B1/C_B1	G5/Y5
PD0	B0/C_B0	G4/Y4

Table 13. Pin assignment for input format 1

5 + 5 + 5-bit 4 : 4 : 4 non-interlaced RGB		
Pin	**Falling clock edge**	**Rising clock edge**
PD7	G2	X
PD6	G1	R4
PD5	G0	R3
PD4	B4	R2
PD3	B3	R1
PD2	B2	R0
PD1	B1	G4
PD0	B0	G3

Table 14. Pin assignment for input format 2

5 + 6 + 5-bit 4 : 4 : 4 non-interlaced RGB		
Pin	**Falling clock edge**	**Rising clock edge**
PD7	G2	R4
PD6	G1	R3
PD5	G0	R2
PD4	B4	R1
PD3	B3	R0
PD2	B2	G5
PD1	B1	G4
PD0	B0	G3

Table 15. Pin assignment for input format 3

8 + 8 + 8-bit 4 : 2 : 2 non-interlaced C_B-Y-C_R				
Pin	**Falling clock edge n**	**Rising clock edge n**	**Falling clock edge n + 1**	**Rising clock edge n + 1**
PD7	$C_B7(0)$	Y7(0)	$C_R7(0)$	Y7(1)
PD6	$C_B6(0)$	Y6(0)	$C_R6(0)$	Y6(1)
PD5	$C_B5(0)$	Y5(0)	$C_R5(0)$	Y5(1)
PD4	$C_B4(0)$	Y4(0)	$C_R4(0)$	Y4(1)
PD3	$C_B3(0)$	Y3(0)	$C_R3(0)$	Y3(1)
PD2	$C_B2(0)$	Y2(0)	$C_R2(0)$	Y2(1)
PD1	$C_B1(0)$	Y1(0)	$C_R1(0)$	Y1(1)
PD0	$C_B0(0)$	Y0(0)	$C_R0(0)$	Y0(1)

Table 16. Pin assignment for input format 4

8 + 8 + 8-bit 4 : 2 : 2 interlaced C_B-Y-C_R (ITU-R BT.656, 27 MHz clock)				
Pin	**Rising clock edge n**	**Rising clock edge n + 1**	**Rising clock edge n + 2**	**Rising clock edge n + 3**
PD7	$C_B7(0)$	Y7(0)	$C_R7(0)$	Y7(1)
PD6	$C_B6(0)$	Y6(0)	$C_R6(0)$	Y6(1)
PD5	$C_B5(0)$	Y5(0)	$C_R5(0)$	Y5(1)

Table 16. Pin assignment for input format 4 *...continued*

8 + 8 + 8-bit 4 : 2 : 2 interlaced C_B-Y-C_R (ITU-R BT.656, 27 MHz clock)				
Pin	**Rising clock edge n**	**Rising clock edge n + 1**	**Rising clock edge n + 2**	**Rising clock edge n + 3**
PD4	C_B4(0)	Y4(0)	C_R4(0)	Y4(1)
PD3	C_B3(0)	Y3(0)	C_R3(0)	Y3(1)
PD2	C_B2(0)	Y2(0)	C_R2(0)	Y2(1)
PD1	C_B1(0)	Y1(0)	C_R1(0)	Y1(1)
PD0	C_B0(0)	Y0(0)	C_R0(0)	Y0(1)

Table 17. Pin assignment for input format 5[1]

8-bit non-interlaced index color		
Pin	**Falling clock edge**	**Rising clock edge**
PD11	X	X
PD10	X	X
PD9	X	X
PD8	X	X
PD7	INDEX7	X
PD6	INDEX6	X
PD5	INDEX5	X
PD4	INDEX4	X
PD3	INDEX3	X
PD2	INDEX2	X
PD1	INDEX1	X
PD0	INDEX0	X

[1] X = don't care.

Table 18. Pin assignment for input format 6

8 + 8 + 8-bit 4 : 4 : 4 non-interlaced RGB/C_B-Y-C_R		
Pin	**Falling clock edge**	**Rising clock edge**
PD11	G4/Y4	R7/C_R7
PD10	G3/Y3	R6/C_R6
PD9	G2/Y2	R5/C_R5
PD8	B7/C_B7	R4/C_R4
PD7	B6/C_B6	R3/C_R3
PD6	B5/C_B5	G7/Y7
PD5	B4/C_B4	G6/Y6
PD4	B3/C_B3	G5/Y5
PD3	G0/Y0	R2/C_R2
PD2	B2/C_B2	R1/C_R1
PD1	B1/C_B1	R0/C_R0
PD0	B0/C_B0	G1/Y1

9. Functional description of digital video decoder part

9.1 Decoder

9.1.1 Analog input processing

The SAA7108AE; SAA7109AE offers six analog signal inputs, two analog main channels with source switch, clamp circuit, analog amplifier, anti-alias filter and video 9-bit CMOS ADC; see Figure 16.

9.1.2 Analog control circuits

The anti-alias filters are adapted to the line-locked clock frequency via a filter control circuit. The characteristic is shown in Figure 13. During the vertical blanking period gain and clamping control are frozen.

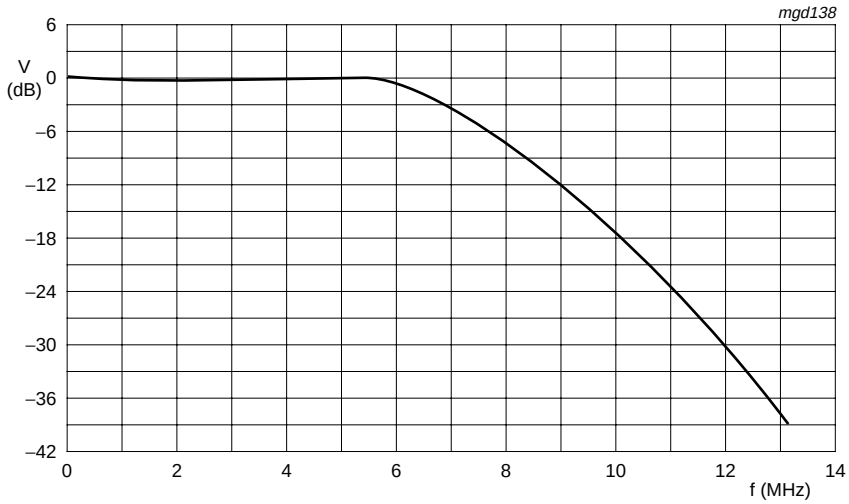


Fig 13. Anti-alias filter

9.1.2.1 Clamping

The clamp control circuit controls the correct clamping of the analog input signals. The coupling capacitor is also used to store and filter the clamping voltage. An internal digital clamp comparator generates the information with respect to clamp-up or clamp-down. The clamping levels for the two ADC channels are fixed for luminance (60) and chrominance (128). Clamping time in normal use is set with the HCL pulse on the back porch of the video signal; see Figure 14 and Figure 15.

9.1.2.2 Gain control

The gain control circuit receives (via the I^2C-bus) the static gain levels for the two analog amplifiers or controls one of these amplifiers automatically via a built-in Automatic Gain Control (AGC) as part of the Analog Input Control (AICO).

The AGC for luminance is used to amplify a CVBS or Y signal to the required signal amplitude, matched to the ADCs input voltage range. The AGC active time is the sync bottom of the video signal.

Signal (white) peak control limits the gain at signal overshoots. The influence of supply voltage variation within the specified range is automatically eliminated by clamping and automatic gain control. The flow charts show more details of the AGC; see Figure 17 and Figure 18.

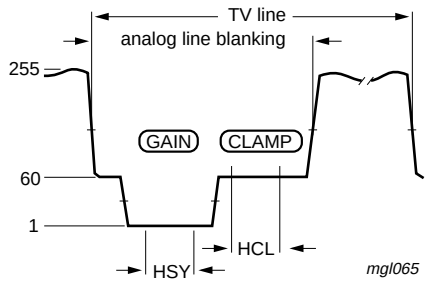


Fig 14. Analog line with clamp (HCL) and gain range (HSY)

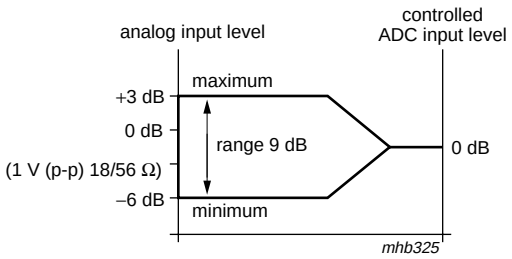


Fig 15. Automatic gain range

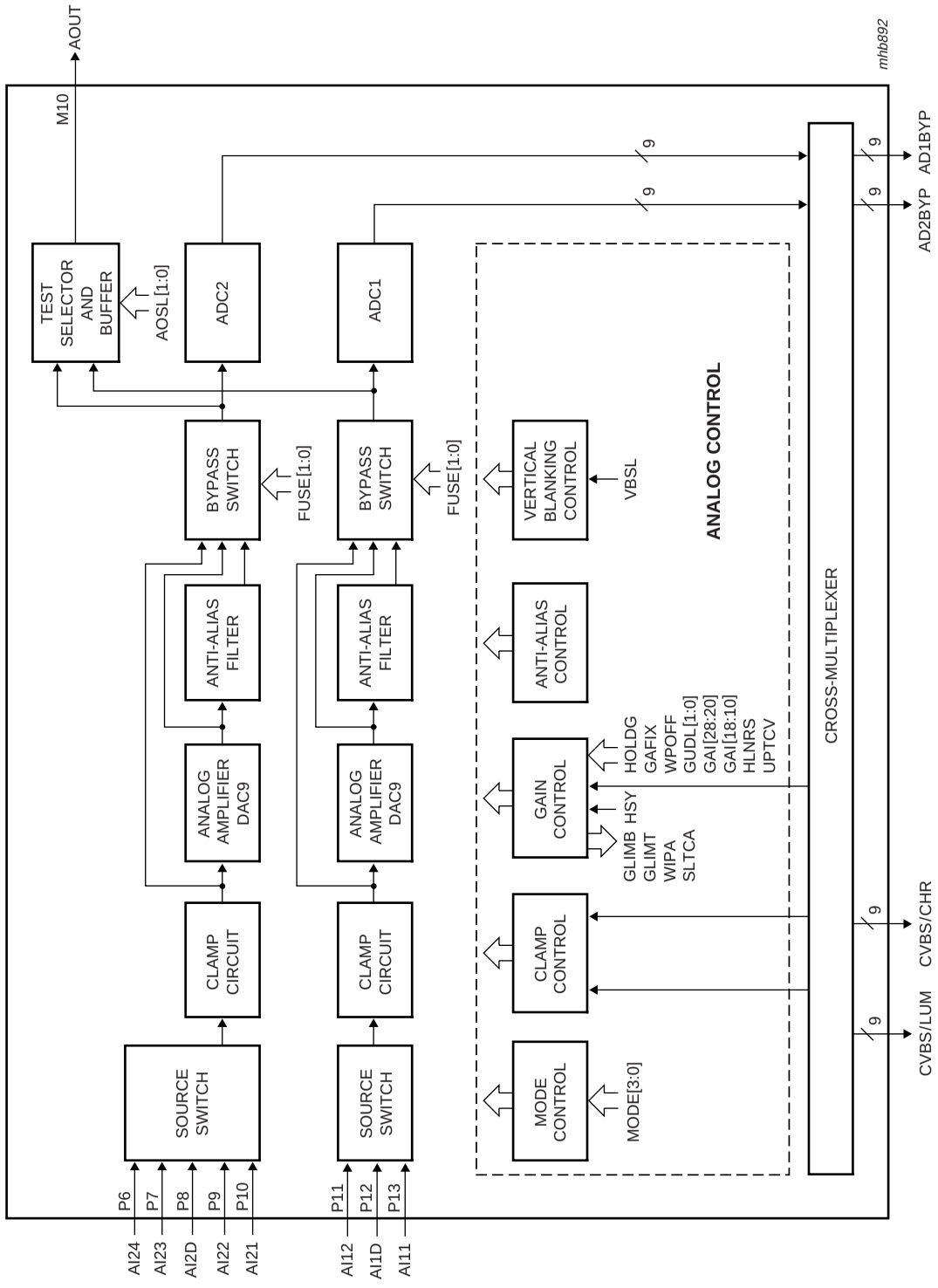
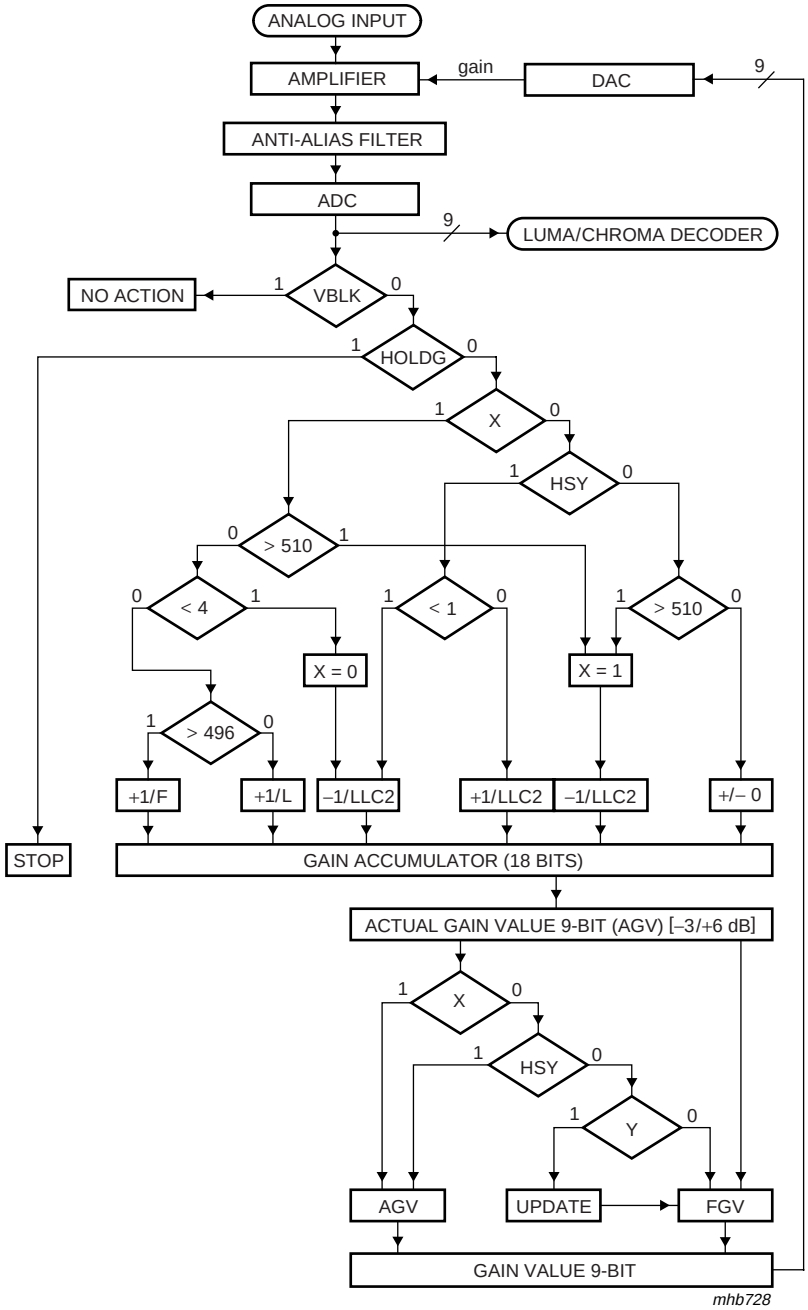


Fig 16. Analog input processing using the SAA7108AE; SAA7109AE as differential front-end with 9-bit ADC



X = system variable.

Y = |AGV – FGV| > GUDL.

GUDL = gain update level (adjustable).

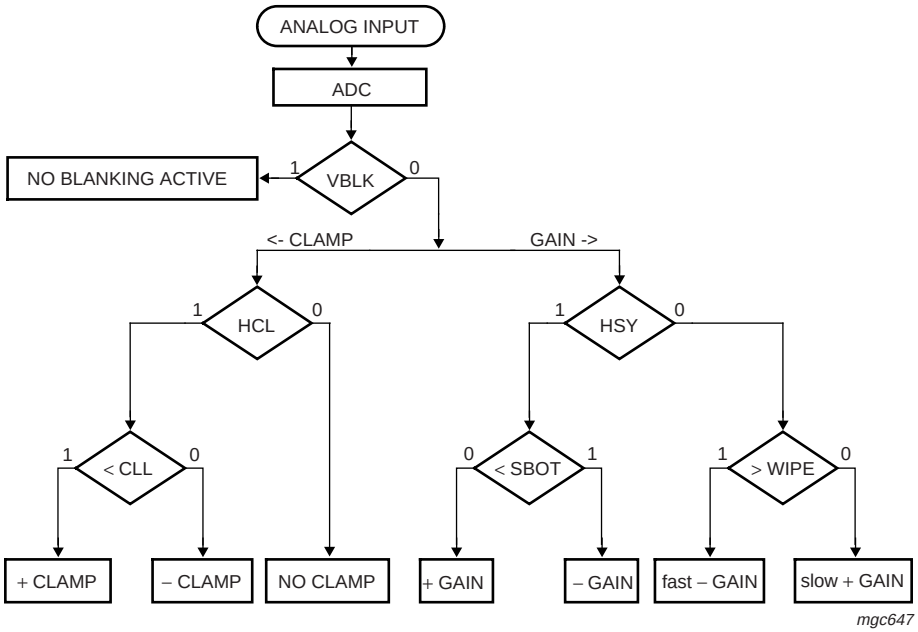
VBLK = vertical blanking pulse.

HSY = horizontal sync pulse.

AGV = actual gain value.

FGV = frozen gain value.

Fig 17. Gain flow chart



WIPE = white peak level (254).

SBOT = sync bottom level (1).

CLL = clamp level [60 Y (128 C)].

HSY = horizontal sync pulse.

HCL = horizontal clamp pulse.

Fig 18. Clamp and gain flow

9.1.3 Chrominance and luminance processing

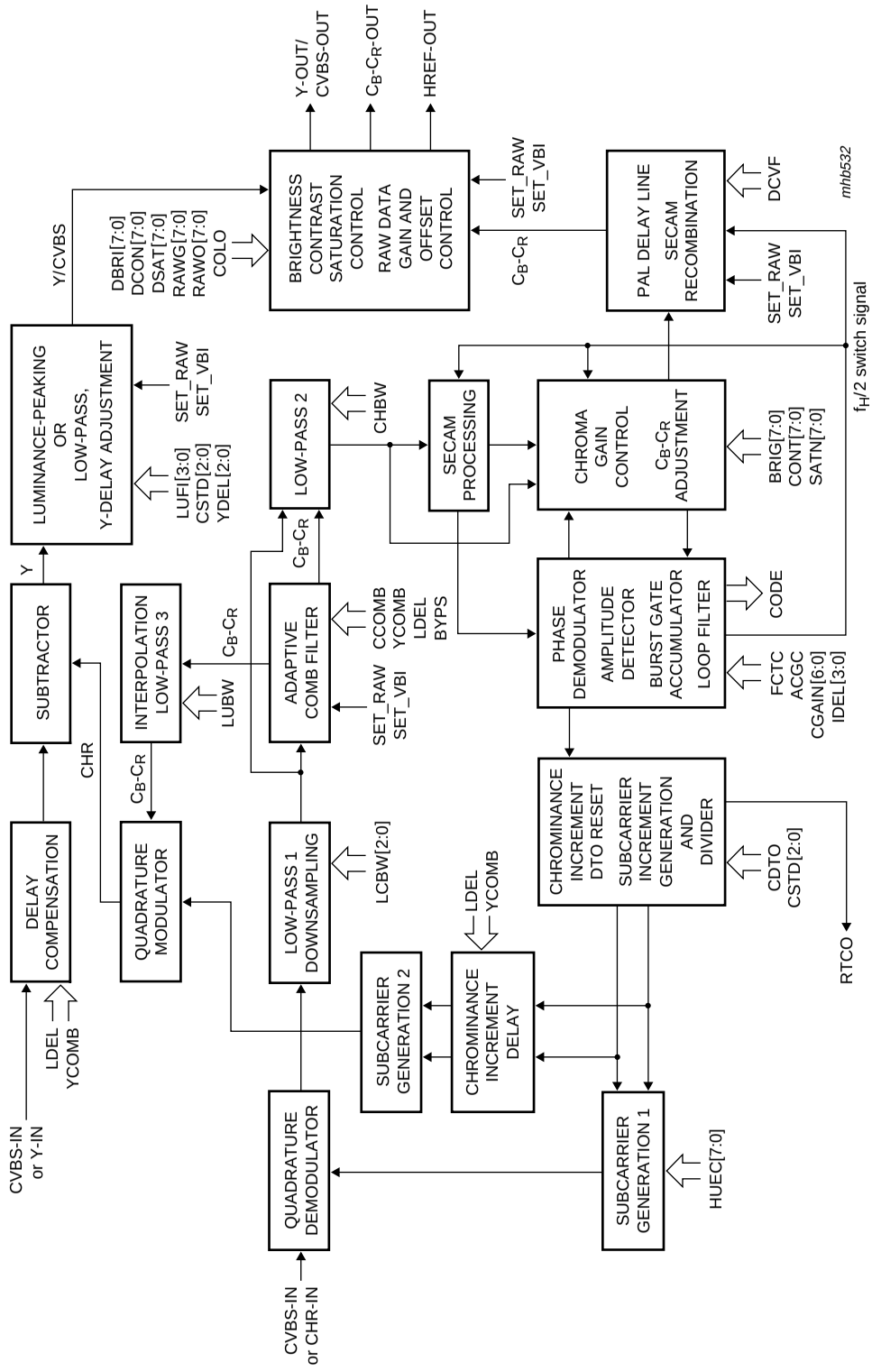


Fig 19. Chrominance and luminance processing

9.1.3.1 Chrominance path

The 9-bit CVBS or chrominance input signal is fed to the input of a quadrature demodulator, where it is multiplied by two time-multiplexed subcarrier signals from the subcarrier generation block 1 (0° and 90° phase relationship to the demodulator axis). The frequency is dependent on the chosen color standard.

The time-multiplexed output signals of the multipliers are low-pass filtered (low-pass 1). Eight characteristics are programmable via LCBW2 to LCBW0 to achieve the desired bandwidth for the color difference signals (PAL, NTSC) or the 0° and 90° FM signals (SECAM).

The chrominance low-pass 1 characteristic also influences the grade of cross luminance reduction during horizontal color transients (large chrominance bandwidth means strong suppression of cross luminance). If the Y-comb filter is disabled by YCOMB = 0 the filter influences directly the width of the chrominance notch within the luminance path (a large chrominance bandwidth means wide chrominance notch resulting in a lower luminance bandwidth).

The low-pass filtered signals are fed to the adaptive comb filter block. The chrominance components are separated from the luminance via a two-line vertical stage (four lines for PAL standards) and a decision logic between the filtered and the non-filtered output signals. This block is bypassed for SECAM signals. The comb filter logic can be enabled independently for the succeeding luminance and chrominance processing by YCOMB (subaddress 09h, bit 6) and/or CCOMB (subaddress 0Eh, bit 0). It is always bypassed during VBI or raw data lines programmable by the LCRn registers (subaddresses 41h to 57h); see Section 9.2.

The separated C_B-C_R components are further processed by a second filter stage (low-pass 2) to modify the chrominance bandwidth without influencing the luminance path. Its characteristic is controlled by CHBW (subaddress 10h, bit 3). For the complete transfer characteristic of low-pass filters 1 and 2, see Figure 20 and Figure 21.

The SECAM processing (bypassed for QAM standards) contains the following blocks:

- Baseband ‘bell’ filters to reconstruct the amplitude and phase equalized 0° and 90° FM signals
- Phase demodulator and differentiator (FM-demodulation)
- De-emphasis filter to compensate the pre-emphasized input signal, including frequency offset compensation (DB or DR white carrier values are subtracted from the signal, controlled by the SECAM switch signal)

The succeeding chrominance gain control block amplifies or attenuates the C_B-C_R signal according to the required ITU 601/656 levels. It is controlled by the output signal from the amplitude detection circuit within the burst processing block.

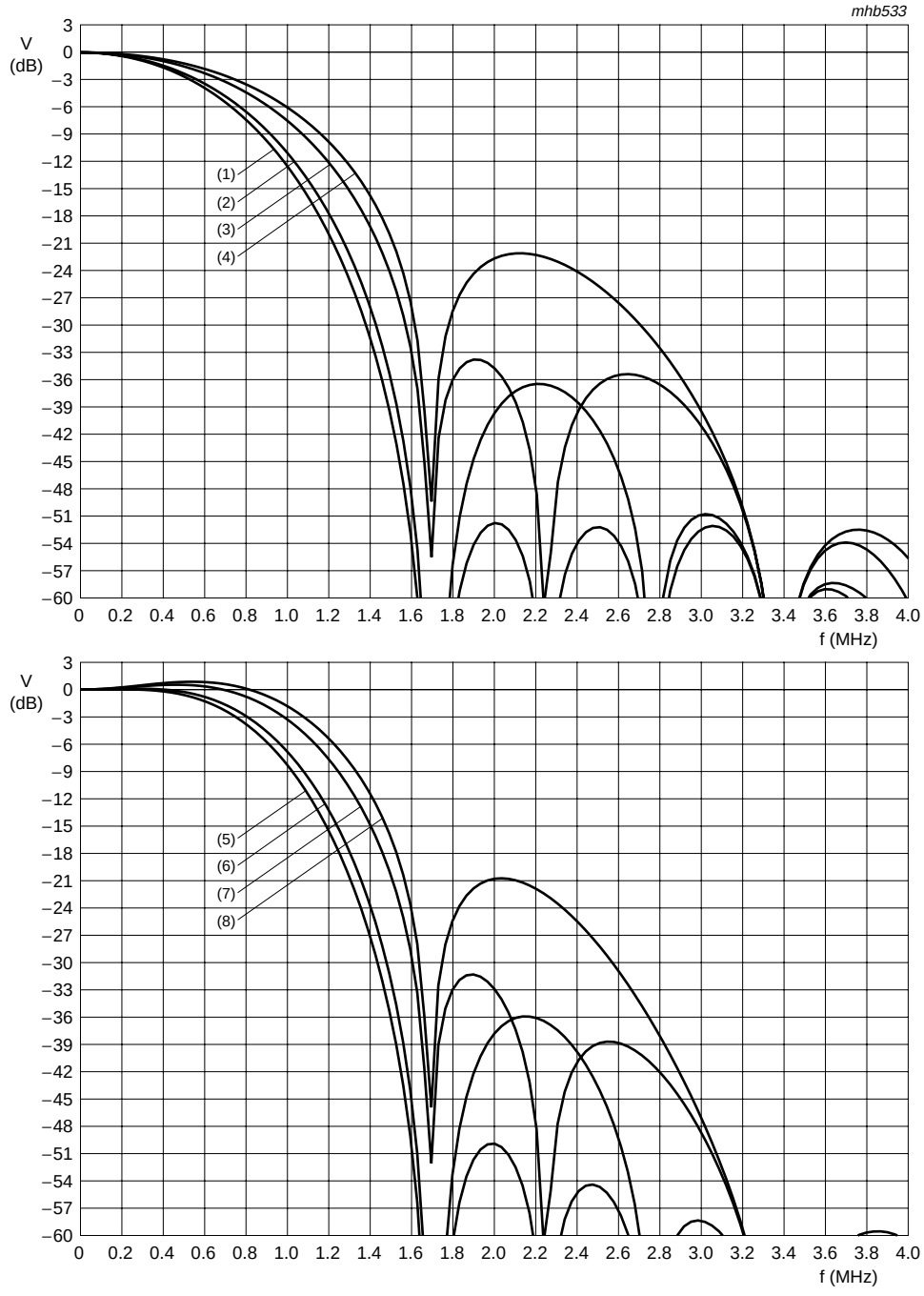
The burst processing block provides the feedback loop of the chrominance PLL and contains the following:

- Burst gate accumulator
- Color identification and color killer
- Comparison nominal/actual burst amplitude (PAL/NTSC standards only)
- Loop filter chrominance gain control (PAL/NTSC standards only)

- Loop filter chrominance PLL (only active for PAL/NTSC standards)
- PAL/SECAM sequence detection, H/2-switch generation

The increment generation circuit produces the Discrete Time Oscillator (DTO) increment for both subcarrier generation blocks. It contains a division by the increment of the line-locked clock generator to create a stable phase-locked sine signal under all conditions (e.g. for non-standard signals).

The PAL delay line block eliminates crosstalk between the chrominance channels in accordance with the PAL standard requirements. For NTSC color standards the delay line can be used as an additional vertical filter. If desired, it can be switched off by DCVF = 1. It is always disabled during VBI or raw data lines programmable by the LCRn registers (subaddresses 41h to 57h); see Section 9.2. The embedded line delay is also used for SECAM recombination (cross-over switches).



(1) LCBW[2:0] = 000.
(2) LCBW[2:0] = 010.
(3) LCBW[2:0] = 100.
(4) LCBW[2:0] = 110.

(5) LCBW[2:0] = 001.
(6) LCBW[2:0] = 011.
(7) LCBW[2:0] = 101.
(8) LCBW[2:0] = 111.

Fig 20. Transfer characteristics of the chrominance low-pass at CHBW = 0

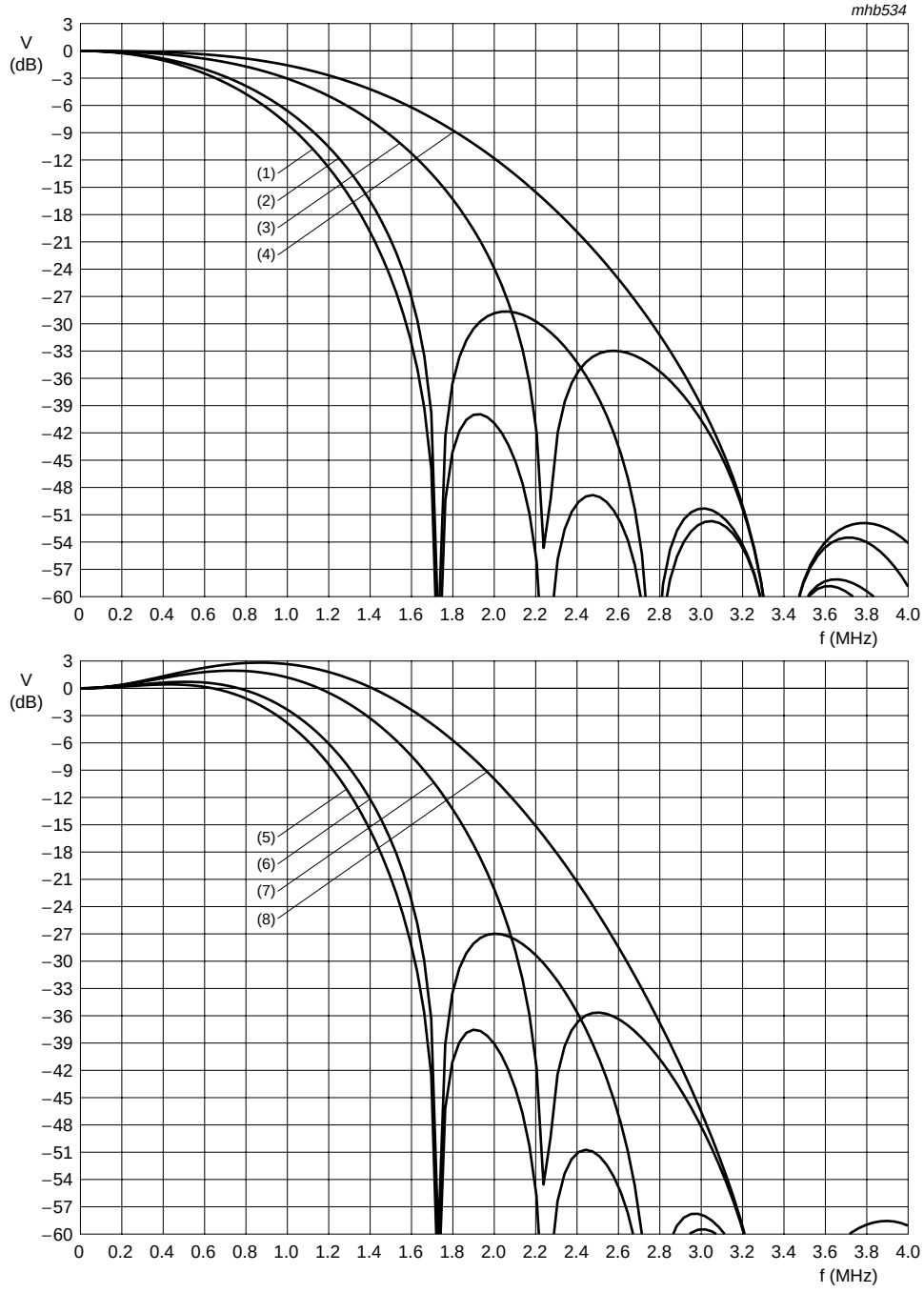


Fig 21. Transfer characteristics of the chrominance low-pass at CHBW = 1

9.1.3.2 Luminance path

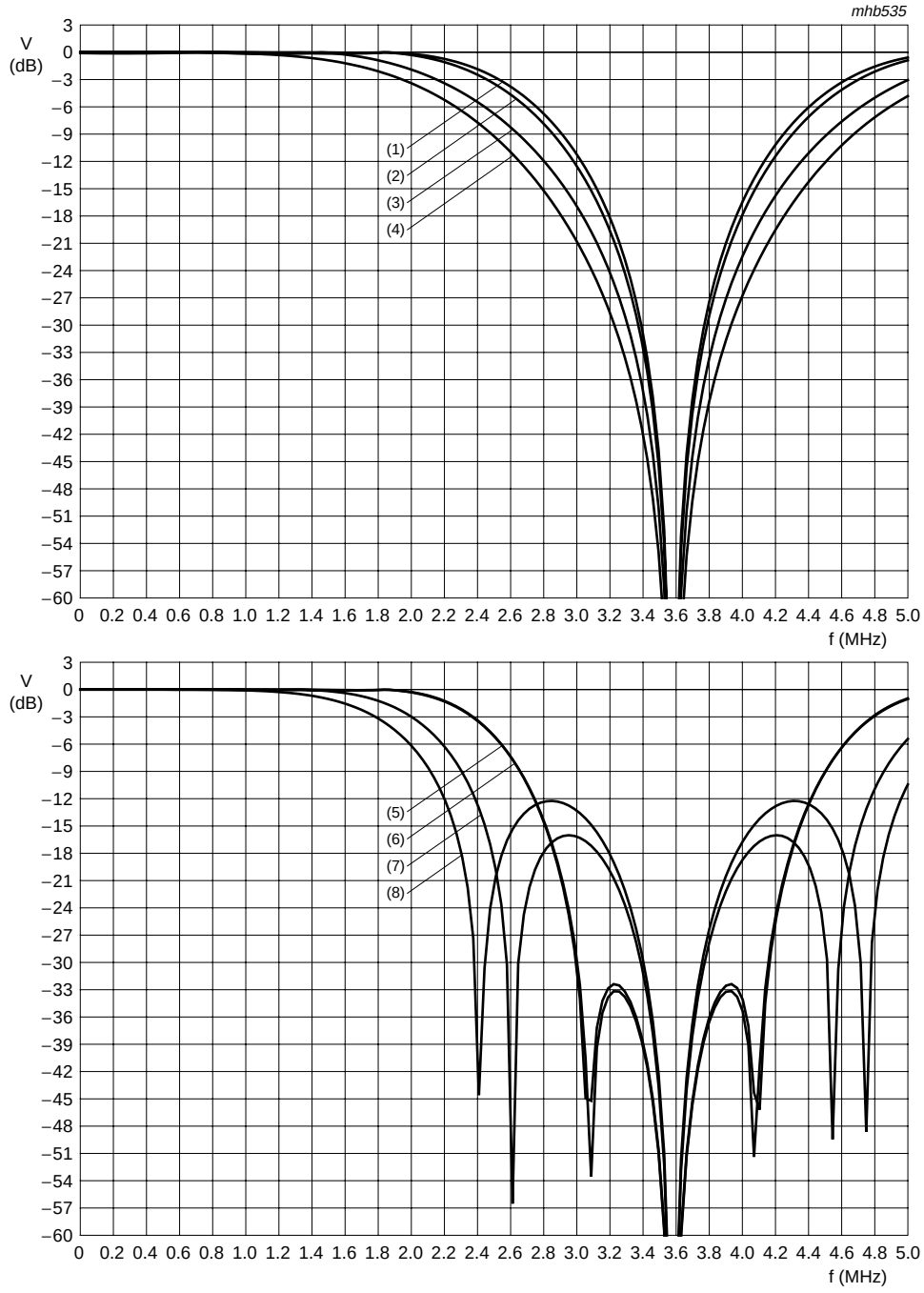
The rejection of the chrominance components within the 9-bit CVBS or Y input signal is achieved by subtracting the remodulated chrominance signal from the CVBS input.

The comb filtered C_B-C_R components are interpolated (upsampled) by the low-pass 3 block. Its characteristic is controlled by LUBW (subaddress 09h, bit 4) to modify the width of the chrominance 'notch' without influencing the chrominance path. The programmable frequency characteristics available, in conjunction with the LCBW2 to LCBW0 settings, can be seen in Figure 22 to Figure 25. It should be noted that these frequency curves are only valid for Y-comb disabled filter mode (YCOMB = 0). In comb filter mode the frequency response is flat. The center frequency of the notch is automatically adapted to the chosen color standard.

The interpolated C_B-C_R samples are multiplied by two time-multiplexed subcarrier signals from the subcarrier generation block 2. This second DTO is locked to the first subcarrier generator by an increment delay circuit matched to the processing delay, which is different for PAL and NTSC standards according to the chosen comb filter algorithm. The two modulated signals are finally added to build the remodulated chrominance signal.

The frequency characteristic of the separated luminance signal can be further modified by the succeeding luminance filter block. It can be configured as peaking (resolution enhancement) or low-pass block by LUFI3 to LUFI0 (subaddress 09h, bits 3 to 0). The 16 resulting frequency characteristics can be seen in Figure 26. The LUFI3 to LUFI0 settings can be used as a user programmable sharpness control.

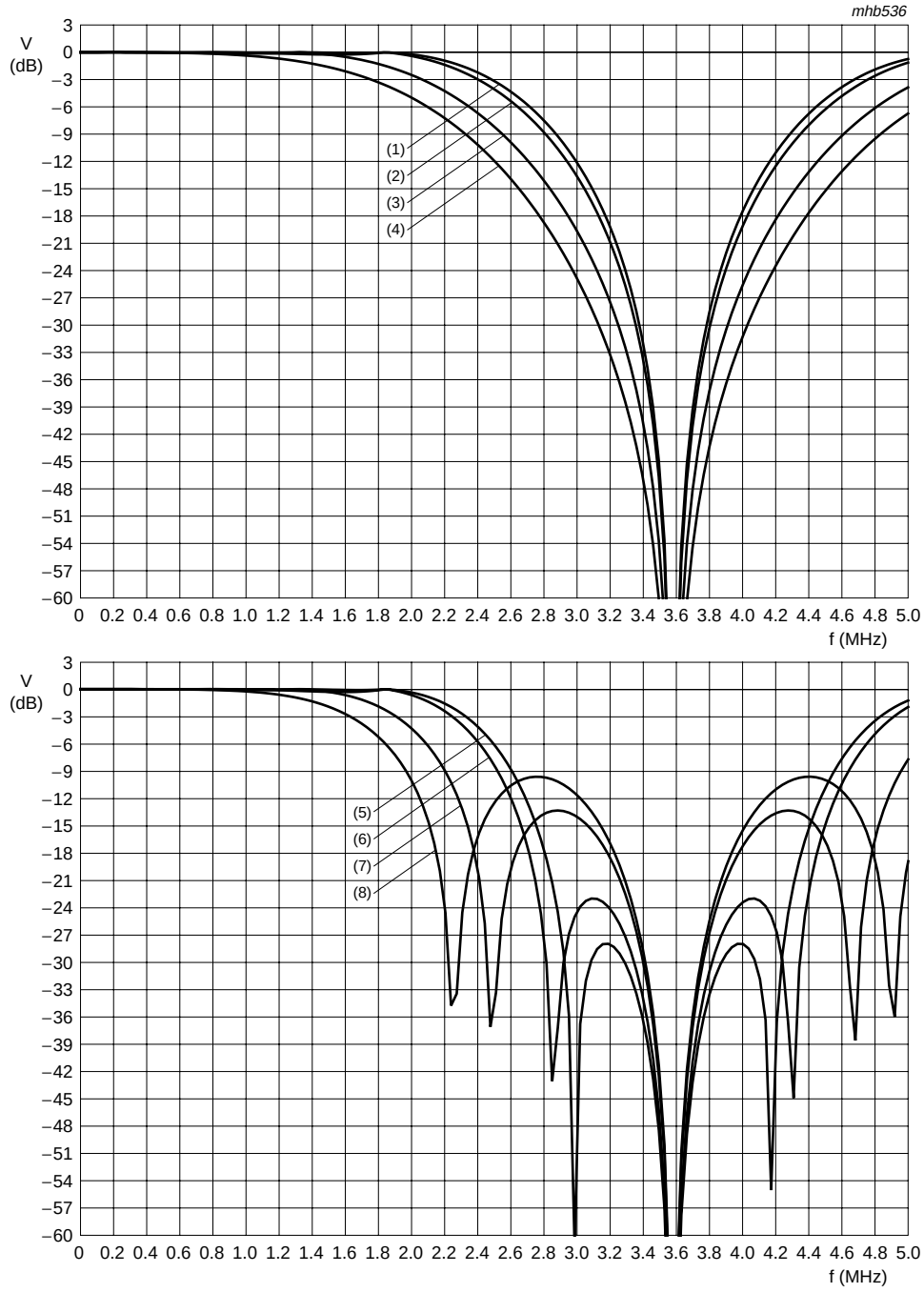
The luminance filter block also contains the adjustable Y-delay part; programmable by YDEL2 to YDEL0 (subaddress 11h, bits 2 to 0).



(1) LCBW[2:0] = 000.
(2) LCBW[2:0] = 010.
(3) LCBW[2:0] = 100.
(4) LCBW[2:0] = 110.

(5) LCBW[2:0] = 001.
(6) LCBW[2:0] = 011.
(7) LCBW[2:0] = 101.
(8) LCBW[2:0] = 111.

Fig 22. Transfer characteristics of the luminance notch filter in 3.58 MHz mode (Y-comb filter disabled) at LUBW = 0



(1) LCBW[2:0] = 000.
(2) LCBW[2:0] = 010.
(3) LCBW[2:0] = 100.
(4) LCBW[2:0] = 110.

(5) LCBW[2:0] = 001.
(6) LCBW[2:0] = 011.
(7) LCBW[2:0] = 101.
(8) LCBW[2:0] = 111.

Fig 23. Transfer characteristics of the luminance notch filter in 3.58 MHz mode (Y-comb filter disabled) at LUBW = 1

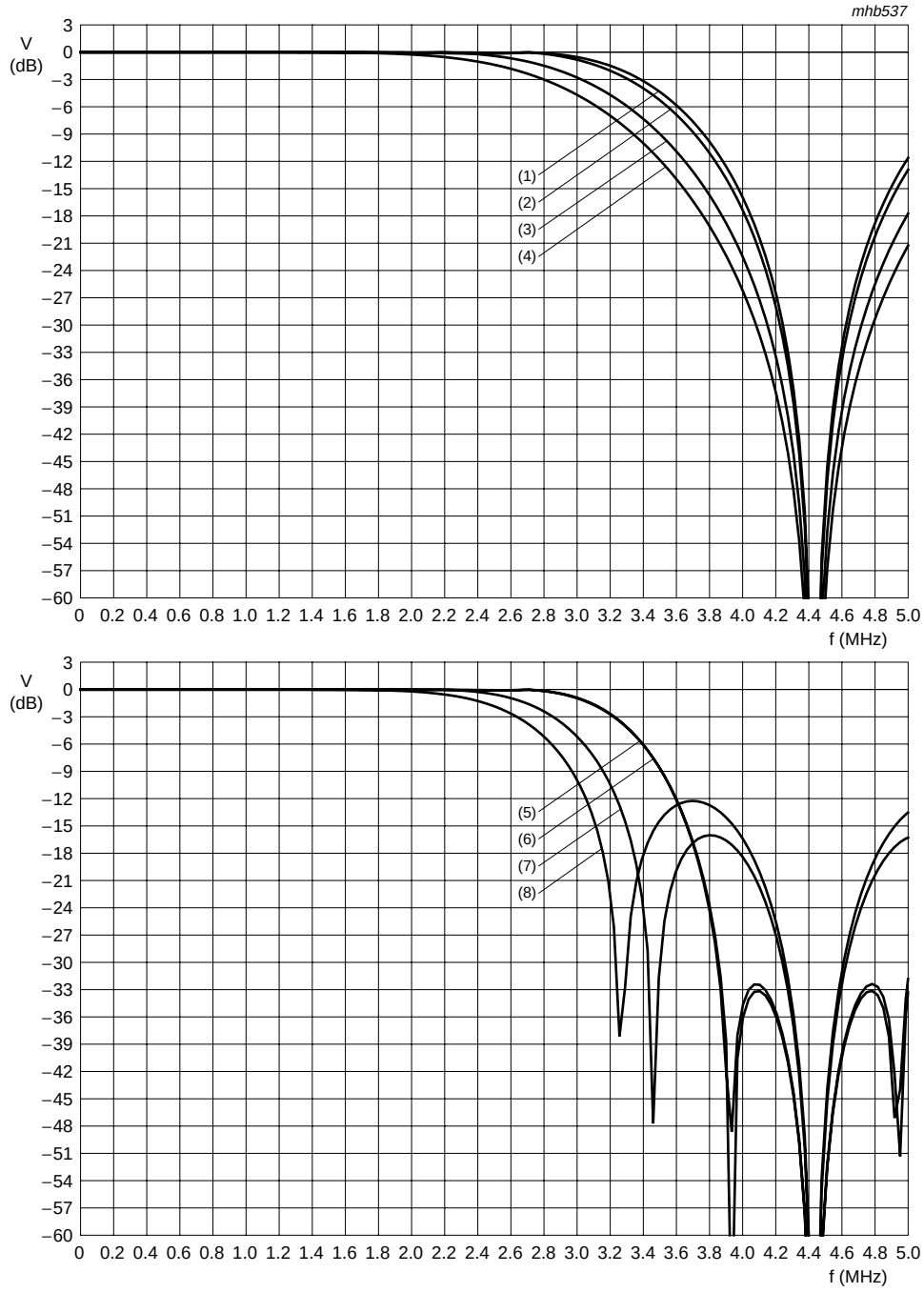


Fig 24. Transfer characteristics of the luminance notch filter in 4.43 MHz mode (Y-comb filter disabled) at LUBW = 0

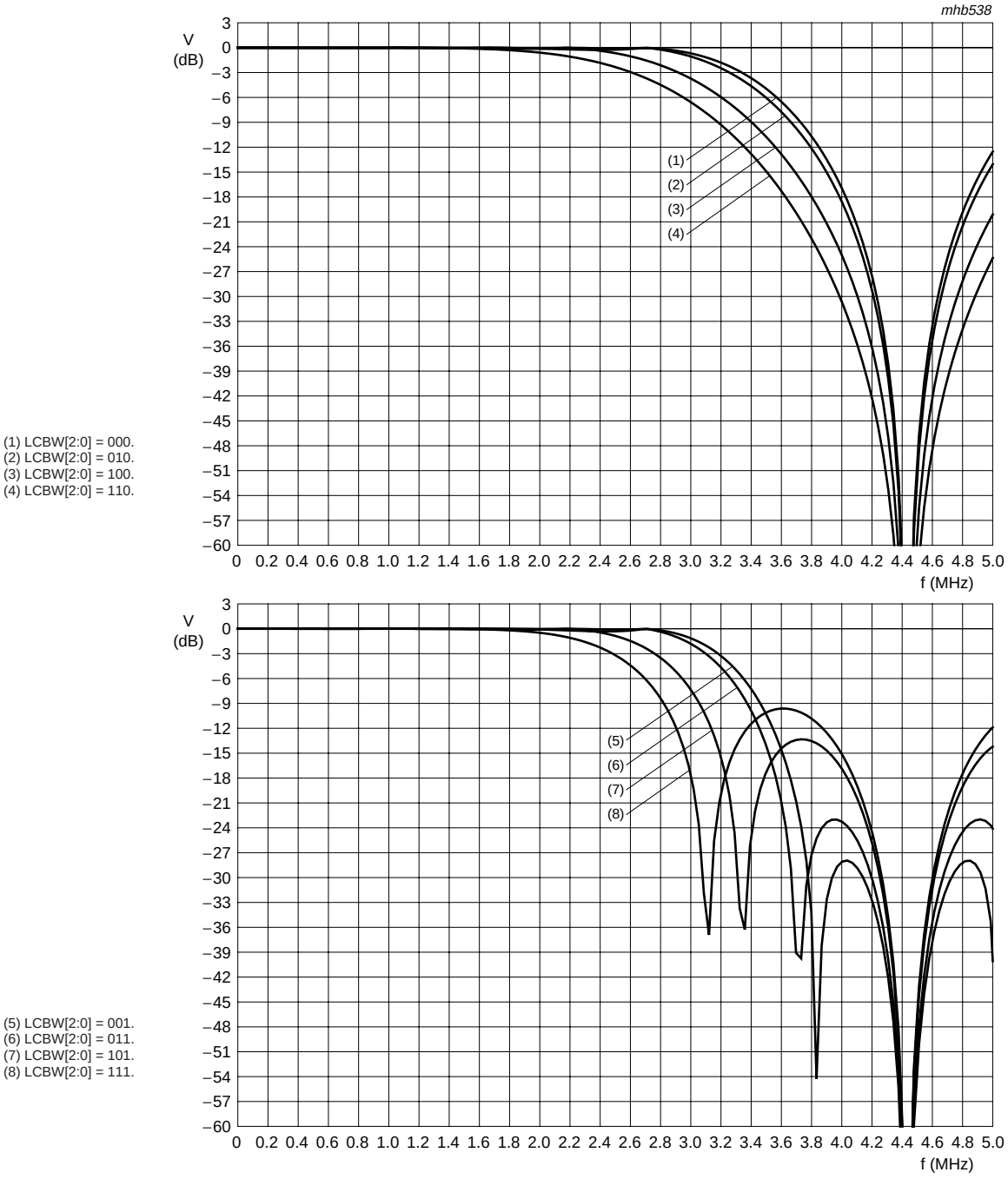
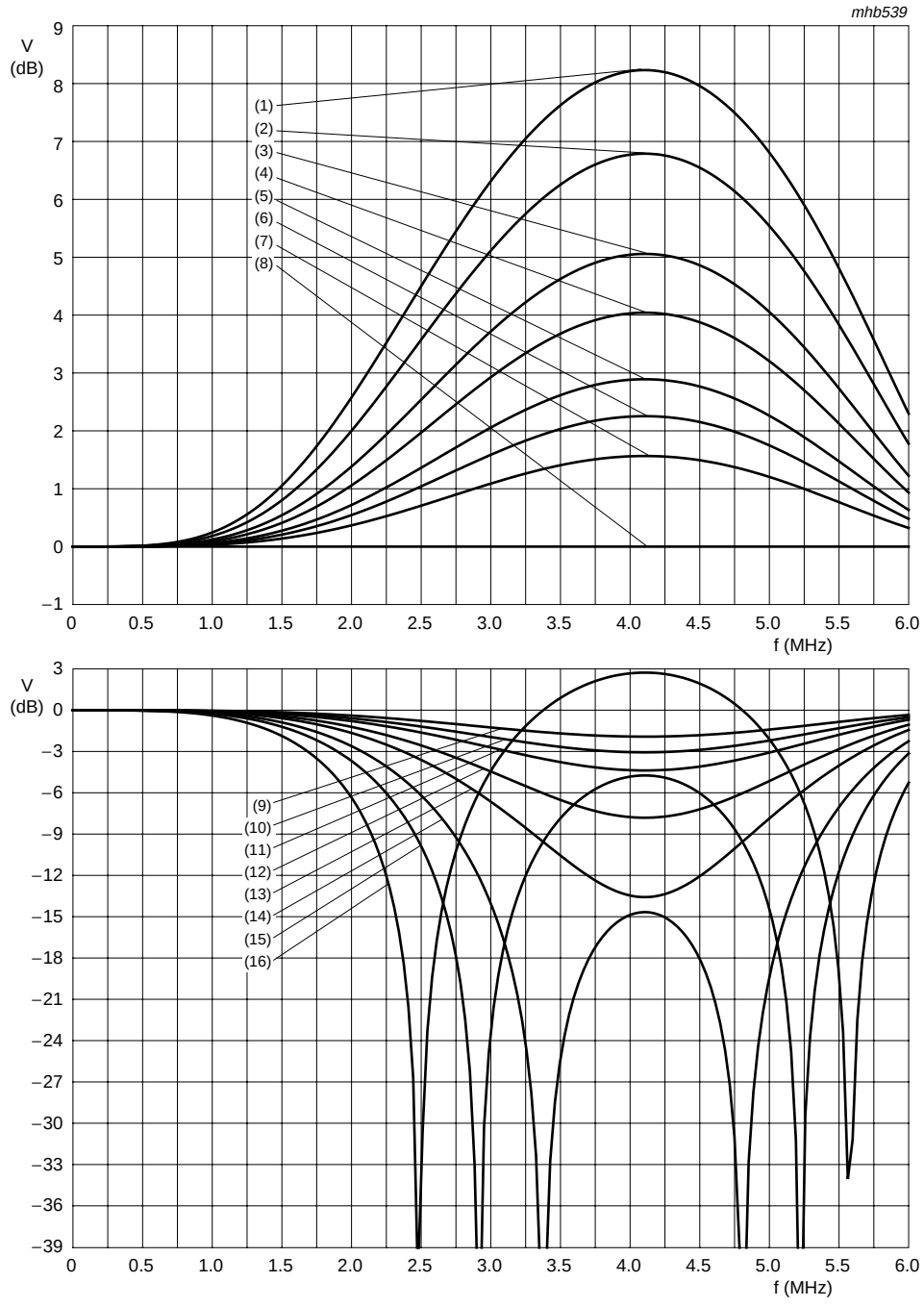


Fig 25. Transfer characteristics of the luminance notch filter in 4.43 MHz mode (Y-comb filter disabled) at LUBW = 1



(1) LUFI[3:0] = 0001.
(2) LUFI[3:0] = 0010.
(3) LUFI[3:0] = 0011.
(4) LUFI[3:0] = 0100.
(5) LUFI[3:0] = 0101.
(6) LUFI[3:0] = 0110.
(7) LUFI[3:0] = 0111.
(8) LUFI[3:0] = 0000.

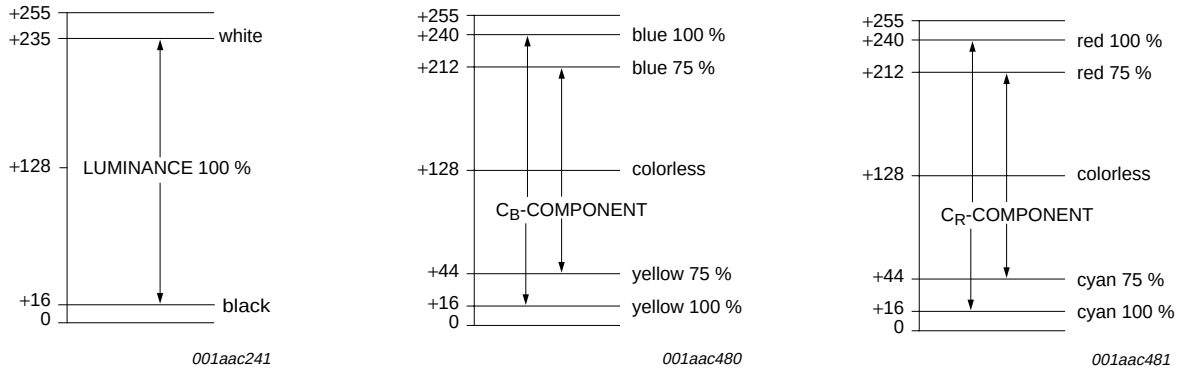
(9) LUFI[3:0] = 1000.
(10) LUFI[3:0] = 1001.
(11) LUFI[3:0] = 1010.
(12) LUFI[3:0] = 1011.
(13) LUFI[3:0] = 1100.
(14) LUFI[3:0] = 1101.
(15) LUFI[3:0] = 1110.
(16) LUFI[3:0] = 1111.

Fig 26. Transfer characteristics of the luminance peaking/low-pass filter (sharpness)

9.1.3.3 Brightness Contrast Saturation (BCS) control and decoder output levels

The resulting Y (CVBS) and C_B-C_R signals are fed to the BCS block, which contains the following functions:

- Chrominance saturation control by DSAT7 to DSAT0
- Luminance contrast and brightness control by DCON7 to DCON0 and DBRI7 to DBRI0
- Raw data (CVBS) gain and offset adjustment by RAWG7 to RAWG0 and RAWO7 to RAWO0
- Limiting Y-C_B-C_R or CVBS to the values 1 (minimum) and 254 (maximum) to fulfil *'ITU Recommendation 601/656'*



'ITU Recommendation 601/656' digital levels with default BCS (decoder) settings DCON[7:0] = 44h, DBRI[7:0] = 80h and DSAT[7:0] = 40h.

Equations for modification to the Y-C_B-C_R levels via BCS control I^2C-bus bytes DBRI, DCON and DSAT.

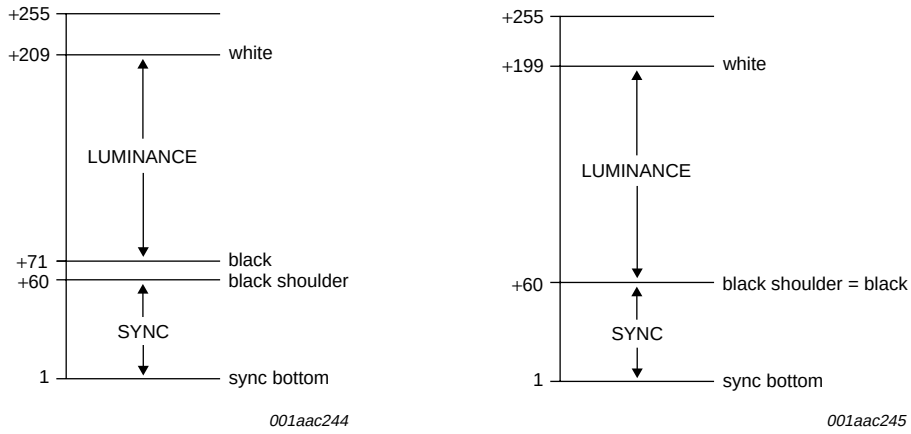
Luminance: $$Y_{OUT} = Int\left[\frac{DCON}{68} \times (Y - 128)\right] + DBRI$$

Chrominance: $$(C_R C_B)_{OUT} = Int\left[\frac{DSAT}{64} \times (C_R, C_B - 128)\right] + 128$$

It should be noted that the resulting levels are limited to 1 to 254 in accordance with *'ITU Recommendation 601/656'*

a. Y output range. b. C_B output range. c. C_R output range.

Fig 27. Y-C_B-C_R range for scaler input and X port output



CVBS levels with default settings RAWG[7:0] = 64 and RAWO[7:0] = 128.

Equation for modification of the raw data levels via bytes RAWG and RAWO:

$$CVBS_{OUT} = Int\left[\frac{RAWG}{64} \times (CVBS_{nom} - 128)\right] + RAWO$$

It should be noted that the resulting levels are limited to 1 to 254 in accordance with *'ITU Recommendation 601/656'*.

a. Sources containing 7.5 IRE black level offset (e.g. NTSC M).

b. Sources not containing black level offset.

Fig 28. CVBS (raw data) range for scaler input, data slicer and X port output

9.1.4 Synchronization

The prefiltered luminance signal is fed to the synchronization stage. Its bandwidth is further reduced to 1 MHz by a low-pass filter. The sync pulses are sliced and fed to the phase detectors where they are compared with the sub-divided clock frequency. The resulting output signal is applied to the loop filter to accumulate all phase deviations. Internal signals (e.g. HCL and HSY) are generated in accordance with analog front-end requirements. The loop filter signal drives an oscillator to generate the line frequency control signal LFCO; see Figure 29.

The detection of 'pseudo syncs' as part of the Macrovision copy protection standard is also achieved within the synchronization circuit.

The result is reported as flag COPRO within the decoder status byte at subaddress 1Fh.

9.1.5 Clock generation circuit

The internal CGC generates all clock signals required for the video input processor.

The internal signal LFCO is a digital-to-analog converted signal provided by the horizontal PLL. It is the multiple of the line frequency:

- 6.75 MHz = 429 × f_H (50 Hz), or
- 6.75 MHz = 432 × f_H (60 Hz)

The LFCO signal is multiplied by a factor of 2 and 4 in the internal PLL circuit (including phase detector, loop filtering, VCO and frequency divider) to obtain the output clock signals. The rectangular output clocks have a 50 % duty factor.

Table 19. Decoder clock frequencies

Clock	Frequency (MHz)
XTALO	24.576 or 32.110
LLC	27
LLC2	13.5
LLC4 (internal)	6.75
LLC8 (virtual)	3.375

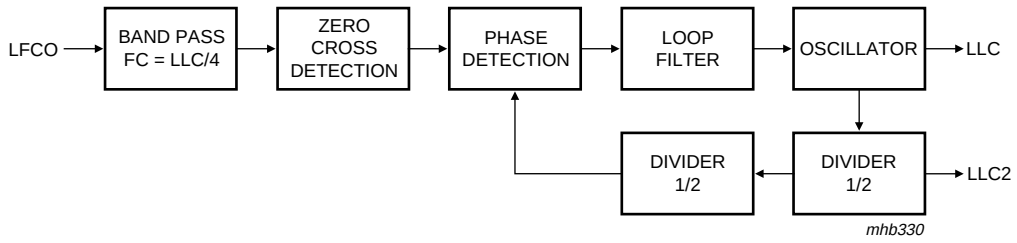
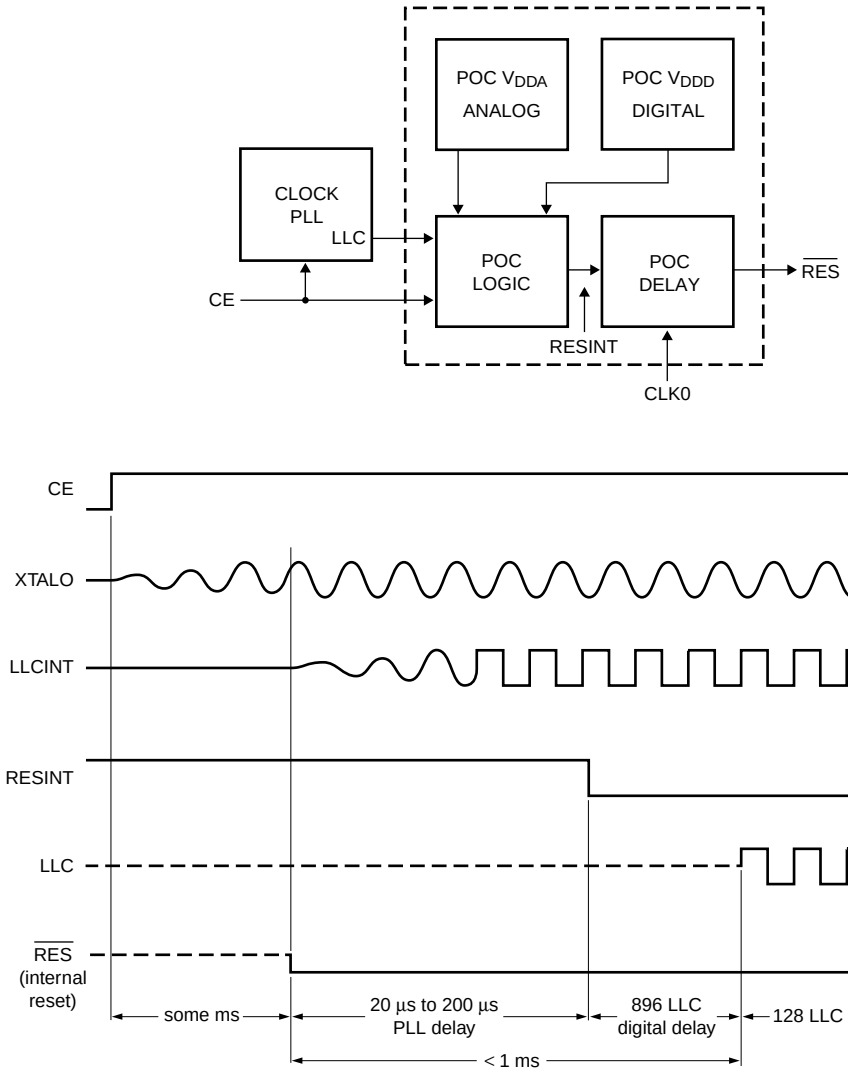


Fig 29. Block diagram of the clock generation circuit

9.1.6 Power-on reset and CE input

A missing clock, insufficient digital or analog V_{DDAd} supply voltages (below 2.7 V) will start the reset sequence; all outputs are forced to 3-state (see Figure 30). The indicator output $\overline{\text{RESd}}$ is LOW for approximately 128 LLC after the internal reset and can be applied to reset other circuits of the digital TV system.

It is possible to force a reset by pulling the CE input to ground. After the rising edge of CE and sufficient power supply voltage, the outputs LLC, LLC2 and SDAd return from 3-state to active, while the other signals have to be activated via programming.



POC = power-on control.

CE = chip enable input.

XTALO = crystal oscillator output.

LLCINT = internal system clock.

RESINT = internal reset.

LLC = line-locked clock output.

$\overline{RES}$ = reset output.

Fig 30. Power-on control circuit

9.2 Decoder output formatter

The output interface block of the decoder part contains the ITU 656 formatter for the expansion port data output XPD7 to XPD0 (for a detailed description see Section 10.4.1) and the control circuit for the signals needed for the internal paths to the scaler and data slicer part. It also controls the selection of the reference signals for the RT port (RTCO, RTS0 and RTS1) and the expansion port (XRH, XRV and XDQ).

The generation of the decoder data type control signals SET_RAW and SET_VBI is also done within this block. These signals are decoded from the requested data type for the scaler input and/or the data slicer, selectable by the control registers LCR2 to LCR24 (see also Section 11.2.4.2 “Subaddresses 41h to 57h”).

For each LCR value from 2 to 23 the data type can be programmed individually; LCR2 to LCR23 refer to line numbers. The selection in LCR24 values is valid for the rest of the corresponding field. The upper nibble contains the value for field 1 (odd), the lower nibble for field 2 (even). The relationship between LCR values and line numbers can be adjusted via VOFF8 to VOFF0, located in subaddresses 5Bh (bit 4) and 5Ah (bits 7 to 0) and FOFF subaddress 5Bh (bit 7). The recommended values are VOFF[8:0] = 03h for 50 Hz sources (with FOFF = 0) and VOFF[8:0] = 06h for 60 Hz sources (with FOFF = 1), to accommodate line number conventions as used for PAL, SECAM and NTSC standards; see Figure 31 and Figure 32.

Table 20. Data formats at decoder output

Data type number	Data type	Decoder output data format
0	teletext EuroWST, CCST	raw
1	European closed caption	raw
2	Video Programming Service (VPS)	raw
3	wide screen signalling bits	raw
4	US teletext (WST)	raw
5	US closed caption (line 21)	raw
6	video component signal, VBI region	Y-C_B-C_R 4 : 2 : 2
7	CVBS data	raw
8	teletext	raw
9	VITC/EBU time codes (Europe)	raw
10	VITC/SMPTE time codes (USA)	raw
11	reserved	raw
12	US NABTS	raw
13	MOJI (Japanese)	raw
14	Japanese format switch (L20/22)	raw
15	video component signal, active video region	Y-C_B-C_R 4 : 2 : 2

LINE NUMBER (1st FIELD)	521	522	523	524	525	1	2	3	4	5	6	7	8	9	
	active video					equalization pulses			serration pulses			equalization pulses			
LINE NUMBER (2nd FIELD)	259	260	261	262	263	264	265	266	267	268	269	270	271	272	
	active video					equalization pulses			serration pulses			equalization pulses			
LCR	24						2	3	4	5	6	7	8	9	

LINE NUMBER (1st FIELD)	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
	nominal VBI lines F1												active video			
LINE NUMBER (2nd FIELD)	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288
	nominal VBI lines F2												active video			
LCR	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	

001aad425

Vertical line offset, VOFF[8:0] = 06h (subaddresses 5Bh[4] and 5Ah[7:0]); horizontal pixel offset, HOFF[10:0] = 347h (subaddresses 5Bh[2:0] and 59h[7:0]); FOFF = 1 (subaddress 5Bh[7])

Fig 31. Relationship of LCR to line numbers in 525 lines/60 Hz systems

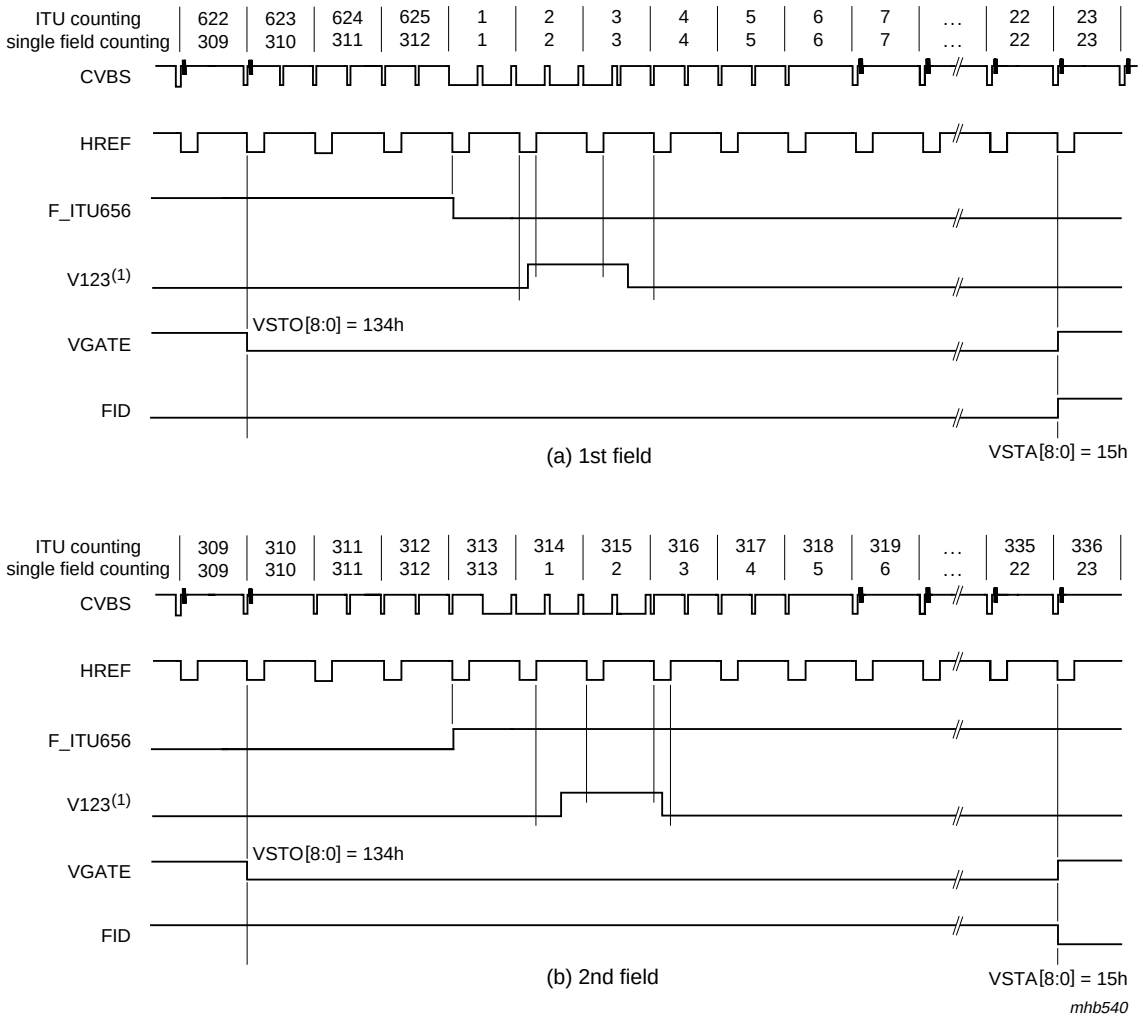
LINE NUMBER (1st FIELD)	621	622	623	624	625	1	2	3	4	5
	active video		equalization pulses			serration pulses		equalization pulses		
LINE NUMBER (2nd FIELD)	309	310	311	312	313	314	315	316	317	318
	active video		equalization pulses			serration pulses		equalization pulses		
LCR	24						2	3	4	5

LINE NUMBER (1st FIELD)	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
	nominal VBI lines F1																		active video	
LINE NUMBER (2nd FIELD)	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338
	nominal VBI lines F2																	active video		
LCR	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	

001aad426

Vertical line offset, VOFF[8:0] = 03h (subaddresses 5Bh[4] and 5Ah[7:0]); horizontal pixel offset, HOFF[10:0] = 347h (subaddresses 5Bh[2:0] and 59h[7:0]); FOFF = 0 (subaddress 5Bh[7])

Fig 32. Relationship of LCR to line numbers in 625 lines/50 Hz systems



(1) The inactive going edge of the V123 signal indicates whether the field is odd or even. If HREF is active during the falling edge of V123, the field is ODD (field 1). If HREF is inactive during the falling edge of V123, the field is EVEN. The specific position of the slope is dependent on the internal processing delay and may change a few clock cycles from version to version.

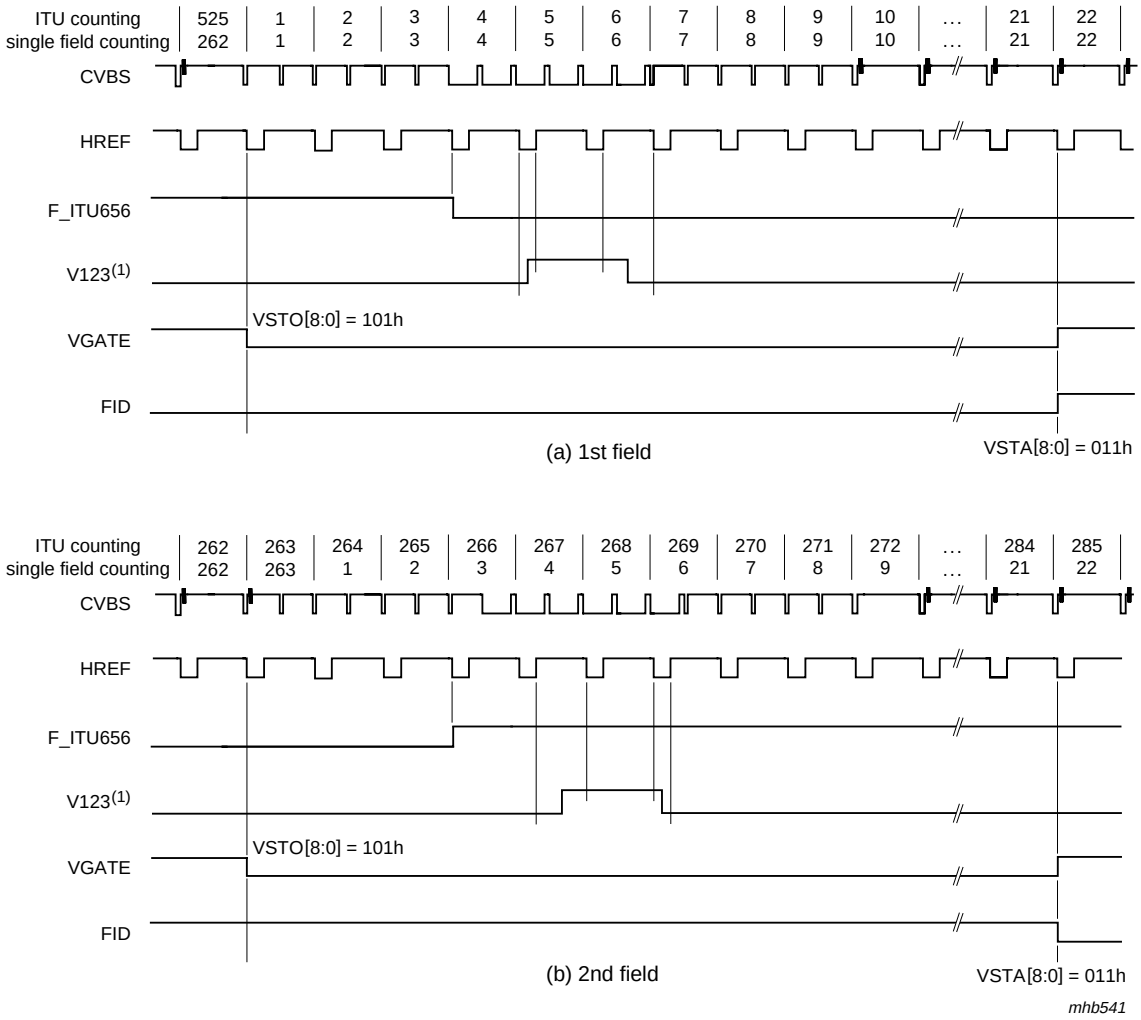
The control signals listed above are available on pins RTS0, RTS1, XRH and XRV according to Table 21.

For further information see Table 160, Table 161 and Table 162.

Fig 33. Vertical timing diagram for 50 Hz/625 line systems

Table 21. Control signals

Name	RTS0 (pin K13)	RTS1 (pin L10)	XRH (pin N2)	XRV (pin L5)
HREF	X	X	X	-
F_ITU656	-	-	-	X
V123	X	X	-	X
VGATE	X	X	-	-
FID	X	X	-	-

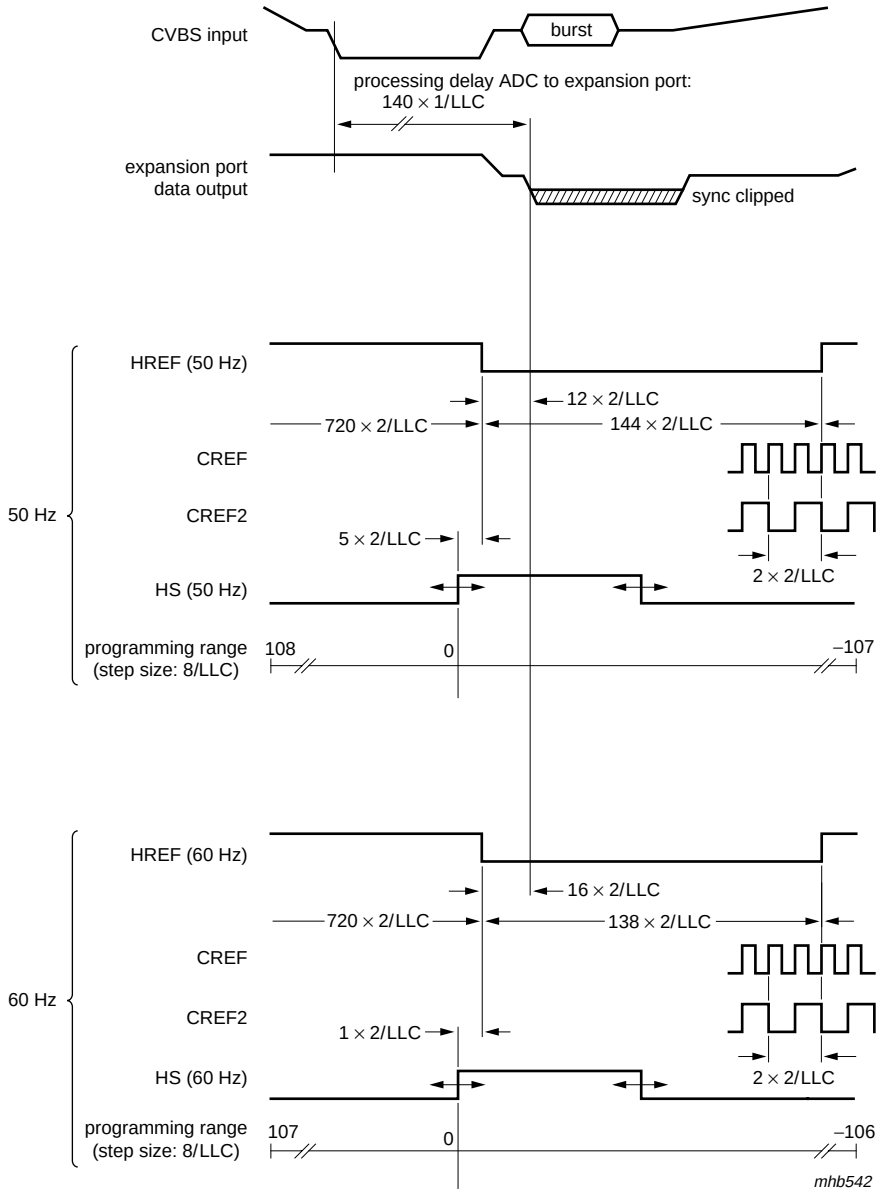


(1) The inactive going edge of the V123 signal indicates whether the field is odd or even. If HREF is active during the falling edge of V123, the field is ODD (field 1). If HREF is inactive during the falling edge of V123, the field is EVEN. The specific position of the slope is dependent on the internal processing delay and may change a few clock cycles from version to version.

The control signals listed above are available on pins RTS0, RTS1, XRH and XRV according to Table 21.

For further information see Table 160, Table 161 and Table 162.

Fig 34. Vertical timing diagram for 60 Hz/525 line systems



The signals HREF, HS, CREF2 and CREF are available on pins RTS0 and/or RTS1 (see Table 160 and Table 161); their polarity can be inverted via RTP0 and/or RTP1.

The signals HREF and HS are available on pin XRH (see Table 162).

Fig 35. Horizontal timing diagram (50/60 Hz)

9.3 Scaler

The High Performance video Scaler (HPS) is based on the system as implemented in previous products (e.g. SAA7140), but with some aspects enhanced. Vertical upsampling is supported and the processing pipeline buffer capacity is enhanced, to allow more flexible video stream timing at the image port, discontinuous transfers and handshake. The internal data flow from block to block is discontinuous dynamically, due to the scaling process.

The flow is controlled by internal data valid and data request flags (internal handshake signalling) between the sub-blocks; therefore the entire scaler acts as a pipeline buffer. Depending on the actual programmed scaling parameters the effective buffer can exceed to an entire line. The access/bandwidth requirements to the VGA frame buffer are reduced significantly.

The high performance video scaler in the SAA7108AE; SAA7109AE has the following major blocks:

- Acquisition control (horizontal and vertical timer) and task handling (the region/field/frame based processing)
- Prescaler, for horizontal downscaling by an integer factor, combined with appropriate band limiting filters, especially anti-aliasing for CIF format
- Brightness, saturation and contrast control for scaled output data
- Line buffer, with asynchronous read and write, to support vertical upscaling (e.g. for videophone application, converting 240 into 288 lines, Y-C_B-C_R 4 : 2 : 2)
- Vertical scaling, with phase accurate Linear Phase Interpolation (LPI) for zoom and downscale, or phase accurate Accumulation Mode (ACM) for large downscaling ratios and better anti-alias suppression
- Variable Phase Delay (VPD), operates as horizontal phase accurate interpolation for arbitrary non-integer scaling ratios, supporting conversion between square and rectangular pixel sampling
- Output formatter for scaled Y-C_B-C_R 4 : 2 : 2, Y-C_B-C_R 4 : 1 : 1 and Y only (format also used for raw data)
- FIFO, 32-bit wide, with 64 pixel capacity in Y-C_B-C_R formats
- Output interface, 8-bit or 16-bit (only if extended by H port) data pins wide, synchronous or asynchronous operation, with stream events on discrete pins, or coded in the data stream

The overall H and V zooming (HV_zoom) is restricted by the input/output data rate relationships. With a safety margin of 2 % for running in and running out, the maximum HV_zoom is equal to: $0.98 \times \frac{T\_input\_field - T\_v\_blanking}{in\_pixel \times in\_lines \times out\_cycle\_per\_pix \times T\_out\_clk}$

For example:

1. Input from decoder: 50 Hz, 720 pixel, 288 lines, 16-bit data at 13.5 MHz data rate, 1 cycle per pixel; output: 8-bit data at 27 MHz, 2 cycles per pixel; the maximum HV_zoom is equal to: $0.98 \times \frac{20\ ms - 24 \times 64\ \mu s}{720 \times 288 \times 2 \times 37\ ns} = 1.18$

2. Input from X port: 60 Hz, 720 pixel, 240 lines, 8-bit data at 27 MHz data rate (ITU 656), 2 cycles per pixel; output via I + H port: 16-bit data at 27 MHz clock, 1 cycle per pixel; the maximum HV_zoom is equal to:

$$0.98 \times \frac{16.666\ ms - 22 \times 64\ \mu s}{720 \times 240 \times 1 \times 37\ ns} = 2.34$$

The video scaler receives its input signal from the video decoder or from the expansion port (X port). It gets 16-bit Y-C_B-C_R 4 : 2 : 2 input data at a continuous rate of 13.5 MHz from the decoder. A discontinuous data stream can be accepted from the expansion port (X port), normally 8-bit wide ITU 656 such as Y-C_B-C_R data, accompanied by a pixel qualifier on XDQ.

The input data stream is sorted into two data paths, one for luminance (or raw samples) and one for time-multiplexed chrominance C_B and C_R samples. A Y-C_B-C_R 4 : 1 : 1 input format is converted to 4 : 2 : 2 for the horizontal prescaling and vertical filter scaling operation.

The scaler operation is defined by two programming pages A and B, representing two different tasks, that can be applied field alternating or to define two regions in a field (e.g. with different scaling range, factors and signal source during odd and even fields).

Each programming page contains control for:

- Signal source selection and formats
- Task handling and trigger conditions
- Input and output acquisition window definition
- H-prescaler, V-scaler and H-phase scaling

Raw VBI data is handled as a specific input format and needs its own programming page (equals own task).

In VBI pass through operation the processing of prescaler and vertical scaling has to be disabled, however, the horizontal fine scaling VPD can be activated. Upscaling (oversampling, zooming), free of frequency folding, up to a factor of 3.5 can be achieved, as required by some software data slicing algorithms.

These raw samples are transported through the image port as valid data and can be output as Y only format. The lines are framed by SAV and EAV codes.

9.3.1 Acquisition control and task handling (subaddresses 80h, 90h, 91h, 94h to 9Fh and C4h to CFh)

The acquisition control receives horizontal and vertical synchronization signals from the decoder section or from the X port. The acquisition window is generated via pixel and line counters at the appropriate places in the data path. From X port only qualified pixels and lines (lines with qualified pixel) are counted.

The acquisition window parameters are as follows:

- Signal source selection regarding input video stream and formats from the decoder, or from the X port (programming bits SCSRC[1:0] 91h[5:4] and FSC[2:0] 91h[2:0])

  Remark: The input of raw VBI data from the internal decoder should be controlled via the decoder output formatter and the LCR registers; see Section 9.2

- Vertical offset defined in lines of the video source, parameter YO[11:0] 99h[3:0] 98h[7:0]
- Vertical length defined in lines of the video source, parameter YS[11:0] 9Bh[3:0] 9Ah[7:0]
- Vertical length defined in number of target lines, as a result of vertical scaling, parameter YD[11:0] 9Fh[3:0] 9Eh[7:0]
- Horizontal offset defined in number of pixels of the video source, parameter XO[11:0] 95h[3:0] 94h[7:0]
- Horizontal length defined in number of pixels of the video source, parameter XS[11:0] 97h[3:0] 96h[7:0]
- Horizontal destination size defined in target pixels after fine scaling, parameter XD[11:0] 9Dh[3:0] 9Ch[7:0]

The source start offset (XO11 to XO0 and YO11to YO0) opens the acquisition window, and the target size (XD11 to XD0 and YD11 to YD0) closes the window, however the window is cut vertically if there are less output lines than expected. The trigger events for the pixel and line counts are the horizontal and vertical reference edges as defined in subaddress 92h. The task handling is controlled by subaddress 90h; see Section 9.3.1.2.

9.3.1.1 Input field processing

The trigger event for the field sequence detection from external signals (X port) are defined in subaddress 92h. From the X port the state of the scalers horizontal reference signal at the time of the vertical reference edge is taken as field sequence identifier FID. For example, if the falling edge of the XRV input signal is the reference and the state of XRH input is logic 0 at that time, the detected field ID is logic 0.

The bits XFDV[92h[7]] and XFDH[92h[6]] define the detection event and state of the flag from the X port. For the default setting of XFDV and XFDH at ‘00’ the state of the horizontal input at the falling edge of the vertical input is taken.

The scaler directly gets a corresponding field ID information from the SAA7108AE; SAA7109AE decoder path.

The FID flag is used to determine whether the first or second field of a frame is going to be processed within the scaler and it is also used as trigger condition for the task handling (see bits STRC[1:0] 90h[1:0]).

According to ITU 656, when FID is at logic 0 means first field of a frame. To ease the application, the polarities of the detection results on the X port signals and the internal decoder ID can be changed via XFDH.

As the V-sync from the decoder path has a half line timing (due to the interlaced video signal), but the scaler processing only knows about full lines, during 1st fields from the decoder the line count of the scaler possibly shifts by one line, compared to the 2nd field. This can be compensated for by switching the vertical trigger event, as defined by XDV0, to the opposite V-sync edge or by using the vertical scalers phase offsets. The vertical timing of the decoder can be seen in Figure 33 and Figure 34.

As the horizontal and vertical reference events inside the ITU 656 data stream (from X port) and the real-time reference signals from the decoder path are processed differently, the trigger events for the input acquisition also have to be programmed differently.

Table 22. Processing trigger and start

XDV1 92h[5]	XDV0 92h[4]	XDH 92h[2]	Description
			Internal decoder: The processing triggers at the falling edge of the V123 pulse [see Figure 33 (50 Hz) and Figure 34 (60 Hz)], and starts earliest with the rising edge of the decoder HREF at line number:
0	1	0	4/7 (50/60 Hz, 1st field), respectively 3/6 (50/60 Hz, 2nd field) (decoder count)
0	0	0	2/5 (50/60 Hz, 1st field), respectively 2/5 (50/60 Hz, 2nd field) (decoder count)
0	0	0	**External ITU 656 stream**: The processing starts earliest with SAV at line number 23 (50 Hz system), respectively line 20 (60 Hz system) (according to ITU 656 count)

9.3.1.2 Task handling

The task handler controls the switching between the two programming register sets. It is controlled by subaddresses 90h and C0h. A task is enabled via the global control bits TEA[80h[4]] and TEB[80h[5]].

The handler is then triggered by events which can be defined for each register set.

In the event of a programming error the task handling and the complete scaler can be reset to the initial states by setting the software reset bit SWRST[88h[5]] to logic 0. Especially if the programming registers, related acquisition window and scaler are reprogrammed while a task is active, a software reset **must** be performed after programming.

Contrary to the disabling/enabling of a task, which is evaluated at the end of a running task, when SWRST is at logic 0 it sets the internal state machines directly to their idle states.

The start condition for the handler is defined by bits STRC[1:0] 90h[1:0] and means: start immediately, wait for next V-sync, next FID at logic 0 or next FID at logic 1. The FID is evaluated, if the vertical and horizontal offsets are reached.

When RPTSK[90h[2]] is at logic 1 the actual running task is repeated (under the defined trigger conditions), before handing control over to the alternate task.

To support field rate reduction, the handler is also enabled to skip fields (bits FSKP[2:0] 90h[5:3]) before executing the task. A TOGGLE flag is generated (used for the correct output field processing), which changes state at the beginning of a task, every time a task is activated; examples are given in Section 9.3.1.3.

Remarks:

- **To activate a task the start condition must be fulfilled and the acquisition window offsets must be reached**. For example, in case of ‘start immediately’, and two regions are defined for one field, the offset of the lower region must be greater than (offset + length) of the upper region, if not, the actual counted H and V position at the end of the upper task is beyond the programmed offsets and the processing will ‘wait for next V’.

- **Basically the trigger conditions are checked, when a task is activated**. It is important to realize, that they are not checked while a task is inactive. So you can not trigger to next logic 0 or logic 1 with overlapping offset and active video ranges between the tasks (e.g. task A STRC[1:0] = 2, YO[11:0] = 310 and task B STRC[1:0] = 3, YO[11:0] = 310 results in an output field rate of $50/3$ Hz).
- **After power-on or software reset (via SWRST[88h[5]]) task B gets priority over task A**

9.3.1.3 Output field processing

As a reference for the output field processing, two signals are available for the back-end hardware.

These signals are the input field ID from the scaler source and a TOGGLE flag, which shows that an active task is used an odd (1, 3, 5...) or even (2, 4, 6...) number of times. Using a single or both tasks and reducing the field or frame rate with the task handling function, the TOGGLE information can be used to reconstruct an interlaced scaled picture at a reduced frame rate. The TOGGLE flag is not synchronized to the input field detection, as it is only dependent on the interpretation of this information by the external hardware, whether the output of the scaler is processed correctly; see Section 9.3.3.

When OFIDC = 0, the scalers input field ID is available as output field ID on bit 6 of SAV and EAV, respectively on pin IGP0 (IGP1), if the FID output is selected.

When OFIDC[90h[6]] = 1, the TOGGLE information is available as output field ID on bit 6 of SAV and EAV, respectively on pin IGP0 (IGP1), if the FID output is selected.

Additionally the bit 7 of SAV and EAV can be defined via CONLH[90h[7]]. CONLH[90h[7]] = 0 (default) sets bit 7 to logic 1, a logic 1 inverts the SAV/EAV bit 7. So it is possible to mark the output of both tasks by different SAV/EAV codes. This bit can also be seen as ‘task flag’ on pins IGP0 (IGP1), if TASK output is selected.

Table 23. Examples for field processing

Subject	Field sequence frame/field																			
	Example 1[1]			Example 2[2][3]				Example 3[2][4][5]						Example 4[2][4][6]					
	1/1	1/2	2/1	1/1	1/2	2/1	2/2	1/1	1/2	2/1	2/2	3/1	3/2	1/1	1/2	2/1	2/2	3/1	3/2
Processed by task	A	A	A	B	A	B	A	B	B	A	B	B	A	B	B	A	B	B	A
State of detected ITU 656 FID	0	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
TOGGLE flag	1	0	1	1	1	0	0	1	0	1	1	0	0	0[7]	1	1	1[7]	0	0
Bit 6 of SAV/EAV byte	0	1	0	0	1	0	1	1	0	1	1	0	0	0[7]	1	1	1[7]	0	0
Required sequence conversion at the vertical scaler[8]	UP ↓ UP	LO ↓ LO	UP ↓ UP	UP ↓ UP	LO ↓ LO	UP ↓ UP	LO ↓ LO	UP ↓ LO	LO ↓ UP	UP ↓ LO	LO ↓ LO	UP ↓ UP	LO ↓ UP	UP ↓ UP	LO ↓ LO	UP ↓ LO	LO ↓ LO	UP ↓ UP	LO ↓ UP
Output[9]	O	O	O	O	O	O	O	O	O	O	O	O	O	NO	O	O	NO	O	O

[1] Single task every field; OFIDC = 0; subaddress 90h at 40h; TEB[80h[5]] = 0.

[2] Tasks are used to scale to different output windows, priority on task B after SWRST.

[3] Both tasks at ½ frame rate; OFIDC = 0; subaddresses 90h at 43h and C0h at 42h.

[4] In examples 3 and 4 the association between input FID and tasks can be flipped, dependent on which time the SWRST is de-asserted.

[5] Task B at ⅔ frame rate constructed from neighboring motion phases; task A at ⅓ frame rate of equidistant motion phases; OFIDC = 1; subaddresses 90h at 41h and C0h at 45h.

[6] Task A and B at ⅓ frame rate of equidistant motion phases; OFIDC = 1; subaddresses 90h at 41h and C0h at 49h.

[7] State of prior field.

[8] It is assumed that input/output FID = 0 (= upper lines); UP = upper lines; LO = lower lines.

[9] O = data output; NO = no output.

9.3.2 Horizontal scaling

The overall horizontal required scaling factor has to be split into a binary and a rational value according to the following equation:

$$H\text{-}scale\ ratio = \frac{output\ pixel}{input\ pixel}$$

$$H\text{-}scale\ ratio = \frac{1}{XPSC[5:0]} \times \frac{1024}{XSCY[12:0]}$$

where the parameter of the prescaler XPSC[5:0] = 1 to 63 and the parameter of VPD phase interpolation XSCY[12:0] = 300 to 8191 (0 to 299 are only theoretical values). For example, $1/3.5$ is to split in $1/4 \times 1.14286$. The binary factor is processed by the prescaler, the arbitrary non-integer ratio is achieved via the variable phase delay VPD circuitry, called horizontal fine scaling. The latter calculates horizontally interpolated new samples with a 6-bit phase accuracy, which relates to less than 1 ns jitter for regular sampling schemes. Prescaler and fine scaler create the horizontal scaler of the SAA7108AE; SAA7109AE.

Using the accumulation length function of the prescaler (XACL[5:0] A1h[5:0]), application and destination dependent (e.g. scale for display or for a compression machine), a compromise between visible bandwidth and alias suppression can be determined.

9.3.2.1 Horizontal prescaler (subaddresses A0h to A7h and D0h to D7h)

The prescaling function consists of an FIR anti-alias filter stage and an integer prescaler, which creates an adaptive prescale dependent low-pass filter to balance the sharpness and aliasing effects.

The FIR prefilter stage implements different low-pass characteristics to reduce the anti-alias for downscales in the range of 1 to $\frac{1}{2}$. A CIF optimized filter is built-in, which reduces artefacts for CIF output formats (to be used in combination with the prescaler set to $\frac{1}{2}$ scale); see Table 24.

The function of the prescaler is defined by:

- An integer prescaling ratio XPSC[5:0] A0h[5:0] (equals 1 to 63), which covers the integer downscale range 1 to $\frac{1}{63}$
- An averaging sequence length XACL[5:0] A1h[5:0] (equals 0 to 63); range 1 to 64
- A DC gain renormalization XDCG[2:0] A2h[2:0]; 1 down to $\frac{1}{128}$
- The bit XC2_1[A2h[3]], which defines the weighting of the incoming pixels during the averaging process:
  - XC2_1 = 0 $\Rightarrow$ 1 + 1...+ 1 + 1
  - XC2_1 = 1 $\Rightarrow$ 1 + 2...+ 2 + 1

The prescaler creates a prescale dependent FIR low-pass, with up to 64 + 7 filter taps. The parameter XACL[5:0] can be used to vary the low-pass characteristic for a given integer prescale of $\frac{1}{XPSC[5:0]}$. The user can therefore decide between signal bandwidth (sharpness impression) and alias.

The equation for the XPSC[5:0] calculation is: $XPSC[5:0] = lower\ integer\ of\ \frac{Npix\_in}{Npix\_out}$

Where:

- The range is 1 to 63 (**value 0 is not allowed**)
- Npix_in = number of input pixel, and
- Npix_out = number of desired output pixel over the complete horizontal scaler

The use of the prescaler results in a XACL[5:0] and XC2_1 dependent gain amplification. The amplification can be calculated according to the equation:

DC gain = [(XACL[5:0] − XC2_1) + 1] × (XC2_1 + 1)

It is recommended to use sequence lengths and weights, which results in a 2^N DC gain amplification, as these amplitudes can be renormalized by the XDCG[2:0] controlled $\frac{1}{2^N}$ shifter of the prescaler.

The renormalization range of XDCG[2:0] is 1, $\frac{1}{2}$ down to $\frac{1}{128}$.

Other amplifications have to be normalized by using the following BCS control circuitry. In these cases the prescaler has to be set to an overall gain of ≤ 1, e.g. for an accumulation sequence of '1 + 1 + 1' (XACL[5:0] = 2 and XC2_1 = 0), XDCG[2:0] must be set to '010', this equals $^{1}/_{4}$ and the BCS has to amplify the signal to $^{4}/_{3}$ (SATN[7:0] and CONT[7:0] value = lower integer of $^{4}/_{3} \times 64$).

The use of XACL[5:0] is XPSC[5:0] dependent. XACL[5:0] must be < 2 × XPSC[5:0].

XACL[5:0] can be used to find a compromise between bandwidth (sharpness) and alias effects.

Remark: Due to bandwidth considerations XPSC[5:0] and XACL[5:0] can be chosen differently to the previously mentioned equations or Table 25, as the horizontal phase scaling is able to scale in the range from zooming up by factor 3 to downscaling by a factor of $^{1024}/_{8191}$.

Figure 38 and Figure 39 show some resulting frequency characteristics of the prescaler.

Table 25 shows the recommended prescaler programming. Other programming, other than given in Table 25, may result in better alias suppression, but the resulting DC gain amplification needs to be compensated by the BCS control, according to the equation:

$$CONT[7:0] = SATN[7:0] = lower\ integer\ of\ \frac{2^{XDCG[2:0]}}{DC\ gain \times 64}$$

Where:

- $2^{XDCG[2:0]} \geq$ DC gain
- DC gain = [(XACL[5:0] – XC2_1) + 1] × (XC2_1 + 1)

For example, if XACL[5:0] = 5, XC2_1 = 1, then the DC gain = 10 and the required XDCG[2:0] = 4.

The horizontal source acquisition timing and the prescaling ratio is identical for both the luminance path and chrominance path, but the FIR filter settings can be defined differently in the two channels.

Fade-in and fade-out of the filters is achieved by copying an original source sample each as first and last pixel after prescaling.

Figure 36 and Figure 37 show the frequency characteristics of the selectable FIR filters.

Table 24. FIR prefilter functions

PFUV[1:0] A2h[7:6] and PFY[1:0] A2h[5:4]	Luminance filter coefficients	Chrominance coefficients
00	bypassed	bypassed
01	1 2 1	1 2 1
10	–1 1 1.75 4.5 1.75 1 –1	3 8 10 8 3
11	1 2 2 2 1	1 2 2 2 1

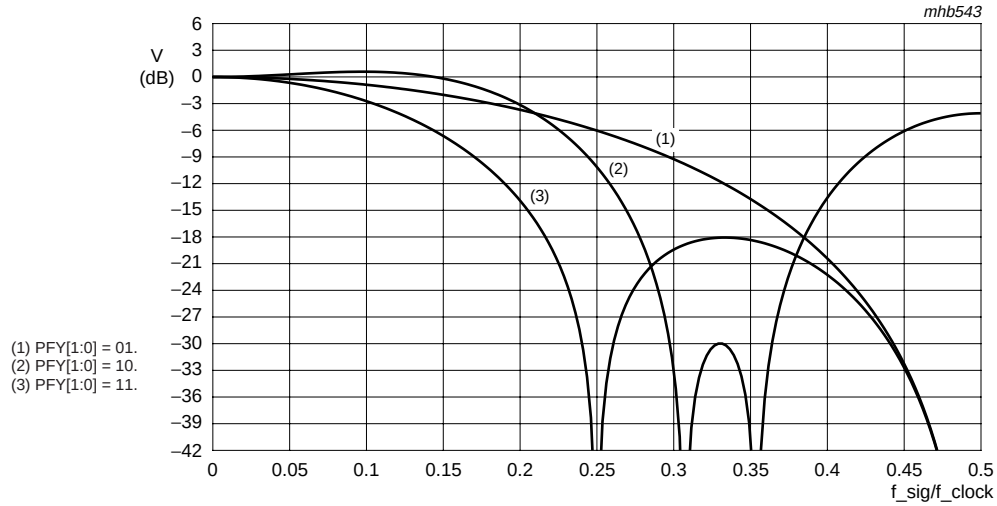


Fig 36. Luminance prefilter characteristic

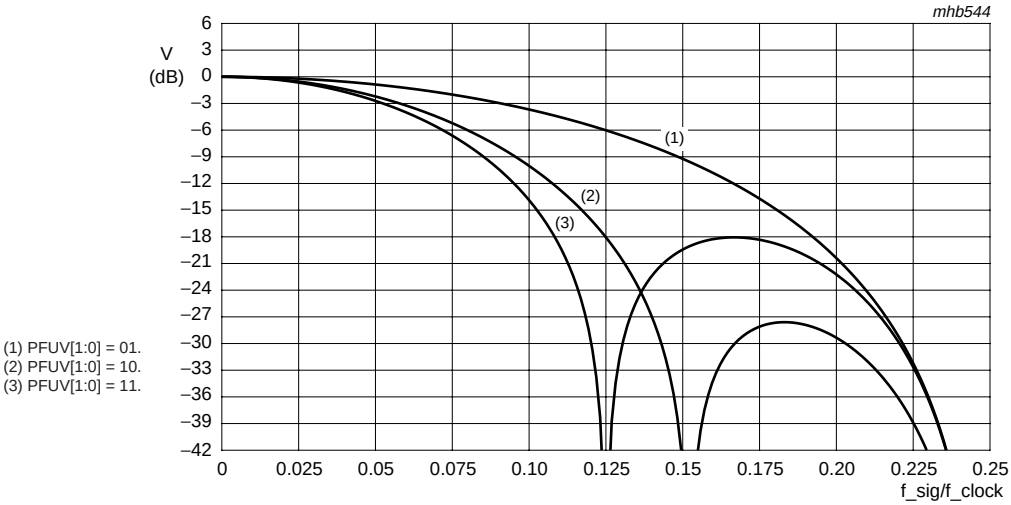
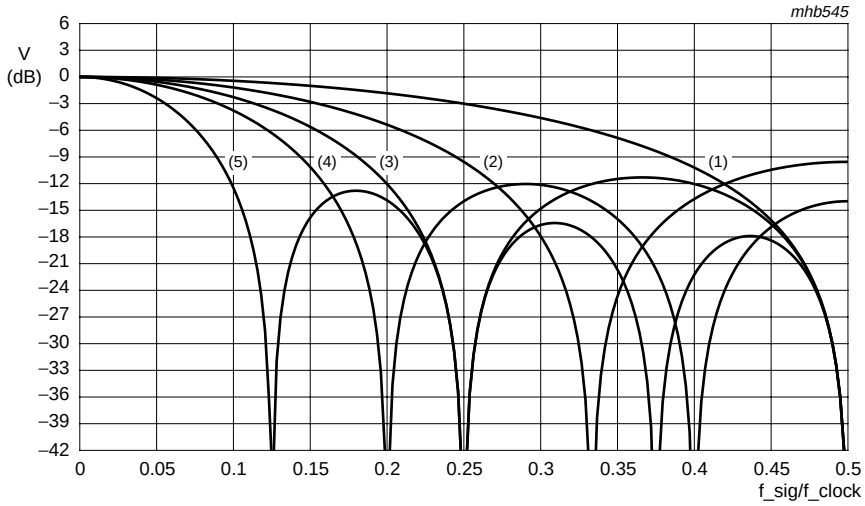
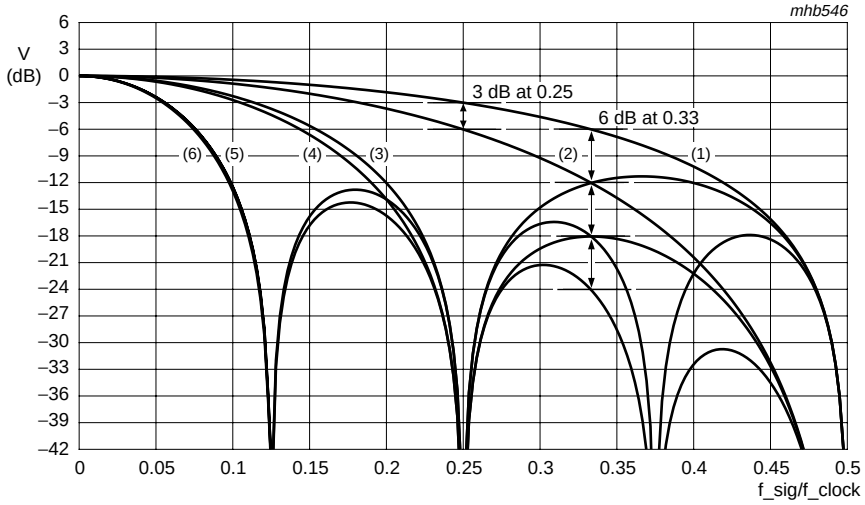


Fig 37. Chrominance prefilter characteristic



XC2_1 = 0; Zero's at $f = n \times \frac{1}{XACL + 1}$ with XACL = (1), (2), (3), (4) or (5)

Fig 38. Examples for prescaler filter characteristics: effect of increasing XACL[5:0]



(1) XC2_1 = 0 and XACL[5:0] = 1.
(2) XC2_1 = 1 and XACL[5:0] = 2.
(3) XC2_1 = 0 and XACL[5:0] = 3.
(4) XC2_1 = 1 and XACL[5:0] = 4.
(5) XC2_1 = 0 and XACL[5:0] = 7.
(6) XC2_1 = 1 and XACL[5:0] = 8.

Fig 39. Examples for prescaler filter characteristics: setting XC2_1

Table 25. Example of XACL[5:0] usage

Prescale ratio	XPSC [5:0]	Recommended values						FIR prefilter PFY[1:0]/ PFUV[1:0]
		For lower bandwidth requirements			For higher bandwidth requirements			
		XACL[5:0]	XC2_1	XDCG[2:0]	XACL[5:0]	XC2_1	XDCG[2:0]	
1	1	0	0	0	0	0	0	0 to 2
1/2	2	2	1	2	1	0	1	0 to 2
		(1 2 1) × 1/4[1]			(1 1) × 1/2[1]			
1/3	3	4	1	3	3	0	2	2
		(1 2 2 2 1) × 1/8[1]			(1 1 1 1) × 1/4[1]			
1/4	4	7	0	3	4	1	3	2
		(1 1 1 1 1 1 1 1) × 1/8[1]			(1 2 2 2 1) × 1/8[1]			
1/5	5	8	1	4	7	0	3	2
		(1 2 2 2 2 2 2 2 1) × 1/16[1]			(1 1 1 1 1 1 1 1) × 1/8[1]			
1/6	6	8	1	4	7	0	3	3
		(1 2 2 2 2 2 2 2 1) × 1/16[1]			(1 1 1 1 1 1 1 1) × 1/8[1]			
1/7	7	8	1	4	7	0	3	3
		(1 2 2 2 2 2 2 2 1) × 1/16[1]			(1 1 1 1 1 1 1 1) × 1/8[1]			
1/8	8	15	0	4	8	1	4	3
		(1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1) × 1/16[1]			(1 2 2 2 2 2 2 2 1) × 1/16[1]			
1/9	9	15	0	4	8	1	4	3
		(1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1) × 1/16[1]			(1 2 2 2 2 2 2 2 1) × 1/16[1]			
1/10	10	16	1	5	8	1	4	3
		(1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 1) × 1/32[1]			(1 2 2 2 2 2 2 2 1) × 1/16[1]			
1/13	13	16	1	5	16	1	5	3
1/15	15	31	0	5	16	1	5	3
1/16	16	31	0	5	16	1	5	3
1/19	19	32	1	6	32	1	6	3
1/31	31	32	1	6	32	1	6	3
1/32	32	63	1	7	32	1	6	3
1/35	35	63	1	7	63	1	7	3

[1] Resulting FIR function.

9.3.2.2 Horizontal fine scaling (variable phase delay filter; subaddresses A8h to AFh and D8h to DFh)

The horizontal fine scaling (VPD) should operate at scaling ratios between 1/2 and 2 (0.8 and 1.6), but can also be used for direct scaling in the range from $1/7.999$ to (theoretical) zoom 3.5 (restriction due to the internal data path architecture), without prescaler.

In combination with the prescaler a compromise between sharpness impression and alias can be found. This is signal source and application dependent.

For the luminance channel a filter structure with 10 taps is implemented, for the chrominance a filter with 4 taps.

Luminance and chrominance scale increments (XSCY[12:0] A9h[4:0] A8h[7:0] and XSCC[12:0] ADh[4:0] ACh[7:0]) are defined independently, but must be set in a 2 : 1 relationship in the actual data path implementation. The phase offsets XPHY[7:0] AAh[7:0] and XPHC[7:0] AEh[7:0] can be used to shift the sample phases slightly. XPHY[7:0] and XPHC[7:0] covers the phase offset range 7.999T to $\frac{1}{32}$T. The phase offsets should also be programmed in a 2 : 1 ratio.

The underlying phase controlling DTO has a 13-bit resolution.

According to the equations:

$$XSCY[12:0] = 1024 \times \frac{Npix\_in}{XPSC[5:0]} \times \frac{1}{Npix\_out} \text{ and } XSCC[12:0] = \frac{XSCY[12:0]}{2}$$

the VPD covers the scale range from 0.125 to zoom 3.5. VPD acts equivalent to a polyphase filter with 64 possible phases. In combination with the prescaler, it is possible to get very accurate samples from a highly anti-aliased integer downscaled input picture.

9.3.3 Vertical scaling

The vertical scaler of the SAA7108AE; SAA7109AE decoder part consists of a line FIFO buffer for line repetition and the vertical scaler block, which implements the vertical scaling on the input data stream in 2 different operational modes from theoretical zoom by 64 down to icon size $\frac{1}{64}$. The vertical scaler is located between the BCS and horizontal fine scaler, so that the BCS can be used to compensate the DC gain amplification of the ACM mode (see Section 9.3.3.2) as the internal RAMs are only 8-bit wide.

9.3.3.1 Line FIFO buffer (subaddresses 91h, B4h and C1h, E4h)

The line FIFO buffer is a dual ported RAM structure for 768 pixels, with asynchronous write and read access. The line buffer can be used for various functions, but not all functions may be available simultaneously.

The line buffer can buffer a complete unscaled active video line or more than one shorter lines (only for non-mirror mode), for selective repetition for vertical zoom-up.

For zooming up 240 lines to 288 lines e.g., every fourth line is requested (read) twice from the vertical scaling circuitry for calculation.

For conversion of a 4 : 2 : 0 or 4 : 1 : 0 input sampling scheme (MPEG, video phone, Indeo YUV-9) to ITU like sampling scheme 4 : 2 : 2, the chrominance line buffer is read twice or four times, before being refilled again by the source. It has to be preserved by means of the input acquisition window definition, so that the processing starts with a line containing luminance and chrominance information for 4 : 2 : 0 and 4 : 1 : 0 input. The bits FSC[2:1] 91h[2:1] define the distance between the Y/C lines. In the event of 4 : 2 : 2 and 4 : 1 : 1 FSC2 and FSC1 have to be set to ‘00’.

The line buffer can also be used for mirroring, i.e. for flipping the image left to right, for the vanity picture in video phone applications (bit YMIR[B4h[4]]). In mirror mode only one active prescaled line can be held in the FIFO at a time.

The line buffer can be utilized as an excessive pipeline buffer for discontinuous and variable rate transfer conditions at the expansion port or image port.

9.3.3.2 Vertical scaler (subaddresses B0h to BFh and E0h to EFh)

Vertical scaling of any ratio from 64 (theoretical zoom) to $^{1}/_{63}$ (icon) can be applied.

The vertical scaling block consists of another line delay, and the vertical filter structure, that can operate in two different modes; Linear Phase Interpolation (LPI) and Accumulation (ACM) mode. These are controlled by YMODE[B4h[0]]:

- **LPI mode**: In the LPI mode (YMODE = 0) two neighboring lines of the source video stream are added together, but weighted by factors corresponding to the vertical position (phase) of the target output line relative to the source lines. This linear interpolation has a 6-bit phase resolution, which equals 64 intra line phases. It interpolates between two consecutive input lines only. The LPI mode should be applied for scaling ratios around 1 (down to $^{1}/_{2}$), **it must be applied for vertical zooming**.
- **ACM mode**: The vertical ACM mode (YMODE = 1) represents a vertical averaging window over multiple lines, sliding over the field. This mode also generates phase correct output lines. The averaging window length corresponds to the scaling ratio, resulting in an adaptive vertical low-pass effect, to greatly reduce aliasing artefacts. ACM can be applied for downscales only from ratio 1 down to $^{1}/_{64}$. ACM results in a scale dependent **DC gain amplification**, which has to be precorrected by the BCS control of the scaler part.

The phase and scale controlling DTO calculates in 16-bit resolution, controlled by parameters YSCY[15:0] B1h[7:0] B0h[7:0] and YSCC[15:0] B3h[7:0] B2h[7:0], continuously over the entire field. A start offset can be applied to the phase processing by means of the parameters YPY3[7:0] to YPY0[7:0] in BFh[7:0] to BCh[7:0] and YPC3[7:0] to YPC0[7:0] in BBh[7:0] to B8h[7:0]. The start phase covers the range of $^{255}/_{32}$ to $^{1}/_{32}$ lines offset.

By programming appropriate, opposite, vertical start phase values (subaddresses B8h to BFh and E8h to EFh) depending on odd or even field ID of the source video stream and A or B page cycle, frame ID conversion and field rate conversion are supported (i.e. de-interlacing, re-interlacing).

Figure 40 and Figure 41 and Table 26 and Table 27 describe the use of the offsets.

Remark: The vertical start phase, as well as the scaling ratio are defined independently for the luminance and chrominance channel, but must be set to the same values in the actual implementation for accurate 4 : 2 : 2 output processing.

The vertical processing communicates on its input side with the line FIFO buffer. The scale related equations are:

- Scaling increment calculation for ACM and LPI mode, downscale and zoom:

  YSCY[15:0] and YSCC[15:0] = lower integer of $\left(1024 \times \frac{Nline\_in}{Nline\_out}\right)$

- BCS value to compensate DC gain in ACM mode (contrast and saturation have to be set): CONT[7:0] A5h[7:0] respectively SATN[7:0] A6h[7:0]

  = lower integer of $\left(\frac{Nline\_out}{Nline\_in} \times 64\right)$, or = lower integer of $\left(\frac{1024}{YSCY[15:0]} \times 64\right)$

9.3.3.3 Use of the vertical phase offsets

As described in Section 9.3.1.3, the scaler processing may run randomly over the interlaced input sequence. Additionally the interpretation and timing between ITU 656 field ID and real-time detection by means of the state of H-sync at the falling edge of V-sync may result in different field ID interpretation.

A vertically scaled interlaced output also gets a larger vertical sampling phase error, if the interlaced input fields are processed, without regard to the actual scale at the starting point of operation (see Figure 40).

Four events should be considered, they are illustrated in Figure 41.

In Table 26 and Table 27 PHO is a usable common phase offset.

It should be noted that the equations of Figure 41 produce an interpolated output, also for the unscaled case, as the geometrical reference position for all conversions is the position of the first line of the lower field; see Table 26.

If there is no need for UP-LO and LO-UP conversion and the input field ID is the reference for the back-end operation, then it is UP-LO = UP-UP and LO-UP = LO-LO and the $\frac{1}{2}$ line phase shift (PHO + 16) that can be skipped. This case is listed in Table 27.

The SAA7108AE; SAA7109AE supports 4 phase offset registers per task and component (luminance and chrominance). The value of 20h represents a phase shift of one line.

The registers are assigned to the following events; e.g. subaddresses B8h to BBh:

- B8h: 00 = input field ID 0, task status bit 0 (toggle status; see Section 9.3.1.3)
- B9h: 01 = input field ID 0, task status bit 1
- BAh: 10 = input field ID 1, task status bit 0
- BBh: 11 = input field ID 1, task status bit 1

Depending on the input signal (interlaced or non-interlaced) and the task processing 50 Hz or field reduced processing with one or two tasks (see examples in Section 9.3.1.3), other combinations may also be possible, but the basic equations are the same.

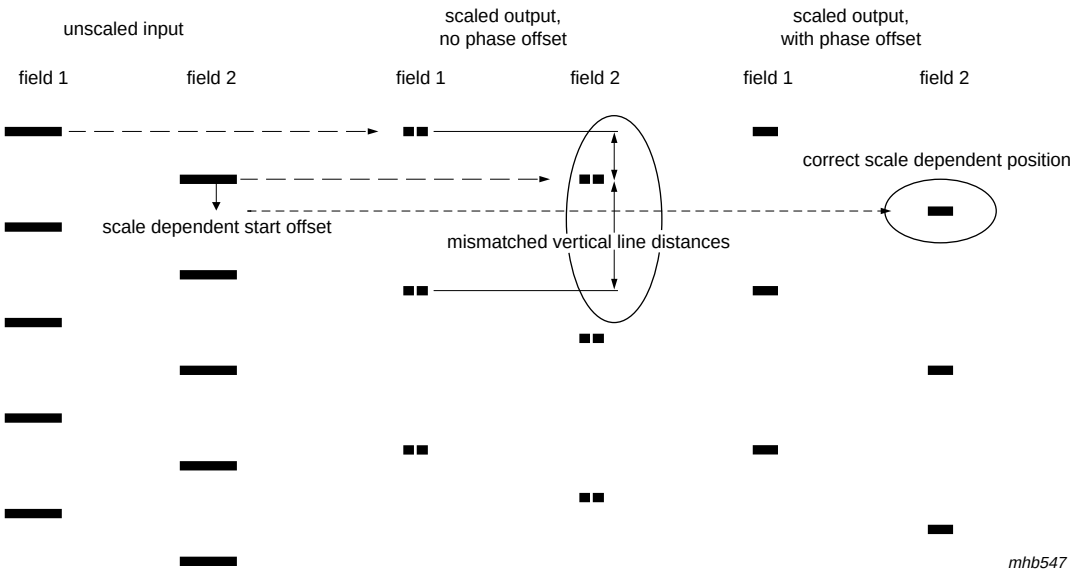
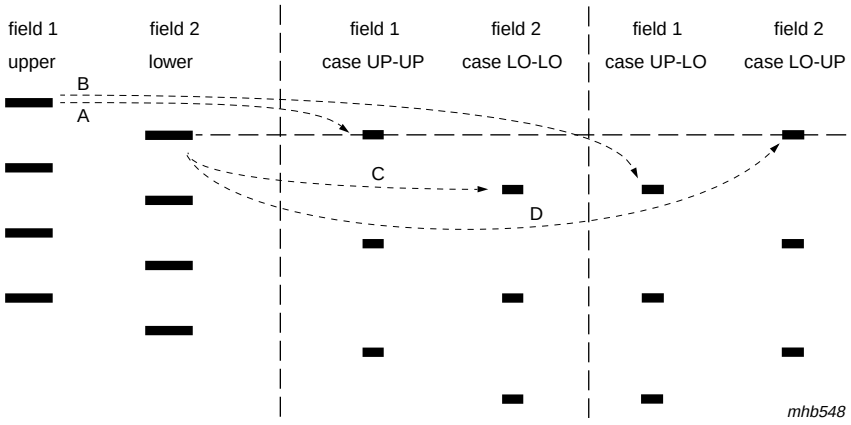


Fig 40. Basic problem of interlaced vertical scaling (example: downscale 3⁄5)



Offset = $\frac{1024}{32}$ = 32 = 1 line shift

A = $\frac{1}{2}$ input line shift = 16

B = $\frac{1}{2}$ input line shift + $\frac{1}{2}$ scale increment = $\frac{YSCY[15:0]}{64} + 16$

C = $\frac{1}{2}$ scale increment + $\frac{YSCY[15:0]}{64}$

D = no offset = 0

Fig 41. Derivation of the phase related equations (example: interlace vertical scaling down to 3⁄5, with field conversion)

Table 26. Examples for vertical phase offset usage: global equations

Input field under processing	Output field interpretation	Used abbreviation	Equation for phase offset calculation (decimal values)
Upper input lines	upper output lines	UP-UP	PHO + 16
Upper input lines	lower output lines	UP-LO	$PHO + \frac{YSCY[15:0]}{64} + 16$
Lower input lines	upper output lines	LO-UP	PHO
Lower input lines	lower output lines	LO-LO	$PHO + \frac{YSCY[15:0]}{64}$

Table 27. Vertical phase offset usage; assignment of the phase offsets

Detected input field ID	Task status bit	Vertical phase offset	Case	Equation to be used
0 = upper lines	0	YPY0[7:0] and YPC0[7:0]	case 1[1]	UP-UP (PHO)
			case 2[2]	UP-UP
			case 3[3]	UP-LO
0 = upper lines	1	YPY1[7:0] and YPC1[7:0]	case 1	UP-UP (PHO)
			case 2	UP-LO
			case 3	UP-UP
1 = lower lines	0	YPY2[7:0] and YPC2[7:0]	case 1	LO-LO $\left(PHO + \frac{YSCY[15:0]}{64} - 16\right)$
			case 2	LO-UP
			case 3	LO-LO
1 = lower lines	1	YPY3[7:0] and YPC3[7:0]	case 1	LO-LO $\left(PHO + \frac{YSCY[15:0]}{64} - 16\right)$
			case 2	LO-LO
			case 3	LO-UP

[1] Case 1: OFIDC[90h[6]] = 0; scaler input field ID as output ID; back-end interprets output field ID at logic 0 as upper output lines.

[2] Case 2: OFIDC[90h[6]] = 1; task status bit as output ID; back-end interprets output field ID at logic 0 as upper output lines.

[3] Case 3: OFIDC[90h[6]] = 1; task status bit as output ID; back-end interprets output field ID at logic 1 as upper output lines.

9.4 VBI data decoder and capture (subaddresses 40h to 7Fh)

The SAA7108AE; SAA7109AE contains a versatile VBI data decoder.

The implementation and programming model is in accordance with the VBI data slicer built into the multimedia video data acquisition circuit SAA5284.

The circuitry recovers the actual clock phase during the clock run-in period, slices the data bits with the selected data rate, and groups them into bytes. The result is buffered into a dedicated VBI data FIFO with a capacity of 2×56 bytes (2×14 double words). The clock frequency, signal source, field frequency and accepted error count must be defined in subaddress 40h.

The supported VBI data standards are shown in Table 28.

For lines 2 to 24 of a field, per VBI line, 1 of 16 standards can be selected (LCR24_[7:0] to LCR2_[7:0] in 57h[7:0] to 41h[7:0]: $23 \times 2 \times 4$ bit programming bits).

The definition for line 24 is valid for the rest of the corresponding field, normally no text data (video data) should be selected there (LCR24_[7:0] = FFh) to stop the activity of the VBI data slicer during active video.

To adjust the slicers processing to the input signal source, there are offsets in the horizontal and vertical direction available: parameters HOFF[10:0] 5Bh[2:0] 59h[7:0], VOFF[8:0] 5Bh[4] 5Ah[7:0] and FOFF[5Bh[7]].

Contrary to the scalers counting, the slicers offsets define the position of the horizontal and vertical trigger events related to the processed video field. The trigger events are the falling edge of HREF and the falling edge of V123 from the decoder processing part.

The relationship of these programming values to the input signal and the recommended values are given in Figure 31 and Figure 32.

Table 28. Data types supported by the data slicer block

DT[3:0] 62h[3:0]	Standard type	Data rate (Mbit/s)	Framing Code (FC)	FC window	Hamming check
0000	teletext EuroWST, CCST	6.9375	27h	WST625	always
0001	European closed caption	0.500	001	CC625	
0010	VPS	5	9951h	VPS	
0011	wide screen signalling bits	5	1E 3C1Fh	WSS	
0100	US teletext (WST)	5.7272	27h	WST525	always
0101	US closed caption (line 21)	0.503	001	CC525	
0110	(video data selected)	5	none	disable	
0111	(raw data selected)	5	none	disable	
1000	teletext	6.9375	programmable	general text	optional
1001	VITC/EBU time codes (Europe)	1.8125	programmable	VITC625	
1010	VITC/SMPTE time codes (USA)	1.7898	programmable	VITC525	
1011	reserved				
1100	US NABTS	5.7272	programmable	NABTS	optional
1101	MOJI (Japanese)	5.7272	programmable (A7h)	Japtext	
1110	Japanese format switch (L20/22)	5	programmable	open	
1111	no sliced data transmitted (video data selected)	5	none	disable	

9.5 Image port output formatter (subaddresses 84h to 87h)

The output interface consists of a FIFO for video and for sliced text data, an arbitration circuit, which controls the mixed transfer of video and sliced text data over the I port and a decoding and multiplexing unit, which generates the 8-bit or 16-bit wide output data stream and the accompanied reference and supporting information.

The clock for the output interface can be derived from an internal clock, decoder, expansion port or an externally provided clock which is appropriate for e.g. VGA and frame buffer. The clock can be up to 33 MHz. The scaler provides the following video related timing reference events (signals), which are available on pins as defined by subaddresses 84h and 85h:

- Output field ID
- Start and end of vertical active video range
- Start and end of active video line
- Data qualifier or gated clock
- Actually activated programming page (if CONLH is used)
- Threshold controlled FIFO filling flags (empty, full and filled)
- Sliced data marker

The discontinuous data stream at the scaler output is accompanied by a data valid flag (or data qualifier), or is transported via a gated clock. Clock cycles with invalid data on the I port data bus (including the HPD pins in 16-bit output mode) are marked with code 00h.

The output interface also arbitrates the transfer between scaled video data and sliced text data over the I port output.

The bits VITX1 and VITX0 (subaddress 86h) are used to control the arbitration.

As a further operation the serialization of the internal 32-bit double words to 8-bit or optional 16-bit output, as well as the insertion of the extended ITU 656 codes (SAV/EAV for video data, ANC or SAV/EAV codes for sliced text data) are done here.

For handshake with the VGA controller, or other memory or bus interface circuitry, programmable FIFO flags are provided; see Section 9.5.2.

9.5.1 Scaler output formatter (subaddresses 93h and C3h)

The output formatter organizes the packing into the output FIFO. The following formats are available: Y-C_B-C_R 4 : 2 : 2, Y-C_B-C_R 4 : 1 : 1, Y-C_B-C_R 4 : 2 : 0, Y-C_B-C_R 4 : 1 : 0 and Y only (e.g. for raw samples). The formatting is controlled by FSI[2:0] 93h[2:0], FOI[1:0] 93h[4:3] and FYSK[93h[5]].

The data formats are defined on double words, or multiples, and are similar to the video formats as recommended for PCI multimedia applications (compares to SAA7146A), but planar formats are not supported.

FSI[2:0] defines the horizontal packing of the data, FOI[1:0] defines how many Y only lines are expected, before a Y/C line will be formatted. If FYSK is set to logic 0 preceding Y only lines will be skipped, and the output will always start with a Y/C line.

Additionally the output formatter limits the amplitude range of the video data (controlled by ILLV[85h[5]]); see Table 31.

Table 29. Byte stream for different output formats

Output format	Byte sequence for 8-bit output modes													
Y-C_B-C_R 4 : 2 : 2	C_B0	Y0	C_R0	Y1	C_B2	Y2	C_R2	Y3	C_B4	Y4	C_R4	Y5	C_B6	Y6
Y-C_B-C_R 4 : 1 : 1	C_B0	Y0	C_R0	Y1	C_B4	Y2	C_R4	Y3	Y4	Y5	Y6	Y7	C_B8	Y8
Y only	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	Y10	Y11	Y12	Y13

Table 30. Explanation to Table 29

Name	Explanation
C_Bn	C_B (B – Y) color difference component, pixel number n = 0, 2, 4 to 718
Yn	Y (luminance) component, pixel number n = 0, 1, 2, 3 to 719
C_Rn	C_R (R – Y) color difference component, pixel number n = 0, 2, 4 to 718

Table 31. Limiting range on I port

Limit step ILLV[85h[5]]	Valid range		Suppressed codes (hexadecimal value)	
	Decimal value	Hexadecimal value	Lower range	Upper range
0	1 to 254	01 to FE	00	FF
1	8 to 247	08 to F7	00 to 07	F8 to FF

9.5.2 Video FIFO (subaddress 86h)

The video FIFO at the scaler output contains 32 double words. That corresponds to 64 pixels in 16-bit Y-C_B-C_R 4 : 2 : 2 format. But as the entire scaler can act as a pipeline buffer, the actual available buffer capacity for the image port is much higher, and can exceed beyond a video line.

The image port and the video FIFO, can operate with the video source clock (synchronous mode) or with an externally provided clock (asynchronous and burst mode), as appropriate for the VGA controller or attached frame buffer.

The video FIFO provides 4 internal flags, reporting to what extent the FIFO is actually filled.

These are:

- The FIFO Almost Empty (FAE) flag
- The FIFO Combined Flag (FCF) or FIFO filled, which is set at almost full level and reset, with hysteresis, only after the level crosses below the almost empty mark
- The FIFO Almost Full (FAF) flag
- The FIFO Overflow (FOVL) flag

The trigger levels for FAE and FAF are programmable by FFL[1:0] 86h[3:2] (16, 24, 28, full) and FEL[1:0] 86h[1:0] (16, 8, 4, empty).

The state of this flag can be seen on pins IGP0 or IGP1. The pin mapping is defined by subaddresses 84h and 85h; see Section 10.5.

9.5.3 Text FIFO

The data of the internal VBI data slicer is collected in the text FIFO before the transmission over the I port is requested (normally before the video window starts). It is partitioned into two FIFO sections. A complete line is filled into the FIFO before a data transfer is requested. So normally, one line of text data is ready for transfer, while the next text line is collected. Thus sliced text data is delivered as a block of qualified data, without any qualification gaps in the byte stream of the I port.

The decoded VBI data is collected in the dedicated VBI data FIFO. After the capture of a line has been completed, the FIFO can be streamed through the image port, preceded by a header, giving line number and standard.

The VBI data period can be signalled via the sliced data flag on pin IGP0 or IGP1. The decoded VBI data is lead by the ITU ancillary data header (DID[5:0] 5Dh[5:0] at value < 3Eh) or by SAV/EAV codes selectable by DID[5:0] at value 3Eh or 3Fh. Pin IGP0 or IGP1 is set if the first byte of the ANC header is valid on the I port bus. It is reset if an SAV occurs. So it may frame multiple lines of text data output, in the event that the video processing starts with a distance of several video lines to the region of text data. Valid sliced data from the text FIFO is available on the I port as long as the IGP0 or IGP1 flag is set and the data qualifier is active on pin IDQ.

The decoded VBI data is presented in two different data formats, controlled by bit RECODE.

- RECODE = 1: values 00h and FFh will be recoded to even parity values 03h and FCh
- RECODE = 0: values 00h and FFh may occur in the data stream as detected

9.5.4 Video and text arbitration (subaddress 86h)

Sliced text data and scaled video data are transferred over the same bus, the I port. The mixed transfer is controlled by an arbitration circuit.

If the video data is transferred without any interrupt and the video FIFO does not need to buffer any output pixel, the text data is inserted after the end of a scaled video line, normally during the blanking interval of the video.

9.5.5 Data stream coding and reference signal generation (subaddresses 84h, 85h and 93h)

As horizontal and vertical reference signals are logic 1, active gate signals are generated, which frame the transfer of the valid output data. As an alternative to the gates, the horizontal and vertical trigger pulses are generated on the rising edges of the gates.

Due to the dynamic FIFO behavior of the complete scaler path, the output signal timing has no fixed timing relationship to the real-time input video stream. So fixed propagation delays, in terms of clock cycles, related to the analog input cannot be defined.

The data stream is accompanied by a data qualifier. Additionally invalid data cycles are marked with code 00h.

If ITU 656 like codes are not required, they can be suppressed in the output stream.

As a further option, it is possible to provide the scaler with an external gating signal on pin ITRDY. Thereby making it possible to hold the data output for a certain time and to get valid output data in bursts of a guaranteed length.

The sketched reference signals and events can be mapped to the I port output pins IDQ, IGPH, IGPV, IGP0 and IGP1. For flexible use the polarities of all the outputs can be modified. The default polarity for the qualifier and reference signals is logic 1 (active).

Table 32 shows the relevant and supported SAV and EAV coding.

Table 32. SAV/EAV codes on the I port

Event description	SAV/EAV codes on I port[1] (hexadecimal)				Comment
	MSB[2] of SAV/EAV byte = 0		MSB[2] of SAV/EAV byte = 1		
	Field ID = 0	Field ID = 1	Field ID = 0	Field ID = 1	
Next pixel is FIRST pixel of any active line	0E	49	80	C7	HREF = active; VREF = active
Previous pixel was LAST pixel of any active line, but not the last	13	54	9D	DA	HREF = inactive; VREF = active
Next pixel is FIRST pixel of any V-blanking line	25	62	AB	EC	HREF = active; VREF = inactive
Previous pixel was LAST pixel of the last active line or of any V-blanking line	38	7F	B6	F1	HREF = inactive; VREF = inactive
No valid data, do not capture and do not increment pointer	00				IDQ pin inactive

[1] The leading byte sequence is: FFh-00h-00h.

[2] The MSB of the SAV/EAV code byte is controlled by:

a) Scaler output data: task A ⇒ MSB = $\overline{\text{CONLH}}$[90h[7]]; task B ⇒ MSB = $\overline{\text{CONLH}}$[C0h[7]].

b) VBI data slicer output data: DID[5:0] 5Dh[5:0] = 3Eh ⇒ MSB = 1; DID[5:0] 5Dh[5:0] = 3Fh ⇒ MSB = 0.

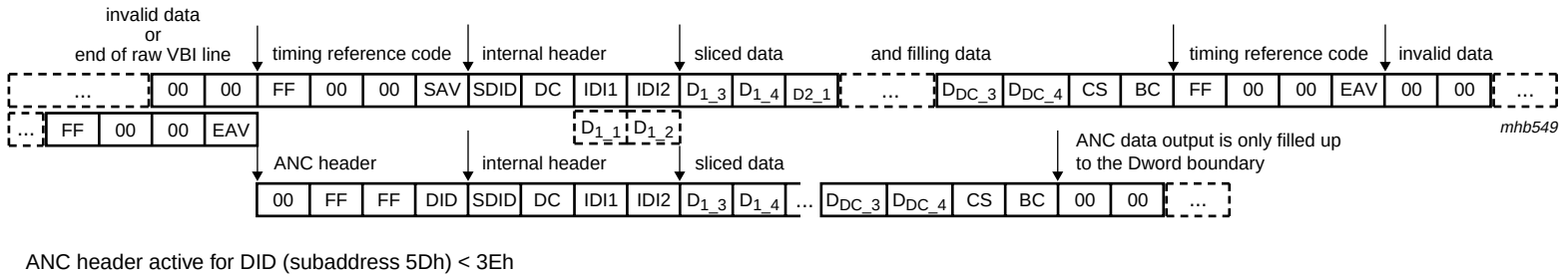


Fig 42. Sliced data formats on the I port in 8-bit mode

Table 33. Explanation to Figure 42

Name	Explanation
SAV	start of active data; see Table 34
SDID	sliced data identification: NEP[1], EP[2], SDID5 to SDID0, freely programmable via I^2C-bus subaddress 5Eh, bits 5 to 0, e.g. to be used as source identifier
DC	double word count: NEP[1], EP[2], DC5 to DC0. DC describes the number of succeeding 32-bit words:
	For SAV/EAV mode DC is fixed to 11 double words (byte value 4Bh)
	For ANC mode it is: DC = ¼(C + n), where C = 2 (the two data identification bytes IDI1 and IDI2) and n = number of decoded bytes according to the chosen text standard
	It should be noted that the number of valid bytes inside the stream can be seen in the BC byte.
IDI1	internal data identification 1: OP[3], FID (field 1 = 0, field 2 = 1), LineNumber8 to LineNumber3 = double word 1 byte 1; see Table 34
IDI2	internal data identification 2: OP[3], LineNumber2 to LineNumber0, DataType3 to DataType0 = double word 1 byte 2; see Table 34
D_{n_m}	double word number **n**, byte number **m**
D_{DC_4}	last double word byte 4; remark: for SAV/EAV framing DC is fixed to 0Bh, missing data bytes are filled up; the fill value is A0h
CS	the check sum byte, the check sum is accumulated from the SAV (respectively DID) byte to the D_{DC_4} byte
BC	number of valid sliced bytes counted from the IDI1 byte
EAV	end of active data; see Table 34

[1] Inverted EP (bit 7); for EP see Table note 2.

[2] Even parity (bit 6) of bits 5 to 0.

[3] Odd parity (bit 7) of bits 6 to 0.

Table 34. Bytes stream of the data slicer

Nick name	Comment	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DID, SAV, EAV	subaddress 5Dh = 00h	NEP[1]	EP[2]	0	1	0	FID[3]	I1[4]	I0[4]
	subaddress 5Dh bit 5 = 1	NEP[1]	EP[2]	0	D4[5Dh]	D3[5Dh]	D2[5Dh]	D1[5Dh]	D0[5Dh]
	subaddress 5Dh bit 5 = 3Eh[5]	1	FID[3]	V[6]	H[7]	P3	P2	P1	P0
	subaddress 5Dh bit 5 = 3Fh[5]	0	FID[3]	V[6]	H[7]	P3	P2	P1	P0
SDID	programmable via subaddress 5Eh	NEP[1]	EP[2]	D5[5Eh]	D4[5Eh]	D3[5Eh]	D2[5Eh]	D1[5Eh]	D0[5Eh]
DC[8]		NEP[1]	EP[2]	DC5	DC4	DC3	DC2	DC1	DC0
IDI1		OP[9]	FID[3]	LN8[10]	LN7[10]	LN6[10]	LN5[10]	LN4[10]	LN3[10]
IDI2		OP[9]	LN2[10]	LN1[10]	LN0[10]	DT3[11]	DT2[11]	DT1[11]	DT0[11]
CS	check sum byte	$\overline{CS6}$	CS6	CS5	CS4	CS3	CS2	CS1	CS0
BC	valid byte count	OP[9]	0	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0

[1] NEP = inverted EP; see Table note 2.

[2] EP = even parity of bits 5 to 0.

[3] FID = 0: field 1; FID = 1: field 2.

[4] I1 = 0 and I0 = 0: before line 1; I1 = 0 and I0 = 1: lines 1 to 23; I1 = 1 and I0 = 0: after line 23; I1 = 1 and I0 = 1: line 24 to end of field.

[5] Subaddress 5Dh at 3Eh and 3Fh are used for ITU 656 like SAV/EAV header generation; recommended value.

[6] V = 0: active video; V = 1: blanking.

[7] H = 0: start of line; H = 1: end of line.

[8] DC = data count in double words according to the data type.

[9] OP = odd parity of bits 6 to 0.

[10] LN = line number.

[11] DT = data type according to Table 28.

9.6 Audio clock generation (subaddresses 30h to 3Fh)

The SAA7108AE; SAA7109AE incorporates the generation of a field-locked audio clock as an auxiliary function for video capture. An audio sample clock, that is locked to the field frequency, ensures that there is always the same predefined number of audio samples associated with a field, or a set of fields. This ensures synchronous playback of audio and video after digital recording (e.g. capture to hard disk), MPEG or other compression, or non-linear editing.

9.6.1 Master audio clock

The audio clock is synthesized from the same crystal frequency as the line-locked video clock is generated. The master audio clock is defined by the parameters:

- Audio master Clocks Per Field, ACPF[17:0] 32h[1:0] 31h[7:0] 30h[7:0] according to the equation: $ACPF[17{:}0] = round\left(\frac{audio\ frequency}{field\ frequency}\right)$

- Audio master Clocks Nominal Increment, ACNI[21:0] 36h[5:0] 35h[7:0] 34h[7:0]

  according to the equation: $ACNI[21:0] = round\left(\frac{audio\ frequency}{crystal\ frequency} \times 2^{23}\right)$

See Table 35 for examples.

Remark: For standard applications the synthesized audio clock AMCLK can be used directly as master clock and as input clock for port AMXCLK (short cut) to generate ASCLK and ALRCLK. For high-end applications it is recommended to use an external analog PLL circuit to enhance the performance of the generated audio clock.

Table 35. Programming examples for audio master clock generation

Crystal frequency (MHz)	Field (Hz)	ACPF		ACNI	
		Decimal	Hex	Decimal	Hex
AMCLK = 256 × 48 kHz (12.288 MHz)					
32.11	50	245760	3 C000	3210190	30 FBCE
	59.94	205005	3 20CD	3210190	30 FBCE
24.576	50	-	-	-	-
	59.94	-	-	-	-
AMCLK = 256 × 44.1 kHz (11.2896 MHz)					
32.11	50	225792	3 7200	2949362	2D 00F2
	59.94	188348	2 DFBC	2949362	2D 00F2
24.576	50	225792	3 7200	3853517	3A CCCD
	59.94	188348	2 DFBC	3853517	3A CCCD
AMCLK = 256 × 32 kHz (8.192 MHz)					
32.11	50	163840	2 8000	2140127	20 A7DF
	59.94	136670	2 15DE	2140127	20 A7DF
24.576	50	163840	2 8000	2796203	2A AAAB
	59.94	136670	2 15DE	2796203	2A AAAB

9.6.2 Signals ASCLK and ALRCLK

Two binary divided signals ASCLK and ALRCLK are provided for slower serial digital audio signal transmission and for channel-select. The frequencies of these signals are defined by the following parameters:

- SDIV[5:0] 38h[5:0] according to the equation: $f_{ASCLK} = \frac{f_{AMXCLK}}{(SDIV + 1) \times 2} \Rightarrow$

  $SDIV[5:0] = \frac{f_{AMXCLK}}{2 f_{ASCLK}} - 1$

- LRDIV[5:0] 39h[5:0] according to the equation: $f_{ALRCLK} = \frac{f_{ASCLK}}{LRDIV \times 2} \Rightarrow$

  $LRDIV[5:0] = \frac{f_{ASCLK}}{2 f_{ALRCLK}}$

See Table 36 for examples.

Table 36. Programming examples for ASCLK/ALRCLK clock generation

AMXCLK (MHz)	ASCLK (kHz)	SDIV		ALRCLK (kHz)	LRDIV	
		Decimal	Hex		Decimal	Hex
12.288	1536	3	03	48	16	10
	768	7	07	48	8	08
11.2896	1411.2	3	03	44.1	16	10
	2822.4	1	01	44.1	32	10
8.192	1024	3	03	32	16	10
	2048	1	01	32	32	10

9.6.3 Other control signals

Further control signals are available to define reference clock edges and vertical references; see Table 37.

Table 37. Control signals

Control signal	Description
APLL[3Ah[3]]	Audio PLL mode
	0 = PLL closed
	1 = PLL open
AMVR[3Ah[2]]	Audio Master clock Vertical Reference
	0 = internal vertical reference
	1 = external vertical reference
LRPH[3Ah[1]]	ALRCLK phase
	0 = invert ASCLK, ALRCLK edges triggered by falling edge of ASCLK
	1 = do not invert ASCLK, ALRCLK edges triggered by rising edge of ASCLK
SCPH[3Ah[0]]	ASCLK phase
	0 = invert AMXCLK, ASCLK edges triggered by falling edge of AMXCLK
	1 = do not invert AMXCLK, ASCLK edges triggered by rising edge of AMXCLK

10. Input/output interfaces and ports of digital video decoder part

The SAA7108AE; SAA7109AE has 5 different I/O interfaces:

- Analog video input interface, for analog CVBS and/or Y and C input signals
- Audio clock port
- Digital real-time signal port (RT port)
- Digital video expansion port (X port), for unscaled digital video input and output
- Digital image port (I port) for scaled video data output and programming
- Digital host port (H port) for extension of the image port or expansion port from 8-bit to 16-bit

10.1 Analog terminals

The SAA7108AE; SAA7109AE has 6 analog inputs AI21 to AI24, AI11 and AI12 (see Table 38) for composite video CVBS or S-video Y/C signal pairs. Additionally, there are two differential reference inputs, which must be connected to ground via a capacitor equivalent to the decoupling capacitors at the 6 inputs. There are no peripheral components required other than these decoupling capacitors and 18 Ω/56 Ω termination resistors, one set per connected input signal; see also application example in Figure 68. Two anti-alias filters are integrated, and self adjusting via the clock frequency.

Clamp and gain control for the two ADCs are also integrated. An analog video output (pin AOUT) is provided for testing purposes.

Table 38. Analog pin description

Symbol	Pin	I/O	Description	Bit
AI24 to AI21	P6, P7, P9 and P10	I	analog video signal inputs, e.g. 2 CVBS signals and two Y/C pairs can be connected simultaneously	MODE3 to MODE0
AI12 and AI11	P11 and P13	I	analog video signal inputs, e.g. 2 CVBS signals and two Y/C pairs can be connected simultaneously	MODE3 to MODE0
AOUT	M10	O	analog video output, for test purposes	AOSL1 and AOSL0
AI1D and AI2D	P12 and P8	I	analog reference pins for differential ADC operation	-

10.2 Audio clock signals

The SAA7108AE; SAA7109AE also synchronizes the audio clock and sampling rate to the video frame rate, via a very slow PLL. This ensures that the multimedia capture and compression processes always gather the same predefined number of samples per video frame.

An audio master clock AMCLK and two divided clocks, ASCLK and ALRCLK, are generated; see Table 39.

- ASCLK: can be used as audio serial clock
- ALRCLK: audio left/right channel clock

The ratios are programmable; see Section 9.6.

Table 39. Audio clock pin description

Symbol	Pin	I/O	Description	Bit
AMCLK	K12	O	audio master clock output	ACPF[17:0] 32h[1:0] 31h[7:0] 30h[7:0] and ACNI[21:0] 36h[5:0] 35h[7:0] 34h[7:0]
AMXCLK	J12	I	external audio master clock input for the clock division circuit, can be directly connected to output AMCLK for standard applications	-
ASCLK	K14	O	serial audio clock output, can be synchronized to rising or falling edge of AMXCLK	SDIV[5:0] 38h[5:0] and SCPH[3Ah[0]]
ALRCLK	J13	O	audio channel (left/right) clock output, can be synchronized to rising or falling edge of ASCLK	LRDIV[5:0] 39h[5:0] and LRPH[3Ah[1]]

10.3 Clock and real-time synchronization signals

For the generation of the line-locked video (pixel) clock LLC, and of the frame-locked audio serial bit clock, a crystal accurate frequency reference is required. An oscillator is built-in for fundamental or third harmonic crystals. The supported crystal frequencies are 32.11 MHz or 24.576 MHz (defined during reset by strapping pin ALRCLK).

Alternatively pins XTALId and XTALIe can be driven from an external single-ended oscillator.

The crystal oscillation can be propagated as a clock to other ICs in the system via pin XTOUTd.

The Line-Locked Clock (LLC) is the double pixel clock of nominal 27 MHz. It is locked to the selected video input, generating baseband video pixels according to *"ITU recommendation 601"*. In order to support interfacing circuits, a direct pixel clock (LLC2) is also provided.

The pins for line and field timing reference signals are RTCO, RTS1 and RTS0. Various real-time status information can be selected for the RTS pins. The signals are always available (output) and reflect the synchronization operation of the decoder part in the SAA7108AE; SAA7109AE. The function of the RTS1 and RTS0 pins can be defined by bits RTSE1[3:0] 12h[7:4] and RTSE0[3:0] 12h[3:0]; see Table 40.

Table 40. Clock and real-time synchronization signals

Symbol	Pin	I/O	Description	Bit
Crystal oscillator				
XTALId	P2	I	input for crystal oscillator or reference clock	-
XTALOd	P3	O	output of crystal oscillator	-
XTOUTd	P4	O	reference (crystal) clock output drive (optional)	XTOUTE[14h[3]]
Real-time signals (RT port)				
LLC	M14	O	line-locked clock, nominal 27 MHz, double pixel clock locked to the selected video input signal	-

Table 40. Clock and real-time synchronization signals *...continued*

Symbol	Pin	I/O	Description	Bit
LLC2	L14	O	line-locked pixel clock, nominal 13.5 MHz	-
RTCO	L13	O	real-time control output, transfers real-time status information supporting RTC level 3.1 (see document *"How to use Real Time Control (RTC)"*, available on request)	-
RTS0	K13	O	real-time status information line 0, can be programmed to carry various real-time information; see Table 160	RTSE0[3:0] 12h[3:0]
RTS1	L10	O	real-time status information line 1, can be programmed to carry various real-time information; see Table 161	RTSE1[3:0] 12h[7:4]

10.4 Video expansion port (X port)

The expansion port is intended for transporting video streams of image data from other digital video circuits such as MPEG encoder/decoder and video phone codec, to the image port (I port); see Table 41.

The expansion port consists of two groups of signals/pins:

- 8-bit data, I/O, regular components video Y-C_B-C_R 4 : 2 : 2, i.e. C_B-Y-C_R-Y, byte serial, exceptionally raw video samples (e.g. ADC test); in input mode the data bus can be extended to 16-bit by pins HPD7 to HPD0.
- Clock, synchronization and auxiliary signals, accompanying the data stream, I/O

As output, these are direct copies of the decoder signals.

The data transfers through the expansion port represent a single D1 port, with half duplex mode. The SAV and EAV codes may be inserted optionally for data input (controlled by bit XCODE[92h[3]]). The input/output direction is switched for complete fields only.

Table 41. Signals dedicated to the expansion port

Symbol	Pin	I/O	Description	Bit
XPD7 to XPD0	K2, K3, L1 to L3, M1, M2 and N1	I/O	X port data: in output mode controlled by decoder section, data format see Table 42; in input mode Y-C_B-C_R 4 : 2 : 2 serial input data or luminance part of a 16-bit Y-C_B-C_R 4 : 2 : 2 input	OFTS[2:0] 13h[2:0], 91h[7:0] and C1h[7:0]
XCLK	M3	I/O	clock at expansion port: if output, then copy of LLC; as input normally a double pixel clock of up to 32 MHz or a gated clock (clock gated with a qualifier)	XCKS[92h[0]]
XDQ	M4	I/O	data valid flag of the expansion port input (qualifier): if output, then decoder (HREF and VGATE) gate; see Figure 35	-
XRDY	N3	O	data request flag = ready to receive, to work with optional buffer in external device, to prevent internal buffer overflow; second function: input related task flag A/B	XRQT[83h[2]]

Table 41. Signals dedicated to the expansion port *…continued*

Symbol	Pin	I/O	Description	Bit
XRH	N2	I/O	horizontal reference signal for the X port: as output: HREF or HS from the decoder (see Figure 35); as input: a reference edge for horizontal input timing and a polarity for input field ID detection can be defined	XRHS[13h[6]], XFDH[92h[6]] and XDH[92h[2]]
XRV	L5	I/O	vertical reference signal for the X port: as output: V123 or field ID from the decoder (see Figure 33 and Figure 34); as input: a reference edge for vertical input timing and for input field ID detection can be defined	XRVS[1:0] 13h[5:4], XFDV[92h[7]] and XDV[1:0] 92h[5:4]
XTRI	K1	I	port control: switches X port input to 3-state	XPE[1:0] 83h[1:0]

10.4.1 X port configured as output

If the data output is enabled at the expansion port, then the data stream from the decoder is presented. The data format of the 8-bit data bus is dependent on the chosen data type, selectable by the line control registers LCR2 to LCR24; see Table 20. In contrast to the image port, the sliced data format is not available on the expansion port. Instead, raw CVBS samples are always transferred if any sliced data type is selected.

Some details of data types on the expansion port are as follows:

- **Active video** (data type 15): contains component Y-C_B-C_R 4 : 2 : 2 signal, 720 active pixels per line. The amplitude and offsets are programmable via DBRI7 to DBRI0, DCON7 to DCON0, DSAT7 to DSAT0, OFFU1, OFFU0, OFFV1 and OFFV0. The nominal levels are illustrated in Figure 27.
- **Test line** (data type 6): is similar to the active video format, with some constraints within the data processing:
  - Adaptive chrominance comb filter, vertical filter (chrominance comb filter for NTSC standards, PAL phase error correction) within the chrominance processing are disabled
  - Adaptive luminance comb filter, peaking and chrominance trap are bypassed within the luminance processing

  This data type is defined for future enhancements. It could be activated for lines containing standard test signals within the vertical blanking period. Currently most sources do not contain test lines. The nominal levels are illustrated in Figure 27.
- **Raw samples** (data types 0 to 5 and 7 to 14): C_B-C_R samples are similar to data type 6, but CVBS samples are transferred instead of processed luminance samples within the Y time slots.

  The amplitude and offset of the CVBS signal is programmable via RAWG7 to RAWG0 and RAWO7 to RAWO0; see Section 11, Table 167 and Table 168. The nominal levels are illustrated in Figure 28.

The relationship of LCR programming to line numbers is described in Section 9.2, Figure 31 and Figure 32.

The data type selections by LCR are overruled by setting OFTS2 = 1 (subaddress 13h bit 2). This setting is mainly intended for device production testing. The VPO-bus carries the upper or lower 8 bits of the two ADCs depending on the OFTS[1:0] 13h[1:0] settings; see Table 162. The input configuration is done via MODE[3:0] 02h[3:0] settings; see Table 144. If a Y/C mode is selected, the expansion port carries the multiplexed output signals of both ADCs, and in CVBS mode the output of only one ADC. No timing reference codes are generated in this mode.

Remark: The LSBs (bit 0) of the ADCs are also available on pin RTS0; see Table 160.

The SAV/EAV timing reference codes define the start and end of valid data regions. The ITU-blanking code sequence '- 80 - 10 - 80 - 10 -...' is transmitted during the horizontal blanking period between EAV and SAV.

The position of the F-bit is constant in accordance with ITU 656; see Table 44 and Table 45.

The V-bit can be generated in two different ways (see Table 44 and Table 45) controlled via OFTS1 and OFTS0; see Table 162.

The F and V bits change synchronously with the EAV code.

Table 42. Data format on the expansion port

Blanking period			Timing reference code (hexadecimal)[1]				720 pixels Y-C_B-C_R 4 : 2 : 2 data[2]									Timing reference code (hexadecimal)[1]				Blanking period		
...	80	10	FF	00	00	SAV	C_B0	Y0	C_R0	Y1	C_B2	Y2	...	C_R718	Y719	FF	00	00	EAV	80	10	...

[1] The generation of the timing reference codes can be suppressed by setting OFTS[2:0] to '010'; see Table 162. In this event the code sequence is replaced by the standard '- 80 - 10 -' blanking values.

[2] If raw samples or sliced data are selected by the line control registers (LCR2 to LCR24), the Y samples are replaced by CVBS samples.

Table 43. SAV/EAV format on expansion port XPD7 to XPD0

Bit	Symbol	Description
7		logic 1
6	F	field bit
		1st field: F = 0
		2nd field: F = 1
		for vertical timing see Table 44 and Table 45
5	V	vertical blanking bit
		VBI: V = 1
		active video: V = 0
		for vertical timing see Table 44 and Table 45
4	H	format
		H = 0 in SAV format
		H = 1 in EAV format
3 to 0	P[3:0]	reserved; evaluation not recommended (protection bits according to ITU-R BT 656)

Table 44. 525 lines/60 Hz vertical timing

Line number	F (ITU 656)	V	
		OFTS[2:0] = 000 (ITU 656)	OFTS[2:0] = 001
1 to 3	1	1	according to selected VGATE position type via VSTA and VSTO (subaddresses 15h to 17h); see Table 164 to Table 166
4 to 19	0	1	
20	0	0	
21	0	0	
22 to 261	0	0	
262	0	0	
263	0	0	
264 and 265	0	1	
266 to 282	1	1	
283	1	0	
284	1	0	
285 to 524	1	0	
525	1	0	

Table 45. 625 lines/50 Hz vertical timing

Line number	F (ITU 656)	V	
		OFTS[2:0] = 000 (ITU 656)	OFTS[1:0] = 10
1 to 22	0	1	according to selected VGATE position type via VSTA and VSTO (subaddresses 15h to 17h); see Table 164 to Table 166
23	0	0	
24 to 309	0	0	
310	0	0	
311 and 312	0	1	
313 to 335	1	1	
336	1	0	
337 to 622	1	0	
623	1	0	
624 and 625	1	1	

10.4.2 X port configured as input

If the data input mode is selected at the expansion port, then the scaler can select its input data stream from the on-chip video decoder, or from the expansion port (controlled by bit SCSRC[1:0] 91h[5:4]). Byte serial Y-C_B-C_R 4 : 2 : 2, or subsets for other sampling schemes, or raw samples from an external ADC may be input (see also bits FSC[2:0] 91h[2:0]). The input data stream must be accompanied by an external clock (XCLK), qualifier XDQ and reference signals XRH and XRV. Instead of the reference signal, embedded SAV and EAV codes according to ITU 656 are also accepted. The protection bits are not evaluated.

XRH and XRV carry the horizontal and vertical synchronization signals for the digital video stream through the expansion port. The field ID of the input video stream is carried in the phase (edge) of XRV and state of XRH, or directly as FS (frame sync, odd/even signal) on the XRV pin (controlled by XFDV[92h[7]], XFDH[92h[6]] and XDV[1:0] 92h[5:4]).

The trigger events on XRH (rising/falling edge) and XRV (rising/falling/both edges) for the scalers acquisition window are defined by XDV[1:0] 92h[5:4] and XDH[92h[2]]. The signal polarity of the qualifier can also be defined (bit XDQ[92h[1]]). Alternatively to a qualifier, the input clock can be applied to a gated clock (clock gated with a data qualifier, controlled by bit XCKS[92h[0]]). In this event, all input data will be qualified.

10.5 Image port (I port)

The image port transfers data from the scaler as well as from the VBI data slicer, if selected (maximum 33 MHz). The reference clock is available at the ICLK pin, as an output or as an input (maximum 33 MHz). As output, ICLK is derived from the line-locked decoder or expansion port input clock. The data stream from the scaler output is normally discontinuous. Therefore valid data during a clock cycle is accompanied by a data qualifying (data valid) flag on pin IDQ. For pin constrained applications the IDQ pin can be programmed to function as a gated clock output (bit ICKS2[80h[2]]).

The data formats at the image port are defined in double words of 32 bits (4 bytes), such as the related FIFO structures. However, the physical data stream at the image port is only 16-bit or 8-bit wide; in 16-bit mode data pins HPD7 to HPD0 are used for chrominance data. The four bytes of the double words are serialized in words or bytes.

Available formats are as follows:

- Y-C_B-C_R 4 : 2 : 2
- Y-C_B-C_R 4 : 1 : 1
- Raw samples
- Decoded VBI data

For handshake with the receiving VGA controller, or other memory or bus interface circuitry, F, H and V reference signals and programmable FIFO flags are provided. The information is provided on pins IGP0, IGP1, IGPH and IGPV. The functionality on these pins is controlled via subaddresses 84h and 85h.

VBI data is collected over an entire line in its own FIFO and transferred as an uninterrupted block of bytes. Decoded VBI data can be signed by the VBI flag on pin IGP0 or IGP1.

As scaled video data and decoded VBI data may come from different and asynchronous sources, an arbitration scheme is needed. Normally the VBI data slicer has priority.

The image port consists of the pins and/or signals, as listed in Table 46.

For pin constrained applications, or interfaces, the relevant timing and data reference signals can also be encoded into the data stream. Therefore the corresponding pins do not need to be connected. The minimum image port configuration requires 9 pins only, i.e. 8 pins for data including codes, and 1 pin for clock or gated clock. The inserted codes are defined in close relationship to the ITU-R BT.656 (D1) recommendation, where possible.

The following deviations from *"ITU 656 recommendation"* are implemented at the SAA7108AE; SAA7109AEs image port interface:

- SAV and EAV codes are only present in those lines, where data is to be transferred, i.e. active video lines, or VBI raw samples, no codes for empty lines

- There may be more or less than 720 pixels between SAV and EAV
- Data content and number of clock cycles during horizontal and vertical blanking is undefined, and may not be constant
- Data stream may be interleaved with not-valid data codes, 00h, but SAV and EAV 4-byte codes are not interleaved with not-valid data codes
- There may be an irregular pattern of not-valid data, or IDQ, and as a result, C_B-Y-C_R-Y is not in a fixed phase to a regular clock divider
- VBI raw sample streams are enveloped with SAV and EAV, like normal video
- Decoded VBI data is transported as Ancillary (ANC) data, two modes:
  - Direct decoded VBI data bytes (8-bit) are directly placed in the ANC data field, 00h and FFh codes may appear in the data block (violation to ITU-R BT.656)
  - Recoded VBI data bytes (8-bit) directly placed in ANC data field, 00h and FFh codes will be recoded to even parity codes 03h and FCh to suppress invalid ITU-R BT.656 codes

There are no empty cycles in the ancillary code and its data field. The data codes 00h and FFh are suppressed (changed to 01h or FEh respectively) in the active video stream, as well as in the VBI raw sample stream (VBI pass-through). Optionally, the number range can be further limited.

Table 46. Signals dedicated to the image port

Symbol	Pin	I/O	Description	Bit
IPD7 to IPD0	E14, D14, C14, B14, E13, D13, C13 and B13	O	I port data	ICODE[93h[7]], ISWP[1:0] 85h[7:6] and IPE[1:0] 87h[1:0]
ICLK	H12	I/O	continuous reference clock at image port, can be input or output, as output decoder LLC or XCLK from X port	ICKS[1:0] 80h[1:0] and IPE[1:0] 87h[1:0]
IDQ	H14	O	data valid flag at image port, qualifier, with programmable polarity; secondary function: gated clock	ICKS2[80h[2]], IDQP[85h[0]] and IPE[1:0] 87h[1:0]
IGPH	G12	O	horizontal reference output signal, copy of the horizontal gate signal of the scaler, with programmable polarity; alternative function: HRESET pulse	IDH[1:0] 84h[1:0], IRHP[85h[1]] and IPE[1:0] 87h[1:0]
IGPV	F13	O	vertical reference output signal, copy of the vertical gate signal of the scaler, with programmable polarity; alternative function: VRESET pulse	IDV[1:0] 84h[3:2], IRVP[85h[2]] and IPE[1:0] 87h[1:0]
IGP1	G13	O	general purpose output signal for I port	IDG12[86h[4]], IDG1[1:0] 84h[5:4], IG1P[85h[3]] and IPE[1:0] 87h[1:0]
IGP0	F14	O	general purpose output signal for I port	IDG02[86h[5]], IDG0[1:0] 84h[7:6], IG0P[85h[4]] and IPE[1:0] 87h[1:0]
ITRDY	J14	I	target ready input signals	-
ITRI	G14	I	port control, switches I port into 3-state	IPE[1:0] 87h[1:0]

10.6 Host port for 16-bit extension of video data I/O (H port)

The H port pins HPD can be used for extension of the data I/O paths to 16-bit.

The I port has functional priority. If I8_16[93h[6]] is set to logic 1 the output drivers of the H port are enabled depending on the I port enable control. For I8_16 = 0, the HPD output is disabled.

Table 47. Signals dedicated to the host port

Symbol	Pin	I/O	Description	Bit
HPD7 to HPD0	A13, D12, C12, B12, A12, C11, B11 and A11	I/O	16-bit extension for digital I/O (chrominance component)	IPE[1:0] 87h[1:0], ITRI[8Fh[6]] and I8_16[93h[6]]

10.7 Basic input and output timing diagrams for the I and X ports

10.7.1 I port output timing

Figure 43 to Figure 49 illustrate the output timing via the I port. IGPH and IGPV are logic 1 active gate signals. If reference pulses are programmed, these pulses are generated on the rising edge of the logic 1 active gates. Valid data is accompanied by the output data qualifier on pin IDQ. In addition, invalid cycles are marked with output code 00h.

The IDQ output pin may be defined to be a gated clock output signal (ICLK AND internal IDQ).

10.7.2 X port input timing

At the X port the input timing requirements are the same as those for the I port output. But different to those below:

- It is not necessary to mark invalid cycles with a 00h code
- No constraints on the input qualifier (can be a random pattern)
- XCLK may be a gated clock (XCLK AND external XDQ)

Remark: All timings illustrated in Figure 43 to Figure 49 are given for an uninterrupted output stream (no handshake with the external hardware).

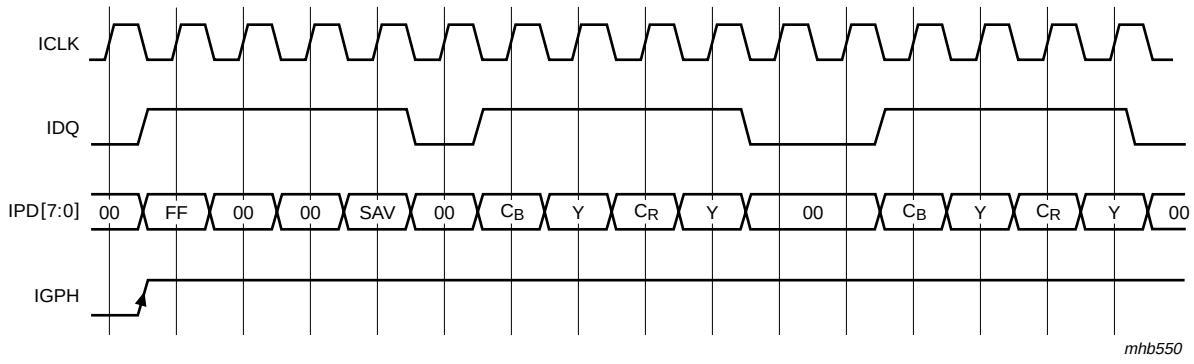


Fig 43. Output timing I port for serial 8-bit data at start of a line (ICODE = 1)

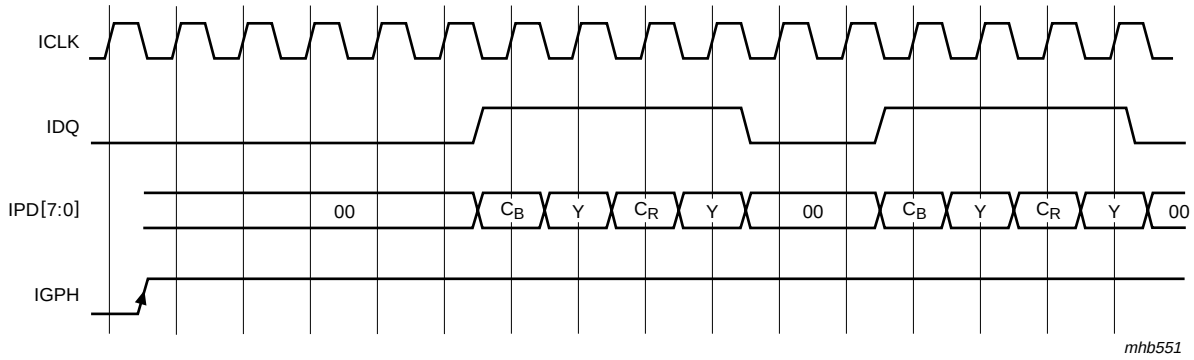


Fig 44. Output timing at the I port for serial 8-bit data at start of a line (ICODE = 0)

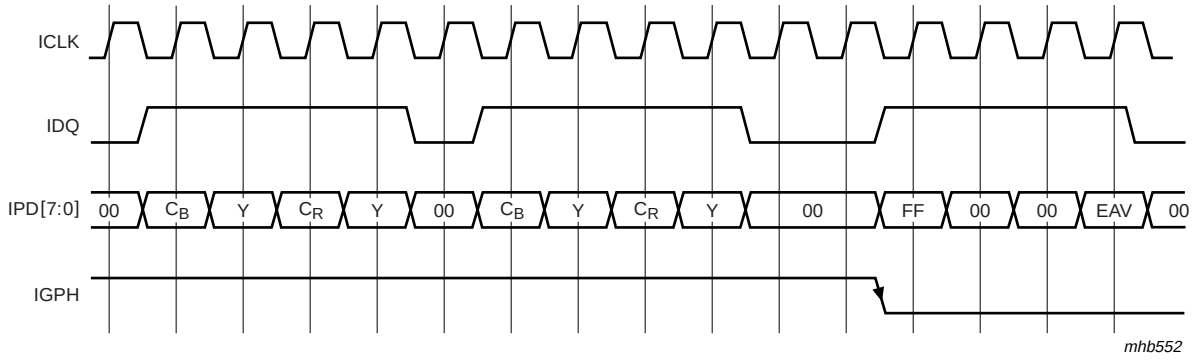


Fig 45. Output timing at the I port for serial 8-bit data at end of a line (ICODE = 1)

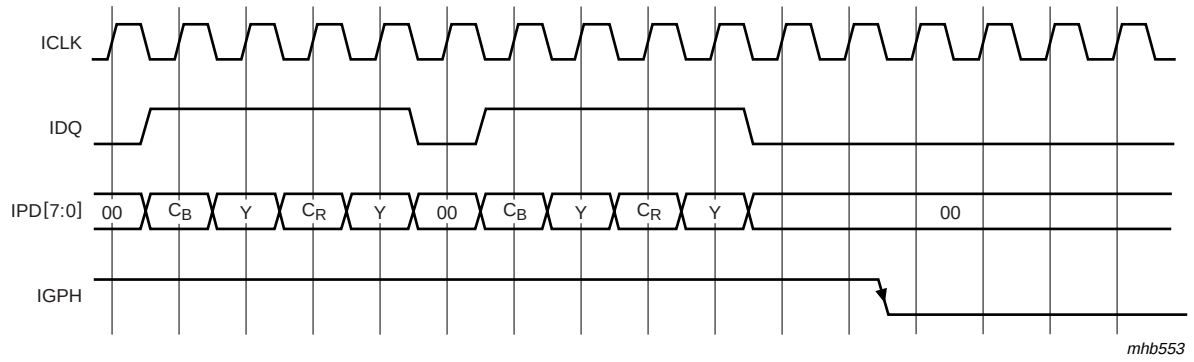


Fig 46. Output timing at the I port for serial 8-bit data at end of a line (ICODE = 0)

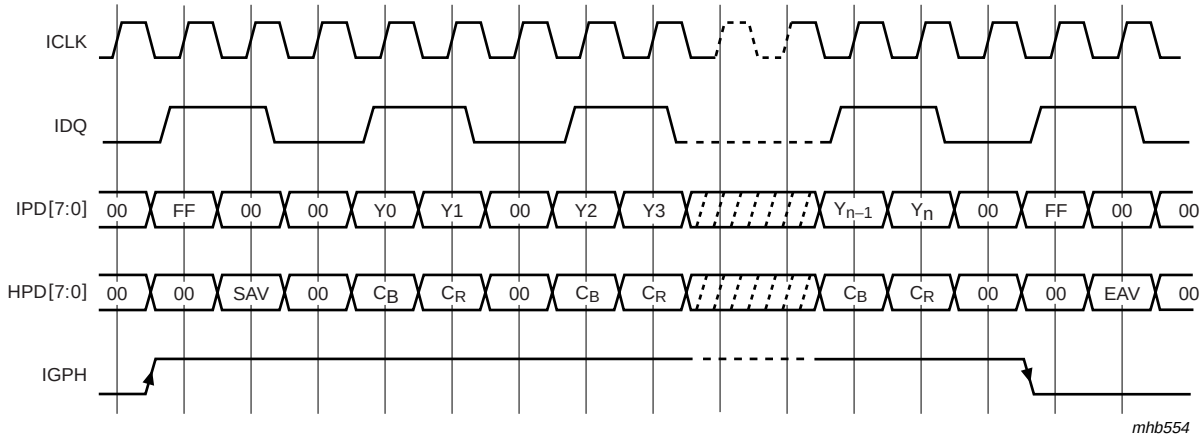


Fig 47. Output timing for 16-bit data output via the I port and the H port with codes (ICODE = 1), timing is like 8-bit output, but packages of 2 bytes per valid cycle

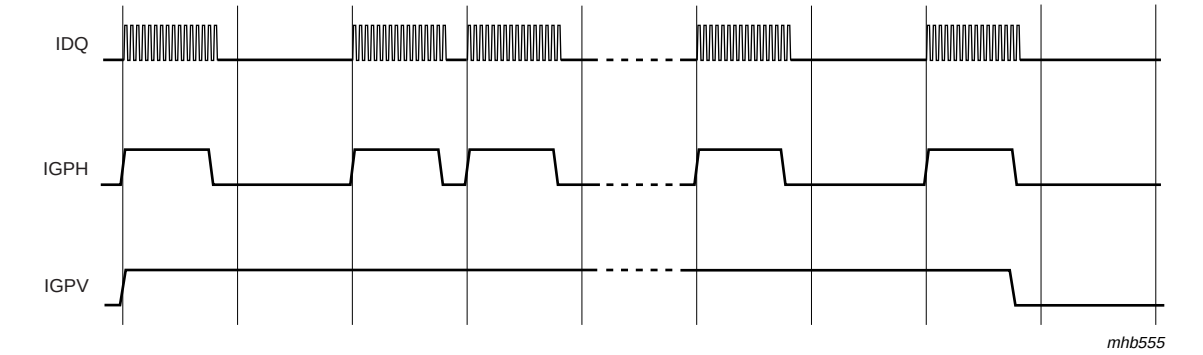


Fig 48. Horizontal and vertical gate output timing

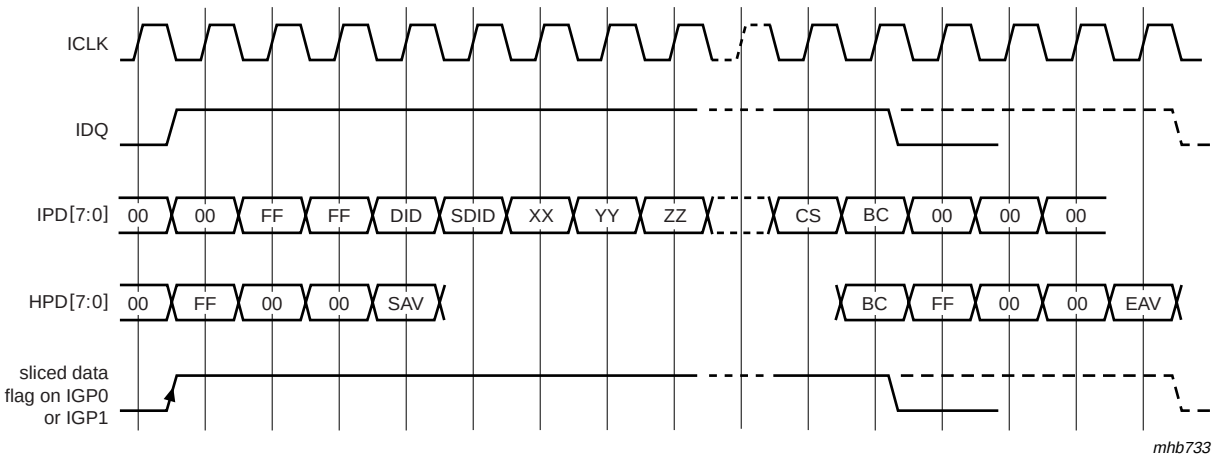


Fig 49. Output timing for sliced VBI data in 8-bit serial output mode (dotted graphs for SAV/EAV mode)

11.1 Digital video encoder part

Table 48. Slave receiver bit allocation map (slave address 88h)

Register function	Subaddress (hexadecimal)	D7	D6	D5	D4	D3	D2	D1	D0
Status byte (read only)	00	VER2	VER1	VER0	CCRDO	CCRDE	-	FSEQ	O_E
Null	01 to 15	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Common DAC adjust fine	16	[1]	[1]	[1]	[1]	DACF3	DACF2	DACF1	DACF0
R DAC adjust coarse	17	[1]	[1]	[1]	RDACC4	RDACC3	RDACC2	RDACC1	RDACC0
G DAC adjust coarse	18	[1]	[1]	[1]	GDACC4	GDACC3	GDACC2	GDACC1	GDACC0
B DAC adjust coarse	19	[1]	[1]	[1]	BDACC4	BDACC3	BDACC2	BDACC1	BDACC0
MSM threshold	1A	MSMT7	MSMT6	MSMT5	MSMT4	MSMT3	MSMT2	MSMT1	MSMT0
Monitor sense mode	1B	MSM	MSA	MSOE	[1]	[1]	RCOMP	GCOMP	BCOMP
Chip ID (read only)	1C	CID7	CID6	CID5	CID4	CID3	CID2	CID1	CID0
Wide screen signal	26	WSS7	WSS6	WSS5	WSS4	WSS3	WSS2	WSS1	WSS0
Wide screen signal	27	WSSON	[1]	WSS13	WSS12	WSS11	WSS10	WSS9	WSS8
Real-time control, burst start	28	[1]	[1]	BS5	BS4	BS3	BS2	BS1	BS0
Sync reset enable, burst end	29	SRES	[1]	BE5	BE4	BE3	BE2	BE1	BE0
Copy generation 0	2A	CG07	CG06	CG05	CG04	CG03	CG02	CG01	CG00
Copy generation 1	2B	CG15	CG14	CG13	CG12	CG11	CG10	CG09	CG08
CG enable, copy generation 2	2C	CGEN	[1]	[1]	[1]	CG19	CG18	CG17	CG16
Output port control	2D	VBSEN	CVBSEN1	CVBSEN0	CEN	ENCOFF	CLK2EN	CVBSEN2	[1]
Null	2E to 36	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Input path control	37	[1]	YUPSC	YFIL1	YFIL0	[1]	CZOOM	IGAIN	XINT
Gain luminance for RGB	38	[1]	[1]	[1]	GY4	GY3	GY2	GY1	GY0
Gain color difference for RGB	39	[1]	[1]	[1]	GCD4	GCD3	GCD2	GCD1	GCD0
Input port control 1	3A	CBENB	[1]	SYNTV	SYMP	DEMOFF	CSYNC	Y2C	UV2C
VPS enable, input control 2	54	VPSEN	[1]	GPVAL	GPEN	[1]	[1]	EDGE	SLOT
VPS byte 5	55	VPS57	VPS56	VPS55	VPS54	VPS53	VPS52	VPS51	VPS50
VPS byte 11	56	VPS117	VPS116	VPS115	VPS114	VPS113	VPS112	VPS111	VPS110
VPS byte 12	57	VPS127	VPS126	VPS125	VPS124	VPS123	VPS122	VPS121	VPS120
VPS byte 13	58	VPS137	VPS136	VPS135	VPS134	VPS133	VPS132	VPS131	VPS130
VPS byte 14	59	VPS147	VPS146	VPS145	VPS144	VPS143	VPS142	VPS141	VPS140
Chrominance phase	5A	CHPS7	CHPS6	CHPS5	CHPS4	CHPS3	CHPS2	CHPS1	CHPS0

Table 48. Slave receiver bit allocation map (slave address 88h) *…continued*

Register function	Subaddress (hexadecimal)	D7	D6	D5	D4	D3	D2	D1	D0
Gain U	5B	GAINU7	GAINU6	GAINU5	GAINU4	GAINU3	GAINU2	GAINU1	GAINU0
Gain V	5C	GAINV7	GAINV6	GAINV5	GAINV4	GAINV3	GAINV2	GAINV1	GAINV0
Gain U MSB, black level	5D	GAINU8	[1]	BLCKL5	BLCKL4	BLCKL3	BLCKL2	BLCKL1	BLCKL0
Gain V MSB, blanking level	5E	GAINV8	[1]	BLNNL5	BLNNL4	BLNNL3	BLNNL2	BLNNL1	BLNNL0
CCR, blanking level VBI	5F	CCRS1	CCRS0	BLNVB5	BLNVB4	BLNVB3	BLNVB2	BLNVB1	BLNVB0
Null	60	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Standard control	61	DOWND	DOWNA	INPI	YGS	[1]	SCBW	PAL	FISE
Burst amplitude	62	RTCE	BSTA6	BSTA5	BSTA4	BSTA3	BSTA2	BSTA1	BSTA0
Subcarrier 0	63	FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00
Subcarrier 1	64	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
Subcarrier 2	65	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16
Subcarrier 3	66	FSC31	FSC30	FSC29	FSC28	FSC27	FSC26	FSC25	FSC24
Line 21 odd 0	67	L21O07	L21O06	L21O05	L21O04	L21O03	L21O02	L21O01	L21O00
Line 21 odd 1	68	L21O17	L21O16	L21O15	L21O14	L21O13	L21O12	L21O11	L21O10
Line 21 even 0	69	L21E07	L21E06	L21E05	L21E04	L21E03	L21E02	L21E01	L21E00
Line 21 even 1	6A	L21E17	L21E16	L21E15	L21E14	L21E13	L21E12	L21E11	L21E10
Null	6B	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Trigger control	6C	HTRIG7	HTRIG6	HTRIG5	HTRIG4	HTRIG3	HTRIG2	HTRIG1	HTRIG0
Trigger control	6D	HTRIG10	HTRIG9	HTRIG8	VTRIG4	VTRIG3	VTRIG2	VTRIG1	VTRIG0
Multi control	6E	NVTRIG	BLCKON	PHRES1	PHRES0	LDEL1	LDEL0	FLC1	FLC0
Closed caption, teletext enable	6F	CCEN1	CCEN0	TTXEN	SCCLN4	SCCLN3	SCCLN2	SCCLN1	SCCLN0
Active display window horizontal start	70	ADWHS7	ADWHS6	ADWHS5	ADWHS4	ADWHS3	ADWHS2	ADWHS1	ADWHS0
Active display window horizontal end	71	ADWHE7	ADWHE6	ADWHE5	ADWHE4	ADWHE3	ADWHE2	ADWHE1	ADWHE0
MSBs ADWH	72	[1]	ADWHE10	ADWHE9	ADWHE8	[1]	ADWHS10	ADWHS9	ADWHS8
TTX request horizontal start	73	TTXHS7	TTXHS6	TTXHS5	TTXHS4	TTXHS3	TTXHS2	TTXHS1	TTXHS0
TTX request horizontal delay	74	[1]	[1]	[1]	[1]	TTXHD3	TTXHD2	TTXHD1	TTXHD0
CSYNC advance	75	CSYNCA4	CSYNCA3	CSYNCA2	CSYNCA1	CSYNCA0	[1]	[1]	[1]
TTX odd request vertical start	76	TTXOVS7	TTXOVS6	TTXOVS5	TTXOVS4	TTXOVS3	TTXOVS2	TTXOVS1	TTXOVS0
TTX odd request vertical end	77	TTXOVE7	TTXOVE6	TTXOVE5	TTXOVE4	TTXOVE3	TTXOVE2	TTXOVE1	TTXOVE0

Table 48. Slave receiver bit allocation map (slave address 88h) *…continued*

Register function	Subaddress (hexadecimal)	D7	D6	D5	D4	D3	D2	D1	D0
TTX even request vertical start	78	TTXEVS7	TTXEVS6	TTXEVS5	TTXEVS4	TTXEVS3	TTXEVS2	TTXEVS1	TTXEVS0
TTX even request vertical end	79	TTXEVE7	TTXEVE6	TTXEVE5	TTXEVE4	TTXEVE3	TTXEVE2	TTXEVE1	TTXEVE0
First active line	7A	FAL7	FAL6	FAL5	FAL4	FAL3	FAL2	FAL1	FAL0
Last active line	7B	LAL7	LAL6	LAL5	LAL4	LAL3	LAL2	LAL1	LAL0
TTX mode, MSB vertical	7C	TTX60	LAL8	TTXO	FAL8	TTXEVE8	TTXOVE8	TTXEVS8	TTXOVS8
Null	7D	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Disable TTX line	7E	LINE12	LINE11	LINE10	LINE9	LINE8	LINE7	LINE6	LINE5
Disable TTX line	7F	LINE20	LINE19	LINE18	LINE17	LINE16	LINE15	LINE14	LINE13
FIFO status (read only)	80	-	-	-	-	IFERR	BFERR	OVFL	UDFL
Pixel clock 0	81	PCL07	PCL06	PCL05	PCL04	PCL03	PCL02	PCL01	PCL00
Pixel clock 1	82	PCL15	PCL14	PCL13	PCL12	PCL11	PCL10	PCL09	PCL08
Pixel clock 2	83	PCL23	PCL22	PCL21	PCL20	PCL19	PCL18	PCL17	PCL16
Pixel clock control	84	DCLK	PCLSY	IFRA	IFBP	PCLE1	PCLE0	PCLI1	PCLI0
FIFO control	85	EIDIV	[1]	[1]	[1]	FILI3	FILI2	FILI1	FILI0
Null	86 to 8F	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Horizontal offset	90	XOFS7	XOFS6	XOFS5	XOFS4	XOFS3	XOFS2	XOFS1	XOFS0
Pixel number	91	XPIX7	XPIX6	XPIX5	XPIX4	XPIX3	XPIX2	XPIX1	XPIX0
Vertical offset odd	92	YOFSO7	YOFSO6	YOFSO5	YOFSO4	YOFSO3	YOFSO2	YOFSO1	YOFSO0
Vertical offset even	93	YOFSE7	YOFSE6	YOFSE5	YOFSE4	YOFSE3	YOFSE2	YOFSE1	YOFSE0
MSBs	94	YOFSE9	YOFSE8	YOFSO9	YOFSO8	XPIX9	XPIX8	XOFS9	XOFS8
Line number	95	YPIX7	YPIX6	YPIX5	YPIX4	YPIX3	YPIX2	YPIX1	YPIX0
Scaler CTRL, MCB YPIX	96	EFS	PCBN	SLAVE	ILC	YFIL	[1]	YPIX9	YPIX8
Sync control	97	HFS	VFS	OFS	PFS	OVS	PVS	OHS	PHS
Line length	98	HLEN7	HLEN6	HLEN5	HLEN4	HLEN3	HLEN2	HLEN1	HLEN0
Input delay, MSB line length	99	IDEL3	IDEL2	IDEL1	IDEL0	HLEN11	HLEN10	HLEN9	HLEN8
Horizontal increment	9A	XINC7	XINC6	XINC5	XINC4	XINC3	XINC2	XINC1	XINC0
Vertical increment	9B	YINC7	YINC6	YINC5	YINC4	YINC3	YINC2	YINC1	YINC0
MSBs vertical and horizontal increment	9C	YINC11	YINC10	YINC9	YINC8	XINC11	XINC10	XINC9	XINC8
Weighting factor odd	9D	YIWGTO7	YIWGTO6	YIWGTO5	YIWGTO4	YIWGTO3	YIWGTO2	YIWGTO1	YIWGTO0

Table 48. Slave receiver bit allocation map (slave address 88h) *…continued*

Register function	Subaddress (hexadecimal)	D7	D6	D5	D4	D3	D2	D1	D0
Weighting factor even	9E	YIWGTE7	YIWGTE6	YIWGTE5	YIWGTE4	YIWGTE3	YIWGTE2	YIWGTE1	YIWGTE0
Weighting factor MSB	9F	YIWGTE11	YIWGTE10	YIWGTE9	YIWGTE8	YIWGTO11	YIWGTO10	YIWGTO9	YIWGTO8
Vertical line skip	A0	YSKIP7	YSKIP6	YSKIP5	YSKIP4	YSKIP3	YSKIP2	YSKIP1	YSKIP0
Blank enable for NI-bypass, vertical line skip MSB	A1	BLEN	[1]	[1]	[1]	YSKIP11	YSKIP10	YSKIP9	YSKIP8
Border color Y	A2	BCY7	BCY6	BCY5	BCY4	BCY3	BCY2	BCY1	BCY0
Border color U	A3	BCU7	BCU6	BCU5	BCU4	BCU3	BCU2	BCU1	BCU0
Border color V	A4	BCV7	BCV6	BCV5	BCV4	BCV3	BCV2	BCV1	BCV0
HD sync line count array	D0	RAM address (see Table 112)							
HD sync line type array	D1	RAM address (see Table 114)							
HD sync line pattern array	D2	RAM address (see Table 116)							
HD sync value array	D3	RAM address (see Table 118)							
HD sync trigger state 1	D4	HLCT7	HLCT6	HLCT5	HLCT4	HLCT3	HLCT2	HLCT1	HLCT0
HD sync trigger state 2	D5	HLCPT3	HLCPT2	HLCPT1	HLCPT0	HLPPT1	HLPPT0	HLCT9	HLCT8
HD sync trigger state 3	D6	HDCT7	HDCT6	HDCT5	HDCT4	HDCT3	HDCT2	HDCT1	HDCT0
HD sync trigger state 4	D7	[1]	HEPT2	HEPT1	HEPT0	[1]	[1]	HDCT9	HDCT8
HD sync trigger phase x	D8	HTX7	HTX6	HTX5	HTX4	HTX3	HTX2	HTX1	HTX0
	D9	[1]	[1]	[1]	[1]	HTX11	HTX10	HTX9	HTX8
HD sync trigger phase y	DA	HTY7	HTY6	HTY5	HTY4	HTY3	HTY2	HTY1	HTY0
	DB	[1]	[1]	[1]	[1]	[1]	[1]	HTY9	HTY8
HD output control	DC	[1]	[1]	[1]	[1]	HDSYE	HDTC	HDGY	HDIP
Cursor color 1 R	F0	CC1R7	CC1R6	CC1R5	CC1R4	CC1R3	CC1R2	CC1R1	CC1R0
Cursor color 1 G	F1	CC1G7	CC1G6	CC1G5	CC1G4	CC1G3	CC1G2	CC1G1	CC1G0
Cursor color 1 B	F2	CC1B7	CC1B6	CC1B5	CC1B4	CC1B3	CC1B2	CC1B1	CC1B0
Cursor color 2 R	F3	CC2R7	CC2R6	CC2R5	CC2R4	CC2R3	CC2R2	CC2R1	CC2R0
Cursor color 2 G	F4	CC2G7	CC2G6	CC2G5	CC2G4	CC2G3	CC2G2	CC2G1	CC2G0
Cursor color 2 B	F5	CC2B7	CC2B6	CC2B5	CC2B4	CC2B3	CC2B2	CC2B1	CC2B0
Auxiliary cursor color R	F6	AUXR7	AUXR6	AUXR5	AUXR4	AUXR3	AUXR2	AUXR1	AUXR0
Auxiliary cursor color G	F7	AUXG7	AUXG6	AUXG5	AUXG4	AUXG3	AUXG2	AUXG1	AUXG0
Auxiliary cursor color B	F8	AUXB7	AUXB6	AUXB5	AUXB4	AUXB3	AUXB2	AUXB1	AUXB0

Table 48. Slave receiver bit allocation map (slave address 88h) *…continued*

Register function	Subaddress (hexadecimal)	D7	D6	D5	D4	D3	D2	D1	D0
Horizontal cursor position	F9	XCP7	XCP6	XCP5	XCP4	XCP3	XCP2	XCP1	XCP0
Horizontal hot spot, MSB XCP	FA	XHS4	XHS3	XHS2	XHS1	XHS0	XCP10	XCP9	XCP8
Vertical cursor position	FB	YCP7	YCP6	YCP5	YCP4	YCP3	YCP2	YCP1	YCP0
Vertical hot spot, MSB YCP	FC	YHS4	YHS3	YHS2	YHS1	YHS0	[1]	YCP9	YCP8
Input path control	FD	LUTOFF	CMODE	LUTL	IF2	IF1	IF0	MATOFF	DFOFF
Cursor bit map	FE	RAM address (see Table 133)							
Color look-up table	FF	RAM address (see Table 134)							

[1] All unused control bits must be programmed with logic 0 to ensure compatibility to future enhancements.

11.1.1 I²C-bus format

S	1000 1000	A	SUBADDRESS	A	DATA 0	A	.....	DATA n	A	P

001aad411

a. to control registers

S	1000 1000	A	D0h	A	RAM ADDRESS	A	DATA 00	A	DATA 01	A	.....	DATA n	A	P

001aad412

b. to the HD line count array (subaddress D0h)

S	1000 1000	A	FEh	A	RAM ADDRESS	A	DATA 0	A	.....	DATA n	A	P

001aad413

c. to cursor bit map (subaddress FEh)

S	1000 1000	A	FFh	A	RAM ADDRESS	A	DATA 0R	A	DATA 0G	A	DATA 0B	A	.....	P

001aad414

d. to color look-up table (subaddress FFh)

See Table 49 for explanations.

Fig 50. I²C-bus write access

S	1000 1000	A	SUBADDRESS	A	Sr	1000 1001	A	DATA 0	Am	.....	DATA n	Am	P

001aad415

a. to control registers

S	1000 1000	A	FEh or FFh	A	RAM ADDRESS	A	Sr	1000 1001	A	DATA 0	Am	.....	DATA n	Am	P

001aad416

b. to cursor bit map or color LUT

See Table 49 for explanations.

Fig 51. I²C-bus read access

Table 49. Explanations of Figure 50 and Figure 51

Code	Description
S	START condition
Sr	repeated START condition
1000 100X[1]	slave address
A	acknowledge generated by the slave
Am	acknowledge generated by the master
SUBADDRESS[2]	subaddress byte
DATA	data byte
--------	continued data bytes and acknowledges
P	STOP condition
RAM ADDRESS	start address for RAM access

[1] X is the read/write control bit; X = logic 0 is order to write; X = logic 1 is order to read.

[2] If more than 1 byte of DATA is transmitted, then auto-increment of the subaddress is performed.

11.1.2 Slave receiver

Table 50. Common DAC adjust fine register, subaddress 16h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 4	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
3 to 0	DACF[3:0]	R/W		DAC fine output voltage adjustment, 1 % steps for all DACs
			0111	7 %
			0110	6 %
			0101	5 %
			0100	4 %
			0011	3 %
			0010	2 %
			0001	1 %
			0000*	0 %
			1000	0 %
			1001	−1 %
			1010	−2 %
			1011	−3 %
			1100	−4 %
			1101	−5 %
			1110	−6 %
			1111	−7 %

Table 51. RGB DAC adjust coarse registers, subaddresses 17h to 19h, bit description

Subaddress	Bit	Symbol	Description
17h to 19h	7 to 5	-	must be programmed with logic 0 to ensure compatibility to future enhancements
17h	4 to 0	RDACC[4:0]	output level coarse adjustment for RED DAC; default after reset is 1Bh for output of C signal 0 0000b ≡ 0.585 V to 1 1111b ≡ 1.240 V at 37.5 Ω nominal for full-scale conversion
18h	4 to 0	GDACC[4:0]	output level coarse adjustment for GREEN DAC; default after reset is 1Bh for output of VBS signal 0 0000b ≡ 0.585 V to 1 1111b ≡ 1.240 V at 37.5 Ω nominal for full-scale conversion
19h	4 to 0	BDACC[4:0]	output level coarse adjustment for BLUE DAC; default after reset is 1Fh for output of CVBS signal 0 0000b ≡ 0.585 V to 1 1111b ≡ 1.240 V at 37.5 Ω nominal for full-scale conversion

Table 52. MSM threshold, subaddress 1Ah, bit description

Bit	Symbol	Description
7 to 0	MSMT[7:0]	monitor sense mode threshold for DAC output voltage, should be set to 70h

Table 53. Monitor sense mode register, subaddress 1Bh, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	MSM	R/W		monitor sense mode
			0*	off; RCOMP, GCOMP and BCOMP bits are not valid
			1	on
6	MSA	R/W		automatic monitor sense mode
			0*	off; RCOMP, GCOMP and BCOMP bits are not valid
			1	on if MSM = 0
5	MSOE	R/W	0	pin TVD is active
			1*	pin TVD is 3-state
4 and 3	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
2	RCOMP	R		check comparator at DAC on pin RED_CR_C_CVBS
			0	active, output is loaded
			1	inactive, output is not loaded
1	GCOMP	R		check comparator at DAC on pin GREEN_VBS_CVBS
			0	active, output is loaded
			1	inactive, output is not loaded
0	BCOMP	R		check comparator at DAC on pin BLUE_CB_CVBS
			0	active, output is loaded
			1	inactive, output is not loaded

Table 54. Wide screen signal registers, subaddresses 26h and 27h, bit description

*Legend: * = default value after reset.*

Subaddress	Bit	Symbol	Access	Value	Description
27h	7	WSSON	R/W	0*	wide screen signalling output is disabled
				1	wide screen signalling output is enabled
	6	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
	5 to 3	WSS[13:11]	R/W	-	wide screen signalling bits, reserved
	2 to 0	WSS[10:8]	R/W	-	wide screen signalling bits, subtitles
26h	7 to 4	WSS[7:4]	R/W	-	wide screen signalling bits, enhanced services
	3 to 0	WSS[3:0]	R/W	-	wide screen signalling bits, aspect ratio

Table 55. Real-time control and burst start register, subaddress 28h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 and 6	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
5 to 0	BS[5:0]	R/W		starting point of burst in clock cycles
			21h*	PAL: BS = 33; strapping pin FSVGC tied to HIGH
			19h*	NTSC: BS = 25; strapping pin FSVGC tied to LOW

Table 56. Sync reset enable and burst end register, subaddress 29h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	SRES	R/W	0*	pin TTX_SRES accepts a teletext bit stream (TTX)
			1	pin TTX_SRES accepts a sync reset input (SRES); a HIGH impulse resets synchronization of the encoder (first field, first line)
6	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
5 to 0	BE[5:0]	R/W		ending point of burst in clock cycles
			1Dh*	PAL: BE = 29; strapping pin FSVGC tied to HIGH
			1Dh*	NTSC: BE = 29; strapping pin FSVGC tied to LOW

Table 57. Copy generation 0, 1, 2 and CG enable registers, subaddresses 2Ah to 2Ch, bit description

*Legend: * = default value after reset.*

Subaddress	Bit	Symbol	Access	Value	Description
2Ch	7	CGEN	R/W		copy generation data output
				0*	disabled
				1	enabled
	6 to 4	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
	3 to 0	CG[19:16]	R/W	-	LSBs of the respective bytes are encoded immediately after run-in, the MSBs of the respective bytes have to carry the CRCC bits, in accordance with the definition of copy generation management system encoding format.
2Bh	7 to 0	CG[15:8]			
2Ah	7 to 0	CG[7:0]			

Table 58. Output port control register, subaddress 2Dh, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	VBSEN	R/W		pin GREEN_VBS_CVBS provides a
			0	component GREEN signal (CVBSEN1 = 0) or CVBS signal (CVBSEN1 = 1)
			1*	luminance (VBS) signal
6	CVBSEN1	R/W		pin GREEN_VBS_CVBS provides a
			0*	component GREEN (G) or luminance (VBS) signal
			1	CVBS signal
5	CVBSEN0	R/W		pin BLUE_CB_CVBS provides a
			0	component BLUE (B) or color difference BLUE (C_B) signal
			1*	CVBS signal
4	CEN	R/W		pin RED_CR_C_CVBS provides a
			0	component RED (R) or color difference RED (C_R) signal
			1*	chrominance signal (C) as modulated subcarrier for S-video
3	ENCOFF	R/W		encoder
			0*	active
			1	bypass, DACs are provided with RGB signal after cursor insertion block
2	CLK2EN	R/W		pin TTXRQ_XCLKO2 provides
			0	teletext request signal (TTXRQ)
			1*	buffered crystal clock divided by two (13.5 MHz)
1	CVBSEN2	R/W		pin RED_CR_C_CVBS provides a
			0*	signal according to CEN
			1	CVBS signal
0	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements

Table 59. Input path control register, subaddress 37h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
6	YUPSC	R/W		vertical scaler
			0*	normal operation
			1	upscaling is enabled
5 and 4	YFIL[1:0]	R/W		vertical interpolation filter control; the filter is not available if YUPSC = 1
			00*	no filter active
			01	filter is inserted before vertical scaling
			10	filter is inserted after vertical scaling; YSKIP should be logic 0
			11	reserved
3	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
2	CZOOM	R/W		cursor generator
			0*	normal operation
			1	cursor will be zoomed by a factor of 2 in both directions
1	IGAIN	R/W		expected input level swing is
			0*	16 to 235 (8-bit RGB)
			1	0 to 255 (8-bit RGB)
0	XINT	R/W		interpolation filter for horizontal upscaling
			0*	not active
			1	active

Table 60. Gain luminance for RGB register, subaddress 38h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 5	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
4 to 0	GY[4:0]	R/W	-	Gain luminance of RGB (C_R, Y and C_B) output, ranging from $(1 - {}^{16}/_{32})$ to $(1 + {}^{15}/_{32})$. Suggested nominal value = 0, depending on external application.

Table 61. Gain color difference for RGB register, subaddress 39h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 5	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
4 to 0	GCD[4:0]	R/W	-	Gain color difference of RGB (C_R, Y and C_B) output, ranging from $(1 - {}^{16}/_{32})$ to $(1 + {}^{15}/_{32})$. Suggested nominal value = 0, depending on external application.

Table 62. Input port control 1 register, subaddress 3Ah, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	CBENB	R/W	0	data from input ports is encoded
			1	color bar with fixed colors is encoded
6	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
5	SYNTV	R/W		in Slave mode
			0*	the encoder is only synchronized at the beginning of an odd field
			1	the encoder receives a vertical sync signal
4	SYMP	R/W		horizontal and vertical trigger
			0*	taken from FSVGC or both VSVGC and HSVGC
			1	decoded out of *'ITU-R BT.656'* compatible data at PD port
3	DEMOFF	R/W		$Y\text{-}C_B\text{-}C_R$ to RGB dematrix
			0*	active
			1	bypassed
2	CSYNC	R/W		pin HSM_CSYNC provides
			0	horizontal sync for non-interlaced VGA components output (at PIXCLK)
			1	composite sync for interlaced components output (at XTAL clock)
1	Y2C	R/W		input luminance data
			0	twos complement from PD input port
			1*	straight binary from PD input port
0	UV2C	R/W		input color difference data
			0	twos complement from PD input port
			1*	straight binary from PD input port

Table 63. VPS enable, input control 2, subaddress 54h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	VPSEN	R/W		video programming system data insertion
			0*	is disabled
			1	in line 16 is enabled
6	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
5	GPVAL	R/W		if GPEN = 1, pin VSM provides
			0	LOW level
			1	HIGH level
4	GPEN	R/W		pin VSM provides
			0*	vertical sync for a monitor
			1	constant signal according to GPVAL
3 and 2	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements

Table 63. VPS enable, input control 2, subaddress 54h, bit description *…continued*

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
1	EDGE	R/W		input data is sampled with
			0	inverse clock edges
			1*	the clock edges specified in Table 12 to Table 18
0	SLOT	R/W	0*	normal assignment of the input data to the clock edge
			1	correct time misalignment due to inverted assignment of input data to the clock edge

Table 64. VPS byte 5, 11, 12, 13 and 14 registers, subaddresses 55h to 59h, bit description[1]

Subaddress	Bit	Symbol	Access	Value	Description
55h	7 to 0	VPS5[7:0]	R/W	-	fifth byte of video programming system data
56h	7 to 0	VPS11[7:0]	R/W	-	eleventh byte of video programming system data
57h	7 to 0	VPS12[7:0]	R/W	-	twelfth byte of video programming system data
58h	7 to 0	VPS13[7:0]	R/W	-	thirteenth byte of video programming system data
59h	7 to 0	VPS14[7:0]	R/W	-	fourteenth byte of video programming system data

[1] In line 16; LSB first; all other bytes are not relevant for VPS.

Table 65. Chrominance phase register, subaddress 5Ah, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 0	CHPS[7:0]	R/W	00h*	phase of encoded color subcarrier (including burst) relative to horizontal sync; can be adjusted in steps of 360/256 degrees
			6Bh	PAL B/G and data from input ports in Master mode
			16h	PAL B/G and data from look-up table
			25h	NTSC M and data from input ports in Master mode
			46h	NTSC M and data from look-up table

Table 66. Gain U and gain U MSB, black level registers, subaddresses 5Bh and 5Dh, bit description

Subaddress	Bit	Symbol	Conditions	Remarks
5Bh	7 to 0	GAINU[8:0][1]	white-to-black = 92.5 IRE	GAINU = –2.17 × nominal to +2.16 × nominal
5Dh	7		GAINU = 0	output subcarrier of U contribution = 0
			GAINU = 118 (76h)	output subcarrier of U contribution = nominal
			white-to-black = 100 IRE	GAINU = –2.05 × nominal to +2.04 × nominal
			GAINU = 0	output subcarrier of U contribution = 0
			GAINU = 125 (7Dh)	output subcarrier of U contribution = nominal
	6	-	must be programmed with logic 0 to ensure compatibility to future enhancements	
	5 to 0	BLCKL[5:0][2]	white-to-sync = 140 IRE[3]	recommended value: BLCKL = 58 (3Ah)
			BLCKL = 0[3]	output black level = 29 IRE
			BLCKL = 63 (3Fh)[3]	output black level = 49 IRE
			white-to-sync = 143 IRE[4]	recommended value: BLCKL = 51 (33h)
			BLCKL = 0[4]	output black level = 27 IRE
			BLCKL = 63 (3Fh)[4]	output black level = 47 IRE

[1] Variable gain for C_B signal; input representation in accordance with *'ITU-R BT.601'*.

[2] Variable black level; input representation in accordance with *'ITU-R BT.601'*.

[3] Output black level/IRE = BLCKL × 2/6.29 + 28.9.

[4] Output black level/IRE = BLCKL × 2/6.18 + 26.5.

Table 67. Gain V and gain V MSB, blanking level registers, subaddresses 5Ch and 5Eh, bit description

Subaddress	Bit	Symbol	Conditions	Remarks
5Ch	7 to 0	GAINV[8:0][1]	white-to-black = 92.5 IRE	GAINV = –1.55 × nominal to +1.55 × nominal
5Eh	7		GAINV = 0	output subcarrier of V contribution = 0
			GAINV = 165 (A5h)	output subcarrier of V contribution = nominal
			white-to-black = 100 IRE	GAINV = –1.46 × nominal to +1.46 × nominal
			GAINV = 0	output subcarrier of V contribution = 0
			GAINV = 175 (AFh)	output subcarrier of V contribution = nominal
	6	-	must be programmed with logic 0 to ensure compatibility to future enhancements	
	5 to 0	BLNNL[5:0][2]	white-to-sync = 140 IRE[3]	recommended value: BLNNL = 46 (2Eh)
			BLNNL = 0[3]	output blanking level = 25 IRE
			BLNNL = 63 (3Fh)[3]	output blanking level = 45 IRE
			white-to-sync = 143 IRE[4]	recommended value: BLNNL = 53 (35h)
			BLNNL = 0[4]	output blanking level = 26 IRE
			BLNNL = 63 (3Fh)[4]	output blanking level = 46 IRE

[1] Variable gain for C_R signal; input representation in accordance with *'ITU-R BT.601'*.

[2] Variable blanking level.

[3] Output black level/IRE = BLNNL × 2/6.29 + 25.4.

[4] Output black level/IRE = BLNNL × 2/6.18 + 25.9; default after reset: 35h.

Table 68. CCR and blanking level VBI register, subaddress 5Fh, bit description

Bit	Symbol	Access	Value	Description
7 and 6	CCRS[1:0]	R/W		select cross-color reduction filter in luminance; for overall transfer characteristic of luminance see Figure 9
			00	no cross-color reduction
			01	cross-color reduction #1 active
			10	cross-color reduction #2 active
			11	cross-color reduction #3 active
5 to 0	BLNVB[5:0]	R/W	-	variable blanking level during vertical blanking interval is typically identical to value of BLNNL

Table 69. Standard control register, subaddress 61h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	DOWND	R/W		digital core
			0*	in normal operational mode
			1	in Sleep mode and is reactivated with an I^2C-bus address
6	DOWNA	R/W		DACs
			0*	in normal operational mode
			1	in Power-down mode
5	INPI	R/W		PAL switch
			0*	phase is nominal
			1	is inverted compared to nominal if RTCE = 1
4	YGS	R/W		luminance gain for white – black
			0	100 IRE
			1	92.5 IRE including 7.5 IRE set-up of black
3	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
2	SCBW	R/W		bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figure 7 and Figure 8)
			0	enlarged
			1*	standard
1	PAL	R/W		encoding
			0	NTSC (non-alternating V component)
			1	PAL (alternating V component)
0	FISE	R/W		total pixel clocks per line
			0	864
			1	858

Table 70. Burst amplitude register, subaddress 62h, bit description

*Legend: * = default value after reset, ^ = recommended value.*

Bit	Symbol	Access	Value	Description
7	RTCE	R/W		real-time control
			0*	no real-time control of generated subcarrier frequency
			1	real-time control of generated subcarrier frequency through a NXP video decoder; for a specification of the RTC protocol see document *"How to use Real Time Control (RTC)"*, available on request
6 to 0	BSTA[6:0]	R/W		amplitude of color burst; input representation in accordance with *'ITU-R BT.601'*
			3Fh (63)^	white-to-black = 92.5 IRE; burst = 40 IRE; NTSC encoding; BSTA = 0 to 2.02 × nominal
			2Dh (45)^	white-to-black = 92.5 IRE; burst = 40 IRE; PAL encoding; BSTA = 0 to 2.82 × nominal
			43h (67)^	white-to-black = 100 IRE; burst = 43 IRE; NTSC encoding; BSTA = 0 to 1.90 × nominal
			2Fh (47)*^	white-to-black = 100 IRE; burst = 43 IRE; PAL encoding; BSTA = 0 to 3.02 × nominal

Table 71. Subcarrier 0, 1, 2 and 3 registers, subaddresses 63h to 66h, bit description

Subaddress	Bit	Symbol	Access	Value	Description
66h	7 to 0	FSC[31:24]	R/W	-	f_{fsc} = subcarrier frequency (in multiples of line frequency); f_{llc} = clock frequency (in multiples of line frequency); FSC[31:24] = most significant byte; FSC[07:00] = least significant byte[1]
65h	7 to 0	FSC[23:16]	R/W	-	
64h	7 to 0	FSC[15:08]	R/W	-	
63h	7 to 0	FSC[07:00]	R/W	-	

[1] $$FSC = round\left(\frac{f_{fsc}}{f_{llc}} \times 2^{32}\right)$$

Examples:

a) NTSC M: f_{fsc} = 227.5, f_{llc} = 1716 → FSC = 569408543 (21F0 7C1Fh).

b) PAL B/G: f_{fsc} = 283.7516, f_{llc} = 1728 → FSC = 705268427 (2A09 8ACBh).

Table 72. Line 21 odd 0, 1 and even 0, 1 registers, subaddresses 67h to 6Ah, bit description[1]

Subaddress	Bit	Symbol	Access	Value	Description
67h	7 to 0	L21O[07:00]	R/W	-	first byte of captioning data, odd field
68h	7 to 0	L21O[17:10]	R/W	-	second byte of captioning data, odd field
69h	7 to 0	L21E[07:00]	R/W	-	first byte of extended data, even field
6Ah	7 to 0	L21E[17:10]	R/W	-	second byte of extended data, even field

[1] LSBs of the respective bytes are encoded immediately after run-in and framing code, the MSBs of the respective bytes have to carry the parity bit, in accordance with the definition of line 21 encoding format.

Table 73. Trigger control registers, subaddresses 6Ch and 6Dh, bit description

*Legend: * = default value after reset.*

Subaddress	Bit	Symbol	Access	Value	Description
6Ch	7 to 0	HTRIG[7:0]	R/W	00h*	sets the horizontal trigger phase related to chip-internal horizontal input[1]
6Dh	7 to 5	HTRIG[10:8]	R/W	0h*	
	4 to 0	VTRIG[4:0]	R/W	00h*	sets the vertical trigger phase related to chip-internal vertical input[2]

[1] Values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed; increasing HTRIG decreases delays of all internally generated timing signals.

[2] Increasing VTRIG decreases delays of all internally generated timing signals, measured in half lines; variation range of VTRIG = 0 to 31 (1Fh).

Table 74. Multi control register, subaddress 6Eh, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	NVTRIG	R/W		values of the VTRIG register are
			0	positive
			1	negative
6	BLCKON	R/W	0*	encoder in normal operation mode
			1	output signal is forced to blanking level
5 and 4	PHRES[1:0]	R/W		selects the phase reset mode of the color subcarrier generator
			00	no subcarrier reset
			01	subcarrier reset every two lines
			10	subcarrier reset every eight fields
			11	subcarrier reset every four fields
3 and 2	LDEL[1:0]	R/W		selects the delay on luminance path with reference to chrominance path
			00*	no luminance delay
			01	1 LLC luminance delay
			10	2 LLC luminance delay
			11	3 LLC luminance delay
1 and 0	FLC[1:0]	R/W		field length control
			00*	interlaced 312.5 lines/field at 50 Hz, 262.5 lines/field at 60 Hz
			01	non-interlaced 312 lines/field at 50 Hz, 262 lines/field at 60 Hz
			10	non-interlaced 313 lines/field at 50 Hz, 263 lines/field at 60 Hz
			11	non-interlaced 313 lines/field at 50 Hz, 263 lines/field at 60 Hz

Table 75. Closed caption, teletext enable register, subaddress 6Fh, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 and 6	CCEN[1:0]	R/W		enables individual line 21 encoding
			00*	line 21 encoding off
			01	enables encoding in field 1 (odd)
			10	enables encoding in field 2 (even)
			11	enables encoding in both fields
5	TTXEN	R/W		teletext insertion
			0*	disabled
			1	enabled
4 to 0	SCCLN[4:0]	R/W	-	selects the actual line, where closed caption or extended data are encoded; line = (SCCLN + 4) for M-systems; line = (SCCLN + 1) for other systems

Table 76. Active Display Window Horizontal (ADWH) start and end registers, subaddresses 70h to 72h, bit description

Subaddress	Bit	Symbol	Access	Value	Description
70h	7 to 0	ADWHS[7:0]	R/W	-	active display window horizontal start; defines the start of the active TV display portion after the border color[1]
71h	7 to 0	ADWHE[7:0]	R/W	-	active display window horizontal end; defines the end of the active TV display portion before the border color[1]
72h	7	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
	6 to 4	ADWHE[10:8]	R/W	-	active display window horizontal end; defines the end of the active TV display portion before the border color[1]
	3	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
	2 to 0	ADWHS[10:8]	R/W	-	active display window horizontal start; defines the start of the active TV display portion after the border color[1]

[1] Values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed.

Table 77. TTX request horizontal start register, subaddress 73h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 0	TTXHS[7:0]	R/W		start of signal TTXRQ on pin TTXRQ_XCLKO2 (CLK2EN = 0); see Figure 66
			42h*	if strapped to PAL
			54h*	if strapped to NTSC

Table 78. TTX request horizontal delay register, subaddress 74h, bit description

*Legend: * = default value after reset and minimum value.*

Bit	Symbol	Access	Value	Description
7 to 4	-	R/W	0h	must be programmed with logic 0 to ensure compatibility to future enhancements
3 to 0	TTXHD[3:0]	R/W	2h*	indicates the delay in clock cycles between rising edge of TTXRQ output signal on pin TTXRQ_XCLKO2 (CLK2EN = 0) and valid data at pin TTX_SRES

Table 79. CSYNC advance register, subaddress 75h, bit description

Bit	Symbol	Access	Value	Description
7 to 3	CSYNCA[4:0]	R/W	-	advanced composite sync against RGB output from 0 XTAL clocks to 31 XTAL clocks
2 to 0	-	R/W	000	must be programmed with logic 0 to ensure compatibility to future enhancements

Table 80. TTX odd request vertical start register, subaddress 76h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 0	TTXOVS[7:0]	R/W		with TTXOVS8 (see Table 86) first line of occurrence of signal TTXRQ on pin TTXRQ_XCLKO2 (CLK2EN = 0) in odd field, line = (TTXOVS + 4) for M-systems and line = (TTXOVS + 1) for other systems
			05h*	if strapped to PAL
			06h*	if strapped to NTSC

Table 81. TTX odd request vertical end register, subaddress 77h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 0	TTXOVE[7:0]	R/W		with TTXOVE8 (see Table 86) last line of occurrence of signal TTXRQ on pin TTXRQ_XCLKO2 (CLK2EN = 0) in odd field, line = (TTXOVE + 3) for M-systems and line = TTXOVE for other systems
			16h*	if strapped to PAL
			10h*	if strapped to NTSC

Table 82. TTX even request vertical start register, subaddress 78h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 0	TTXEVS[7:0]	R/W		with TTXEVS8 (see Table 86) first line of occurrence of signal TTXRQ on pin TTXRQ_XCLKO2 (CLK2EN = 0) in even field, line = (TTXEVS + 4) for M-systems and line = (TTXEVS + 1) for other systems
			04h*	if strapped to PAL
			05h*	if strapped to NTSC

Table 83. TTX even request vertical end register, subaddress 79h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 0	TTXEVE[7:0]	R/W		with TTXEVE8 (see Table 86) last line of occurrence of signal TTXRQ on pin TTXRQ_XCLKO2 (CLK2EN = 0) in even field, line = (TTXEVE + 3) for M-systems and line = TTXEVE for other systems
			16h*	if strapped to PAL
			10h*	if strapped to NTSC

Table 84. First active line register, subaddress 7Ah, bit description

Bit	Symbol	Access	Value	Description
7 to 0	FAL[7:0]	R/W		with FAL8 (see Table 86) first active line = (FAL + 4) for M-systems and (FAL + 1) for other systems, measured in lines
			00h	coincides with the first field synchronization pulse

Table 85. Last active line register, subaddress 7Bh, bit description

Bit	Symbol	Access	Value	Description
7 to 0	LAL[7:0]	R/W		with LAL8 (see Table 86) last active line = (LAL + 3) for M-systems and LAL for other system, measured in lines
			00h	coincides with the first field synchronization pulse

Table 86. TTX mode, MSB vertical register, subaddress 7Ch, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	TTX60	R/W	0*	enables NABTS (FISE = 1) or European TTX (FISE = 0)
			1	enables world standard teletext 60 Hz (FISE = 1)
6	LAL8	R/W		see Table 85
5	TTXO	R/W		teletext protocol selected (see Figure 66)
			0*	new teletext protocol selected; at each rising edge of TTXRQ a single teletext bit is requested
			1	old teletext protocol selected; the encoder provides a window of TTXRQ going HIGH; the length of the window depends on the chosen teletext standard
4	FAL8	R/W		see Table 84
3	TTXEVE8	R/W		see Table 83
2	TTXOVE8	R/W		see Table 81
1	TTXEVS8	R/W		see Table 82
0	TTXOVS8	R/W		see Table 80

Table 87. Disable TTX line registers, subaddresses 7Eh and 7Fh, bit description[1]

Subaddress	Bit	Symbol	Access	Value	Description
7Eh	7 to 0	LINE[12:5]	R/W	-	individual lines in both fields (PAL counting) can be disabled for insertion of teletext by the respective bits, disabled line = LINExx (50 Hz field rate)
7Fh	7 to 0	LINE[20:13]	R/W	-	

[1] This bit mask is effective only if the lines are enabled by TTXOVS/TTXOVE and TTXEVS/TTXEVE.

Table 88. Pixel clock 0, 1 and 2 registers, subaddresses 81h to 83h, bit description

Subaddress	Bit	Symbol	Access	Value	Description
81h	7 to 0	PCL[07:00]	R/W		defines the frequency of the synthesized pixel clock PIXCLKO; $f_{PIXCLK} = \left(\frac{PCL}{2^{24}} \times f_{XTAL}\right) \times 8$; f_{XTAL} = 27 MHz nominal
82h	7 to 0	PCL[15:08]			
83h	7 to 0	PCL[23:16]			
				20 F63Bh	640 × 480 to NTSC M
				1B 5A73h	640 × 480 to PAL B/G (as by strapping pins)

Table 89. Pixel clock control register, subaddress 84h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	DCLK	R/W	0*	set to logic 1
			1	set to logic 1
6	PCLSY	R/W		pixel clock generator
			0*	runs free
			1	gets synchronized with the vertical sync
5	IFRA	R/W		input FIFO gets reset
			0	explicitly at falling edge
			1*	every field
4	IFBP	R/W		input FIFO
			0	active
			1*	bypassed
3 and 2	PCLE[1:0]	R/W		controls the divider for the external pixel clock
			00	divider ratio for PIXCLK output is 1
			01*	divider ratio for PIXCLK output is 2
			10	divider ratio for PIXCLK output is 4
			11	divider ratio for PIXCLK output is 8
1 and 0	PCLI[1:0]	R/W		controls the divider for the internal pixel clock
			00	divider ratio for internal PIXCLK is 1
			01*	divider ratio for internal PIXCLK is 2
			10	divider ratio for internal PIXCLK is 4
			11	not allowed

Table 90. FIFO control register, subaddress 85h, bit description

*Legend: * = default value after reset, ^ = nominal value.*

Bit	Symbol	Access	Value	Description
7	EIDIV	R/W	0*	DVO compliant signals are applied
			1	non-DVO compliant signals are applied
6 to 4	-	R/W	000	must be programmed with logic 0 to ensure compatibility to future enhancements
3 to 0	FILI[3:0]	R/W	8h*^	threshold for FIFO internal transfers

Table 91. Horizontal offset register, subaddress 90h, bit description

Bit	Symbol	Description
7 to 0	XOFS[7:0]	with XOFS[9:8] (see Table 95) horizontal offset; defines the number of PIXCLKs from horizontal sync (HSVGC) output to composite blanking ($\overline{CBO}$) output

Table 92. Pixel number register, subaddress 91h, bit description

Bit	Symbol	Description
7 to 0	XPIX[7:0]	with XPIX[9:8] (see Table 95) pixel in X direction; defines half the number of active pixels per input line (identical to the length of $\overline{CBO}$ pulses)

Table 93. Vertical offset odd register, subaddress 92h, bit description

Bit	Symbol	Description
7 to 0	YOFSO[7:0]	with YOFSO[9:8] (see Table 95) vertical offset in odd field; defines (in the odd field) the number of lines from VSVGC to first line with active $\overline{CBO}$; if no LUT data is requested, the first active $\overline{CBO}$ will be output at YOFSO + 2; usually, YOFSO = YOFSE with the exception of extreme vertical downscaling and interlacing

Table 94. Vertical offset even register, subaddress 93h, bit description

Bit	Symbol	Description
7 to 0	YOFSE[7:0]	with YOFSE[9:8] (see Table 95) vertical offset in even field; defines (in the even field) the number of lines from VSVGC to first line with active $\overline{CBO}$; if no LUT data is requested, the first active $\overline{CBO}$ will be output at YOFSE + 2; usually, YOFSE = YOFSO with the exception of extreme vertical downscaling and interlacing

Table 95. MSBs register, subaddress 94h, bit description

Bit	Symbol	Description
7 and 6	YOFSE[9:8]	see Table 94
5 and 4	YOFSO[9:8]	see Table 93
3 and 2	XPIX[9:8]	see Table 92
1 and 0	XOFS[9:8]	see Table 91

Table 96. Line number register, subaddress 95h, bit description

Bit	Symbol	Description
7 to 0	YPIX[7:0]	with YPIX[9:8] (see Table 97) defines the number of requested input lines from the feeding device; number of requested lines = YPIX + YOFSE – YOFSO

Table 97. Scaler CTRL, MCB and YPIX register, subaddress 96h, bit description

Bit	Symbol	Access	Value	Description
7	EFS	R/W		in Slave mode frame sync signal at pin FSVGC
			0	ignored
			1	accepted
6	PCBN	R/W		polarity of $\overline{\text{CBO}}$ signal
			0	normal (HIGH during active video)
			1	inverted (LOW during active video)
5	SLAVE	R/W		from the SAA7104E; SAA7105E the timing to the graphics controller is
			0	master
			1	slave
4	ILC	R/W		if hardware cursor insertion is active
			0	set LOW for non-interlaced input signals
			1	set HIGH for interlaced input signals
3	YFIL	R/W		luminance sharpness booster
			0	disabled
			1	enabled
2	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
1 and 0	YPIX[9:8]			see Table 96

Table 98. Sync control register, subaddress 97h, bit description

Bit	Symbol	Access	Value	Description
7	HFS	R/W		horizontal sync is derived from
			0	input signal (Save mode) at pin HSVGC
			1	a frame sync signal (Slave mode) at pin FSVGC (only if EFS is set HIGH)
6	VFS	R/W		vertical sync (field sync) is derived from
			0	input signal (Slave mode) at pin VSVGC
			1	a frame sync signal (Slave mode) at pin FSVGC (only if EFS is set HIGH)
5	OFS	R/W		pin FSVGC is
			0	input
			1	active output
4	PFS	R/W		polarity of signal at pin FSVGC in output mode (Master mode) is
			0	active HIGH; rising edge of the input signal is used in Slave mode
			1	active LOW; falling edge of the input signal is used in Slave mode
3	OVS	R/W		pin VSVGC is
			0	input
			1	active output

Table 98. Sync control register, subaddress 97h, bit description *...continued*

Bit	Symbol	Access	Value	Description
2	PVS	R/W		polarity of signal at pin VSVGC in output mode (Master mode) is
			0	active HIGH; rising edge of the input signal is used in Slave mode
			1	active LOW; falling edge of the input signal is used in Slave mode
1	OHS	R/W		pin HSVGC is
			0	input
			1	active output
0	PHS	R/W		polarity of signal at pin HSVGC in output mode (Master mode) is
			0	active HIGH; rising edge of the input signal is used in Slave mode
			1	active LOW; falling edge of the input signal is used in Slave mode

Table 99. Line length register, subaddress 98h, bit description

Bit	Symbol	Description
7 to 0	HLEN[7:0]	with HLEN[11:8] (see Table 100) horizontal length; $HLEN = \frac{number\ of\ PIXCLKs}{line} - 1$

Table 100. Input delay, MSB line length register, subaddress 99h, bit description

Bit	Symbol	Description
7 to 4	IDEL[3:0]	input delay; defines the distance in PIXCLKs between the active edge of $\overline{CBO}$ and the first received valid pixel
3 to 0	HLEN[11:8]	see Table 99

Table 101. Horizontal increment register, subaddress 9Ah, bit description

Bit	Symbol	Description
7 to 0	XINC[7:0]	with XINC[11:8] (see Table 103) incremental fraction of the horizontal scaling engine; $XINC = \frac{\frac{number\ of\ output\ pixels}{line}}{\frac{number\ of\ input\ pixels}{line}} \times 4096$

Table 102. Vertical increment register, subaddress 9Bh, bit description

Bit	Symbol	Description
7 to 0	YINC[7:0]	with YINC[11:8] (see Table 103) incremental fraction of the vertical scaling engine; $YINC = \frac{number\ of\ active\ output\ lines}{number\ of\ active\ input\ lines} \times 4096$

Table 103. MSBs vertical and horizontal increment register, subaddress 9Ch, bit description

Bit	Symbol	Description
7 to 4	YINC[11:8]	see Table 102
3 to 0	XINC[11:8]	see Table 101

Table 104. Weighting factor odd register, subaddress 9Dh, bit description

Bit	Symbol	Description
7 to 0	YIWGTO[7:0]	with YIWGTO[11:8] (see Table 106) weighting factor for the first line of the odd field; $YIWGTO = \frac{YINC}{2} + 2048$

Table 105. Weighting factor even, subaddress 9Eh, bit description

Bit	Symbol	Description
7 to 0	YIWGTE[7:0]	with YIWGTE[11:8] (see Table 106) weighting factor for the first line of the even field; $YIWGTE = \frac{YINC - YSKIP}{2}$

Table 106. Weighting factor MSB register, subaddress 9Fh, bit description

Bit	Symbol	Description
7 to 4	YIWGTE[11:8]	see Table 105
3 to 0	YIWGTO[11:8]	see Table 104

Table 107. Vertical line skip register, subaddress A0h, bit description

Bit	Symbol	Access	Value	Description
7 to 0	YSKIP[7:0]	R/W		with YSKIP[11:8] (see Table 108) vertical line skip; defines the effectiveness of the anti-flicker filter
			000h	most effective
			FFFh	anti-flicker filter switched off

Table 108. Blank enable for NI-bypass, vertical line skip MSB register, subaddress A1h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	BLEN	R/W		for non-interlaced graphics in bypass mode
			0*	no internal blanking
			1	forced internal blanking
6 to 4	-	R/W	000	must be programmed with logic 0 to ensure compatibility to future enhancements
3 to 0	YSKIP[11:8]	R/W		see Table 107

Table 109. Border color Y register, subaddress A2h, bit description

Bit	Symbol	Description
7 to 0	BCY[7:0]	luminance portion of border color in underscan area

Table 110. Border color U register, subaddress A3h, bit description

Bit	Symbol	Description
7 to 0	BCU[7:0]	color difference portion of border color in underscan area

Table 111. Border color V register, subaddress A4h, bit description

Bit	Symbol	Description
7 to 0	BCV[7:0]	color difference portion of border color in underscan area

Table 112. Subaddress D0h

Data byte	Description
HLCA	RAM start address for the HD sync line count array; the byte following subaddress D0 points to the first cell to be loaded with the next transmitted byte; succeeding cells are loaded by auto-incrementing until stop condition. Each line count array entry consists of 2 bytes; see Table 113. The array has 15 entries.
HLC	HD line counter. The system will repeat the pattern described in 'HLT' HLC times and then start with the next entry in line count array.
HLT	HD line type pointer. If not 0, the value points into the line type array, index HLT – 1 with the description of the current line. 0 means the entry is not used.

Table 113. Layout of the data bytes in the line count array

Byte	Description							
0	HLC7	HLC6	HLC5	HLC4	HLC3	HLC2	HLC1	HLC0
1	HLT3	HLT2	HLT1	HLT0	0	0	HLC9	HLC8

Table 114. Subaddress D1h

Data byte	Description
HLTA	RAM start address for the HD sync line type array; the byte following subaddress D1 points to the first cell to be loaded with the next transmitted byte; succeeding cells are loaded by auto-incrementing until stop condition. Each line type array entry consists of 4 bytes; see Table 115. The array has 15 entries.
HLP	HD line type; if not 0, the value points into the line pattern array. The index used is HLP – 1. It consists of value-duration pairs. Each entry consists of 8 pointers, used from index 0 to 7. The value 0 means that the entry is not used.

Table 115. Layout of the data bytes in the line type array

Byte	Description							
0	0	HLP12	HLP11	HLP10	0	HLP02	HLP01	HLP00
1	0	HLP32	HLP31	HLP30	0	HLP22	HLP21	HLP20
2	0	HLP52	HLP51	HLP50	0	HLP42	HLP41	HLP40
3	0	HLP72	HLP71	HLP70	0	HLP62	HLP61	HLP60

Table 116. Subaddress D2h

Data byte	Description
HLPA	RAM start address for the HD sync line pattern array; the byte following subaddress D2 points to the first cell to be loaded with the next transmitted byte; succeeding cells are loaded by auto-incrementing until stop condition. Each line pattern array entry consists of 4 value-duration pairs occupying 2 bytes; see Table 117. The array has 7 entries.
HPD	HD pattern duration. The value defines the time in pixel clocks (HPD + 1) the corresponding value HPV is added to the HD output signal. If 0, this entry will be skipped.
HPV	HD pattern value pointer. This gives the index in the HD value array containing the level to be inserted into the HD output path. If the MSB of HPV is logic 1, the value will only be inserted into the Y/GREEN channel of the HD data path, the other channels remain unchanged.

Table 117. Layout of the data bytes in the line pattern array

Byte	Description							
0	HPD07	HPD06	HPD05	HPD04	HPD03	HPD02	HPD01	HPD00
1	HPV03	HPV02	HPV01	HPV00	0	0	HPD09	HPD08
2	HPD17	HPD16	HPD14	HPD14	HPD13	HPD12	HPD11	HPD10
3	HPV13	HPV12	HPV11	HPV10	0	0	HPD19	HPD18
4	HPD27	HPD26	HPD25	HPD24	HPD23	HPD22	HPD21	HPD20
5	HPV23	HPV22	HPV21	HPV20	0	0	HPD29	HPD28
6	HPD37	HPD36	HPD35	HPD34	HPD33	HPD32	HPD31	HPD30
7	HPV33	HPV32	HPV31	HPV30	0	0	HPD39	HPD38

Table 118. Subaddress D3h

Data byte	Description
HPVA	RAM start address for the HD sync value array; the byte following subaddress D3 points to the first cell to be loaded with the next transmitted byte; succeeding cells are loaded by auto-incrementing until stop condition. Each line pattern array entry consists of 2 bytes. The array has 8 entries.
HPVE	HD pattern value entry. The HD path will insert a level of (HPV + 52) $\times$ 0.66 IRE into the data path. The value is signed 8-bits wide; see Table 119.
HHS	HD horizontal sync. If the HD engine is active, this value will be provided at pin HSM_CSYNC; see Table 119.
HVS	HD vertical sync. If the HD engine is active, this value will be provided at pin VSM; see Table 119.

Table 119. Layout of the data bytes in the value array

Byte	Description							
0	HPVE7	HPVE6	HPVE5	HPVE4	HPVE3	HPVE2	HPVE1	HPVE0
1	0	0	0	0	0	0	HVS	HHS

Table 120. HD sync trigger state 1 register, subaddress D4h, bit description

Bit	Symbol	Description
7 to 0	HLCT[7:0]	with HLCT[9:8] (see Table 121) state of the HD line counter after trigger (counts backwards)

Table 121. HD sync trigger state 2 register, subaddress D5h, bit description

Bit	Symbol	Description
7 to 4	HLCPT[3:0]	state of the HD line type pointer after trigger
3 and 2	HLPPT[1:0]	state of the HD pattern pointer after trigger
1 and 0	HLCT[9:8]	see Table 120

Table 122. HD sync trigger state 3 register, subaddress D6h, bit description

Bit	Symbol	Description
7 to 0	HDCT[7:0]	with HDCT[9:8] (see Table 123) state of the HD duration counter after trigger (counts backwards)

Table 123. HD sync trigger state 4 register, subaddress D7h, bit description

Bit	Symbol	Description
7	-	must be programmed with logic 0 to ensure compatibility to future enhancements
6 to 4	HEPT[2:0]	state of the HD event type pointer in the line type array after trigger
3 and 2	-	must be programmed with logic 0 to ensure compatibility to future enhancements
1 and 0	HDCT[9:8]	see Table 122

Table 124. HD sync trigger phase x registers, subaddresses D8h and D9h, bit description

Subaddress	Bit	Symbol	Description
D9h	7 to 4	-	must be programmed with logic 0 to ensure compatibility to future enhancements
	3 to 0	HTX[11:8]	horizontal trigger phase for the HD sync engine in pixel clocks
D8h	7 to 0	HTX[7:0]	

Table 125. HD sync trigger phase y registers, subaddresses DAh and DBh, bit description

Subaddress	Bit	Symbol	Description
DBh	7 to 2	-	must be programmed with logic 0 to ensure compatibility to future enhancements
	1 and 0	HTY[9:8]	vertical trigger phase for the HD sync engine in input lines
DAh	7 to 0	HTY[7:0]	

Table 126. HD output control register, subaddress DCh, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 4	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
3	HDSYE	R/W		HD sync engine
			0*	off
			1	active
2	HDTC	R/W		HD output path processes
			0*	RGB
			1	YUV

Table 126. HD output control register, subaddress DCh, bit description *...continued*

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
1	HDGY	R/W	0*	gain in the HD output path is reduced, insertion of sync pulses is possible
			1	full level swing at the input causes full level swing at the DACs in HD mode
0	HDIP	R/W		interpolator for the color difference signal in the HD output path
			0*	active
			1	off

Table 127. Cursor color 1 R, G and B registers, subaddresses F0h to F2h, bit description

Subaddress	Bit	Symbol	Description
F0h	7 to 0	CC1R[7:0]	RED portion of first cursor color
F1h	7 to 0	CC1G[7:0]	GREEN portion of first cursor color
F2h	7 to 0	CC1B[7:0]	BLUE portion of first cursor color

Table 128. Cursor color 2 R, G and B registers, subaddresses F3h to F5h, bit description

Subaddress	Bit	Symbol	Description
F3h	7 to 0	CC2R[7:0]	RED portion of second cursor color
F4h	7 to 0	CC2G[7:0]	GREEN portion of second cursor color
F5h	7 to 0	CC2B[7:0]	BLUE portion of second cursor color

Table 129. Auxiliary cursor color R, G and B registers, subaddresses F6h to F8h, bit description

Subaddress	Bit	Symbol	Description
F6h	7 to 0	AUXR[7:0]	RED portion of auxiliary cursor color
F7h	7 to 0	AUXG[7:0]	GREEN portion of auxiliary cursor color
F8h	7 to 0	AUXB[7:0]	BLUE portion of auxiliary cursor color

Table 130. Horizontal cursor position and horizontal hot spot, MSB XCP registers, subaddresses F9h and FAh, bit description

Subaddress	Bit	Symbol	Description
FAh	7 to 3	XHS[4:0]	horizontal hot spot of cursor
	2 to 0	XCP[10:8]	horizontal cursor position
F9h	7 to 0	XCP[7:0]	

Table 131. Vertical cursor position and vertical hot spot, MSB YCP registers, subaddresses FBh and FCh, bit description

Subaddress	Bit	Symbol	Description
FCh	7 to 3	YHS[4:0]	vertical hot spot of cursor
	2	-	must be programmed with logic 0 to ensure compatibility to future enhancements
	1 and 0	YCP[9:8]	vertical cursor position
FBh	7 to 0	YCP[7:0]	

Table 132. Input path control register, subaddress FDh, bit description

Bit	Symbol	Access	Value	Description
7	LUTOFF	R/W		color look-up table
			0	active
			1	bypassed
6	CMODE	R/W		cursor mode
			0	cursor mode; input color will be inverted
			1	auxiliary cursor color will be inserted
5	LUTL	R/W		LUT loading via input data stream
			0	inactive
			1	color and cursor LUTs are loaded
4 to 2	IF[2:0]	R/W		input format
			000	8 + 8 + 8-bit 4 : 4 : 4 non-interlaced RGB or C_B-Y-C_R
			001	5 + 5 + 5-bit 4 : 4 : 4 non-interlaced RGB
			010	5 + 6 + 5-bit 4 : 4 : 4 non-interlaced RGB
			011	8 + 8 + 8-bit 4 : 2 : 2 non-interlaced C_B-Y-C_R
			100	8 + 8 + 8-bit 4 : 2 : 2 interlaced C_B-Y-C_R (ITU-R BT.656, 27 MHz clock) (in subaddresses 91h and 94h set XPIX = number of active pixels/line)
			101	8-bit non-interlaced index color
			110	8 + 8 + 8-bit 4 : 4 : 4 non-interlaced RGB or C_B-Y-C_R (special bit ordering)
1	MATOFF	R/W		RGB to C_R-Y-C_B matrix
			0	active
			1	bypassed
0	DFOFF	R/W		down formatter
			0	(4 : 4 : 4 to 4 : 2 : 2) in input path is active
			1	bypassed

Table 133. Cursor bit map register, subaddress FEh, bit description

Data byte	Description
CURSA	RAM start address for cursor bit map; the byte following subaddress FEh points to the first cell to be loaded with the next transmitted byte; succeeding cells are loaded by auto-incrementing until stop condition

Table 134. Color look-up table register, subaddress FFh, bit description

Data byte	Description
COLSA	RAM start address for color LUT; the byte following subaddress FFh points to the first cell to be loaded with the next transmitted byte; succeeding cells are loaded by auto-incrementing until stop condition

In subaddresses 5Bh, 5Ch, 5Dh, 5Eh, 62h and D3h all IRE values are rounded up.

11.1.3 Slave transmitter

Table 135. Status byte register, subaddress 00h, bit description

Bit	Symbol	Access	Value	Description
7 to 5	VER[2:0]	R	101	version identification of the device: it will be changed with all versions of the IC that have different programming models; current version is 101 binary
4	CCRDO	R	1	set immediately after the closed caption bytes of the odd field have been encoded
			0	reset after information has been written to the subaddresses 67h and 68h
3	CCRDE	R	1	set immediately after the closed caption bytes of the even field have been encoded
			0	reset after information has been written to the subaddresses 69h and 6Ah
2	-	R	0	-
1	FSEQ	R	1	during first field of a sequence (repetition rate: NTSC = 4 fields, PAL = 8 fields)
			0	not first field of a sequence
0	O_E	R	1	during even field
			0	during odd field

Table 136. Slave transmitter (slave address 89h)

Register function	Subaddress	Data byte							
		D7	D6	D5	D4	D3	D2	D1	D0
Status byte	00h	VER2	VER1	VER0	CCRDO	CCRDE	0	FSEQ	O_E
Chip ID	1Ch	CID7	CID6	CID5	CID4	CID3	CID2	CID1	CID0
FIFO status	80h	0	0	0	0	0	0	OVFL	UDFL

Table 137. Chip ID register, subaddress 1Ch, bit description

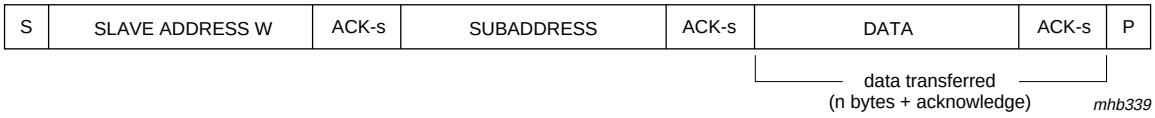
Bit	Symbol	Access	Value	Description
7 to 0	CID[7:0]	R		chip ID
			04h	SAA7108AE
			05h	SAA7109AE

Table 138. FIFO status register, subaddress 80h, bit description

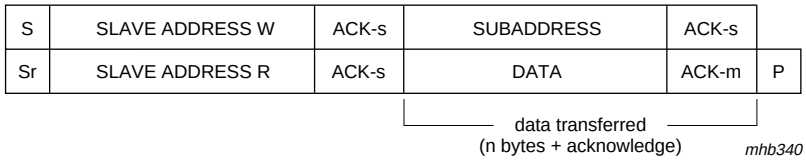
Bit	Symbol	Access	Value	Description
7 to 4	-	R	0h	-
3	IFERR	R	0	normal FIFO state
			1	input FIFO overflow/underflow has occurred
2	BFERR	R	0	normal FIFO state
			1	buffer FIFO overflow, only if YUPSC = 1
1	OVFL	R	0	no FIFO overflow
			1	FIFO overflow has occurred; this bit is reset after this subaddress has been read
0	UDFL	R	0	no FIFO underflow
			1	FIFO underflow has occurred; this bit is reset after this subaddress has been read

11.2 Digital video decoder part

11.2.1 I²C-bus format



a. Write procedure.



b. Read procedure (combined).

Fig 52. I²C-bus format

Table 139. Description of I²C-bus format[1]

Code	Description
S	START condition
Sr	repeated START condition
SLAVE ADDRESS W	0100 0010 (42h, default) or 0100 0000 (40h)[2]
SLAVE ADDRESS R	0100 0011 (43h, default) or 0100 0001 (41h)[2]
ACK-s	acknowledge generated by the slave
ACK-m	acknowledge generated by the master
SUBADDRESS	subaddress byte; see Table 140 and Table 141
DATA	data byte; see Table 141; if more than one byte DATA is transmitted the subaddress pointer is automatically incremented
P	STOP condition

[1] The SAA7108AE; SAA7109AE supports the 'fast mode' I²C-bus specification extension (data rate up to 400 kbit/s).

[2] If pin RTCO is strapped to V_{DDD} via a 3.3 kΩ resistor.

Table 140. Subaddress description and access

Subaddress	Description	Access (read/write)
00h	chip version	read only
F0h to FFh	reserved	-
Video decoder: 01h to 2Fh		
01h to 05h	front-end part	read and write
06h to 19h	decoder part	read and write
1Ah to 1Eh	reserved	-
1Fh	video decoder status byte	read only
20h to 2Fh	reserved	-
Audio clock generation: 30h to 3Fh		
30h to 3Ah	audio clock generator	read and write
3Bh to 3Fh	reserved	-
General purpose VBI data slicer: 40h to 7Fh		
40h to 5Eh	VBI data slicer	read and write
5Fh	reserved	-
60h to 62h	VBI data slicer status	read only
63h to 7Fh	reserved	-
X port, I port and the scaler: 80h to EFh		
80h to 8Fh	task independent global settings	read and write
90h to BFh	task A definition	read and write
C0h to EFh	task B definition	read and write

Table 141. I²C-bus receiver/transmitter overview

Register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Chip version: register 00h									
Chip version (read only)	00h	ID7	ID6	ID5	ID4	-	-	-	-
Video decoder: registers 01h to 2Fh									
Front-end part: registers 01h to 05h									
Increment delay	01h	[1]	[1]	[1]	[1]	IDEL3	IDEL2	IDEL1	IDEL0
Analog input control 1	02h	FUSE1	FUSE0	GUDL1	GUDL0	MODE3	MODE2	MODE1	MODE0
Analog input control 2	03h	[1]	HLNRS	VBSL	WPOFF	HOLDG	GAFIX	GAI28	GAI18
Analog input control 3	04h	GAI17	GAI16	GAI15	GAI14	GAI13	GAI12	GAI11	GAI10
Analog input control 4	05h	GAI27	GAI26	GAI25	GAI24	GAI23	GAI22	GAI21	GAI20
Decoder part: registers 06h to 2Fh									
Horizontal sync start	06h	HSB7	HSB6	HSB5	HSB4	HSB3	HSB2	HSB1	HSB0
Horizontal sync stop	07h	HSS7	HSS6	HSS5	HSS4	HSS3	HSS2	HSS1	HSS0
Sync control	08h	AUFD	FSEL	FOET	HTC1	HTC0	HPLL	VNOI1	VNOI0
Luminance control	09h	BYPS	YCOMB	LDEL	LUBW	LUFI3	LUFI2	LUFI1	LUFI0
Luminance brightness control	0Ah	DBRI7	DBRI6	DBRI5	DBRI4	DBRI3	DBRI2	DBRI1	DBRI0
Luminance contrast control	0Bh	DCON7	DCON6	DCON5	DCON4	DCON3	DCON2	DCON1	DCON0
Chrominance saturation control	0Ch	DSAT7	DSAT6	DSAT5	DSAT4	DSAT3	DSAT2	DSAT1	DSAT0
Chrominance hue control	0Dh	HUEC7	HUEC6	HUEC5	HUEC4	HUEC3	HUEC2	HUEC1	HUEC0
Chrominance control 1	0Eh	CDTO	CSTD2	CSTD1	CSTD0	DCVF	FCTC	[1]	CCOMB
Chrominance gain control	0Fh	ACGC	CGAIN6	CGAIN5	CGAIN4	CGAIN3	CGAIN2	CGAIN1	CGAIN0
Chrominance control 2	10h	OFFU1	OFFU0	OFFV1	OFFV0	CHBW	LCBW2	LCBW1	LCBW0
Mode/delay control	11h	COLO	RTP1	HDEL1	HDEL0	RTP0	YDEL2	YDEL1	YDEL0
RT signal control	12h	RTSE13	RTSE12	RTSE11	RTSE10	RTSE03	RTSE02	RTSE01	RTSE00
RT/X port output control	13h	RTCE	XRHS	XRVS1	XRVS0	HLSEL	OFTS2	OFTS1	OFTS0
Analog/ADC/compatibility control	14h	CM99	UPTCV	AOSL1	AOSL0	XTOUTE	OLDSB	APCK1	APCK0
VGATE start, FID change	15h	VSTA7	VSTA6	VSTA5	VSTA4	VSTA3	VSTA2	VSTA1	VSTA0
VGATE stop	16h	VSTO7	VSTO6	VSTO5	VSTO4	VSTO3	VSTO2	VSTO1	VSTO0
Miscellaneous, VGATE configuration and MSBs	17h	LLCE	LLC2E	[1]	[1]	[1]	VGPS	VSTO8	VSTA8
Raw data gain control	18h	RAWG7	RAWG6	RAWG5	RAWG4	RAWG3	RAWG2	RAWG1	RAWG0
Raw data offset control	19h	RAWO7	RAWO6	RAWO5	RAWO4	RAWO3	RAWO2	RAWO1	RAWO0

Table 141. I²C-bus receiver/transmitter overview *…continued*

Register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Reserved	1Ah to 1Eh	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Status byte video decoder (read only, OLDSB = 0)	1Fh	INTL	HLVLN	FIDT	GLIMT	GLIMB	WIPA	COPRO	RDCAP
Status byte video decoder (read only, OLDSB = 1)	1Fh	INTL	HLCK	FIDT	GLIMT	GLIMB	WIPA	SLTCA	CODE
Reserved	20h to 2Fh	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Audio clock generator part: registers 30h to 3Fh									
Audio master clock cycles per field	30h	ACPF7	ACPF6	ACPF5	ACPF4	ACPF3	ACPF2	ACPF1	ACPF0
	31h	ACPF15	ACPF14	ACPF13	ACPF12	ACPF11	ACPF10	ACPF9	ACPF8
	32h	[1]	[1]	[1]	[1]	[1]	[1]	ACPF17	ACPF16
Reserved	33h	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Audio master clock nominal increment	34h	ACNI7	ACNI6	ACNI5	ACNI4	ACNI3	ACNI2	ACNI1	ACNI0
	35h	ACNI15	ACNI14	ACNI13	ACNI12	ACNI11	ACNI10	ACNI9	ACNI8
	36h	[1]	[1]	ACNI21	ACNI20	ACNI19	ACNI18	ACNI17	ACNI16
Reserved	37h	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Clock ratio AMXCLK to ASCLK	38h	[1]	[1]	SDIV5	SDIV4	SDIV3	SDIV2	SDIV1	SDIV0
Clock ratio ASCLK to ALRCLK	39h	[1]	[1]	LRDIV5	LRDIV4	LRDIV3	LRDIV2	LRDIV1	LRDIV0
Audio clock generator basic setup	3Ah	[1]	[1]	[1]	[1]	APLL	AMVR	LRPH	SCPH
Reserved	3Bh to 3Fh	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
General purpose VBI data slicer part: registers 40h to 7Fh									
Slicer control 1	40h	[1]	HAM_N	FCE	HUNT_N	[1]	[1]	[1]	[1]
LCR2 to LCR24 (n = 2 to 24)	41h to 57h	LCRn_7	LCRn_6	LCRn_5	LCRn_4	LCRn_3	LCRn_2	LCRn_1	LCRn_0
Programmable framing code	58h	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0
Horizontal offset for slicer	59h	HOFF7	HOFF6	HOFF5	HOFF4	HOFF3	HOFF2	HOFF1	HOFF0
Vertical offset for slicer	5Ah	VOFF7	VOFF6	VOFF5	VOFF4	VOFF3	VOFF2	VOFF1	VOFF0
Field offset and MSBs for horizontal and vertical offset	5Bh	FOFF	RECODE	[1]	VOFF8	[1]	HOFF10	HOFF9	HOFF8
Reserved (for testing)	5Ch	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Header and data identification (DID) code control	5Dh	FVREF	[1]	DID5	DID4	DID3	DID2	DID1	DID0
Sliced data identification (SDID) code	5Eh	[1]	[1]	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0
Reserved	5Fh	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]

Table 141. I²C-bus receiver/transmitter overview *…continued*

Register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Slicer status byte 0 (read only)	60h	-	FC8V	FC7V	VPSV	PPV	CCV	-	-
Slicer status byte 1 (read only)	61h	-	-	F21_N	LN8	LN7	LN6	LN5	LN4
Slicer status byte 2 (read only)	62h	LN3	LN2	LN1	LN0	DT3	DT2	DT1	DT0
Reserved	63h to 7Fh	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
X port, I port and the scaler part: registers 80h to EFh									
Task independent global settings: 80h to 8Fh									
Global control 1	80h	[1]	SMOD	TEB	TEA	ICKS3	ICKS2	ICKS1	ICKS0
Reserved	81h and 82h	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
X port I/O enable and output clock phase control	83h	[1]	[1]	XPCK1	XPCK0	[1]	XRQT	XPE1	XPE0
I port signal definitions	84h	IDG01	IDG00	IDG11	IDG10	IDV1	IDV0	IDH1	IDH0
I port signal polarities	85h	ISWP1	ISWP0	ILLV	IG0P	IG1P	IRVP	IRHP	IDQP
I port FIFO flag control and arbitration	86h	VITX1	VITX0	IDG02	IDG12	FFL1	FFL0	FEL1	FEL0
I port I/O enable, output clock and gated clock phase control	87h	IPCK3	IPCK2	IPCK1	IPCK0	[1]	[1]	IPE1	IPE0
Power save control	88h	CH4EN	CH2EN	SWRST	DPROG	SLM3	[1]	SLM1	SLM0
Reserved	89h to 8Eh	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Status information scaler part	8Fh	XTRI	ITRI	FFIL	FFOV	PRDON	ERROF	FIDSCI	FIDSCO
Task A definition: registers 90h to BFh									
Basic settings and acquisition window definition									
Task handling control	90h	CONLH	OFIDC	FSKP2	FSKP1	FSKP0	RPTSK	STRC1	STRC0
X port formats and configuration	91h	CONLV	HLDFV	SCSRC1	SCSRC0	SCRQE	FSC2	FSC1	FSC0
X port input reference signal definitions	92h	XFDV	XFDH	XDV1	XDV0	XCODE	XDH	XDQ	XCKS
I port output formats and configuration	93h	ICODE	I8_16	FYSK	FOI1	FOI0	FSI2	FSI1	FSI0
Horizontal input window start	94h	XO7	XO6	XO5	XO4	XO3	XO2	XO1	XO0
	95h	[1]	[1]	[1]	[1]	XO11	XO10	XO9	XO8
Horizontal input window length	96h	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0
	97h	[1]	[1]	[1]	[1]	XS11	XS10	XS9	XS8
Vertical input window start	98h	YO7	YO6	YO5	YO4	YO3	YO2	YO1	YO0
	99h	[1]	[1]	[1]	[1]	YO11	YO10	YO9	YO8

Table 141. I²C-bus receiver/transmitter overview *…continued*

Register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Vertical input window length	9Ah	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0
	9Bh	[1]	[1]	[1]	[1]	YS11	YS10	YS9	YS8
Horizontal output window length	9Ch	XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0
	9Dh	[1]	[1]	[1]	[1]	XD11	XD10	XD9	XD8
Vertical output window length	9Eh	YD7	YD6	YD5	YD4	YD3	YD2	YD1	YD0
	9Fh	[1]	[1]	[1]	[1]	YD11	YD10	YD9	YD8
FIR filtering and prescaling									
Horizontal prescaling	A0h	[1]	[1]	XPSC5	XPSC4	XPSC3	XPSC2	XPSC1	XPSC0
Accumulation length	A1h	[1]	[1]	XACL5	XACL4	XACL3	XACL2	XACL1	XACL0
Prescaler DC gain and FIR prefilter control	A2h	PFUV1	PFUV0	PFY1	PFY0	XC2_1	XDCG2	XDCG1	XDCG0
Reserved	A3h	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Luminance brightness control	A4h	BRIG7	BRIG6	BRIG5	BRIG4	BRIG3	BRIG2	BRIG1	BRIG0
Luminance contrast control	A5h	CONT7	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0
Chrominance saturation control	A6h	SATN7	SATN6	SATN5	SATN4	SATN3	SATN2	SATN1	SATN0
Reserved	A7h	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Horizontal phase scaling									
Horizontal luminance scaling increment	A8h	XSCY7	XSCY6	XSCY5	XSCY4	XSCY3	XSCY2	XSCY1	XSCY0
	A9h	[1]	[1]	[1]	XSCY12	XSCY11	XSCY10	XSCY9	XSCY8
Horizontal luminance phase offset	AAh	XPHY7	XPHY6	XPHY5	XPHY4	XPHY3	XPHY2	XPHY1	XPHY0
Reserved	ABh	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Horizontal chrominance scaling increment	ACh	XSCC7	XSCC6	XSCC5	XSCC4	XSCC3	XSCC2	XSCC1	XSCC0
	ADh	[1]	[1]	[1]	XSCC12	XSCC11	XSCC10	XSCC9	XSCC8
Horizontal chrominance phase offset	AEh	XPHC7	XPHC6	XPHC5	XPHC4	XPHC3	XPHC2	XPHC1	XPHC0
Reserved	AFh	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Vertical scaling									
Vertical luminance scaling increment	B0h	YSCY7	YSCY6	YSCY5	YSCY4	YSCY3	YSCY2	YSCY1	YSCY0
	B1h	YSCY15	YSCY14	YSCY13	YSCY12	YSCY11	YSCY10	YSCY9	YSCY8
Vertical chrominance scaling increment	B2h	YSCC7	YSCC6	YSCC5	YSCC4	YSCC3	YSCC2	YSCC1	YSCC0
	B3h	YSCC15	YSCC14	YSCC13	YSCC12	YSCC11	YSCC10	YSCC9	YSCC8
Vertical scaling mode control	B4h	[1]	[1]	[1]	YMIR	[1]	[1]	[1]	YMODE
Reserved	B5h to B7h	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]

Table 141. I²C-bus receiver/transmitter overview *…continued*

Register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Vertical chrominance phase offset ‘00’	B8h	YPC07	YPC06	YPC05	YPC04	YPC03	YPC02	YPC01	YPC00
Vertical chrominance phase offset ‘01’	B9h	YPC17	YPC16	YPC15	YPC14	YPC13	YPC12	YPC11	YPC10
Vertical chrominance phase offset ‘10’	BAh	YPC27	YPC26	YPC25	YPC24	YPC23	YPC22	YPC21	YPC20
Vertical chrominance phase offset ‘11’	BBh	YPC37	YPC36	YPC35	YPC34	YPC33	YPC32	YPC31	YPC30
Vertical luminance phase offset ‘00’	BCh	YPY07	YPY06	YPY05	YPY04	YPY03	YPY02	YPY01	YPY00
Vertical luminance phase offset ‘01’	BDh	YPY17	YPY16	YPY15	YPY14	YPY13	YPY12	YPY11	YPY10
Vertical luminance phase offset ‘10’	BEh	YPY27	YPY26	YPY25	YPY24	YPY23	YPY22	YPY21	YPY20
Vertical luminance phase offset ‘11’	BFh	YPY37	YPY36	YPY35	YPY34	YPY33	YPY32	YPY31	YPY30
Task B definition registers C0h to EFh									
Basic settings and acquisition window definition									
Task handling control	C0h	CONLH	OFIDC	FSKP2	FSKP1	FSKP0	RPTSK	STRC1	STRC0
X port formats and configuration	C1h	CONLV	HLDFV	SCSRC1	SCSRC0	SCRQE	FSC2	FSC1	FSC0
Input reference signal definition	C2h	XFDV	XFDH	XDV1	XDV0	XCODE	XDH	XDQ	XCKS
I port formats and configuration	C3h	ICODE	I8_16	FYSK	FOI1	FOI0	FSI2	FSI1	FSI0
Horizontal input window start	C4h	XO7	XO6	XO5	XO4	XO3	XO2	XO1	XO0
	C5h	[1]	[1]	[1]	[1]	XO11	XO10	XO9	XO8
Horizontal input window length	C6h	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0
	C7h	[1]	[1]	[1]	[1]	XS11	XS10	XS9	XS8
Vertical input window start	C8h	YO7	YO6	YO5	YO4	YO3	YO2	YO1	YO0
	C9h	[1]	[1]	[1]	[1]	YO11	YO10	YO9	YO8
Vertical input window length	CAh	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0
	CBh	[1]	[1]	[1]	[1]	YS11	YS10	YS9	YS8
Horizontal output window length	CCh	XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0
	CDh	[1]	[1]	[1]	[1]	XD11	XD10	XD9	XD8
Vertical output window length	CEh	YD7	YD6	YD5	YD4	YD3	YD2	YD1	YD0
	CFh	[1]	[1]	[1]	[1]	YD11	YD10	YD9	YD8
FIR filtering and prescaling									
Horizontal prescaling	D0h	[1]	[1]	XPSC5	XPSC4	XPSC3	XPSC2	XPSC1	XPSC0
Accumulation length	D1h	[1]	[1]	XACL5	XACL4	XACL3	XACL2	XACL1	XACL0
Prescaler DC gain and FIR prefilter control	D2h	PFUV1	PFUV0	PFY1	PFY0	XC2_1	XDCG2	XDCG1	XDCG0
Reserved	D3h	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]

Table 141. I²C-bus receiver/transmitter overview *…continued*

Register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Luminance brightness control	D4h	BRIG7	BRIG6	BRIG5	BRIG4	BRIG3	BRIG2	BRIG1	BRIG0
Luminance contrast control	D5h	CONT7	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0
Chrominance saturation control	D6h	SATN7	SATN6	SATN5	SATN4	SATN3	SATN2	SATN1	SATN0
Reserved	D7h	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Horizontal phase scaling									
Horizontal luminance scaling increment	D8h	XSCY7	XSCY6	XSCY5	XSCY4	XSCY3	XSCY2	XSCY1	XSCY0
	D9h	[1]	[1]	[1]	XSCY12	XSCY11	XSCY10	XSCY9	XSCY8
Horizontal luminance phase offset	DAh	XPHY7	XPHY6	XPHY5	XPHY4	XPHY3	XPHY2	XPHY1	XPHY0
Reserved	DBh	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Horizontal chrominance scaling increment	DCh	XSCC7	XSCC6	XSCC5	XSCC4	XSCC3	XSCC2	XSCC1	XSCC0
	DDh	[1]	[1]	[1]	XSCC12	XSCC11	XSCC10	XSCC9	XSCC8
Horizontal chrominance phase offset	DEh	XPHC7	XPHC6	XPHC5	XPHC4	XPHC3	XPHC2	XPHC1	XPHC0
Reserved	DFh	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Vertical scaling									
Vertical luminance scaling increment	E0h	YSCY7	YSCY6	YSCY5	YSCY4	YSCY3	YSCY2	YSCY1	YSCY0
	E1h	YSCY15	YSCY14	YSCY13	YSCY12	YSCY11	YSCY10	YSCY9	YSCY8
Vertical chrominance scaling increment	E2h	YSCC7	YSCC6	YSCC5	YSCC4	YSCC3	YSCC2	YSCC1	YSCC0
	E3h	YSCC15	YSCC14	YSCC13	YSCC12	YSCC11	YSCC10	YSCC9	YSCC8
Vertical scaling mode control	E4h	[1]	[1]	[1]	YMIR	[1]	[1]	[1]	YMODE
Reserved	E5h to E7h	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Vertical chrominance phase offset ‘00’	E8h	YPC07	YPC06	YPC05	YPC04	YPC03	YPC02	YPC01	YPC00
Vertical chrominance phase offset ‘01’	E9h	YPC17	YPC16	YPC15	YPC14	YPC13	YPC12	YPC11	YPC10
Vertical chrominance phase offset ‘10’	EAh	YPC27	YPC26	YPC25	YPC24	YPC23	YPC22	YPC21	YPC20
Vertical chrominance phase offset ‘11’	EBh	YPC37	YPC36	YPC35	YPC34	YPC33	YPC32	YPC31	YPC30
Vertical luminance phase offset ‘00’	ECh	YPY07	YPY06	YPY05	YPY04	YPY03	YPY02	YPY01	YPY00
Vertical luminance phase offset ‘01’	EDh	YPY17	YPY16	YPY15	YPY14	YPY13	YPY12	YPY11	YPY10
Vertical luminance phase offset ‘10’	EEh	YPY27	YPY26	YPY25	YPY24	YPY23	YPY22	YPY21	YPY20
Vertical luminance phase offset ‘11’	EFh	YPY37	YPY36	YPY35	YPY34	YPY33	YPY32	YPY31	YPY30

[1] All unused control bits must be programmed with logic 0 to ensure compatibility to future enhancements.

11.2.2 I²C-bus details

11.2.2.1 Subaddress 00h

Table 142. Chip Version (CV) identification; 00h[7:4]; read only register

Function	Logic levels			
	ID7	ID6	ID5	ID4
Chip Version (CV)	CV3	CV2	CV1	CV0

11.2.2.2 Subaddress 01h

The programming of the horizontal increment delay is used to match internal processing delays to the delay of the ADC. Use recommended position only.

Table 143. Horizontal increment delay; 01h[3:0]

Function	IDEL3	IDEL2	IDEL1	IDEL0
No update	1	1	1	1
Minimum delay	1	1	1	0
Recommended position	**1**	**0**	**0**	**0**
Maximum delay	0	0	0	0

11.2.2.3 Subaddress 02h

Table 144. Analog input control 1 (AICO1); 02h[7:0]

Bit	Description	Symbol	Value	Function
7 and 6	analog function select; see Figure 16	FUSE[1:0]	00	amplifier plus anti-alias filter bypassed
			01	amplifier plus anti-alias filter bypassed
			10	amplifier active
			11	amplifier plus anti-alias filter active
5 and 4	update hysteresis for 9-bit gain; see Figure 17	GUDL[1:0]	00	off
			01	±1 LSB
			10	±2 LSB
			11	±3 LSB

Table 144. Analog input control 1 (AICO1); 02h[7:0] *…continued*

Bit	Description	Symbol	Value	Function
3 to 0	mode selection	MODE[3:0]	0000	**Mode 0**: CVBS (automatic gain) from AI11 (pin P13); see Figure 53
			0001	**Mode 1**: CVBS (automatic gain) from AI12 (pin P11); see Figure 54
			0010	**Mode 2**: CVBS (automatic gain) from AI21 (pin P10); see Figure 55
			0011	**Mode 3**: CVBS (automatic gain) from AI22 (pin P9); see Figure 56
			0100	**Mode 4**: CVBS (automatic gain) from AI23 (pin P7); see Figure 57
			0101	**Mode 5**: CVBS (automatic gain) from AI24 (pin P6); see Figure 58
			0110	**Mode 6**: Y (automatic gain) from AI11 (pin P13) + C (gain adjustable via GAI28 to GAI20) from AI21 (pin P10)[1]; see Figure 59
			0111	**Mode 7**: Y (automatic gain) from AI12 (pin P11) + C (gain adjustable via GAI28 to GAI20) from AI22 (pin P9)[1]; see Figure 60
			1000	**Mode 8**: Y (automatic gain) from AI11 (pin P13) + C (gain adapted to Y gain) from AI21 (pin P10)[1]; see Figure 61
			1001	**Mode 9**: Y (automatic gain) from AI12 (pin P11) + C (gain adapted to Y gain) from AI22 (pin P9)[1]; see Figure 62
			1010 to 1111	**Modes 10 to 15**: reserved

[1] To take full advantage of the Y/C modes 6 to 9, the I²C-bus bit BYPS (subaddress 09h, bit 7) should be set to logic 1 (full luminance bandwidth).

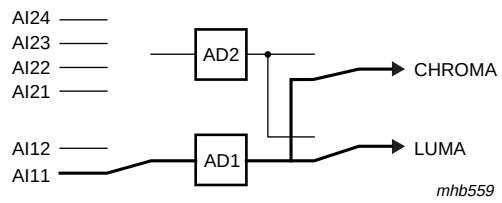


Fig 53. Mode 0 CVBS (automatic gain)

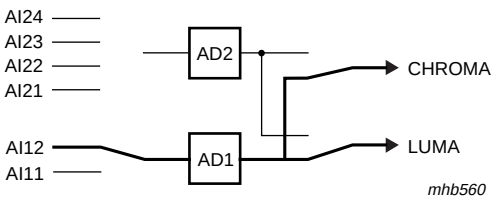


Fig 54. Mode 1 CVBS (automatic gain)

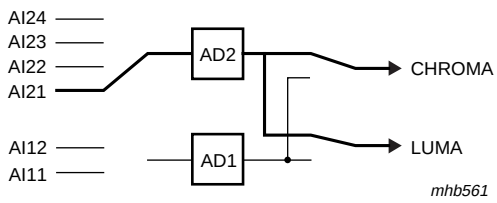


Fig 55. Mode 2 CVBS (automatic gain)

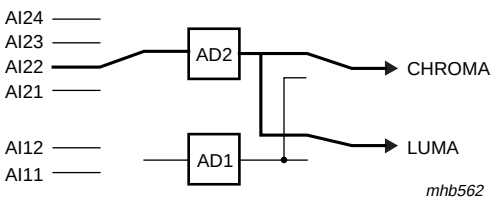


Fig 56. Mode 3 CVBS (automatic gain)

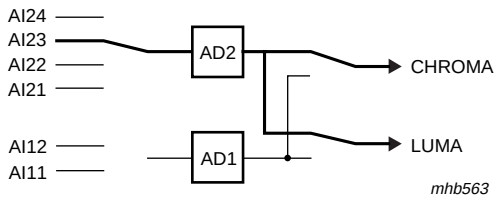


Fig 57. Mode 4 CVBS (automatic gain)

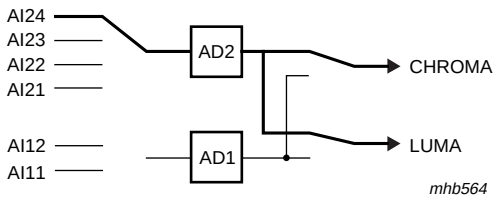
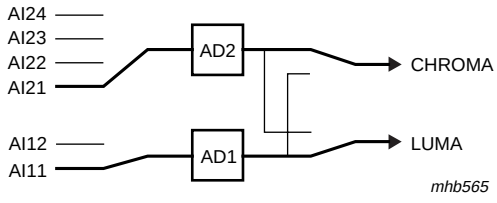
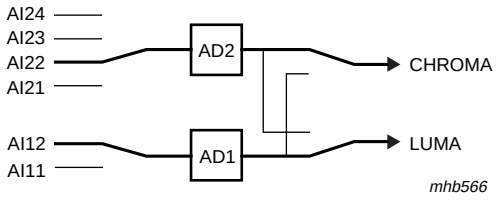


Fig 58. Mode 5 CVBS (automatic gain)



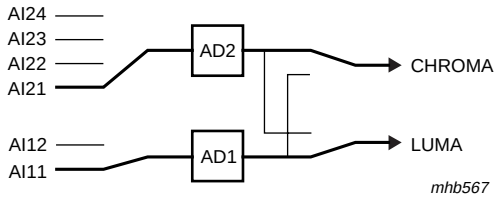
I²C-bus bit BYPS (subaddress 09h, bit D7) should be set to logic 1 (full luminance bandwidth).

Fig 59. Mode 6 Y + C (gain channel 2 adjusted via GAI2)



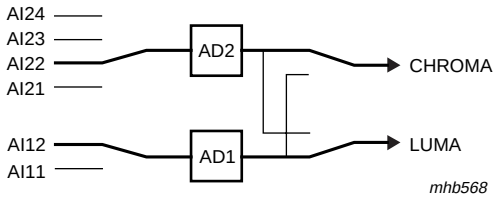
I²C-bus bit BYPS (subaddress 09h, bit D7) should be set to logic 1 (full luminance bandwidth).

Fig 60. Mode 7 Y + C (gain channel 2 adjusted via GAI2)



I²C-bus bit BYPS (subaddress 09h, bit D7) should be set to logic 1 (full luminance bandwidth).

Fig 61. Mode 8 Y + C (gain channel 2 adapted to Y gain)



I²C-bus bit BYPS (subaddress 09h, bit D7) should be set to logic 1 (full luminance bandwidth).

Fig 62. Mode 9 Y + C (gain channel 2 adapted to Y gain)

11.2.2.4 Subaddress 03h

Table 145. Analog input control 2 (AICO2); 03h[6:0]

Bit	Description	Symbol	Value	Function
6	HL not reference select	HLNRS	0	normal clamping if decoder is in unlocked state
			1[1]	reference select if decoder is in unlocked state
5	AGC hold during vertical blanking period	VBSL	0	short vertical blanking (AGC disabled during equalization and serration pulses)
			1	long vertical blanking (AGC disabled from start of pre-equalization pulses until start of active video (line 22 for 60 Hz, line 24 for 50 Hz)
4	white peak control off	WPOFF	0[1]	white peak control active
			1	white peak control off
3	automatic gain control integration	HOLDG	0	AGC active
			1	AGC integration hold (freeze)
2	gain control fix	GAFIX	0	automatic gain controlled by MODE3 to MODE0
			1	gain is user programmable via GAI[17:10] and GAI[27:20]
1	static gain control channel 2 sign bit	GAI28	see Table 147	
0	static gain control channel 1 sign bit	GAI18	see Table 146	

[1] HLNRS = 1 should not be used in combination with WPOFF = 0.

11.2.2.5 Subaddress 04h

Table 146. Analog input control 3 (AICO3); static gain control channel 1; 03h[0] and 04h[7:0]

Decimal value	Gain (dB)	Sign bit 03h[0]	Control bits 7 to 0							
		GAI18	GAI17	GAI16	GAI15	GAI14	GAI13	GAI12	GAI11	GAI10
0...	–3	0	0	0	0	0	0	0	0	0
...144	0	0	1	0	0	1	0	0	0	0
145...	0	0	1	0	0	1	0	0	0	1
...511	+6	1	1	1	1	1	1	1	1	1

11.2.2.6 Subaddress 05h

Table 147. Analog input control 4 (AICO4); static gain control channel 2; 03h[1] and 05h[7:0]

Decimal value	Gain (dB)	Sign bit 03h[1]	Control bits 7 to 0							
		GAI28	GAI27	GAI26	GAI25	GAI24	GAI23	GAI22	GAI21	GAI20
0...	–3	0	0	0	0	0	0	0	0	0
...144	0	0	1	0	0	1	0	0	0	0
145...	0	0	1	0	0	1	0	0	0	1
...511	+6	1	1	1	1	1	1	1	1	1

11.2.2.7 Subaddress 06h

Table 148. Horizontal sync start; 06h[7:0]

Delay time (step size = 8/LLC)	Control bits 7 to 0							
	HSB7	HSB6	HSB5	HSB4	HSB3	HSB2	HSB1	HSB0
–128...–109 (50 Hz)	forbidden (outside available central counter range)							
–128...–108 (60 Hz)	forbidden (outside available central counter range)							
–108 (50 Hz)...	1	0	0	1	0	1	0	0
–107 (60 Hz)...	1	0	0	1	0	1	0	1
...108 (50 Hz)	0	1	1	0	1	1	0	0
...107 (60 Hz)	0	1	1	0	1	0	1	1
109...127 (50 Hz)	forbidden (outside available central counter range)							
108...127 (60 Hz)								

11.2.2.8 Subaddress 07h

Table 149. Horizontal sync stop; 07h[7:0]

Delay time (step size = 8/LLC)	Control bits 7 to 0							
	HSS7	HSS6	HSS5	HSS4	HSS3	HSS2	HSS1	HSS0
–128...–109 (50 Hz)	forbidden (outside available central counter range)							
–128...–108 (60 Hz)	forbidden (outside available central counter range)							
–108 (50 Hz)...	1	0	0	1	0	1	0	0
–107 (60 Hz)...	1	0	0	1	0	1	0	1
...108 (50 Hz)	0	1	1	0	1	1	0	0
...107 (60 Hz)	0	1	1	0	1	0	1	1
109...127 (50 Hz)	forbidden (outside available central counter range)							
108...127 (60 Hz)	forbidden (outside available central counter range)							

11.2.2.9 Subaddress 08h

Table 150. Sync control; 08h[7:0]

Bit	Description	Symbol	Value	Function
7	automatic field detection	AUFD	0	field state directly controlled via FSEL
			1	automatic field detection; **recommended setting**
6	field selection; active if AUFD = 0	FSEL	0	50 Hz, 625 lines
			1	60 Hz, 525 lines
5	forced ODD/EVEN toggle	FOET	0	ODD/EVEN signal toggles only with interlaced source
			1	ODD/EVEN signal toggles fieldwise even if source is non-interlaced

Table 150. Sync control; 08h[7:0] *…continued*

Bit	Description	Symbol	Value	Function
4 and 3	horizontal time constant selection	HTC[1:0]	00	TV mode, recommended for poor quality TV signals only; do not use for new applications
			01	VTR mode, recommended if a deflection control circuit is directly connected to the SAA7108AE; SAA7109AE
			10	reserved
			11	fast locking mode; **recommended setting**
2	horizontal PLL	HPLL	0	PLL closed
			1	PLL open; horizontal frequency fixed
1 and 0	vertical noise reduction	VNOI[1:0]	00	normal mode; **recommended setting**
			01	fast mode, applicable for stable sources only; automatic field detection (AUFD) **must** be disabled
			10	free running mode
			11	vertical noise reduction bypassed

11.2.2.10 Subaddress 09h

Table 151. Luminance control; 09h[7:0]

Bit	Description	Symbol	Value	Function
7	chrominance trap/comb filter bypass	BYPS	0	chrominance trap or luminance comb filter active; default for CVBS mode
			1	chrominance trap or luminance comb filter bypassed; default for S-video mode
6	adaptive luminance comb filter	YCOMB	0	disabled (= chrominance trap enabled, if BYPS = 0)
			1	active, if BYPS = 0
5	processing delay in non comb filter mode	LDEL	0	processing delay is equal to internal pipe-lining delay
			1	one (NTSC standards) or two (PAL standards) video lines additional processing delay
4	remodulation bandwidth for luminance; see Figure 22 to Figure 25	LUBW	0	small remodulation bandwidth (narrow chrominance notch ⇒ higher luminance bandwidth)
			1	large remodulation bandwidth (wider chrominance notch ⇒ smaller luminance bandwidth)

Table 151. Luminance control; 09h[7:0] *…continued*

Bit	Description	Symbol	Value	Function
3 to 0	sharpness control, luminance filter characteristic; see Figure 26	LUFI[3:0]	0001	resolution enhancement filter 8.0 dB at 4.1 MHz
			0010	resolution enhancement filter 6.8 dB at 4.1 MHz
			0011	resolution enhancement filter 5.1 dB at 4.1 MHz
			0100	resolution enhancement filter 4.1 dB at 4.1 MHz
			0101	resolution enhancement filter 3.0 dB at 4.1 MHz
			0110	resolution enhancement filter 2.3 dB at 4.1 MHz
			0111	resolution enhancement filter 1.6 dB at 4.1 MHz
			0000	plain
			1000	low-pass filter 2 dB at 4.1 MHz
			1001	low-pass filter 3 dB at 4.1 MHz
			1010	low-pass filter 3 dB at 3.3 MHz; 4 dB at 4.1 MHz
			1011	low-pass filter 3 dB at 2.6 MHz; 8 dB at 4.1 MHz
			1100	low-pass filter 3 dB at 2.4 MHz; 14 dB at 4.1 MHz
			1101	low-pass filter 3 dB at 2.2 MHz; notch at 3.4 MHz
			1110	low-pass filter 3 dB at 1.9 MHz; notch at 3.0 MHz
			1111	low-pass filter 3 dB at 1.7 MHz; notch at 2.5 MHz

11.2.2.11 Subaddress 0Ah

Table 152. Luminance brightness control: decoder part; 0Ah[7:0]

Offset	Control bits 7 to 0							
	DBRI7	DBRI6	DBRI5	DBRI4	DBRI3	DBRI2	DBRI1	DBRI0
255 (bright)	1	1	1	1	1	1	1	1
128 (ITU level)	1	0	0	0	0	0	0	0
0 (dark)	0	0	0	0	0	0	0	0

11.2.2.12 Subaddress 0Bh

Table 153. Luminance contrast control: decoder part; 0Bh[7:0]

Gain	Control bits 7 to 0							
	DCON7	DCON6	DCON5	DCON4	DCON3	DCON2	DCON1	DCON0
1.984 (maximum)	0	1	1	1	1	1	1	1
1.063 (ITU level)	0	1	0	0	0	1	0	0
1.0	0	1	0	0	0	0	0	0
0 (luminance off)	0	0	0	0	0	0	0	0
–1 (inverse luminance)	1	1	0	0	0	0	0	0
–2 (inverse luminance)	1	0	0	0	0	0	0	0

11.2.2.13 Subaddress 0Ch

Table 154. Chrominance saturation control: decoder part; 0Ch[7:0]

Gain	Control bits 7 to 0							
	DSAT7	DSAT6	DSAT5	DSAT4	DSAT3	DSAT2	DSAT1	DSAT0
1.984 (maximum)	0	1	1	1	1	1	1	1
1.0 (ITU level)	0	1	0	0	0	0	0	0
0 (color off)	0	0	0	0	0	0	0	0
–1 (inverse chrominance)	1	1	0	0	0	0	0	0
–2 (inverse chrominance)	1	0	0	0	0	0	0	0

11.2.2.14 Subaddress 0Dh

Table 155. Chrominance hue control; 0Dh[7:0]

Hue phase (deg)	Control bits 7 to 0							
	HUEC7	HUEC6	HUEC5	HUEC4	HUEC3	HUEC2	HUEC1	HUEC0
+178.6...	0	1	1	1	1	1	1	1
...0...	0	0	0	0	0	0	0	0
...–180	1	0	0	0	0	0	0	0

11.2.2.15 Subaddress 0Eh

Table 156. Chrominance control 1; 0Eh[7:0]

Bit	Description	Symbol	Value	Function
7	clear DTO	CDTO	0	disabled
			1	Every time CDTO is set, the internal subcarrier DTO phase is reset to 0° and the RTCO output generates a logic 0 at time slot 68 (see document *"How to use Real Time Control (RTC)"*, available on request). So an identical subcarrier phase can be generated by an external device (e.g. an encoder); if a DTO reset is programmed via CDTO it has always to be executed in the following order: 1. Set CDTO = 0 2. Set CDTO = 1
6 to 4	color standard selection	CSTD[2:0]	000	50 Hz/625 lines: PAL BGDHI (4.43 MHz)
				60 Hz/525 lines: NTSC M (3.58 MHz)
			001	50 Hz/625 lines: NTSC 4.43 (50 Hz)
				60 Hz/525 lines: PAL 4.43 (60 Hz)
			010	50 Hz/625 lines: combination-PAL N (3.58 MHz)
				60 Hz/525 lines: NTSC 4.43 (60 Hz)
			011	50 Hz/625 lines: NTSC N (3.58 MHz)
				60 Hz/525 lines: PAL M (3.58 MHz)
			100	50 Hz/625 lines: reserved
				60 Hz/525 lines: NTSC-Japan (3.58 MHz)
			101	50 Hz/625 lines: SECAM
				60 Hz/525 lines: reserved
			110	reserved; **do not use**
			111	reserved; **do not use**
3	disable chrominance vertical filter and PAL phase error correction	DCVF	0	chrominance vertical filter and PAL phase error correction on (during active video lines)
			1	chrominance vertical filter and PAL phase error correction permanently off
2	fast color time constant	FCTC	0	nominal time constant
			1	fast time constant for special applications (high quality input source, fast chroma lock required, automatic standard detection off)
0	adaptive chrominance comb filter	CCOMB	0	disabled
			1	active

11.2.2.16 Subaddress 0Fh

Table 157. Chrominance gain control; 0Fh[7:0]

Bit	Description	Symbol	Value	Function
7	automatic chrominance gain control	ACGC	0	on
			1	programmable gain via CGAIN6 to CGAIN0; need to be set for SECAM standard
6 to 0	chrominance gain value (if ACGC is set to logic 1)	CGAIN[6:0]	000 0000	minimum gain (0.5)
			010 0100	nominal gain (1.125)
			111 1111	maximum gain (7.5)

11.2.2.17 Subaddress 10h

Table 158. Chrominance control 2; 10h[7:0]

Bit	Description	Symbol	Value	Function
7 and 6	fine offset adjustment B – Y component	OFFU[1:0]	00	0 LSB
			01	1/4 LSB
			10	1/2 LSB
			11	3/4 LSB
5 and 4	fine offset adjustment R – Y component	OFFV[1:0]	00	0 LSB
			01	1/4 LSB
			10	1/2 LSB
			11	3/4 LSB
3	chrominance bandwidth; see Figure 20 and Figure 21	CHBW	0	small
			1	wide
2 to 0	combined luminance and chrominance bandwidth adjustment; see Figure 20 to Figure 26	LCBW[2:0]	000	smallest chrominance bandwidth and largest luminance bandwidth
			...	... to ...
			111	largest chrominance bandwidth and smallest luminance bandwidth

11.2.2.18 Subaddress 11h

Table 159. Mode/delay control; 11h[7:0]

Bit	Description	Symbol	Value	Function
7	color on	COLO	0	automatic color killer enabled
			1	color forced on
6	polarity of RTS1 output signal	RTP1	0	non-inverted
			1	inverted
5 and 4	fine position of HS (steps in 2/LLC)	HDEL[1:0]	00	0
			01	1
			10	2
			11	3

Table 159. Mode/delay control; 11h[7:0] *…continued*

Bit	Description	Symbol	Value	Function
3	polarity of RTS0 output signal	RTP0	0	non-inverted
			1	inverted
2 to 0	luminance delay compensation (steps in 2/LLC)	YDEL[2:0]	100	–4...
			000	...0...
			011	...3

11.2.2.19 Subaddress 12h

Table 160. RT signal control: RTS0 output; 12h[3:0]

The polarity of any signal on RTS0 can be inverted via RTP0[11h[3]].

RTS0 output	RTSE03	RTSE02	RTSE01	RTSE00
3-state	0	0	0	0
Constant LOW	0	0	0	1
CREF (13.5 MHz toggling pulse; see Figure 35)	0	0	1	0
CREF2 (6.75 MHz toggling pulse; see Figure 35)	0	0	1	1
HL; horizontal lock indicator[1]: HL = 0: unlocked HL = 1: locked	0	1	0	0
VL; vertical and horizontal lock: VL = 0: unlocked VL = 1: locked	0	1	0	1
DL; vertical and horizontal lock and color detected: DL = 0: unlocked DL = 1: locked	0	1	1	0
Reserved	0	1	1	1
HREF, horizontal reference signal; indicates 720 pixels valid data on the expansion port. The positive slope marks the beginning of a new active line. HREF is also generated during the vertical blanking interval (see Figure 35).	1	0	0	0
HS: Programmable width in LLC8 steps via HSB[7:0] 06h[7:0] and HSS[7:0] 07h[7:0] Fine position adjustment in LLC2 steps via HDEL[1:0] 11h[5:4] (see Figure 35)	1	0	0	1
HQ; HREF gated with VGATE	1	0	1	0
Reserved	1	0	1	1
V123; vertical sync (see vertical timing diagrams Figure 33 and Figure 34)	1	1	0	0
VGATE; programmable via VSTA[8:0] 17h[0] 15h[7:0], VSTO[8:0] 17h[1] 16h[7:0] and VGPS[17h[2]]	1	1	0	1
LSBs of the 9-bit ADCs	1	1	1	0
FID; position programmable via VSTA[8:0] 17h[0] 15h[7:0] (see vertical timing diagrams Figure 33 and Figure 34)	1	1	1	1

[1] Function of HL is selectable via HLSEL[13h[3]]:
a) HLSEL = 0: HL is standard horizontal lock indicator.
b) HLSEL = 1: HL is fast horizontal lock indicator (use is not recommended for sources with unstable timebase e.g. VCRs).

Table 161. RT signal control: RTS1 output; 12h[7:4]

The polarity of any signal on RTS1 can be inverted via RTP1[11h[6]].

RTS1 output	RTSE13	RTSE12	RTSE11	RTSE10
3-state	0	0	0	0
Constant LOW	0	0	0	1
CREF (13.5 MHz toggling pulse; see Figure 35)	0	0	1	0
CREF2 (6.75 MHz toggling pulse; see Figure 35)	0	0	1	1
HL; horizontal lock indicator[1]: HL = 0: unlocked HL = 1: locked	0	1	0	0
VL; vertical and horizontal lock: VL = 0: unlocked VL = 1: locked	0	1	0	1
DL; vertical and horizontal lock and color detected: DL = 0: unlocked DL = 1: locked	0	1	1	0
Reserved	0	1	1	1
HREF, horizontal reference signal; indicates 720 pixels valid data on the expansion port. The positive slope marks the beginning of a new active line. HREF is also generated during the vertical blanking interval (see Figure 35).	1	0	0	0
HS: Programmable width in LLC8 steps via HSB[7:0] 06h[7:0] and HSS[7:0] 07h[7:0] Fine position adjustment in LLC2 steps via HDEL[1:0] 11h[5:4] (see Figure 35)	1	0	0	1
HQ; HREF gated with VGATE	1	0	1	0
Reserved	1	0	1	1
V123; vertical sync (see vertical timing diagrams Figure 33 and Figure 34)	1	1	0	0
VGATE; programmable via VSTA[8:0] 17h[0] 15h[7:0], VSTO[8:0] 17h[1] 16h[7:0] and VGPS[17h[2]]	1	1	0	1
Reserved	1	1	1	0
FID; position programmable via VSTA[8:0] 17h[0] 15h[7:0] (see vertical timing diagrams Figure 33 and Figure 34)	1	1	1	1

[1] Function of HL is selectable via HLSEL[13h[3]]:
a) HLSEL = 0: HL is standard horizontal lock indicator.
b) HLSEL = 1: HL is fast horizontal lock indicator (use is not recommended for sources with unstable timebase e.g. VCRs).

11.2.2.20 Subaddress 13h

Table 162. RT/X port output control; 13h[7:0]

Bit	Description	Symbol	Value	Function
7	RTCO output enable	RTCE	0	3-state
			1	enabled
6	X port XRH output selection	XRHS	0	HREF (see Figure 35)
			1	HS: Programmable width in LLC8 steps via HSB[7:0] 06h[7:0] and HSS[7:0] 07h[7:0] Fine position adjustment in LLC2 steps via HDEL[1:0] 11h[5:4] (see Figure 35)
5 and 4	X port XRV output selection	XRVS[1:0]	00	V123 (see Figure 33 and Figure 34)
			01	ITU 656 related field ID (see Figure 33 and Figure 34)
			10	inverted V123
			11	inverted ITU 656 related field ID
3	horizontal lock indicator selection	HLSEL	0	copy of inverted HLCK status bit (default)
			1	fast horizontal lock indicator (for special applications only)
2 to 0	XPD7 to XPD0 (port output format selection); see Section 10.4	OFTS[2:0]	000	ITU 656
			001	ITU 656-like format with modified field blanking according to VGATE position (programmable via VSTA[8:0] 17h[0] 15h[7:0], VSTO[8:0] 17h[1] 16h[7:0] and VGPS[17h[2]])
			010	Y-C_B-C_R 4 : 2 : 2 8-bit format (no SAV/EAV codes inserted)
			011	reserved
			100	multiplexed AD2/AD1 bypass (bits 8 to 1) dependent on mode settings (see Section 11.2.2.3); if both ADCs are selected AD2 is output at CREF = 1 and AD1 is output at CREF = 0
			101	multiplexed AD2/AD1 bypass (bits 7 to 0) dependent on mode settings (see Section 11.2.2.3); if both ADCs are selected AD2 is output at CREF = 1 and AD1 is output at CREF = 0
			110	reserved
			111	multiplexed ADC MSB/LSB bypass dependent on mode settings; only one ADC should be selected at a time; ADx8 to ADx1 are outputs at CREF = 1 and ADx7 to ADx0 are outputs at CREF = 0

11.2.2.21 Subaddress 14h

Table 163. Analog/ADC/compatibility control; 14h[7:0]

Bit	Description	Symbol	Value	Function
7	compatibility bit for SAA7199	CM99	0	off (default)
			1	on (to be set **only** if SAA7199 is used for re-encoding **in conjunction with RTCO active**)
6	update time interval for AGC value	UPTCV	0	horizontal update (once per line)
			1	vertical update (once per field)
5 and 4	analog test select	AOSL[1:0]	00	AOUT connected to internal test point 1
			01	AOUT connected to input AD1
			10	AOUT connected to input AD2
			11	AOUT connected to internal test point 2
3	XTOUTd output enable	XTOUTE	0	pin P4 (XTOUTd) 3-stated
			1	pin P4 (XTOUTd) enabled
2	decoder status byte selection; see Table 169	OLDSB	0	standard
			1	backward compatibility to SAA7112
1 and 0	ADC sample clock phase delay	APCK[1:0]	00	application dependent
			01	application dependent
			10	application dependent
			11	application dependent

11.2.2.22 Subaddress 15h

Table 164. VGATE start; FID polarity change; 17h[0] and 15h[7:0]

Start of VGATE pulse (LOW-to-HIGH transition) and polarity change of FID pulse, VGPS = 0; see Figure 33 and Figure 34.

Field		Frame line counting	Decimal value	MSB 17h[0]	Control bits 7 to 0							
				VSTA8	VSTA7	VSTA6	VSTA5	VSTA4	VSTA3	VSTA2	VSTA1	VSTA0
50 Hz	1st	1	312	1	0	0	1	1	1	0	0	0
	2nd	314										
	1st	2	0...	0	0	0	0	0	0	0	0	0
	2nd	315										
	1st	312	...310	1	0	0	1	1	0	1	1	1
	2nd	625										
60 Hz	1st	4	262	1	0	0	0	0	0	1	1	0
	2nd	267										
	1st	5	0...	0	0	0	0	0	0	0	0	0
	2nd	268										
	1st	265	...260	1	0	0	0	0	0	1	0	1
	2nd	3										

11.2.2.23 Subaddress 16h

Table 165. VGATE stop; 17h[1] and 16h[7:0]

Stop of VGATE pulse (HIGH-to-LOW transition), VGPS = 0; see Figure 33 and Figure 34.

Field		Frame line counting	Decimal value	MSB 17h[1]	Control bits 7 to 0							
				VSTO8	VSTO7	VSTO6	VSTO5	VSTO4	VSTO3	VSTO2	VSTO1	VSTO0
50 Hz	1st	1	312	1	0	0	1	1	1	0	0	0
	2nd	314										
	1st	2	0...	0	0	0	0	0	0	0	0	0
	2nd	315										
	1st	312	...310	1	0	0	1	1	0	1	1	1
	2nd	625										
60 Hz	1st	4	262	1	0	0	0	0	0	1	1	0
	2nd	267										
	1st	5	0...	0	0	0	0	0	0	0	0	0
	2nd	268										
	1st	265	...260	1	0	0	0	0	0	1	0	1
	2nd	3										

11.2.2.24 Subaddress 17h

Table 166. Miscellaneous/VGATE MSBs; 17h[7:6] and 17h[2:0]

Bit	Description	Symbol	Value	Function
7	LLC output enable	LLCE	0	enable
			1	3-state
6	LLC2 output enable	LLC2E	0	enable
			1	3-state
2	alternative VGATE position	VGPS	0	VGATE position according to Table 164 and Table 165
			1	VGATE occurs one line earlier during field 2
1	MSB VGATE stop	VSTO8	see Table 165	
0	MSB VGATE start	VSTA8	see Table 164	

11.2.2.25 Subaddress 18h

Table 167. Raw data gain control; RAWG[7:0] 18h[7:0]; see Figure 28

Gain	Control bits 7 to 0							
	RAWG7	RAWG6	RAWG5	RAWG4	RAWG3	RAWG2	RAWG1	RAWG0
255 (double amplitude)	0	1	1	1	1	1	1	1
128 (nominal level)	0	1	0	0	0	0	0	0
0 (off)	0	0	0	0	0	0	0	0

11.2.2.26 Subaddress 19h

Table 168. Raw data offset control; RAWO[7:0] 19h[7:0]; see Figure 28

Offset	Control bits 7 to 0							
	RAWO7	RAWO6	RAWO5	RAWO4	RAWO3	RAWO2	RAWO1	RAWO0
−128 LSB	0	0	0	0	0	0	0	0
0 LSB	1	0	0	0	0	0	0	0
+128 LSB	1	1	1	1	1	1	1	1

11.2.2.27 Subaddress 1Fh

Table 169. Status byte video decoder; 1Fh[7:0]; read only register

Bit	Description	I²C-bus control bit	OLDSB 14h[2]	Value	Function
7	status bit for interlace detection	INTL	-	0	non-interlaced
				1	interlaced
6	status bit for horizontal and vertical loop	HLVLN	0	0	both loops locked
				1	unlocked
	status bit for locked horizontal frequency	HLCK	1	0	locked
				1	unlocked
5	identification bit for detected field frequency	FIDT	-	0	50 Hz
				1	60 Hz
4	gain value for active luminance channel is limited; maximum (top)	GLIMT	-	0	not active
				1	active
3	gain value for active luminance channel is limited; minimum (bottom)	GLIMB	-	0	not active
				1	active
2	white peak loop is activated	WIPA	-	0	not active
				1	active
1	copy protected source detected according to Macrovision version up to 7.01	COPRO	0	0	not active
				1	active
	slow time constant active in WIPA mode	SLTCA	1	0	not active
				1	active
0	ready for capture (all internal loops locked)	RDCAP	0	0	not active
				1	active
	color signal in accordance with selected standard has been detected	CODE	1	0	not active
				1	active

11.2.3 Programming register audio clock generation

See equations in Section 9.6 and examples in Table 35 and Table 36.

11.2.3.1 Subaddresses 30h to 32h

Table 170. Audio master clock (AMCLK) cycles per field

Subaddress	Control bits 7 to 0							
30h	ACPF7	ACPF6	ACPF5	ACPF4	ACPF3	ACPF2	ACPF1	ACPF0
31h	ACPF15	ACPF14	ACPF13	ACPF12	ACPF11	ACPF10	ACPF9	ACPF8
32h	-	-	-	-	-	-	ACPF17	ACPF16

11.2.3.2 Subaddresses 34h to 36h

Table 171. Audio master clock (AMCLK) nominal increment

Subaddress	Control bits 7 to 0							
34h	ACNI7	ACNI6	ACNI5	ACNI4	ACNI3	ACNI2	ACNI1	ACNI0
35h	ACNI15	ACNI14	ACNI13	ACNI12	ACNI11	ACNI10	ACNI9	ACNI8
36h	-	-	ACNI21	ACNI20	ACNI19	ACNI18	ACNI17	ACNI16

11.2.3.3 Subaddress 38h

Table 172. Clock ratio audio master clock (AMXCLK) to serial bit clock (ASCLK)

Subaddress	Control bits 7 to 0							
38h	-	-	SDIV5	SDIV4	SDIV3	SDIV2	SDIV1	SDIV0

11.2.3.4 Subaddress 39h

Table 173. Clock ratio serial bit clock (ASCLK) to channel select clock (ALRCLK)

Subaddress	Control bits 7 to 0							
39h	-	-	LRDIV5	LRDIV4	LRDIV3	LRDIV2	LRDIV1	LRDIV0

11.2.3.5 Subaddress 3Ah

Table 174. Audio clock control; 3Ah[3:0]

Bit	Description	Symbol	Value	Function
3	audio PLL modes	APLL	0	PLL active, AMCLK is field-locked
			1	PLL open, AMCLK is free-running
2	audio master clock vertical reference	AMVR	0	vertical reference pulse is taken from internal decoder
			1	vertical reference is taken from XRV input (expansion port)
1	ALRCLK phase	LRPH	0	ALRCLK edges triggered by falling edges of ASCLK
			1	ALRCLK edges triggered by rising edges of ASCLK
0	ASCLK phase	SCPH	0	ASCLK edges triggered by falling edges of AMCLK
			1	ASCLK edges triggered by rising edges of AMCLK

11.2.4 Programming register VBI data slicer

11.2.4.1 Subaddress 40h

Table 175. Slicer control 1; 40h[6:4]

Bit	Description	Symbol	Value	Function
6	Hamming check	HAM_N	0	**Hamming check for 2 bytes after framing code, dependent on data type (default)**
			1	no Hamming check
5	framing code error	FCE	0	one framing code error allowed
			1	no framing code errors allowed
4	amplitude searching	HUNT_N	0	amplitude searching active (default)
			1	amplitude searching stopped

11.2.4.2 Subaddresses 41h to 57h

Table 176. Line control register; LCR2 to LCR24 (41h to 57h)

See Section 9.2 and Section 9.4.

Name	Description	Framing code	Bits 7 to 4 (41h to 57h)	Bits 3 to 0 (41h to 57h)
			DT[3:0] 62h[3:0] (field 1)	DT[3:0] 62h[3:0] (field 2)
WST625	teletext EuroWST, CCST	27h	0000	0000
CC625	European closed caption	001	0001	0001
VPS	video programming service	9951h	0010	0010
WSS	wide screen signalling bits	1E 3C1Fh	0011	0011
WST525	US teletext (WST)	27h	0100	0100
CC525	US closed caption (line 21)	001	0101	0101
Test line	video component signal, VBI region	-	0110	0110
Intercast	raw data	-	0111	0111
General text	teletext	programmable	1000	1000
VITC625	VITC/EBU time codes (Europe)	programmable	1001	1001
VITC525	VITC/SMPTE time codes (USA)	programmable	1010	1010
Reserved	reserved	-	1011	1011
NABTS	US NABTS	-	1100	1100
Japtext	MOJI (Japanese)	programmable (A7h)	1101	1101
JFS	Japanese format switch (L20/22)	programmable	1110	1110
Active video	**video component signal, active video region (default)**	-	1111	1111

11.2.4.3 Subaddress 58h

Table 177. Programmable framing code; slicer set 58h[7:0]; see Table 28 and Table 176

Framing code for programmable data types	Control bits 7 to 0
Default value	FC[7:0] = 40h

11.2.4.4 Subaddress 59h

Table 178. Horizontal offset for slicer; slicer set 59h and 5Bh

Horizontal offset	Control bits 5Bh[2:0]	Control bits 59h[7:0]
Recommended value	HOFF[10:8] = 3h	HOFF[7:0] = 47h

11.2.4.5 Subaddress 5Ah

Table 179. Vertical offset for slicer; slicer set 5Ah and 5Bh

Vertical offset	Control bit 5Bh[4]	Control bits 5Ah[7:0]
	VOFF8	VOFF[7:0]
Minimum value 0	0	00h
Maximum value 312	1	38h
Value for 50 Hz 625 lines input	0	03h
Value for 60 Hz 525 lines input	0	06h

11.2.4.6 Subaddress 5Bh

Table 180. Field offset, and MSBs for horizontal and vertical offsets; slicer set 5Bh[7:6]
See Section 11.2.4.4 and Section 11.2.4.5 for HOFF[10:8] 5Bh[2:0] and VOFF8[5Bh[4]].

Bit	Description	Symbol	Value	Function
7	field offset	FOFF	0	no modification of internal field indicator (default for 50 Hz 625 lines input sources)
			1	invert field indicator (default for 60 Hz 525 lines input sources)
6	recode	RECODE	0	**leave data unchanged (default)**
			1	convert 00h and FFh data bytes into 03h and FCh

11.2.4.7 Subaddress 5Dh

Table 181. Header and data identification (DID; ITU 656) code control; slicer set 5Dh[7:0]

Bit	Description	Symbol	Value	Function
7	field ID and V-blank selection for text output (F and V reference selection)	FVREF	0	F and V output of slicer is LCR table dependent
			1	F and V output is taken from decoder real-time signals EVEN_ITU and VBLNK_ITU
5 to 0	**default; DID[5:0] = 00h**	DID[5:0]	00 0000	**ANC header framing**; see Figure 42 and Table 34
	special cases of DID programming		11 1110	DID[5:0] = 3Eh SAV/EAV framing, with FVREF = 1
			11 1111	DID[5:0] = 3Fh SAV/EAV framing, with FVREF = 0

11.2.4.8 Subaddress 5Eh

Table 182. Sliced data identification (SDID) code; slicer set 5Eh[5:0]

Bit	Description	Symbol	Value	Function
5 to 0	SDID codes	SDID[5:0]	00h	**default**

11.2.4.9 Subaddress 60h

Table 183. Slicer status byte 0; 60h[6:2]; read only register

Bit	Description	Symbol	Value	Function
6	framing code valid	FC8V	0	no framing code (0 error) in the last frame detected
			1	framing code with 0 error detected
5	framing code valid	FC7V	0	no framing code (1 error) in the last frame detected
			1	framing code with 1 error detected
4	VPS valid	VPSV	0	no VPS in the last frame
			1	VPS detected
3	PALplus valid	PPV	0	no PALplus in the last frame
			1	PALplus detected
2	closed caption valid	CCV	0	no closed caption in the last frame
			1	closed caption detected

11.2.4.10 Subaddresses 61h and 62h

Table 184. Slicer status byte 1; 61h[5:0] and slicer status byte 2; 62h[7:0]; read only registers

Subaddress	Bit	Symbol	Description
61h	5	F21_N	field ID as seen by the VBI slicer; for field 1: bit 5 = 0
	4 to 0	LN[8:4]	line number
62h	7 to 4	LN[3:0]	line number
	3 to 0	DT[3:0]	data type; according to Table 28

11.2.5 Programming register interfaces and scaler part

11.2.5.1 Subaddress 80h

Table 185. Global control 1; global set 80h[6:4][1]

SWRST moved to subaddress 88h[5].

Task enable control	Control bits 6 to 4		
	SMOD	TEB	TEA
Task of register set A is disabled	X	X	0
Task of register set A is enabled	X	X	1
Task of register set B is disabled	X	0	X
Task of register set B is enabled	X	1	X
The scaler window defines the F and V timing of the scaler output	0	X	X
VBI data slicer defines the F and V timing of the scaler output	1	X	X

[1] X = don't care.

Table 186. Global control 1; global set 80h[3:0][1]

I port and scaler back-end clock selection	Control bits 3 to 0			
	ICKS3	ICKS2	ICKS1	ICKS0
ICLK output and back-end clock is line-locked clock LLC from decoder	X	X	0	0
ICLK output and back-end clock is XCLK from X port	X	X	0	1
ICLK output is LLC and back-end clock is LLC2 clock	X	X[2]	1	0
Back-end clock is the ICLK input	X	X	1	1
IDQ pin carries the data qualifier	X	0	X	X
IDQ pin carries a gated back-end clock (IDQ AND CLK)	X	1	X	X
IDQ generation only for valid data	0	X	X	X
IDQ qualifies valid data inside the scaling region and all data outside the scaling region	1	X	X	X

[1] X = don't care.

[2] Although the ICLK I/O is independent of ICKS2 and ICKS3, this selection can only be used if ICKS2 = 1.

11.2.5.2 Subaddresses 83h to 87h

Table 187. X port I/O enable and output clock phase control; global set 83h[5:4]

Output clock phase control	Control bits 5 and 4	
	XPCK1	XPCK0
XCLK default output phase, recommended value	0	0
XCLK output inverted	0	1
XCLK phase shifted by approximately 3 ns	1	0
XCLK output inverted and shifted by approximately 3 ns	1	1

Table 188. X port I/O enable and output clock phase control; global set 83h[2:0][1]

X port I/O enable	Control bits 2 to 0		
	XRQT	XPE1	XPE0
X port output is disabled by software	X	0	0
X port output is enabled by software	X	0	1
X port output is enabled by pin XTRI at logic 0	X	1	0
X port output is enabled by pin XTRI at logic 1	X	1	1
XRDY output signal is A/B task flag from event handler (A = 1)	0	X	X
XRDY output signal is ready signal from scaler path (XRDY = 1 means the SAA7108AE; SAA7109AE is ready to receive data)	1	X	X

[1] X = don't care.

Table 189. I port signal definitions; global set 84h[7:6] and 86h[5]

I port signal definitions	Control bits		
	86h[5]	84h[7:6]	
	IDG02	IDG01	IDG00
IGP0 is output field ID, as defined by OFIDC[90h[6]]	0	0	0
IGP0 is A/B task flag, as defined by CONLH[90h[7]]	0	0	1
IGP0 is sliced data flag, framing the sliced VBI data at the I port	0	1	0
IGP0 is set to logic 0 (default polarity)	0	1	1
IGP0 is the output FIFO almost filled flag	1	0	0
IGP0 is the output FIFO overflow flag	1	0	1
IGP0 is the output FIFO almost full flag, level to be programmed in subaddress 86h	1	1	0
IGP0 is the output FIFO almost empty flag, level to be programmed in subaddress 86h	1	1	1

Table 190. I port signal definitions; global set 84h[5:4] and 86h[4]

I port signal definitions	Control bits		
	86h[4]	84h[5:4]	
	IDG12	IDG11	IDG10
IGP1 is output field ID, as defined by OFIDC[90h[6]]	0	0	0
IGP1 is A/B task flag, as defined by CONLH[90h[7]]	0	0	1
IGP1 is sliced data flag, framing the sliced VBI data at the I port	0	1	0
IGP1 is set to logic 0 (default polarity)	0	1	1
IGP1 is the output FIFO almost filled flag	1	0	0
IGP1 is the output FIFO overflow flag	1	0	1
IGP1 is the output FIFO almost full flag, level to be programmed in subaddress 86h	1	1	0
IGP1 is the output FIFO almost empty flag, level to be programmed in subaddress 86h	1	1	1

Table 191. I port output signal definitions; global set 84h[3:0][1]

I port output signal definitions	Control bits 3 to 0			
	IDV1	IDV0	IDH1	IDH0
IGPH is a H gate signal, framing the scaler output	X	X	0	0
IGPH is an extended H gate (framing H gate during scaler output and scaler input H reference outside the scaler window)	X	X	0	1
IGPH is a horizontal trigger pulse, on active going edge of H gate	X	X	1	0
IGPH is a horizontal trigger pulse, on active going edge of extended H gate	X	X	1	1
IGPV is a V gate signal, framing scaled output lines	0	0	X	X
IGPV is the V reference signal from scaler input	0	1	X	X
IGPV is a vertical trigger pulse, derived from V gate	1	0	X	X
IGPV is a vertical trigger pulse derived from input V reference	1	1	X	X

[1] X = don't care.

Table 192. X port signal definitions text slicer; global set 85h[7:5][1]

X port signal definitions text slicer	Control bits 7 to 5		
	ISWP1	ISWP0	ILLV
Video data limited to range 1 to 254	X	X	0
Video data limited to range 8 to 247	X	X	1
Double word byte swap, influences serial output timing D0 D1 D2 D3 ⇒ FF 00 00 SAV C_B0 Y0 C_R0 Y1	0	0	X
D1 D0 D3 D2 ⇒ 00 FF SAV 00 Y0 C_B0 Y1 C_R0	0	1	X
D2 D3 D0 D1 ⇒ 00 SAV FF 00 C_R0 Y1 C_B0 Y0	1	0	X
D3 D2 D1 D0 ⇒ SAV 00 00 FF Y1 C_R0 Y0 C_B0	1	1	X

[1] X = don't care.

Table 193. I port reference signal polarities; global set 85h[4:0][1]

I port reference signal polarities	Control bits 4 to 0				
	IG0P	IG1P	IRVP	IRHP	IDQP
IDQ at default polarity (1 = active)	X	X	X	X	0
IDQ is inverted	X	X	X	X	1
IGPH at default polarity (1 = active)	X	X	X	0	X
IGPH is inverted	X	X	X	1	X
IGPV at default polarity (1 = active)	X	X	0	X	X
IGPV is inverted	X	X	1	X	X
IGP1 at default polarity	X	0	X	X	X
IGP1 is inverted	X	1	X	X	X
IGP0 at default polarity	0	X	X	X	X
IGP0 is inverted	1	X	X	X	X

[1] X = don't care.

Table 194. I port FIFO flag control and arbitration; global set 86h[7:4][1]

Function	Control bits 7 to 4			
	VITX1	VITX0	IDG02	IDG12
See subaddress 84h: IDG11 and IDG10	X	X	X	0
	X	X	X	1
See subaddress 84h: IDG01 and IDG00	X	X	0	X
	X	X	1	X
I port signal definitions				
I port data output inhibited	0	0	X	X
Only video data is transferred	0	1	X	X
Only text data is transferred (no EAV, SAV will occur)	1	0	X	X
Text and video data is transferred, text has priority	1	1	X	X

[1] X = don't care.

Table 195. I port FIFO flag control and arbitration; global set 86h[3:0][1]

I port FIFO flag control and arbitration	Control bits 3 to 0			
	FFL1	FFL0	FEL1	FEL0
FAE FIFO flag almost empty level				
< 16 double words	X	X	0	0
< 8 double words	X	X	0	1
< 4 double words	X	X	1	0
0 double words	X	X	1	1
FAF FIFO flag almost full level				
≥ 16 double words	0	0	X	X
≥ 24 double words	0	1	X	X
≥ 28 double words	1	0	X	X
32 double words	1	1	X	X

[1] X = don't care.

Table 196. I port I/O enable, output clock and gated clock phase control; global set 87h[7:4][1]

Output clock and gated clock phase control	Control bits 7 to 4			
	IPCK3[2]	IPCK2[2]	IPCK1	IPCK0
ICLK default output phase	X	X	0	0
ICLK phase shifted by ½ clock cycle ⇒ recommended for ICKS1 = 1 and ICKS0 = 0 (subaddress 80h)	X	X	0	1
ICLK phase shifted by approximately 3 ns	X	X	1	0
ICLK phase shifted by ½ clock cycle + approximately 3 ns ⇒ alternatively to setting '01'	X	X	1	1
IDQ = gated clock default output phase	0	0	X	X
IDQ = gated clock phase shifted by ½ clock cycle ⇒ recommended for gated clock output	0	1	X	X
IDQ = gated clock phase shifted by approximately 3 ns	1	0	X	X
IDQ = gated clock phase shifted by ½ clock cycle + approximately 3 ns ⇒ alternatively to setting '01'	1	1	X	X

[1] X = don't care.

[2] IPCK3 and IPCK2 only affects the gated clock (subaddress 80h, bit ICKS2 = 1).

Table 197. I port I/O enable, output clock and gated clock phase control; global set 87h[1:0]

I port I/O enable	Control bits 1 and 0	
	IPE1	IPE0
I port output is disabled by software	0	0
I port output is enabled by software	0	1
I port output is enabled by pin ITRI at logic 0	1	0
I port output is enabled by pin ITRI at logic 1	1	1

11.2.5.3 Subaddress 88h

Table 198. Power save control; global set 88h[7:4][1]

Power save control	Control bits 7 to 4			
	CH4EN	CH2EN	SWRST[2]	DPROG
DPROG = 0 after reset	X	X	X	0
DPROG = 1 can be used to assign that the device has been programmed; this bit can be monitored in the scalers status byte, bit PRDON; if DPROG was set to logic 1 and PRDON status bit shows a logic 0, a power-up or start-up fail has occurred	X	X	X	1
Scaler path is reset to its idle state, software reset	X	X	0	X
Scaler is switched back to operation	X	X	1	X
AD1x analog channel is in Power-down mode	X	0	X	X
AD1x analog channel is active	X	1	X	X
AD2x analog channel is in Power-down mode	0	X	X	X
AD2x analog channel is active	1	X	X	X

[1] X = don't care.

[2] Bit SWRST is now located here.

Table 199. Power save control; global set 88h[3] and 88h[1:0][1]

Power save control	Control bits 3, 1 and 0		
	SLM3	SLM1	SLM0
Decoder and VBI slicer are in operational mode	X	X	0
Decoder and VBI slicer are in Power-down mode; scaler only operates, if scaler input and ICLK source is the X port (refer to subaddresses 80h and 91h/C1h)	X	X	1
Scaler is in operational mode	X	0	X
Scaler is in Power-down mode; scaler in power-down stops I port output	X	1	X
Audio clock generation active	0	X	X
Audio clock generation in power-down and output disabled	1	X	X

[1] X = don't care.

11.2.5.4 Subaddress 8Fh

Table 200. Status information scaler part; 8Fh[7:0]; read only register

Bit	I^2C-bus status bit	Function[1]
7	XTRI	status on input pin XTRI, if not used for 3-state control, usable as hardware flag for software use
6	ITRI	status on input pin ITRI, if not used for 3-state control, usable as hardware flag for software use
5	FFIL	status of the internal 'FIFO almost filled' flag
4	FFOV	status of the internal 'FIFO overflow' flag
3	PRDON	copy of bit DPROG, can be used to detect power-up and start-up fails

Table 200. Status information scaler part; 8Fh[7:0]; read only register *…continued*

Bit	I²C-bus status bit	Function[1]
2	ERROF	error flag of scalers output formatter, normally set, if the output processing needs to be interrupted, due to input/output data rate conflicts, e.g. if output data rate is much too low and all internal FIFO capacity used
1	FIDSCI	status of the field sequence ID at the scalers input
0	FIDSCO	status of the field sequence ID at the scalers output, scaler processing dependent

[1] Status information is unsynchronized and shows the actual status at the time of I²C-bus read.

11.2.5.5 Subaddresses 90h and C0h

Table 201. Task handling control; register set A [90h[7:6]] and B [C0h[7:6]][1]

Event handler control	Control bits 7 and 6	
	CONLH	OFIDC
Output field ID is field ID from scaler input	X	0
Output field ID is task status flag, which changes every time a selected task is activated (not synchronized to input field ID)	X	1
Scaler SAV/EAV byte bit 7 and task flag = 1, default	0	X
Scaler SAV/EAV byte bit 7 and task flag = 0	1	X

[1] X = don't care.

Table 202. Task handling control; register set A [90h[5:3]] and B [C0h[5:3]]

Event handler control	Control bits 5 to 3		
	FSKP2	FSKP1	FSKP0
Active task is carried out directly	0	0	0
1 field is skipped before active task is carried out	0	0	1
... fields are skipped before active task is carried out	...	...	...
6 fields are skipped before active task is carried out	1	1	0
7 fields are skipped before active task is carried out	1	1	1

Table 203. Task handling control; register set A [90h[2:0]] and B [C0h[2:0]][1]

Event handler control	Control bits 2 to 0		
	RPTSK	STRC1	STRC0
Event handler triggers immediately after finishing a task	X	0	0
Event handler triggers with next V-sync	X	0	1
Event handler triggers with field ID = 0	X	1	0
Event handler triggers with field ID = 1	X	1	1
If active task is finished, handling is taken over by the next task	0	X	X
Active task is repeated once, before handling is taken over by the next task	1	X	X

[1] X = don't care.

11.2.5.6 Subaddresses 91h to 93h

Table 204. X port formats and configuration; register set A [91h[7:3]] and B [C1h[7:3]][1]

Scaler input format and configuration source selection	Control bits 7 to 3				
	CONLV	HLDFV	SCSRC1	SCSRC0	SCRQE
Only if XRQT[83h[2]] = 1: scaler input source reacts on SAA7108AE; SAA7109AE request	X	X	X	X	0
Scaler input source is a continuous data stream, which cannot be interrupted (must be logic 1, if SAA7108AE; SAA7109AE decoder part is source of scaler or XRQT[83h[2]] = 0)	X	X	X	X	1
Scaler input source is data from decoder, data type is provided according to Table 28	X	X	0	0	X
Scaler input source is Y-C_B-C_R data from X port	X	X	0	1	X
Scaler input source is raw digital CVBS from selected analog channel, for backward compatibility only, further use is not recommended	X	X	1	0	X
Scaler input source is raw digital CVBS (or 16-bit Y + C_B-C_R, if no 16-bit outputs are active) from X port	X	X	1	1	X
SAV/EAV code bits 6 and 5 (F and V) may change between SAV and EAV	X	0	X	X	X
SAV/EAV code bits 6 and 5 (F and V) are synchronized to scalers output line start	X	1	X	X	X
SAV/EAV code bit 5 (V) and V gate on pin IGPV as generated by the internal processing; see Figure 48	0	X	X	X	X
SAV/EAV code bit 5 (V) and V gate are inverted	1	X	X	X	X

[1] X = don't care.

Table 205. X port formats and configuration; register set A [91h[2:0]] and B [C1h[2:0]][1]

Scaler input format and configuration format control	Control bits 2 to 0		
	FSC2[2]	FSC1[2]	FSC0
Input is Y-C_B-C_R 4 : 2 : 2 like sampling scheme	X	X	0
Input is Y-C_B-C_R 4 : 1 : 1 like sampling scheme	X	X	1
Chroma is provided every line, default	0	0	X
Chroma is provided every 2nd line	0	1	X
Chroma is provided every 3rd line	1	0	X
Chroma is provided every 4th line	1	1	X

[1] X = don't care.

[2] FSC2 and FSC1 only to be used if X port input source does not provide chroma information for every input line. X port input stream must contain dummy chroma bytes.

Table 206. X port input reference signal definitions; register set A [92h[7:4]] and B [C2h[7:4]][1]

X port input reference signal definitions	Control bits 7 to 4			
	XFDV	XFDH	XDV1	XDV0
Rising edge of XRV input and decoder V123 is vertical reference	X	X	X	0
Falling edge of XRV input and decoder V123 is vertical reference	X	X	X	1
XRV is a V-sync or V gate signal	X	X	0	X
XRV is a frame sync, V pulses are generated internally on both edges of FS input	X	X	1	X
X port field ID is state of XRH at reference edge on XRV (defined by XFDV)	X	0	X	X
Field ID (decoder and X port field ID) is inverted	X	1	X	X
Reference edge for field detection is falling edge of XRV	0	X	X	X
Reference edge for field detection is rising edge of XRV	1	X	X	X

[1] X = don't care.

Table 207. X port input reference signal definitions; register set A [92h[3:0]] and B [C2h[3:0]][1]

X port input reference signal definitions	Control bits 3 to 0			
	XCODE	XDH	XDQ	XCKS
XCLK input clock and XDQ input qualifier are needed	X	X	X	0
Data rate is defined by XCLK only, no XDQ signal used	X	X	X	1
Data are qualified at XDQ input at logic 1	X	X	0	X
Data are qualified at XDQ input at logic 0	X	X	1	X
Rising edge of XRH input is horizontal reference	X	0	X	X
Falling edge of XRH input is horizontal reference	X	1	X	X
Reference signals are taken from XRH and XRV	0	X	X	X
Reference signals are decoded from EAV and SAV	1	X	X	X

[1] X = don't care.

Table 208. I port output format and configuration; register set A [93h[7:5]] and B [C3h[7:5]][1]

I port output format and configuration	Control bits 7 to 5		
	ICODE	I8_16	FYSK
All lines will be output	X	X	0
Skip the number of leading Y only lines, as defined by FOI1 and FOI0	X	X	1
Double words are transferred byte wise, see subaddress 85h bits ISWP1 and ISWP0	X	0	X
Double words are transferred 16-bit word wise via IPD and HPD, see subaddress 85h bits ISWP1 and ISWP0	X	1	X
No ITU 656 like SAV/EAV codes are available	0	X	X
ITU 656 like SAV/EAV codes are inserted in the output data stream, framed by a qualifier	1	X	X

[1] X = don't care.

Table 209. I port output format and configuration; register set A [93h[4:0]] and B [C3h[4:0]][1]

I port output format and configuration	Control bits 4 to 0				
	FOI1	FOI0	FSI2	FSI1	FSI0
4 : 2 : 2 double word formatting	X	X	0	0	0
4 : 1 : 1 double word formatting	X	X	0	0	1
4 : 2 : 0, only every 2nd line Y + C_B-C_R output, in between Y only output	X	X	0	1	0
4 : 1 : 0, only every 4th line Y + C_B-C_R output, in between Y only output	X	X	0	1	1
Y only	X	X	1	0	0
Not defined	X	X	1	0	1
Not defined	X	X	1	1	0
Not defined	X	X	1	1	1
No leading Y only line, before 1st Y + C_B-C_R line is output	0	0	X	X	X
1 leading Y only line, before 1st Y + C_B-C_R line is output	0	1	X	X	X
2 leading Y only lines, before 1st Y + C_B-C_R line is output	1	0	X	X	X
3 leading Y only lines, before 1st Y + C_B-C_R line is output	1	1	X	X	X

[1] X = don't care.

11.2.5.7 Subaddresses 94h to 9Bh

Table 210. Horizontal input window start; register set A [94h[7:0]; 95h[3:0]] and B [C4h[7:0]; C5h[3:0]]

Horizontal input acquisition window definition offset in X (horizontal) direction[1]	Control bits											
	A [95h[3:0]] and B [C5h[3:0]]				A [94h[7:0]] and B [C4h[7:0]]							
	XO11	XO10	XO9	XO8	XO7	XO6	XO5	XO4	XO3	XO2	XO1	XO0
A minimum of 2 should be kept, due to a line counting mismatch	0	0	0	0	0	0	0	0	0	0	1	0
Odd offsets are changing the C_B-C_R sequence in the output stream to C_R-C_B sequence	0	0	0	0	0	0	0	0	0	0	1	1
Maximum possible pixel offset = 4095	1	1	1	1	1	1	1	1	1	1	1	1

[1] Reference for counting are luminance samples.

Table 211. Horizontal input window length; register set A [96h[7:0]; 97h[3:0]] and B [C6h[7:0]; C7h[3:0]]

Horizontal input acquisition window definition input window length in X (horizontal) direction[1]	Control bits											
	A [97h[3:0]] and B [C7h[3:0]]				A [96h[7:0]] and B [C6h[7:0]]							
	XS11	XS10	XS9	XS8	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0
No output	0	0	0	0	0	0	0	0	0	0	0	0
Odd lengths are allowed, but will be rounded up to even lengths	0	0	0	0	0	0	0	0	0	0	0	1
Maximum possible number of input pixels = 4095	1	1	1	1	1	1	1	1	1	1	1	1

[1] Reference for counting are luminance samples.

Table 212. Vertical input window start; register set A [98h[7:0]; 99h[3:0]] and B [C8h[7:0]; C9h[3:0]]

Vertical input acquisition window definition offset in Y (vertical) direction[1]	Control bits											
	A [99h[3:0]] and B [C9h[3:0]]				A [98h[7:0]] and B [C8h[7:0]]							
	YO11	YO10	YO9	YO8	YO7	YO6	YO5	YO4	YO3	YO2	YO1	YO0
Line offset = 0	0	0	0	0	0	0	0	0	0	0	0	0
Line offset = 1	0	0	0	0	0	0	0	0	0	0	0	1
Maximum line offset = 4095	1	1	1	1	1	1	1	1	1	1	1	1

[1] For trigger condition: STRC[1:0] 90h[1:0] = 00; YO + YS > (number of input lines per field – 2), will result in field dropping. Other trigger conditions: YO > (number of input lines per field – 2), will result in field dropping.

Table 213. Vertical input window length; register set A [9Ah[7:0]; 9Bh[3:0]] and B [CAh[7:0]; CBh[3:0]]

Vertical input acquisition window definition input window length in Y (vertical) direction[1]	Control bits											
	A [9Bh[3:0]] and B [CBh[3:0]]				A [9Ah[7:0]] and B [CAh[7:0]]							
	YS11	YS10	YS9	YS8	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0
No input lines	0	0	0	0	0	0	0	0	0	0	0	0
1 input line	0	0	0	0	0	0	0	0	0	0	0	1
Maximum possible number of input lines = 4095	1	1	1	1	1	1	1	1	1	1	1	1

[1] For trigger condition: STRC[1:0] 90h[1:0] = 00; YO + YS > (number of input lines per field – 2), will result in field dropping. Other trigger conditions: YS > (number of input lines per field – 2), will result in field dropping.

11.2.5.8 Subaddresses 9Ch to 9Fh

Table 214. Horizontal output window length; register set A [9Ch[7:0]; 9Dh[3:0]] and B [CCh[7:0]; CDh[3:0]]

Horizontal output acquisition window definition number of desired output pixels in X (horizontal) direction[1]	Control bits											
	A [9Dh[3:0]] and B [CDh[3:0]]				A [9Ch[7:0]] and B [CCh[7:0]]							
	XD11	XD10	XD9	XD8	XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0
No output	0	0	0	0	0	0	0	0	0	0	0	0
Odd lengths are allowed, but will be filled up to even lengths	0	0	0	0	0	0	0	0	0	0	0	1
Maximum possible number of input pixels = 4095[2]	1	1	1	1	1	1	1	1	1	1	1	1

[1] Reference for counting are luminance samples.

[2] If the desired output length is greater than the number of scaled output pixels, the last scaled pixel is repeated.

Table 215. Vertical output window length; register set A [9Eh[7:0]; 9Fh[3:0]] and B [CEh[7:0]; CFh[3:0]]

Vertical output acquisition window definition number of desired output lines in Y (vertical) direction	Control bits											
	A [9Fh[3:0]] and B [CFh[3:0]]				A [9Eh[7:0]] and B [CEh[7:0]]							
	YD11	YD10	YD9	YD8	YD7	YD6	YD5	YD4	YD3	YD2	YD1	YD0
No output	0	0	0	0	0	0	0	0	0	0	0	0
1 pixel	0	0	0	0	0	0	0	0	0	0	0	1
Maximum possible number of output lines = 4095[1]	1	1	1	1	1	1	1	1	1	1	1	1

[1] If the desired output length is greater than the number of scaled output lines, the processing is cut.

11.2.5.9 Subaddresses A0h to A2h

Table 216. Horizontal prescaling; register set A [A0h[5:0]] and B [D0h[5:0]]

Horizontal integer prescaling ratio (XPSC)	Control bits 5 to 0					
	XPSC5	XPSC4	XPSC3	XPSC2	XPSC1	XPSC0
Not allowed	0	0	0	0	0	0
Downscale = 1	0	0	0	0	0	1
Downscale = $\frac{1}{2}$	0	0	0	0	1	0
...	...	...	...	...	...	...
Downscale = $\frac{1}{63}$	1	1	1	1	1	1

Table 217. Accumulation length; register set A [A1h[5:0]] and B [D1h[5:0]]

Horizontal prescaler accumulation sequence length (XACL)	Control bits 5 to 0					
	XACL5	XACL4	XACL3	XACL2	XACL1	XACL0
Accumulation length = 1	0	0	0	0	0	0
Accumulation length = 2	0	0	0	0	0	1
...	...	...	...	...	...	...
Accumulation length = 64	1	1	1	1	1	1

Table 218. Prescaler DC gain and FIR prefilter control; register set A [A2h[7:4]] and B [D2h[7:4]][1]

FIR prefilter control	Control bits 7 to 4			
	PFUV1	PFUV0	PFY1	PFY0
Luminance FIR filter bypassed	X	X	0	0
H_y(z) = $\frac{1}{4}$ (1 2 1)	X	X	0	1
H_y(z) = $\frac{1}{8}$ (–1 1 1.75 4.5 1.75 1 –1)	X	X	1	0
H_y(z) = $\frac{1}{8}$ (1 2 2 2 1)	X	X	1	1
Chrominance FIR filter bypassed	0	0	X	X
H_uv(z) = $\frac{1}{4}$ (1 2 1)	0	1	X	X
H_uv(z) = $\frac{1}{32}$ (3 8 10 8 3)	1	0	X	X
H_uv(z) = $\frac{1}{8}$ (1 2 2 2 1)	1	1	X	X

[1] X = don't care.

Table 219. Prescaler DC gain and FIR prefilter control; register set A [A2h[3:0]] and B [D2h[3:0]][1]

Prescaler DC gain	Control bits 3 to 0			
	XC2_1	XDCG2	XDCG1	XDCG0
Prescaler output is renormalized by gain factor = 1	X	0	0	0
Prescaler output is renormalized by gain factor = $\frac{1}{2}$	X	0	0	1
Prescaler output is renormalized by gain factor = $\frac{1}{4}$	X	0	1	0
Prescaler output is renormalized by gain factor = $\frac{1}{8}$	X	0	1	1
Prescaler output is renormalized by gain factor = $\frac{1}{16}$	X	1	0	0
Prescaler output is renormalized by gain factor = $\frac{1}{32}$	X	1	0	1
Prescaler output is renormalized by gain factor = $\frac{1}{64}$	X	1	1	0

Table 219. Prescaler DC gain and FIR prefilter control; register set A [A2h[3:0]] and B [D2h[3:0]][1] *…continued*

Prescaler DC gain	Control bits 3 to 0			
	XC2_1	XDCG2	XDCG1	XDCG0
Prescaler output is renormalized by gain factor = $^{1}/_{128}$	X	1	1	1
Weighting of all accumulated samples is factor ‘1’; e.g. XACL = 4 ⇒ sequence 1 + 1 + 1 + 1 + 1	0	X	X	X
Weighting of samples inside sequence is factor ‘2’; e.g. XACL = 4 ⇒ sequence 1 + 2 + 2 + 2 + 1	1	X	X	X

[1] X = don’t care.

11.2.5.10 Subaddresses A4h to A6h

Table 220. Luminance brightness control; register set A [A4h[7:0]] and B [D4h[7:0]]

Luminance brightness control	Control bits 7 to 0							
	BRIG7	BRIG6	BRIG5	BRIG4	BRIG3	BRIG2	BRIG1	BRIG0
Value = 0	0	0	0	0	0	0	0	0
Nominal value = 128	1	0	0	0	0	0	0	0
Value = 255	1	1	1	1	1	1	1	1

Table 221. Luminance contrast control; register set A [A5h[7:0]] and B [D5h[7:0]]

Luminance contrast control	Control bits 7 to 0							
	CONT7	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0
Gain = 0	0	0	0	0	0	0	0	0
Gain = $^{1}/_{64}$	0	0	0	0	0	0	0	1
Nominal gain = 64	0	1	0	0	0	0	0	0
Gain = $^{127}/_{64}$	0	1	1	1	1	1	1	1

Table 222. Chrominance saturation control; register set A [A6h[7:0]] and B [D6h[7:0]]

Chrominance saturation control	Control bits 7 to 0							
	SATN7	SATN6	SATN5	SATN4	SATN3	SATN2	SATN1	SATN0
Gain = 0	0	0	0	0	0	0	0	0
Gain = $^{1}/_{64}$	0	0	0	0	0	0	0	1
Nominal gain = 64	0	1	0	0	0	0	0	0
Gain = $^{127}/_{64}$	0	1	1	1	1	1	1	1

11.2.5.11 Subaddresses A8h to AEh

Table 223. Horizontal luminance scaling increment; register set A [A8h[7:0]; A9h[7:0]] and B [D8h[7:0]; D9h[7:0]]

Horizontal luminance scaling increment	Control bits			
	A [A9h[7:4]] B [D9h[7:4]]	A [A9h[3:0]] B [D9h[3:0]]	A [A8h[7:4]] B [D8h[7:4]]	A [A8h[3:0]] B [D8h[3:0]]
	XSCY[15:12][1]	XSCY[11:8]	XSCY[7:4]	XSCY[3:0]
Scale = $^{1024}/_{1}$ (theoretical) zoom	0000	0000	0000	0000
Scale = $^{1024}/_{294}$, lower limit defined by data path structure	0000	0001	0010	0110
Scale = $^{1024}/_{1023}$ zoom	0000	0011	1111	1111
Scale = 1, equals 1024	0000	0100	0000	0000
Scale = $^{1024}/_{1025}$ downscale	0000	0100	0000	0001
Scale = $^{1024}/_{8191}$ downscale	0001	1111	1111	1111

[1] Bits XSCY[15:13] are reserved and are set to logic 0.

Table 224. Horizontal luminance phase offset; register set A [AAh[7:0]] and B [DAh[7:0]]

Horizontal luminance phase offset	Control bits 7 to 0							
	XPHY7	XPHY6	XPHY5	XPHY4	XPHY3	XPHY2	XPHY1	XPHY0
Offset = 0	0	0	0	0	0	0	0	0
Offset = $^{1}/_{32}$ pixel	0	0	0	0	0	0	0	1
Offset = $^{32}/_{32}$ = 1 pixel	0	0	1	0	0	0	0	0
Offset = $^{255}/_{32}$ pixel	1	1	1	1	1	1	1	1

Table 225. Horizontal chrominance scaling increment; register set A [ACh[7:0]; ADh[7:0]] and B [DCh[7:0]; DDh[7:0]]

Horizontal chrominance scaling increment	Control bits			
	A [ADh[7:4]] B [DDh[7:4]]	A [ADh[3:0]] B [DDh[3:0]]	A [ACh[7:4]] B [DCh[7:4]]	A [ACh[3:0]] B [DCh[3:0]]
	XSCC[15:12][1]	XSCC[11:8]	XSCC[7:4]	XSCC[3:0]
This value must be set to the luminance value $^{1}/_{2}$XSCY[15:0]	0000	0000	0000	0000
	0000	0000	0000	0001
	0001	1111	1111	1111

[1] Bits XSCC[15:13] are reserved and are set to logic 0.

Table 226. Horizontal chrominance phase offset; register set A [AEh[7:0]] and B [DEh[7:0]]

Horizontal chrominance phase offset	Control bits 7 to 0							
	XPHC7	XPHC6	XPHC5	XPHC4	XPHC3	XPHC2	XPHC1	XPHC0
This value must be set to $^{1}/_{2}$XPHY[7:0]	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	1
	1	1	1	1	1	1	1	1

11.2.5.12 Subaddresses B0h to BFh

Table 227. Vertical luminance scaling increment; register set A [B0h[7:0]; B1h[7:0]] and B [E0h[7:0]; E1h[7:0]]

Vertical luminance scaling increment	Control bits			
	A [B1h[7:4]] B [E1h[7:4]]	A [B1h[3:0]] B [E1h[3:0]]	A [B0h[7:4]] B [E0h[7:4]]	A [B0h[3:0]] B [E0h[3:0]]
	YSCY[15:12]	YSCY[11:8]	YSCY[7:4]	YSCY[3:0]
Scale = $^{1024}/_{1}$ (theoretical) zoom	0000	0000	0000	0001
Scale = $^{1024}/_{1023}$ zoom	0000	0011	1111	1111
Scale = 1, equals 1024	0000	0100	0000	0000
Scale = $^{1024}/_{1025}$ downscale	0000	0100	0000	0001
Scale = $^{1}/_{63.999}$ downscale	1111	1111	1111	1111

Table 228. Vertical chrominance scaling increment; register set A [B2h[7:0]; B3h[7:0]] and B [E2h[7:0]; E3h[7:0]]

Vertical chrominance scaling increment	Control bits			
	A [B3h[7:4]] B [E3h[7:4]]	A [B3h[3:0]] B [E3h[3:0]]	A [B2h[7:4]] B [E2h[7:4]]	A [B2h[3:0]] B [E2h[3:0]]
	YSCC[15:12]	YSCC[11:8]	YSCC[7:4]	YSCC[3:0]
This value must be set to the luminance value YSCY[15:0]	0000	0000	0000	0001
	1111	1111	1111	1111

Table 229. Vertical scaling mode control; register set A [B4h[4 and 0]] and B [E4h[4 and 0]][1]

Vertical scaling mode control	Control bits 4 and 0	
	YMIR	YMODE
Vertical scaling performs linear interpolation between lines	X	0
Vertical scaling performs higher order accumulating interpolation, better alias suppression	X	1
No mirroring	0	X
Lines are mirrored	1	X

[1] X = don't care.

Table 230. Vertical chrominance phase offset '00'; register set A [B8h[7:0]] and B [E8h[7:0]]

Vertical chrominance phase offset	Control bits 7 to 0							
	YPC07	YPC06	YPC05	YPC04	YPC03	YPC02	YPC01	YPC00
Offset = 0	0	0	0	0	0	0	0	0
Offset = $^{32}/_{32}$ = 1 line	0	0	1	0	0	0	0	0
Offset = $^{255}/_{32}$ lines	1	1	1	1	1	1	1	1

Table 231. Vertical luminance phase offset '00'; register set A [BCh[7:0]] and B [ECh[7:0]]

Vertical luminance phase offset	Control bits 7 to 0							
	YPY07	YPY06	YPY05	YPY04	YPY03	YPY02	YPY01	YPY00
Offset = 0	0	0	0	0	0	0	0	0
Offset = $^{32}/_{32}$ = 1 line	0	0	1	0	0	0	0	0
Offset = $^{255}/_{32}$ lines	1	1	1	1	1	1	1	1

12. Programming start setup of digital video decoder part

12.1 Decoder part

The given values force the following behavior of the SAA7108AE; SAA7109AE decoder part:

- The analog input AI11 expects an NTSC M, PAL B, D, G, H and I or SECAM signal in CVBS format; analog anti-alias filter and AGC active
- Automatic field detection enabled
- Standard ITU 656 output format enabled on expansion (X) port
- Contrast, brightness and saturation control in accordance with ITU standards
- Adaptive comb filter for luminance and chrominance activated
- Pins LLC, LLC2, XTOUTd, RTS0, RTS1 and RTCO are set to 3-state

Table 232. Decoder part start setup values for the three main standards

Subaddress (hexadecimal)	Register function	Bit name[1]	Values (hexadecimal)		
			NTSC M	PAL B, D, G, H and I	SECAM
00	chip version	ID7 to ID4	read only		
01	increment delay	X, X, X, X, IDEL3 to IDEL0	08	08	08
02	analog input control 1	FUSE1, FUSE0, GUDL1, GUDL0 and MODE3 to MODE0	C0	C0	C0
03	analog input control 2	X, HLNRS, VBSL, WPOFF, HOLDG, GAFIX, GAI28 and GAI18	10	10	10
04	analog input control 3	GAI17 to GAI10	90	90	90
05	analog input control 4	GAI27 to GAI20	90	90	90
06	horizontal sync start	HSB7 to HSB0	EB	EB	EB
07	horizontal sync stop	HSS7 to HSS0	E0	E0	E0
08	sync control	AUFD, FSEL, FOET, HTC1, HTC0, HPLL, VNOI1 and VNOI0	98	98	98
09	luminance control	BYPS, YCOMB, LDEL, LUBW and LUFI3 to LUFI0	40	40	1B
0A	luminance brightness control	DBRI7 to DBRI0	80	80	80
0B	luminance contrast control	DCON7 to DCON0	44	44	44
0C	chrominance saturation control	DSAT7 to DSAT0	40	40	40
0D	chrominance hue control	HUEC7 to HUEC0	00	00	00
0E	chrominance control 1	CDTO, CSTD2 to CSTD0, DCVF, FCTC, X and CCOMB	89	81	D0

Table 232. Decoder part start setup values for the three main standards *…continued*

Subaddress (hexadecimal)	Register function	Bit name[1]	Values (hexadecimal)		
			NTSC M	PAL B, D, G, H and I	SECAM
0F	chrominance gain control	ACGC and CGAIN6 to CGAIN0	2A	2A	80
10	chrominance control 2	OFFU1, OFFU0, OFFV1, OFFV0, CHBW and LCBW2 to LCBW0	0E	06	00
11	mode/delay control	COLO, RTP1, HDEL1, HDEL0, RTP0 and YDEL2 to YDEL0	00	00	00
12	RT signal control	RTSE13 to RTSE10 and RTSE03 to RTSE00	00	00	00
13	RT/X port output control	RTCE, XRHS, XRVS1, XRVS0, HLSEL and OFTS2 to OFTS0	00	00	00
14	analog/ADC/compatibility control	CM99, UPTCV, AOSL1, AOSL0, XTOUTE, OLDSB, APCK1 and APCK0	00	00	00
15	VGATE start, FID change	VSTA7 to VSTA0	11	11	11
16	VGATE stop	VSTO7 to VSTO0	FE	FE	FE
17	miscellaneous, VGATE configuration and MSBs	LLCE, LLC2E, X, X, X, VGPS, VSTO8 and VSTA8	40	40	40
18	raw data gain control	RAWG7 to RAWG0	40	40	40
19	raw data offset control	RAWO7 to RAWO0	80	80	80
1A to 1E	reserved	X, X, X, X, X, X, X, X	00	00	00
1F	status byte video decoder (OLDSB = 0)	INTL, HLVLN, FIDT, GLIMT, GLIMB, WIPA, COPRO and RDCAP	read only		

[1] All X values must be set to logic 0.

12.2 Audio clock generation part

The given values force the following behavior of the SAA7108AE; SAA7109AE audio clock generation part:

- Used crystal is 24.576 MHz
- Expected field frequency is 59.94 Hz (e.g. NTSC M standard)
- Generated audio master clock frequency at pin AMCLK is 256 kHz × 44.1 kHz = 11.2896 MHz
- AMCLK is externally connected to AMXCLK (short-cut between pins K12 and J12)
- ASCLK = 32 kHz × 44.1 kHz = 1.4112 MHz
- ALRCLK is 44.1 kHz

Table 233. Audio clock part setup values

Subaddress (hexadecimal)	Register function	Bit name[1]	Values (binary)								Start (hexadecimal)
			7	6	5	4	3	2	1	0	
30	audio master clock cycles per field; bits 7 to 0	ACPF7 to ACPF0	1	0	1	1	1	1	0	0	BC
31	audio master clock cycles per field; bits 15 to 8	ACPF15 to ACPF8	1	1	0	1	1	1	1	1	DF
32	audio master clock cycles per field; bits 17 and 16	X, X, X, X, X, ACPF17 and ACPF16	0	0	0	0	0	0	1	0	02
33	reserved	X, X, X, X, X, X, X, X	0	0	0	0	0	0	0	0	00
34	audio master clock nominal increment; bits 7 to 0	ACNI7 to ACNI0	1	1	0	0	1	1	0	1	CD
35	audio master clock nominal increment; bits 15 to 8	ACNI15 to ACNI8	1	1	0	0	1	1	0	0	CC
36	audio master clock nominal increment; bits 21 to 16	X, X, ACNI21 to ACNI16	0	0	1	1	1	0	1	0	3A
37	reserved	X, X, X, X, X, X, X, X	0	0	0	0	0	0	0	0	00
38	clock ratio AMXCLK to ASCLK	X, X, SDIV5 to SDIV0	0	0	0	0	0	0	1	1	03
39	clock ratio ASCLK to ALRCLK	X, X, LRDIV5 to LRDIV0	0	0	0	1	0	0	0	0	10
3A	audio clock generator basic setup	X, X, X, X, APLL, AMVR, LRPH, SCPH	0	0	0	0	0	0	0	0	00
3B to 3F	reserved	X, X, X, X, X, X, X, X	0	0	0	0	0	0	0	0	00

[1] All X values must be set to logic 0.

12.3 Data slicer and data type control part

The given values force the following behavior of the SAA7108AE; SAA7109AE VBI data slicer part:

- Closed captioning data are expected at line 21 of field 1 (60 Hz/525 line system)
- All other lines are processed as active video
- Sliced data are framed by ITU 656 like SAV/EAV sequence (DID[5:0] = 3Eh ⇒ MSB of SAV/EAV = 1)

Table 234. Data slicer start setup values

Subaddress (hexadecimal)	Register function	Bit name[1]	Values (binary)								Start (hexadecimal)
			7	6	5	4	3	2	1	0	
40	slicer control 1	X, HAM_N, FCE, HUNT_N, X, X, X, X	0	1	0	0	0	0	0	0	40
41 to 53	line control register 2 to 20	LCRn_7 to LCRn_0 (n = 2 to 20)	1	1	1	1	1	1	1	1	FF
54	line control register 21	LCR21_7 to LCR21_0	0	1	0	1	1	1	1	1	5F
55 to 57	line control register	LCRn_7 to LCRn_0 (n = 22 to 24)	1	1	1	1	1	1	1	1	FF
58	programmable framing code	FC7 to FC0	0	0	0	0	0	0	0	0	00
59	horizontal offset for slicer	HOFF7 to HOFF0	0	1	0	0	0	1	1	1	47
5A	vertical offset for slicer	VOFF7 to VOFF0	0	0	0	0	0	1	1	0	06[2]

Table 234. Data slicer start setup values *…continued*

Subaddress (hexadecimal)	Register function	Bit name[1]	Values (binary)								Start (hexadecimal)
			7	6	5	4	3	2	1	0	
5B	field offset and MSBs for horizontal and vertical offset	FOFF, RECODE, X, VOFF8, X, HOFF10 to HOFF8	1	0	0	0	0	0	1	1	83[2]
5C	reserved	X, X, X, X, X, X, X, X	0	0	0	0	0	0	0	0	00
5D	header and data identification code control	FVREF, X, DID5 to DID0	0	0	1	1	1	1	1	0	3E
5E	sliced data identification code	X, X, SDID5 to SDID0	0	0	0	0	0	0	0	0	00
5F	reserved	X, X, X, X, X, X, X, X	0	0	0	0	0	0	0	0	00
60	slicer status byte 0	-, FC8V, FC7V, VPSV, PPV, CCV, -, -	read only register								
61	slicer status byte 1	-, -, F21_N, LN8 to LN4	read only register								
62	slicer status byte 2	LN3 to LN0, DT3 to DT0	read only register								

[1] All X values must be set to logic 0.

[2] Changes for 50 Hz/625 line systems: subaddress 5Ah = 03h and subaddress 5Bh = 03h.

12.4 Scaler and interfaces

Table 235 shows some examples for the scaler programming with:

- prsc = prescale ratio
- fisc = fine scale ratio
- vsc = vertical scale ratio

The ratio is defined as: $\frac{number\ of\ input\ pixel}{number\ of\ output\ pixel}$

In the following settings the VBI data slicer is inactive. To activate the VBI data slicer, VITX[1:0] 86h[7:6] has to be set to ‘11’. Depending on the VBI data slicer settings, the sliced VBI data is inserted after the end of the scaled video lines, if the regions of VBI data slicer and scaler overlaps.

To compensate the running-in of the vertical scaler, the vertical input window lengths are extended by 2 lines to 290 lines, respectively 242 lines for XS, but the scaler increment calculations are done with 288 lines, respectively 240 lines.

12.4.1 Trigger condition

For trigger condition STRC[1:0] 90h[1:0] not equal ‘00’.

If the value of (YO + YS) is greater than or equal to 262 (NTSC), respectively 312 (PAL) the output field rate is reduced to 30 Hz, respectively 25 Hz.

Horizontal and vertical offsets (XO and YO) have to be used to adjust the displayed video in the display window. As this adjustment is application dependent, the listed values are only dummy values.

12.4.2 Maximum zoom factor

The maximum zoom factor is dependent on the back-end data rate and therefore back-end clock and data format dependent (8-bit or 16-bit output). The maximum horizontal zoom is limited to approximately 3.5, due to internal data path restrictions.

12.4.3 Examples

Table 235. Example of configurations

See settings in Table 236.

Example number	Scaler source and reference events	Input window	Output window	Scale ratios
1	analog input to 8-bit I port output, with SAV/EAV codes, 8-bit serial byte stream decoder output at X port; acquisition trigger at falling edge vertical and rising edge horizontal reference signal; H and V gates on IGPH and IGPV, IGP0 = VBI sliced data flag, IGP1 = FIFO almost full, level ≥ 24, IDQ qualifier logic 1 active	720 × 240	720 × 240	prsc = 1; fisc = 1; vsc = 1
2	analog input to 16-bit output, without SAV/EAV codes, Y on I port, C_B-C_R on H port and decoder output at X port; acquisition trigger at falling edge vertical and rising edge horizontal reference signal; H and V pulses on IGPH and IGPV, output FID on IGP0, IGP1 fixed to logic 1, IDQ qualifier logic 0 active	704 × 288	768 × 288	prsc = 1; fisc = 0.91667; vsc = 1
3	X port input 8 bit with SAV/EAV codes, no reference signals on XRH and XRV, XCLK as gated clock; field detection and acquisition trigger on different events; acquisition triggers at rising edge vertical and rising edge horizontal reference signal; I port output 8-bit with SAV/EAV codes like example number 1	720 × 240	352 × 288	prsc = 2; fisc = 1.022; vsc = 0.8333
4	X port and H port for 16-bit Y-C_B-C_R 4 : 2 : 2 input (if no 16-bit output selected); XRH and XRV as references; field detection and acquisition trigger at falling edge vertical and rising edge horizontal reference signal; I port output 8-bit with SAV/EAV codes, but Y only output	720 × 288	200 × 80	prsc = 2; fisc = 1.8; vsc = 3.6

Table 236. Scaler and interface configuration example

I²C-bus address (hex)	Main functionality	Example 1		Example 2		Example 3		Example 4	
		Hex	Dec	Hex	Dec	Hex	Dec	Hex	Dec
Global settings									
80	task enable, IDQ and back-end clock definition	10	-	10	-	10	-	10	-
83	XCLK output phase and X port output enable	01	-	01	-	00	-	00	-
84	IGPH, IGPV, IGP0 and IGP1 output definition	A0	-	C5	-	A0	-	A0	-
85	signal polarity control and I port byte swapping	10	-	09	-	10	-	10	-
86	FIFO flag thresholds and video/text arbitration	45	-	40	-	45	-	45	-
87	ICLK and IDQ output phase and I port enable	01	-	01	-	01	-	01	-
88	power save control and software reset	F0	-	F0	-	F0	-	F0	-
Task A: scaler input configuration and output format settings									
90	task handling	00	-	00	-	00	-	00	-
91	scaler input source and format definition	08	-	08	-	18	-	38	-
92	reference signal definition at scaler input	10	-	10	-	10	-	10	-
93	I port output formats and configuration	80	-	40	-	80	-	84	-
Input and output window definition									
94	horizontal input offset (XO)	10	16	10	16	10	16	10	16
95		00	-	00	-	00	-	00	-
96	horizontal input (source) window length (XS)	D0	720	C0	704	D0	720	D0	720
97		02	-	02	-	02	-	02	-
98	vertical input offset (YO)	0A	10	0A	10	0A	10	0A	10
99		00	-	00	-	00	-	00	-
9A	vertical input (source) window length (YS)	F2	242	22	290	F2	242	22	290
9B		00	-	01	-	00	-	01	-
9C	horizontal output (destination) window length (XD)	D0	720	00	768	60	352	C8	200
9D		02	-	03	-	01	-	00	-
9E	vertical output (destination) window length (YD)	F0	240	20	288	20	288	50	80
9F		00	-	01	-	01	-	00	-
Prefiltering and prescaling									
A0	integer prescale (value ‘00’ not allowed)	01	-	01	-	02	-	02	-
A1	accumulation length for prescaler	00	-	00	-	02	-	03	-
A2	FIR prefilter and prescaler DC normalization	00	-	00	-	AA	-	F2	-

Table 236. Scaler and interface configuration example *…continued*

I²C-bus address (hex)	Main functionality	Example 1		Example 2		Example 3		Example 4	
		Hex	Dec	Hex	Dec	Hex	Dec	Hex	Dec
A4	scaler brightness control	80	128	80	128	80	128	80	128
A5	scaler contrast control	40	64	40	64	40	64	11	17
A6	scaler saturation control	40	64	40	64	40	64	11	17
Horizontal phase scaling									
A8	horizontal scaling increment for luminance	00	1024	AA	938	18	1048	34	1844
A9		04	-	03	-	04	-	07	-
AA	horizontal phase offset luminance	00	-	00	-	00	-	00	-
AC	horizontal scaling increment for chrominance	00	512	D5	469	0C	524	9A	922
AD		02	-	01	-	02	-	03	-
AE	horizontal phase offset chrominance	00	-	00	-	00	-	00	-
Vertical scaling									
B0	vertical scaling increment for luminance	00	1024	00	1024	55	853	66	3686
B1		04	-	04	-	03	-	0E	-
B2	vertical scaling increment for chrominance	00	1024	00	1024	55	853	66	3686
B3		04	-	04	-	03	-	0E	-
B4	vertical scaling mode control	00	-	00	-	00	-	01	-
B8 to BF	vertical phase offsets luminance and chrominance (need to be used for interlace correct scaled output)	start with B8h to BFh at 00h, if there are no problems with the interlaced scaled output optimize according to Section 9.3.3.2							

13. Limiting values

Table 237. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All ground pins connected together and grounded (0 V); all supply pins connected together.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DDD}	digital supply voltage			–0.5	+4.6	V
V_{DDA}	analog supply voltage			–0.5	+4.6	V
$V_{i(A)}$	input voltage at analog inputs			–0.5	+4.6	V
$V_{i(n)}$	input voltage at pins XTALI, SDA and SCL			–0.5	V_{DDD} + 0.5	V
$V_{i(D)}$	input voltage at digital inputs or I/O pins	outputs in 3-state		–0.5	+4.6	V
		outputs in 3-state	[1]	–0.5	+5.5	V
ΔV_{SS}	voltage difference between $V_{SSA(n)}$ and $V_{SSE(n)}$ or $V_{SSI(n)}$			-	100	mV
T_{stg}	storage temperature			–65	+150	°C
T_{amb}	ambient temperature			0	70	°C
V_{esd}	electrostatic discharge voltage	human body model	[2]	-	±2000	V
		machine model	[3]	-	±150	V

[1] Condition for maximum voltage at digital inputs or I/O pins: 3.0 V < V_{DDD} < 3.6 V.

[2] Class 2 according to JESD22-A114D.

[3] Class A according to EIA/JESD22-A115-A.

14. Thermal characteristics

Table 238. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	32[1]	K/W

[1] The overall $R_{th(j-a)}$ value can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$ all power and ground pins must be connected to the power and ground layers directly. An ample copper area directly under the SAA7108AE; SAA7109AE with a number of through-hole plating, connected to the ground layer (four-layer board: second layer), can also reduce the effective $R_{th(j-a)}$. Please do not use any solder-stop varnish under the chip. In addition the usage of soldering glue with a high thermal conductance after curing is recommended.

15. Characteristics

Table 239. Characteristics of the digital video encoder part

T_{amb} = 0 °C to 70 °C (typical values measured at T_{amb} = 25 °C); unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DDA}	analog supply voltage			3.15	3.3	3.45	V
V_{DDIe}	digital supply voltage			3.15	3.3	3.45	V
$V_{DD(DVO)}$	digital supply voltage (DVO)			1.045	1.1	1.155	V
				1.425	1.5	1.575	V
				1.71	1.8	1.89	V
				2.375	2.5	2.625	V
				3.135	3.3	3.465	V
I_{DDA}	analog supply current		[1]	1	110	115	mA
I_{DDD}	digital supply current		[2]	1	175	200	mA
Inputs							
V_{IL}	LOW-level input voltage	$V_{DD(DVO)}$ = 1.1 V, 1.5 V, 1.8 V or 2.5 V	[3]	−0.1	-	+0.2	V
		$V_{DD(DVO)}$ = 3.3 V	[3]	−0.5	-	+0.8	V
		pins $\overline{RESe}$, TMSe, TCKe, $\overline{TRSTe}$ and TDIe		−0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage	$V_{DD(DVO)}$ = 1.1 V, 1.5 V, 1.8 V or 2.5 V	[3]	$V_{DD(DVO)}$ − 0.2	-	$V_{DD(DVO)}$ + 0.1	V
		$V_{DD(DVO)}$ = 3.3 V	[3]	2	-	$V_{DD(DVO)}$ + 0.3	V
		pins $\overline{RESe}$, TMSe, TCKe, $\overline{TRSTe}$ and TDIe		2	-	V_{DDIe} + 0.3	V
I_{LI}	input leakage current			-	-	10	µA
C_i	input capacitance	clocks		-	-	10	pF
		data		-	-	10	pF
		I/Os at high-impedance		-	-	10	pF
Outputs							
V_{OL}	LOW-level output voltage	$V_{DD(DVO)}$ = 1.1 V, 1.5 V, 1.8 V or 2.5 V	[3]	0	-	0.1	V
		$V_{DD(DVO)}$ = 3.3 V	[3]	0	-	0.4	V
		pins TDOe, TTXRQ_XCLKO2, VSM and HSM_CSYNC		0	-	0.4	V
V_{OH}	HIGH-level output voltage	$V_{DD(DVO)}$ = 1.1 V, 1.5 V, 1.8 V or 2.5 V	[3]	$V_{DD(DVO)}$ − 0.1	-	$V_{DD(DVO)}$	V
		$V_{DD(DVO)}$ = 3.3 V	[3]	2.4	-	$V_{DD(DVO)}$	V
		pins TDOe, TTXRQ_XCLKO2, VSM and HSM_CSYNC		2.4	-	V_{DDIe}	V

Table 239. Characteristics of the digital video encoder part *...continued*

T_{amb} = 0 °C to 70 °C (typical values measured at T_{amb} = 25 °C); unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I²C-bus; pins SDAe and SCLe							
V_{IL}	LOW-level input voltage			–0.5	-	$+0.3V_{DDIe}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DDIe}$	-	V_{DDIe} + 0.3	V
I_i	input current	V_i = LOW or HIGH		–10	-	+10	µA
V_{OL}	LOW-level output voltage (pin SDAe)	I_{OL} = 3 mA		-	-	0.4	V
I_o	output current	during acknowledge		3	-	-	mA
Clock timing; pins PIXCLKI and PIXCLKO							
T_{PIXCLK}	cycle time		[4]	12	-	-	ns
$t_{d(CLKD)}$	delay from PIXCLKO to PIXCLKI		[5]	-	-	-	ns
δ	duty factor	t_{HIGH}/T_{PIXCLK}	[4]	40	50	60	%
		t_{HIGH}/T_{CLKO2}; output		40	50	60	%
t_r	rise time		[4]	-	-	1.5	ns
t_f	fall time		[4]	-	-	1.5	ns
Input timing							
$t_{SU;DAT}$	input data set-up time	pins PD11 to PD0		2	-	-	ns
		pins HSVGC, VSVGC and FSVGC	[6]	2	-	-	ns
$t_{HD;DAT}$	input data hold time	pins PD11 to PD0		0.9	-	-	ns
		pins HSVGC, VSVGC and FSVGC	[6]	1.5	-	-	ns
Crystal oscillator							
f_{nom}	nominal frequency			-	27	-	MHz
$\Delta f/f_{nom}$	permissible deviation of nominal frequency		[7]	-50×10^{-6}	-	$+50 \times 10^{-6}$	
Crystal specification							
T_{amb}	ambient temperature			0	-	70	°C
C_L	load capacitance			8	-	-	pF
R_S	series resistance			-	-	80	Ω
C_1	motional capacitance (typical)			1.2	1.5	1.8	fF
C_0	parallel capacitance (typical)			2.8	3.5	4.2	pF
Data and reference signal output timing							
$C_{o(L)}$	output load capacitance			8	-	40	pF
$t_{o(h)(gfx)}$	output hold time to graphics controller	pins HSVGC, VSVGC, FSVGC and $\overline{CBO}$		1.5	-	-	ns
$t_{o(d)(gfx)}$	output delay time to graphics controller	pins HSVGC, VSVGC, FSVGC and $\overline{CBO}$		-	-	10	ns

Table 239. Characteristics of the digital video encoder part *...continued*

T_{amb} = 0 °C to 70 °C (typical values measured at T_{amb} = 25 °C); unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{o(h)}$	output hold time	pins TDOe, TTXRQ_XCLKO2, VSM and HSM_CSYNC		3	-	-	ns
$t_{o(d)}$	output delay time	pins TDOe, TTXRQ_XCLKO2, VSM and HSM_CSYNC		-	-	25	ns
CVBS and RGB outputs							
$V_{o(CVBS)(p-p)}$	output voltage CVBS (peak-to-peak value)	see Table 241		-	1.23	-	V
$V_{o(VBS)(p-p)}$	output voltage VBS (S-video) (peak-to-peak value)	see Table 241		-	1	-	V
$V_{o(C)(p-p)}$	output voltage C (S-video) (peak-to-peak value)	see Table 241		-	0.89	-	V
$V_{o(RGB)(p-p)}$	output voltage R, G, B (peak-to-peak value)	see Table 241		-	0.7	-	V
ΔV_o	inequality of output signal voltages			-	2	-	%
$R_{o(L)}$	output load resistance			-	37.5	-	Ω
B_{DAC}	output signal bandwidth of DACs	–3 dB	[8]	-	170	-	MHz
$ILE_{lf(DAC)}$	LOW frequency integral linearity error of DACs			-	-	±3	LSB
$DLE_{lf(DAC)}$	LOW frequency differential linearity error of DACs			-	-	±1	LSB

[1] Minimum value for I²C-bus bit DOWNA = 1.

[2] Minimum value for I²C-bus bit DOWND = 1.

[3] Levels refer to pins PD11 to PD0, FSVGC, PIXCLKI, VSVGC, PIXCLKO, $\overline{CBO}$, TVD, and HSVGC, being inputs or outputs directly connected to a graphics controller. Input sensitivity is $\frac{1}{2}V_{DD(DVO)}$ + 100 mV for HIGH and $\frac{1}{2}V_{DD(DVO)}$ – 100 mV for LOW. The reference voltage $\frac{1}{2}V_{DD(DVO)}$ is generated on chip.

[4] The data is for both input and output direction.

[5] This parameter is arbitrary, if PIXCLKI is looped through the VGC.

[6] Tested with programming IFBP = 1.

[7] If an internal oscillator is used, crystal deviation of nominal frequency is directly proportional to the deviation of subcarrier frequency and line/field frequency.

[8] $B_{-3dB} = \frac{1}{2\pi(R_{o(L)}(C_{ext} + 5\ pF))}$ with $R_{o(L)}$ = 37.5 Ω and C_{ext} = 20 pF (typical).

Table 240. Characteristics of the digital video decoder part

V_{DDD} = 3.0 V to 3.6 V; V_{DDA} = 3.1 V to 3.5 V; T_{amb} = 0 °C to 70 °C (typical values measured at T_{amb} = 25 °C); timings and levels refer to drawings and conditions illustrated in Figure 67; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DDD}	digital supply voltage			3.15	3.3	3.45	V
I_{DDD}	digital supply current	X port 3-state; 8-bit I port		-	90	-	mA
P_D	power dissipation digital part			-	300	-	mW
V_{DDA}	analog supply voltage			3.15	3.3	3.45	V
I_{DDA}	analog supply current	AOSL1 and AOSL0 = 0					
		CVBS mode		-	47	-	mA
		Y/C mode		-	72	-	mA
P_A	power dissipation analog part	CVBS mode		-	150	-	mW
		Y/C mode		-	240	-	mW
$P_{tot(A+D)}$	total power dissipation analog and digital part	CVBS mode	[1]	-	450	-	mW
		Y/C mode	[1]	-	540	-	mW
$P_{tot(A+D)(pd)}$	total power dissipation analog and digital part in Power-down mode	CE pulled down to ground		-	5	-	mW
$P_{tot(A+D)(ps)}$	total power dissipation analog and digital part in Power-save mode	I^2C-bus controlled via address 88h = 0Fh		-	75	-	mW
Analog part							
I_{clamp}	clamping current	V_I = 0.9 V DC		-	±8	-	µA
$V_{i(p-p)}$	input voltage (peak-to-peak value)	for normal video levels 1 V (p-p), –3 dB termination 27/47 Ω and AC coupling required; coupling capacitor = 22 nF		-	0.7	-	V
$\lvert Z_i \rvert$	input impedance	clamping current off		200	-	-	kΩ
C_i	input capacitance			-	-	10	pF
α_{cs}	channel crosstalk	f_i < 5 MHz		-	-	–50	dB
9-bit analog-to-digital converters							
B	analog bandwidth	at –3 dB		-	7	-	MHz
ϕ_{diff}	differential phase	amplifier plus anti-alias filter bypassed		-	2	-	deg
G_{diff}	differential gain	amplifier plus anti-alias filter bypassed		-	2	-	%
$f_{clk(ADC)}$	ADC clock frequency			12.8	-	14.3	MHz
$LE_{dc(d)}$	DC differential linearity error			-	0.7	-	LSB
$LE_{dc(i)}$	DC integral linearity error			-	1	-	LSB

Table 240. Characteristics of the digital video decoder part *...continued*

V_{DDD} = 3.0 V to 3.6 V; V_{DDA} = 3.1 V to 3.5 V; T_{amb} = 0 °C to 70 °C (typical values measured at T_{amb} = 25 °C); timings and levels refer to drawings and conditions illustrated in Figure 67; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital inputs						
$V_{IL(SDAd,SCLd)}$	LOW-level input voltage pins SDAd and SCLd		–0.5	-	+0.3V_{DDD}	V
$V_{IH(SDAd,SCLd)}$	HIGH-level input voltage pins SDAd and SCLd		0.7V_{DDD}	-	V_{DDD} + 0.5	V
$V_{IL(XTALId)}$	LOW-level CMOS input voltage pin XTALId		–0.3	-	+0.8	V
$V_{IH(XTALId)}$	HIGH-level CMOS input voltage pin XTALId		2.0	-	V_{DDD} + 0.3	V
$V_{IL(n)}$	LOW-level input voltage all other inputs		–0.3	-	+0.8	V
$V_{IH(n)}$	HIGH-level input voltage all other inputs		2.0	-	5.5	V
I_{LI}	input leakage current		-	-	1	µA
$I_{LI/O}$	I/O leakage current		-	-	10	µA
C_i	input capacitance	I/O at high-impedance	-	-	8	pF
Digital outputs[2]						
$V_{OL(SDAd)}$	LOW-level output voltage pin SDAd	SDAd at 3 mA sink current	-	-	0.4	V
$V_{OL(clk)}$	LOW-level output voltage for clocks		0	-	0.6	V
$V_{OH(clk)}$	HIGH-level output voltage for clocks		2.4	-	V_{DDD} + 0.5	V
$V_{OL(n)}$	LOW-level output voltage all other digital outputs		0	-	0.4	V
$V_{OH(n)}$	HIGH-level output voltage all other digital outputs		2.4	-	V_{DDD} + 0.5	V
Clock output timing (LLC and LLC2)[3]						
C_L	output load capacitance		15	-	50	pF
T_{cy}	cycle time	pin LLC	35	-	39	ns
		pin LLC2	70	-	78	ns
δ	duty factor for t_{LLCH}/t_{LLC} and t_{LLC2H}/t_{LLC2}	C_L = 40 pF	40	-	60	%
t_r	rise time LLC and LLC2	0.2 V to V_{DDD} – 0.2 V	-	-	5	ns
t_f	fall time LLC and LLC2	V_{DDD} – 0.2 V to 0.2 V	-	-	5	ns
$t_{d(LLC-LLC2)}$	delay time between LLC and LLC2 output	measured at 1.5 V; C_L = 25 pF	–4	-	+8	ns
Horizontal PLL						
$f_{hor(nom)}$	nominal line frequency	50 Hz field	-	15625	-	Hz
		60 Hz field	-	15734	-	Hz
$\Delta f_{hor}/f_{hor(nom)}$	permissible static deviation		-	-	5.7	%

Table 240. Characteristics of the digital video decoder part *...continued*

V_{DDD} = 3.0 V to 3.6 V; V_{DDA} = 3.1 V to 3.5 V; T_{amb} = 0 °C to 70 °C (typical values measured at T_{amb} = 25 °C); timings and levels refer to drawings and conditions illustrated in Figure 67; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Subcarrier PLL						
$f_{sc(nom)}$	nominal subcarrier frequency	PAL BGHI	-	4433619	-	Hz
		NTSC M	-	3579545	-	Hz
		PAL M	-	3575612	-	Hz
		PAL N	-	3582056	-	Hz
Δf_{sc}	lock-in range		±400	-	-	Hz
Crystal oscillator for 32.11 MHz[4]						
$f_{xtal(nom)}$	nominal crystal frequency	3rd harmonic	-	32.11	-	MHz
$\Delta f/f_{xtal(nom)}$	nominal crystal frequency deviation		-70×10^{-6}	-	$+70 \times 10^{-6}$	
$\Delta f/f_{xtal(nom)(T)}$	nominal crystal frequency deviation with temperature		-30×10^{-6}	-	$+30 \times 10^{-6}$	
Crystal specification (X1)						
$T_{amb(X1)}$	ambient temperature		0	-	70	°C
C_L	load capacitance		8	-	-	pF
R_S	series resonance resistor		-	40	80	Ω
C_1	motional capacitance		-	1.5 ± 20 %	-	fF
C_0	parallel capacitance		-	4.3 ± 20 %	-	pF
Crystal oscillator for 24.576 MHz[4]						
$f_{xtal(nom)}$	nominal crystal frequency	3rd harmonic	-	24.576	-	MHz
$\Delta f/f_{xtal(nom)}$	nominal crystal frequency deviation		-50×10^{-6}	-	$+50 \times 10^{-6}$	
$\Delta f/f_{xtal(nom)(T)}$	nominal crystal frequency deviation with temperature		-20×10^{-6}	-	$+20 \times 10^{-6}$	
Crystal specification (X1)						
$T_{amb(X1)}$	ambient temperature		0	-	70	°C
C_L	load capacitance		8	-	-	pF
R_S	series resonance resistor		-	40	80	Ω
C_1	motional capacitance		-	1.5 ± 20 %	-	fF
C_0	parallel capacitance		-	3.5 ± 20 %	-	pF
Clock input timing (XCLK)						
T_{cy}	cycle time		31	-	45	ns
δ	duty factor for t_{LLCH}/t_{LLC}		40	50	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	5	ns
Data and control signal input timing X port, related to XCLK input						
$t_{SU;DAT}$	input data setup time		-	10	-	ns
$t_{HD;DAT}$	input data hold time		-	3	-	ns

Table 240. Characteristics of the digital video decoder part *...continued*

V_{DDD} = 3.0 V to 3.6 V; V_{DDA} = 3.1 V to 3.5 V; T_{amb} = 0 °C to 70 °C (typical values measured at T_{amb} = 25 °C); timings and levels refer to drawings and conditions illustrated in Figure 67; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Clock output timing						
C_L	output load capacitance		15	-	50	pF
T_{cy}	cycle time		35	-	39	ns
δ	duty factor for t_{XCLKH}/t_{XCLKL}		35	-	65	%
t_r	rise time	0.6 V to 2.6 V	-	-	5	ns
t_f	fall time	2.6 V to 0.6 V	-	-	5	ns
Data and control signal output timing X port, related to XCLK output (for XPCK[1:0] 83h[5:4] = 00 is default)[3]						
C_L	output load capacitance		15	-	50	pF
$t_{OHD;DAT}$	output hold time	C_L = 15 pF	-	14	-	ns
t_{PD}	propagation delay from positive edge of XCLK output	C_L = 15 pF	-	24	-	ns
Control signal output timing RT port, related to LLC output						
C_L	output load capacitance		15	-	50	pF
$t_{OHD;DAT}$	output hold time	C_L = 15 pF	-	14	-	ns
t_{PD}	propagation delay from positive edge of LLC output	C_L = 15 pF	-	24	-	ns
ICLK output timing						
C_L	output load capacitance		15	-	50	pF
T_{cy}	cycle time		31	-	45	ns
δ	duty factor for t_{ICLKH}/t_{ICLKL}		35	-	65	%
t_r	rise time	0.6 V to 2.6 V	-	-	5	ns
t_f	fall time	2.6 V to 0.6 V	-	-	5	ns
Data and control signal output timing I port, related to ICLK output (for IPCK[1:0] 87h[5:4] = 00 is default)						
C_L	output load capacitance at all outputs		15	-	50	pF
$t_{OHD;DAT}$	output data hold time	C_L = 15 pF	-	12	-	ns
$t_{o(d)}$	output delay time	C_L = 15 pF	-	22	-	ns
ICLK input timing						
T_{cy}	cycle time		31	-	100	ns

[1] 8-bit image port output mode, expansion port is 3-stated.

[2] The levels must be measured with load circuits; 1.2 kΩ at 3 V (TTL load); C_L = 50 pF.

[3] The effects of rise and fall times are included in the calculation of $t_{OHD;DAT}$ and t_{PD}. Timings and levels refer to drawings and conditions illustrated in Figure 67.

[4] The crystal oscillator drive level is typically 0.28 mW.

16. Timing

16.1 Digital video encoder part

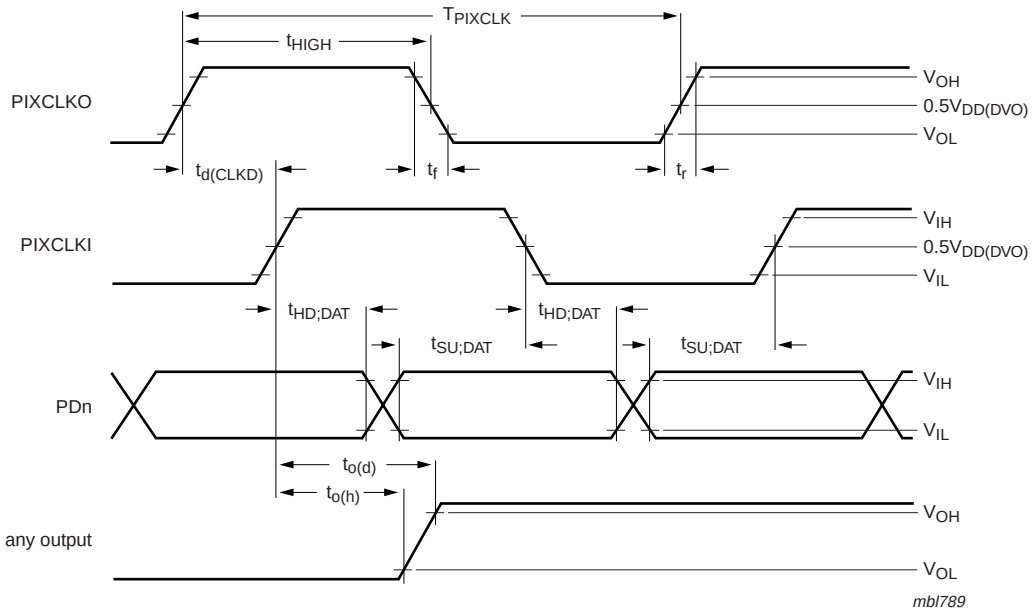


Fig 63. Input/output timing specification

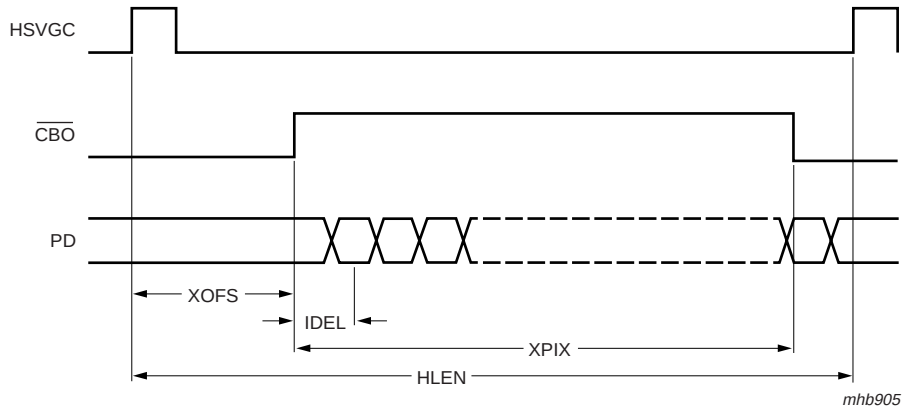


Fig 64. Horizontal input timing

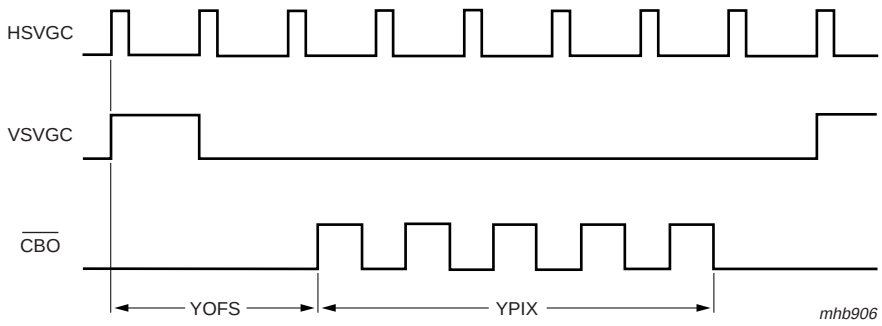


Fig 65. Vertical input timing

16.1.1 Teletext timing

Time t_{FD} is the time needed to interpolate input data TTX and insert it into the CVBS and VBS output signal, such that it appears at t_{TTX} = 9.78 µs (PAL) or t_{TTX} = 10.5 µs (NTSC) after the leading edge of the horizontal synchronization pulse.

Time t_{PD} is the pipeline delay time introduced by the source that is gated by TTXRQ_XCLKO2 in order to deliver TTX data. This delay is programmable by register TTXHD. For every active HIGH state at output pin TTXRQ_XCLKO2, a new teletext bit must be provided by the source.

Since the beginning of the pulses representing the TTXRQ signal and the delay between the rising edge of TTXRQ and valid teletext input data are fully programmable (TTXHS and TTXHD), the TTX data is always inserted at the correct position after the leading edge of the outgoing horizontal synchronization pulse.

Time $t_{i(TTXW)}$ is the internally used insertion window for TTX data; it has a constant length that allows insertion of 360 teletext bits at a text data rate of 6.9375 Mbit/s (PAL), 296 teletext bits at a text data rate of 5.7272 Mbit/s (world standard TTX) or 288 teletext bits at a text data rate of 5.7272 Mbit/s (NABTS). The insertion window is not opened if the control bit TTXEN is zero.

Using appropriate programming, all suitable lines of the odd field (TTXOVS and TTXOVE) plus all suitable lines of the even field (TTXEVS and TTXEVE) can be used for teletext insertion.

It is essential to note that the two pins used for teletext insertion must be configured for this purpose by the correct I^2C-bus register settings.

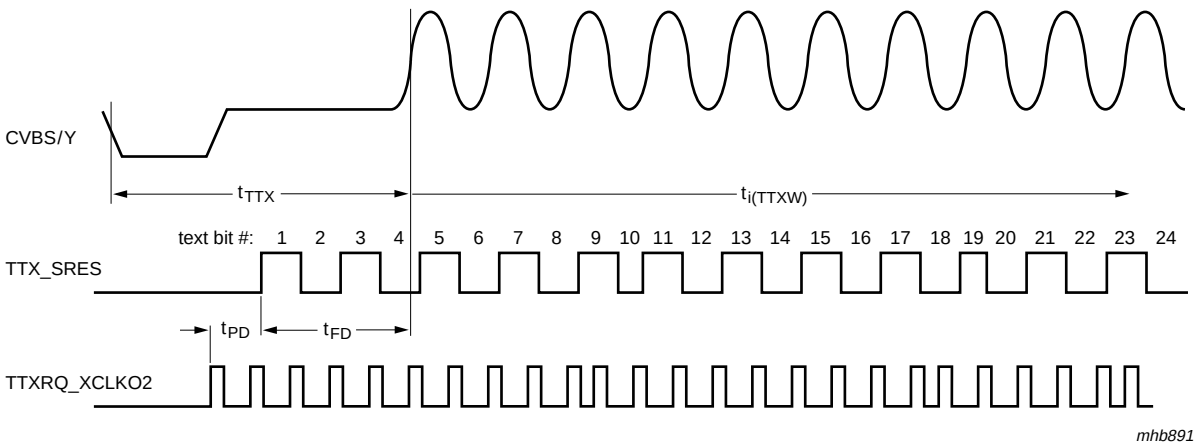


Fig 66. Teletext timing

16.2 Digital video decoder part

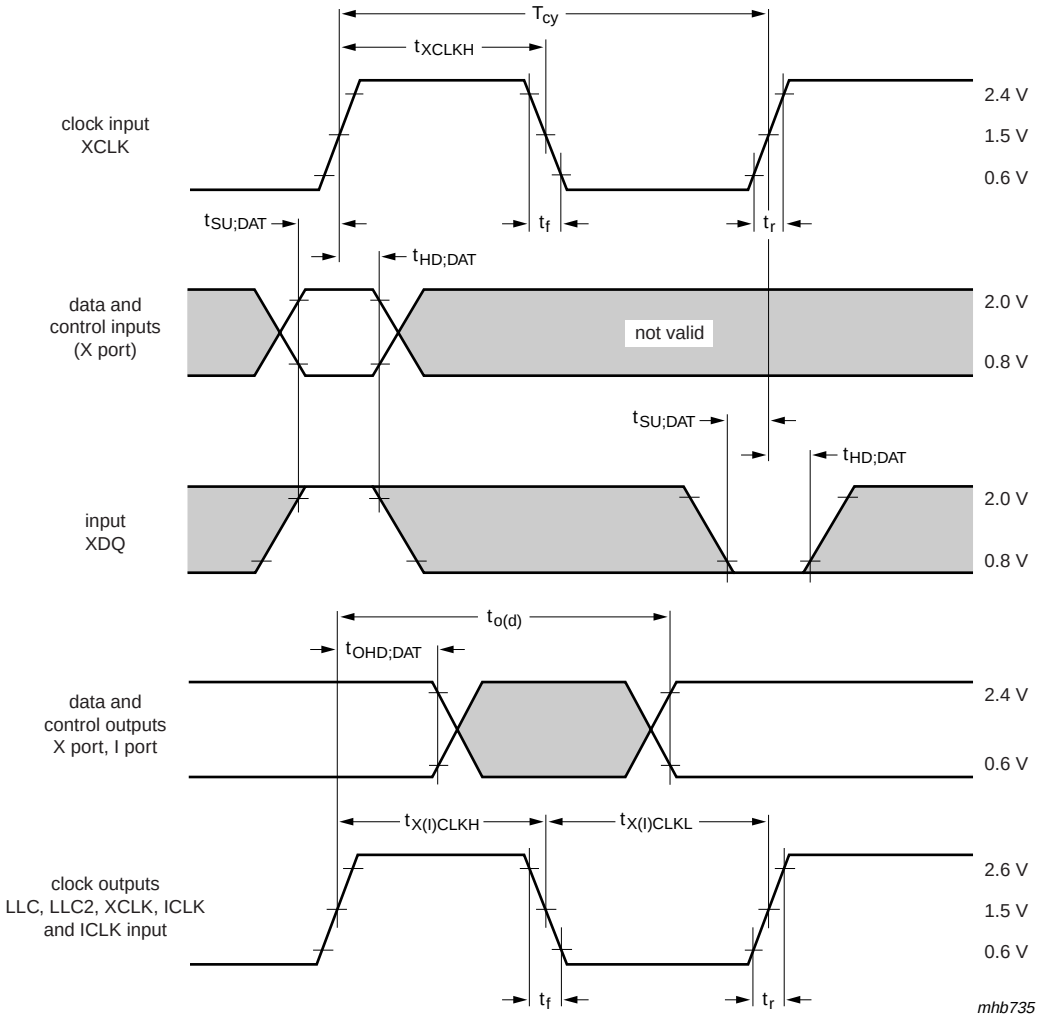


Fig 67. Data input/output timing diagram (X port, RT port and I port)

17. Application information

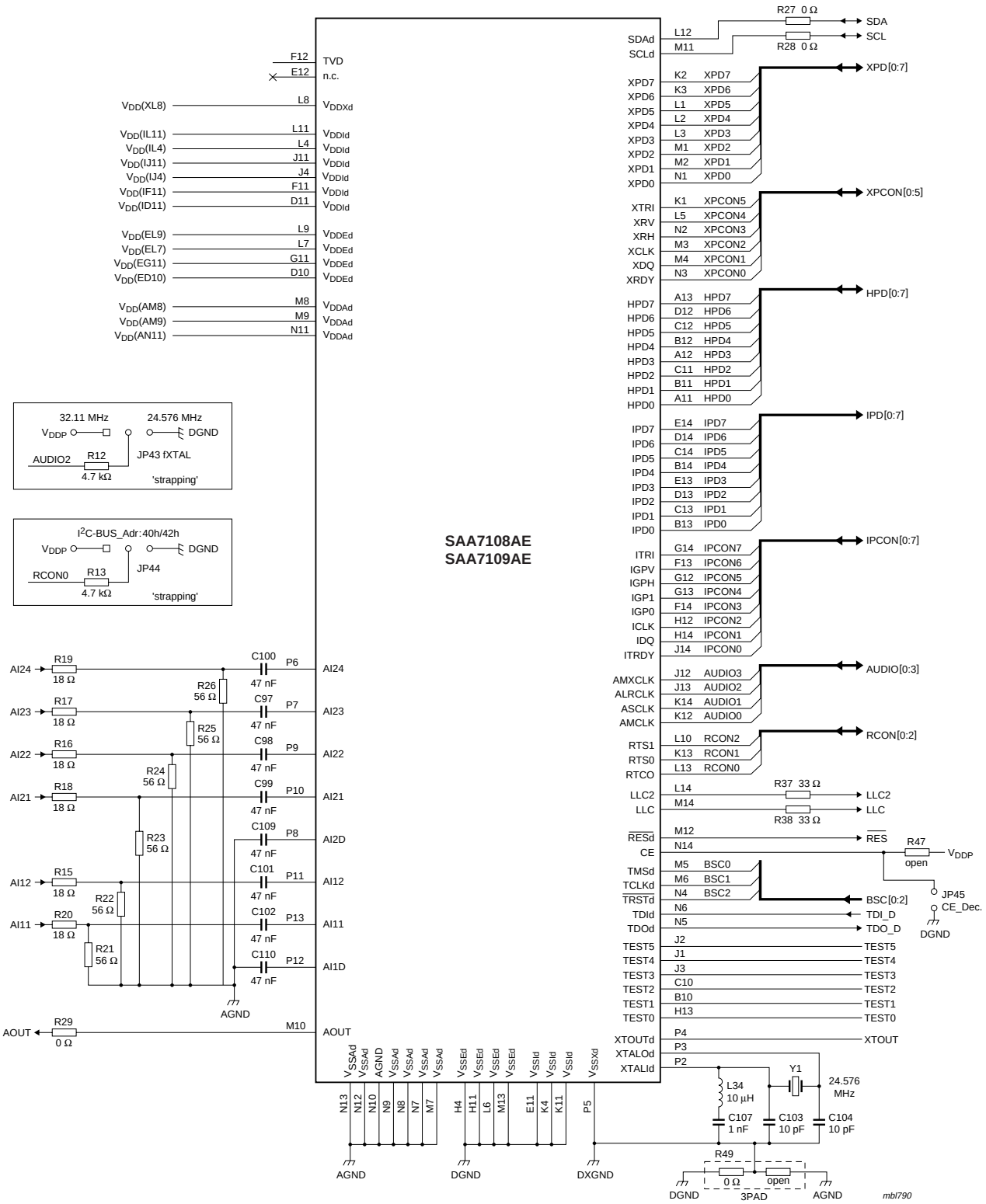


Fig 68. Application circuit (decoder part)

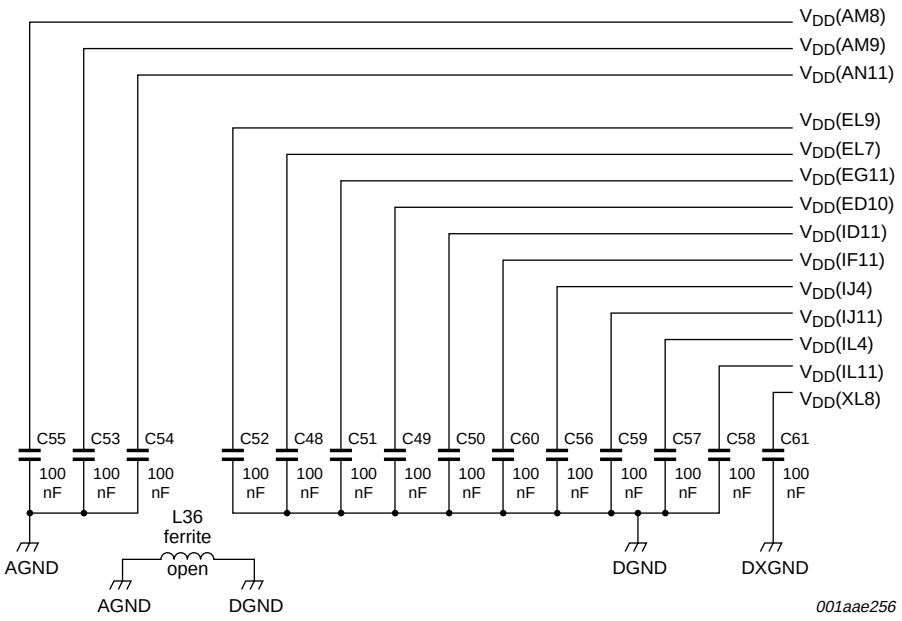


Fig 69. Decoupling circuit supply voltages

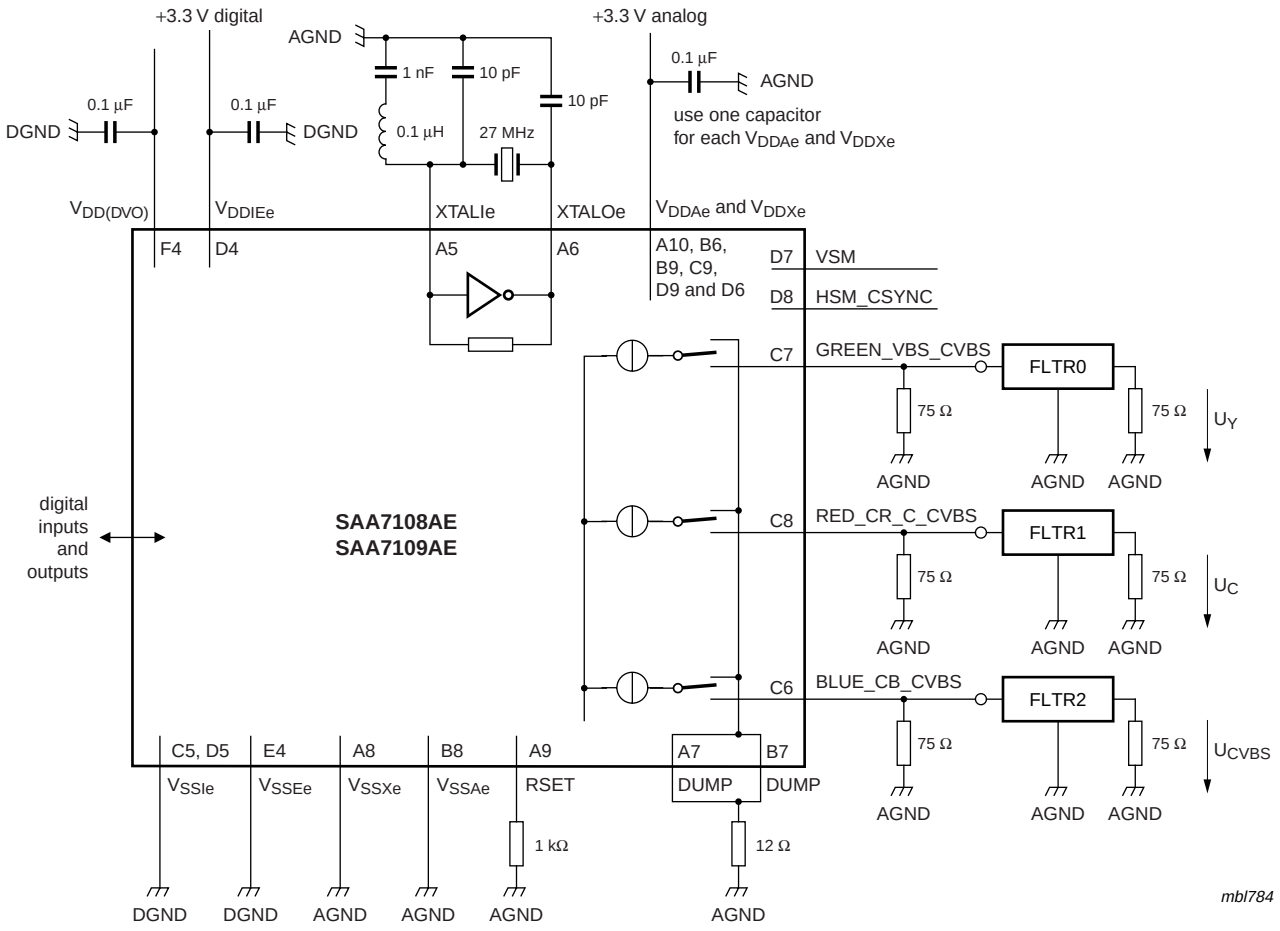


Fig 70. Application circuit (encoder part)

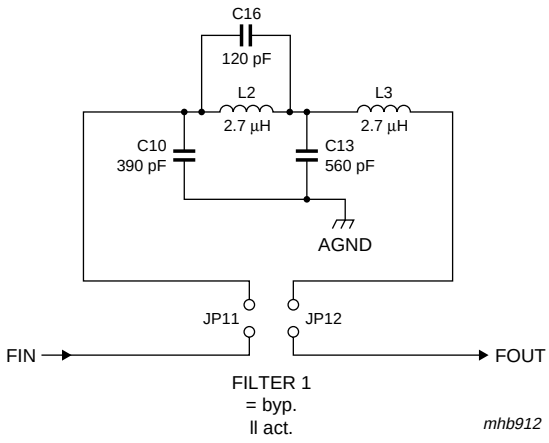
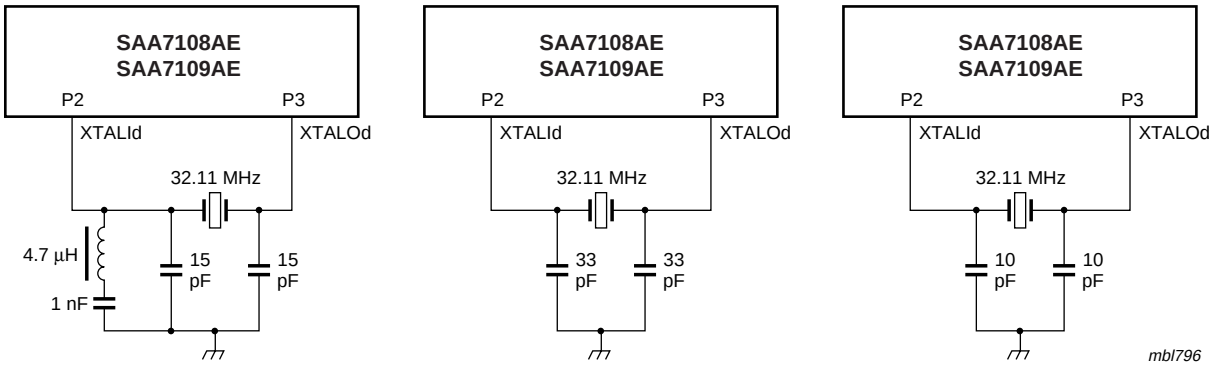


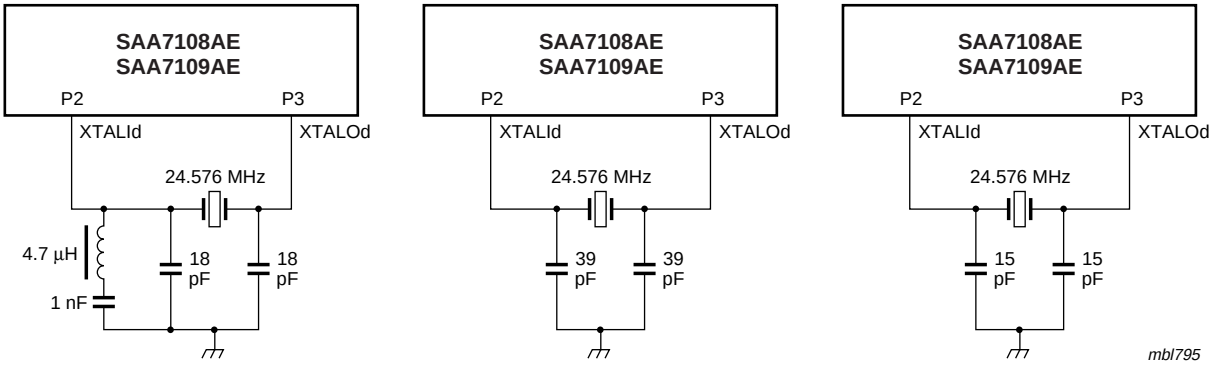
Fig 71. FLTR0, FLTR1 and FLTR2 as shown in Figure 70



a. With 3rd harmonic quartz. Crystal load = 8 pF.

b. With fundamental quartz. Crystal load = 20 pF.

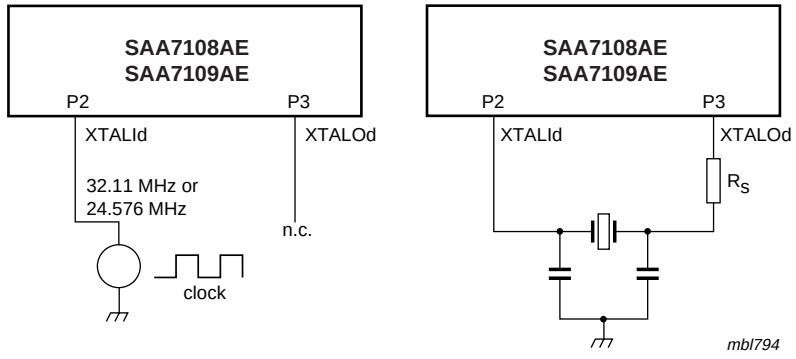
c. With fundamental quartz. Crystal load = 8 pF.



d. With 3rd harmonic quartz. Crystal load = 8 pF.

e. With fundamental quartz. Crystal load = 20 pF.

f. With fundamental quartz. Crystal load = 8 pF.

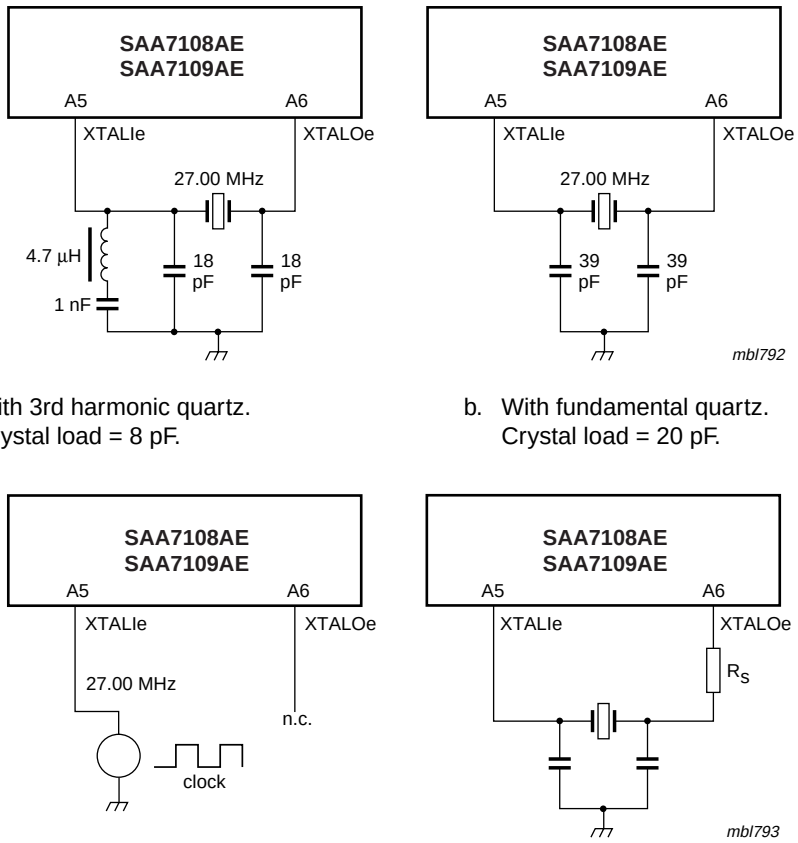


g. With direct clock.

h. With fundamental quartz and restricted drive level. When P_{drive} of the internal oscillator is too high, a resistance R_S can be placed in series with the output of the oscillator XTALOd.

Note: The decreased crystal amplitude results in a lower drive level but on the other hand the jitter performance will decrease.

Fig 72. Oscillator application for decoder part



a. With 3rd harmonic quartz. Crystal load = 8 pF.

b. With fundamental quartz. Crystal load = 20 pF.

c. With direct clock.

d. With fundamental quartz and restricted drive level. When P_{drive} of the internal oscillator is too high, a resistance R_S can be placed in series with the oscillator output XTALOe.

Note: The decreased crystal amplitude results in a lower drive level but on the other hand the jitter performance will decrease.

Fig 73. Oscillator application for encoder part

17.1 Reconstruction filter

Figure 71 shows a possible reconstruction filter for the digital-to-analog converters. Due to its cut-off frequency of ~6 MHz, it is not suitable for HDTV applications.

17.2 Analog output voltages

The analog output voltages are dependent on the total load (typical value 37.5 Ω), the digital gain parameters and the I^2C-bus settings of the DAC reference currents (analog settings).

The digital output signals in front of the DACs under nominal (nominal here stands for the settings given in Table 66 to Table 73 for example a standard PAL or NTSC signal) conditions occupy different conversion ranges, as indicated in Table 241 for a $^{100}/_{100}$ color bar signal.

By setting the reference currents of the DACs as shown in Table 241, standard compliant amplitudes can be achieved for all signal combinations; it is assumed that in subaddress 16h, parameter DACF = 0000b, that means the fine adjustment for all DACs in common is set to 0 %.

If S-video output is desired, the adjustment for the C (chrominance subcarrier) output should be identical to the one for VBS (luminance plus sync) output.

Table 241. Digital output signals conversion range

Set/out	CVBS, sync tip-to-white	VBS, sync tip-to-white	RGB, black-to-white
Digital settings	see Table 66 to Table 73	see Table 66 to Table 73	see Table 61
Digital output	1014	881	876
Analog settings	e.g. B DAC = 1Fh	e.g. G DAC = 1Bh	e.g. R DAC = G DAC = B DAC = 0Bh
Analog output	1.23 V (p-p)	1.00 V (p-p)	0.70 V (p-p)

17.3 Suggestions for a board layout

Use separate ground planes for analog and digital ground. Connect these planes only at one point directly under the device, by using a 0 Ω resistor directly at the supply stage. Use separate supply lines for the analog and digital supply. Place the supply decoupling capacitors close to the supply pins.

Use L_{bead} (ferrite coil) in each digital supply line close to the decoupling capacitors to minimize radiation energy (EMC).

Place the analog coupling (clamp) capacitors close to the analog input pins. Place the analog termination resistors close to the coupling capacitors.

Be careful of hidden layout capacitors around the crystal application.

Use serial resistors in clock, sync and data lines, to avoid clock or data reflection effects and to soften data energy.

The SAA7108AE; SAA7109AE crystal temperature depends on the PCB it is soldered on. For normal airflow conditions at a maximum ambient temperature of 70 °C it will be sufficient to provide:

- PCB dimensions at least 2000 mm^2
- PCB at least 4 layers
- At least 50 vias (connecting PCB layers) close to the chip
- Metal coverage at least 60 % on at least 2 PCB layers near the chip

18. Test information

18.1 Boundary scan test

The SAA7108AE; SAA7109AE has built-in logic and 2 times 5 dedicated pins to support boundary scan testing, separately for the encoder and decoder part, which allows board testing without special hardware (nails). The SAA7108AE; SAA7109AE follows the *"IEEE Std. 1149.1 - Standard Test Access Port and Boundary-Scan Architecture"* set by the Joint Test Action Group (JTAG) chaired by NXP.

The 10 special pins are Test Mode Select (TMSe and TMSd), Test Clock (TCKe and TCKd), Test Reset ($\overline{\text{TRSTe}}$ and $\overline{\text{TRSTd}}$), Test Data Input (TDIe and TDId) and Test Data Output (TDOe and TDOd), where extension 'e' refers to the encoder part and extension 'd' refers to the decoder part.

The Boundary Scan Test (BST) functions BYPASS, EXTEST, SAMPLE, CLAMP and IDCODE are all supported; see Table 242. Details about the JTAG BST-TEST can be found in the specification "*IEEE Std. 1149.1"*. Two files containing the detailed Boundary Scan Description Language (BSDL) of the SAA7108AE; SAA7109AE are available on request.

Table 242. BST instructions supported by the SAA7108AE; SAA7109AE

Instruction	Description
BYPASS	This mandatory instruction provides a minimum length serial path (1 bit) between TDIe (or TDId) and TDOe (or TDOd) when no test operation of the component is required.
EXTEST	This mandatory instruction allows testing of off-chip circuitry and board level interconnections.
SAMPLE	This mandatory instruction can be used to take a sample of the inputs during normal operation of the component. It can also be used to preload data values into the latched outputs of the boundary scan register.
CLAMP	This optional instruction is useful for testing when not all ICs have BST. This instruction addresses the bypass register while the boundary scan register is in external test mode.
IDCODE	This optional instruction will provide information on the components manufacturer, part number and version number.

18.1.1 Initialization of boundary scan circuit

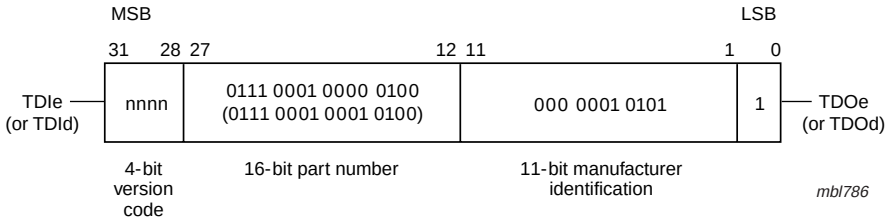
The Test Access Port (TAP) controller of an IC should be in the reset state (TEST_LOGIC_RESET) when the IC is in functional mode. This reset state also forces the instruction register into a functional instruction such as IDCODE or BYPASS.

To solve the power-up reset, the standard specifies that the TAP controller will be forced asynchronously to the TEST_LOGIC_RESET state by setting the $\overline{\text{TRSTe}}$ or $\overline{\text{TRSTd}}$ pin LOW.

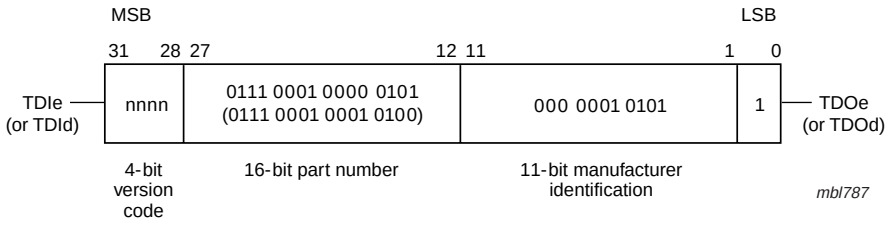
18.1.2 Device identification codes

A device identification register is specified in *"IEEE Std. 1149.1b-1994"*. It is a 32-bit register which contains fields for the specification of the IC manufacturer, the IC part number and the IC version number. Its biggest advantage is the possibility to check for the correct ICs mounted after production and to determine the version number of the ICs during field service.

When the IDCODE instruction is loaded into the BST instruction register, the identification register will be connected between TDIe (or TDId) and TDOe (or TDOd) of the IC. The identification register will load a component specific code during the CAPTURE_DATA_REGISTER state of the TAP controller, this code can subsequently be shifted out. At board level this code can be used to verify component manufacturer, type and version number. The device identification register contains 32 bits, numbered 31 to 0, where bit 31 is the most significant bit (nearest to TDIe or TDId) and bit 0 is the least significant bit (nearest to TDOe or TDOd); see Figure 74.



a. SAA7108AE.

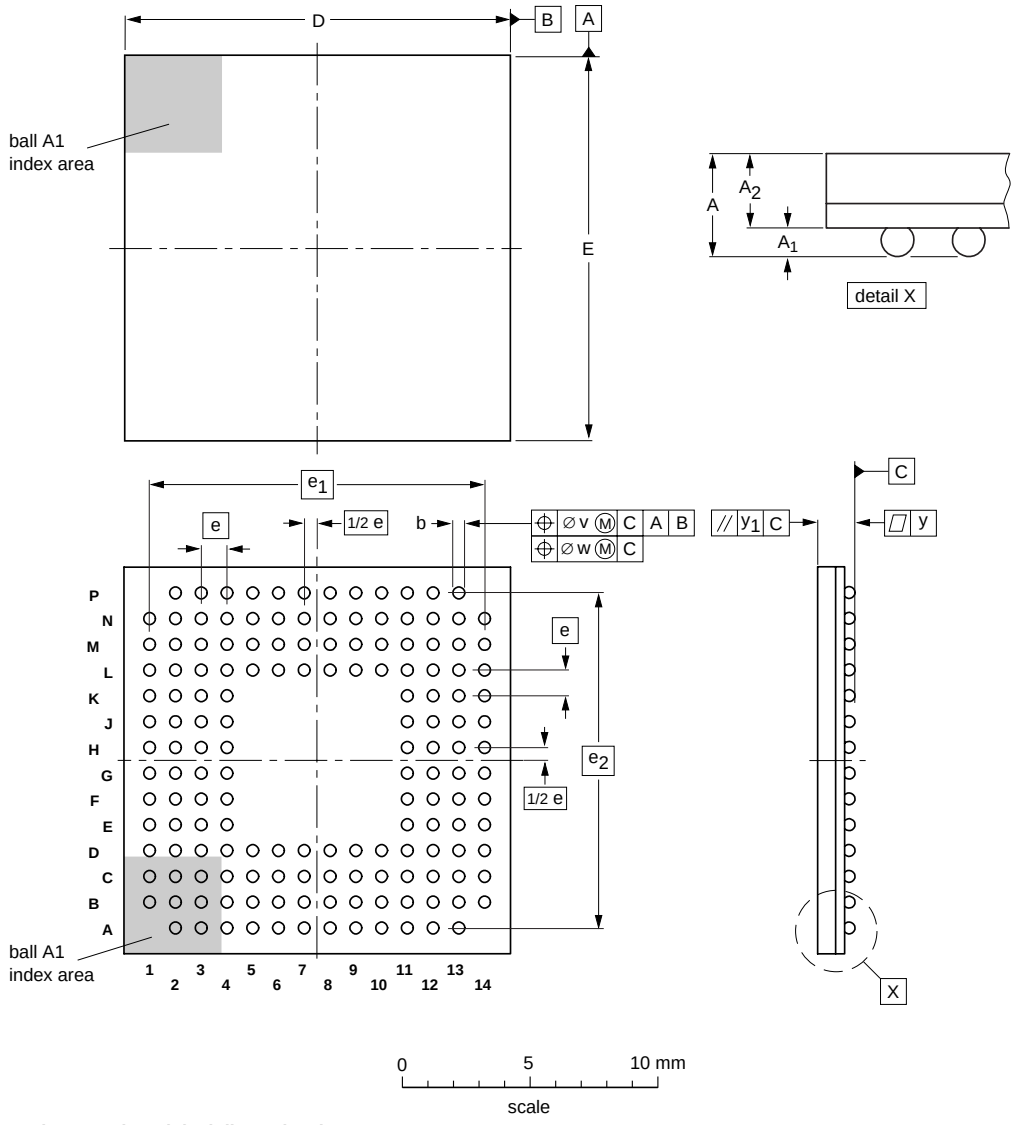


b. SAA7109AE.

Fig 74. 32 bits of identification code

19. Package outline

LBGA156: plastic low profile ball grid array package; 156 balls; body 15 x 15 x 1.05 mm **SOT700-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.65	0.45 0.35	1.20 0.95	0.55 0.45	15.2 14.8	15.2 14.8	1	13	13	0.25	0.1	0.12	0.35

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT700-1	- - -	MO-192	- - -			~~01-05-11~~ 01-11-06

Fig 75. Package outline SOT700-1 (LBGA156)

20. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

20.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

20.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

20.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

20.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 76) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 243 and 244

Table 243. SnPb eutectic process (from J-STD-020C)

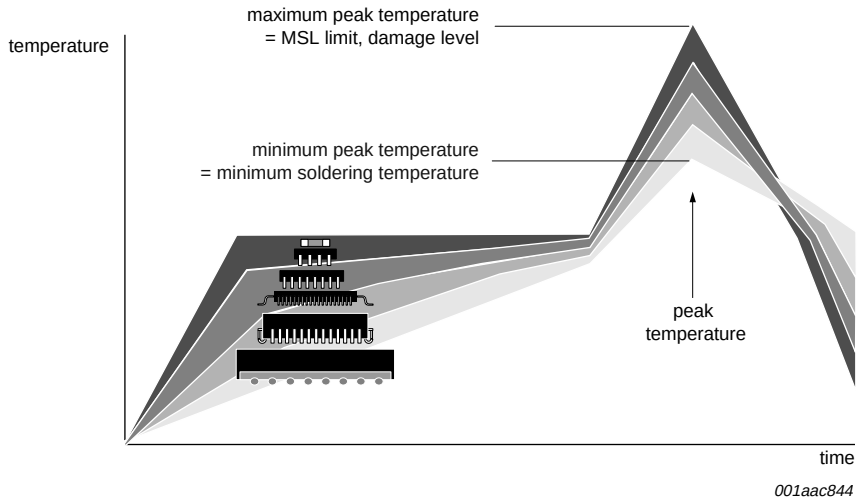
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 244. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 76.



MSL: Moisture Sensitivity Level

Fig 76. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

21. Revision history

Table 245. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SAA7108AE_ SAA7109AE_3	20070206	Product data sheet	CPCN200505019	SAA7108AE_ SAA7109AE_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors • Legal texts have been adapted to the new company name where appropriate • Table 4: Updated description for pin E2, pin G2, pin L12 and pin M11 • Table 240: Digital outputs; LOW-level output voltage for clocks corrected from –0.5 V to 0 V • Package outline changed from SOT472-1 to SOT700-1			
SAA7108AE_ SAA7109AE_2	20040629	Product specification	-	SAA7108AE_ SAA7109AE_1
SAA7108AE_ SAA7109AE_1	20030326	Product specification	-	-

22. Legal information

22.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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24. Contents

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