Features

- Lead free versions available
- RoHS compliant (lead free version)*
- ESD protection > 25k volts
- Protects four unidirectional lines
- Small SMT package

Applications

- Cell phones
- PDAs and notebooks
- Digital cameras
- MP3 players and GPS

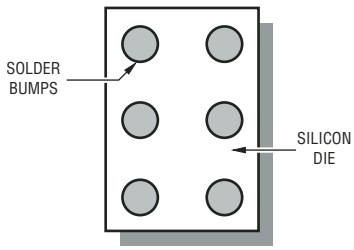
BOURNS®

2DAA-F6R - Integrated Passive & Active Device

General Information

The 2DAA-F6R device provides ESD protection for the I/O port of portable electronic devices such as cell phones, modems and PDAs. The device incorporates four TVS unidirectional diodes configured for interfacing to external lines.

The ESD protection provided by the component enables an I/O port to withstand a minimum ±8 KV Contact / ±15 KV Air Discharge per the ESD test method specified in IEC 61000-4-2. The device measures 1.00 mm x 1.50 mm and is available in a 6 bump Flip Chip package intended to be mounted directly onto an FR4 printed circuit board. The Flip Chip device meets typical thermal cycle and bend test specifications without the use of an underfill material.



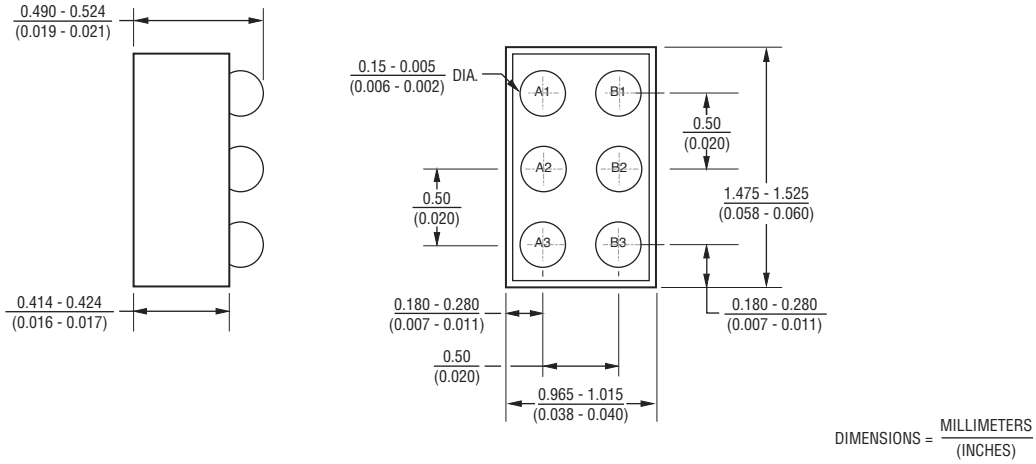
Electrical & Thermal Characteristics

Electrical Characteristics (T_A = 25 °C unless otherwise noted)	**Symbol**	**Minimum**	**Nominal**	**Maximum**	**Unit**
Per TVS Diode Specification Capacitance @ 0 V 1 MHz	C	120	150	180	pF
Rated Standoff Voltage	V_{WM}		5.0		V
Breakdown Voltage @ 1 mA	V_{BR}	6.0			V
Clamping Voltage @ I_P = 5 A t_P = 8/20 μs @ I_{PP} = 24 A t_P = 8/20 μs	 V_C V_C			 9.5 11	 V V
Leakage Current @ 5 V	I_R		1	10	μA
ESD Protection: IEC 61000-4-2 Contact Discharge Air Discharge		 ±8 ±15			 kV kV
Surge Protection: IEC 61000-4-5 8/20 μs - Level 2 (Line - Gnd) 8/20 μs - Level 3 (Line - Line)		 24 24			 A A
Thermal Characteristics (T_A = 25 °C unless otherwise noted)					
Operating Temperature Range	T_J	-40	25	+85	°C
Storage Temperature Range	T_{STG}	-55	25	+150	°C
Peak Pulse Power (t_P = 8/20 μs)	P_{PP}			300	W

*RoHS Directive 2002/95/EC Jan 27 2003 including Annex

Mechanical Characteristics

This is a silicon-based device and is packaged using chip scale packaging technology. Solder bumps, formed on the silicon die, provide the interconnect medium from die to PCB. The bumps are arranged on the die in a regular grid formation. The grid pitch is 0.5 mm and the dimensions for the packaged device are shown below.



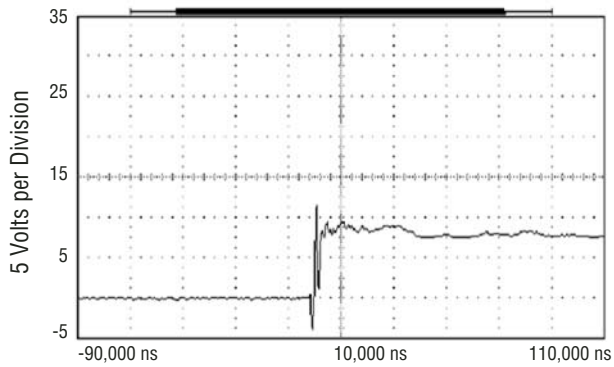
Reliability Data

Reliability data is gathered on an ongoing basis for Bourns® Integrated Passive and Active Devices.

"Package level" testing of the integrity of the solder joint is carried out on an independent Daisy-Chain test device. A 25-Pin Daisy Chain component is available from Bourns for this purpose (part number 2TAD-C25R). This is a 5 x 5 array featuring 0.5 mm pitch solder bumps. The Distance to Neutral Point (DNP) on that component is larger than that of the 2DAA-F6R and is thus deemed suitable for Thermal Cycle testing.

"Silicon level" reliability performance is based on similarity to other integrated passive CSP devices from Bourns.

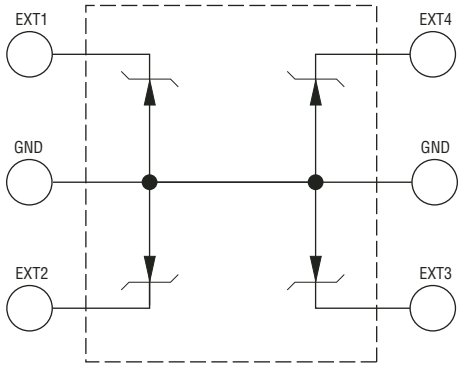
Overshoot and Clamping Voltage Response



ESD Test Pulse - 25 kilovolt, 1/30 ns (waveshape)

Block Diagram

The CSP device block diagram below includes the pin names and basic electrical connections associated with each channel.



PCB Design and SMT Processing

Please consult the “Bourns Design Guide Using CSP” for notes on PCB design and SMT Processing.

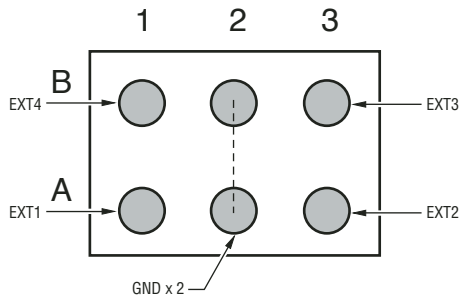
How to Order

2 DAA - F6R __

Thinfilm
Model
Flip Chip
No. of Solder Bumps
Packaging Option
R = Tape and Reel
Packaged 5000 pcs. / 7 ” reel
Terminations
LF = Sn/Ag/Cu (lead free)
Blank = Sn/Pb

Device Pin Out

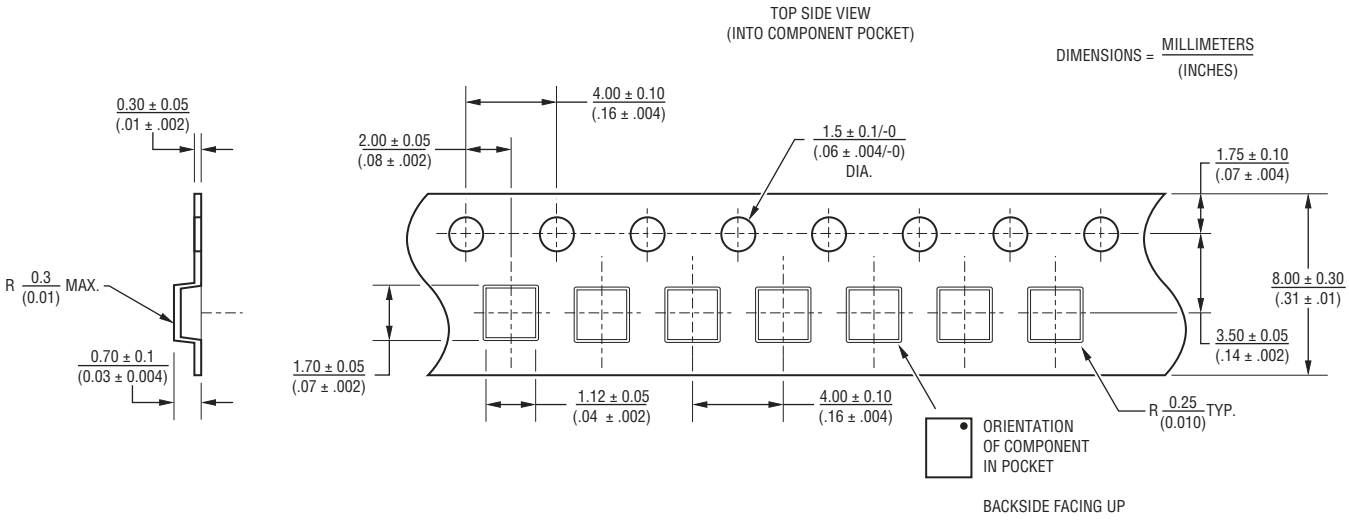
The pin-out for the device is shown below with the bumps facing up.



Pin Out	Function	Pin Out	Function
A1	EXT1	B1	EXT4
A2	GND	B2	GND
A3	EXT2	B3	EXT3

Packaging

The surface mount product is packaged in an 8 mm x 4 mm Tape and Reel format per EIA-481 standard.



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Reliable Electronic Solutions

Asia-Pacific: TEL +886- (0)2 25624117 • FAX +886- (0)2 25624116
Europe: TEL +41-41 768 5555 • FAX +41-41 768 5510
The Americas: TEL +1-951 781-5492 • FAX +1-951 781-5700
www.bourns.com