

Integrated Device Technology, Inc.

FAST CMOS OCTAL LATCHED TRANSCEIVER

IDT54/74FCT543
IDT54/74FCT543A
IDT54/74FCT543C

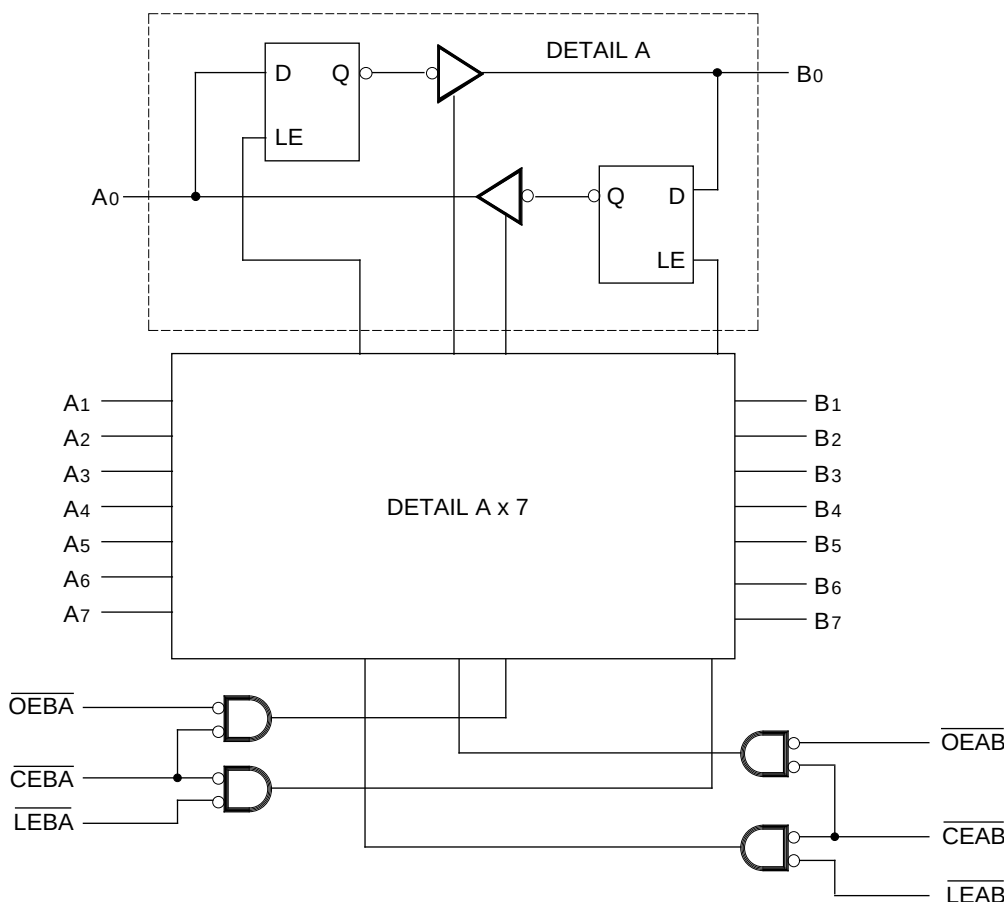
FEATURES:

- IDT54/74FCT543 equivalent to FAST™ speed
- **IDT54/74FCT543A 25% faster than FAST**
- **IDT54/74FCT543C 40% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- IOL = 64mA (commercial), 48mA (military)
- Separate controls for data flow in each direction
- Back-to-back latches for storage
- CMOS power levels (1mW typ. static)
- Substantially lower input current levels than FAST (5μA max.)
- TTL input and output level compatible
- CMOS output level compatible
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT543/A/C is a non-inverting octal transceiver built using an advanced dual metal CMOS technology. These devices contain two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{\text{CEAB}}$) input must be LOW in order to enter data from A0–A7 or to take data from B0–B7, as indicated in the Function Table. With $\overline{\text{CEAB}}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{\text{LEAB}}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{\text{LEAB}}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{\text{CEAB}}$ and $\overline{\text{OEAB}}$ both LOW, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$ and $\overline{\text{OEBA}}$ inputs.

FUNCTIONAL BLOCK DIAGRAMS



2614 drw 01

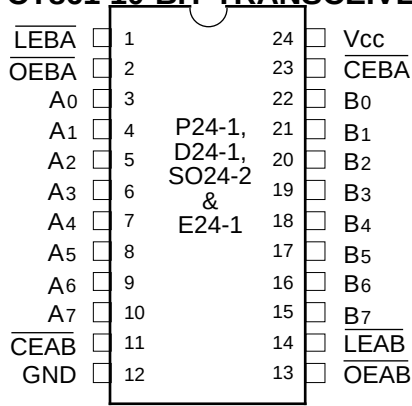
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FAST is a registered trademark of National Semiconductor Co.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

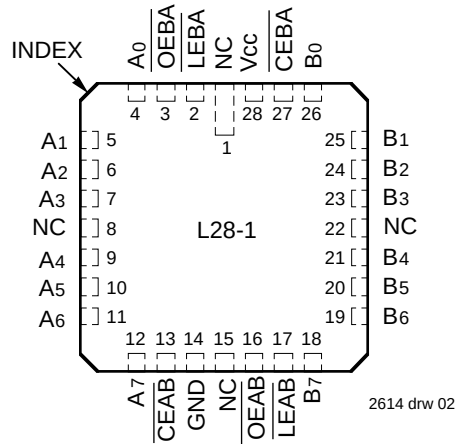
MAY 1992

PIN CONFIGURATIONS

IDT54/74FCT861 10-BIT TRANSCEIVERS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A0–A7	A-to-B Data Inputs or B-to-A 3-State Outputs
B0–B7	B-to-A Data Inputs or A-to-B 3-State Outputs

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FUNCTION TABLE (1,2)

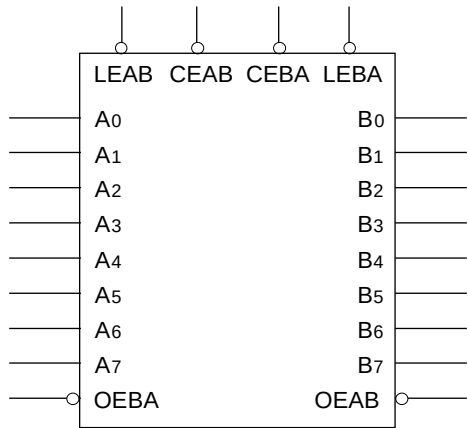
For A-to-B (Symmetric with B-to-A)

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-to-B	B0–B7
H	—	—	Storing	High Z
—	H	—	Storing	—
—	—	H	—	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

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- NOTES:
- * Before $\overline{LEAB}$ LOW-to-HIGH Transition
H = HIGH Voltage Level
L = LOW Voltage Level
— = Don't Care or Irrelevant
 - A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$.

LOGIC SYMBOL



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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	−0.5 to V _{CC}	−0.5 to V _{CC}	V
T _A	Operating Temperature	0 to +70	−55 to +125	°C
T _{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T _{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P _T	Power Dissipation	0.5	0.5	W
I _{OUT}	DC Output Current	120	120	mA

NOTES:

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Inputs and V_{CC} terminals only.
- Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{I/O}	I/O Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

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- This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V, V_{HC} = V_{CC} − 0.2V

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V
I _{IH}	Input HIGH Current (Except I/O pins)	V _{CC} = Max. V _I = V _{CC}	—	—	5	μA
		V _I = 2.7V	—	—	5 ⁽⁴⁾	
I _{IL}	Input LOW Current (Except I/O pins)	V _I = 0.5V	—	—	−5 ⁽⁴⁾	μA
		V _I = GND	—	—	−5	
I _{IH}	Input HIGH Current (I/O pins Only)	V _{CC} = Max. V _I = V _{CC}	—	—	15	μA
		V _I = 2.7V	—	—	15 ⁽⁴⁾	
I _{IL}	Input LOW Current (I/O pins Only)	V _I = 0.5V	—	—	−15 ⁽⁴⁾	μA
		V _I = GND	—	—	−15	
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _N = −18mA	—	−0.7	−1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _O = GND	−60	−120	—	mA
V _{OH}	Output HIGH Voltage	V _{CC} = 3V, V _{IN} = V _{LC} or V _{HC} , I _{OH} = −32μA	V _{HC}	V _{CC}	—	V
		V _{CC} = Min. V _{IN} = V _{IH} or V _{IL} I _{OH} = −300μA	V _{HC} ⁽⁴⁾	V _{CC}	—	
		I _{OH} = −12mA MIL.	2.4	4.3	—	
		I _{OH} = −15mA COM'L.	2.4	4.3	—	
V _{OL}	Output LOW Voltage	V _{CC} = 3V, V _{IN} = V _{LC} or V _{HC} , I _{OL} = 300μA	—	GND	V _{LC}	V
		V _{CC} = Min. V _{IN} = V _{IH} or V _{IL} I _{OL} = 300μA	—	GND	V _{LC} ⁽⁴⁾	
		I _{OL} = 48mA MIL. ⁽⁵⁾	—	0.3	0.55	
		I _{OL} = 64mA COM'L. ⁽⁵⁾	—	0.3	0.55	

NOTES:

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- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- This parameter is guaranteed but not tested.
- These are maximum I_{OL} values per output, for 8 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs exceeding 8 turned on simultaneously.

POWER SUPPLY CHARACTERISTICS $V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$, $V_{IN} = 3.4V$ ⁽³⁾		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$, Outputs Open $\overline{CEAB}$ and $\overline{OEAB} = \text{GND}$ $CEBA = V_{CC}$ One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$, Outputs Open $f_{CP} = 10\text{MHz}$ ($\overline{LEAB}$) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB} = \text{GND}$ $CEBA = V_{CC}$ One Bit Toggling at $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	2.2	6.0	
		$V_{CC} = \text{Max.}$, Outputs Open $f_{CP} = 10\text{MHz}$ ($\overline{LEAB}$) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB} = \text{GND}$ $CEBA = V_{CC}$ Eight Bits Toggling at $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	7.0	12.8 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	9.2	21.8 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
All currents are in milliamperes and all frequencies are in megahertz.

2614 tbl 06

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	IDT54/74FCT543				IDT54/74FCT543A				IDT54/74FCT543C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay Transparent Mode A _n to B _n or B _n to A _n	CL = 50pF RL = 500Ω	2.5	8.5	2.5	10.0	2.5	6.5	2.5	7.5	2.5	5.3	2.5	6.1	ns
tPLH tPHL	Propagation Delay LEBA to A _n , LEAB to B _n		2.5	12.5	2.5	14.0	2.5	8.0	2.5	9.0	2.5	7.0	2.5	8.0	ns
tpZH tpZL	Output Enable Time OEBA or OEAB to A _n or B _n CEBA or CEAB to A _n or B _n		2.0	12.0	2.0	14.0	2.0	9.0	2.0	10.0	2.0	8.0	2.0	9.0	ns
tpHZ tpLZ	Output Disable Time OEBA or OEAB to A _n or B _n CEBA or CEAB to A _n or B _n		2.0	9.0	2.0	13.0	2.0	7.5	2.0	8.5	2.0	6.5	2.0	7.5	ns
tsu	Set-up Time, HIGH or LOW A _n or B _n to LEBA or LEAB		3.0	—	3.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
th	Hold Time, HIGH or LOW A _n or B _n to LEBA or LEAB		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tw	LEBA or LEAB Pulse Width LOW		5.0	—	5.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns

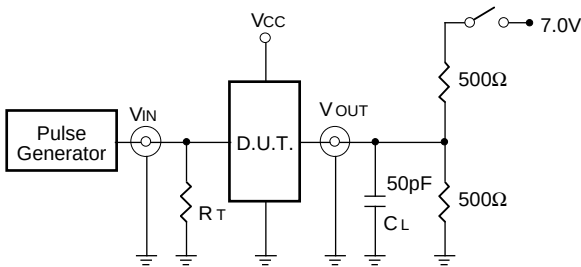
NOTES:

- See test circuits and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.

2513 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



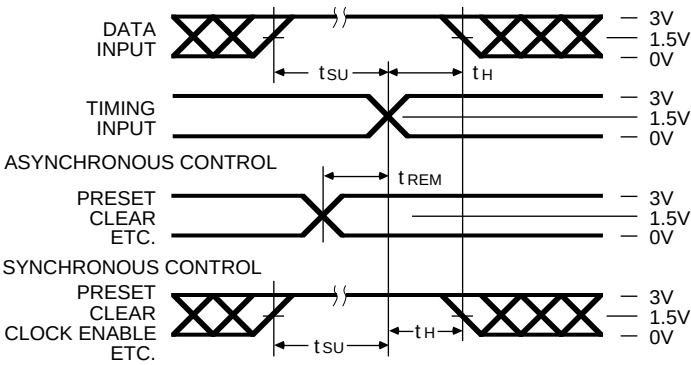
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

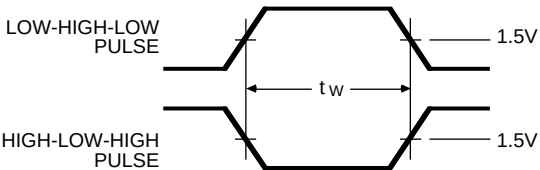
DEFINITIONS:
CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

2614 tbl 08

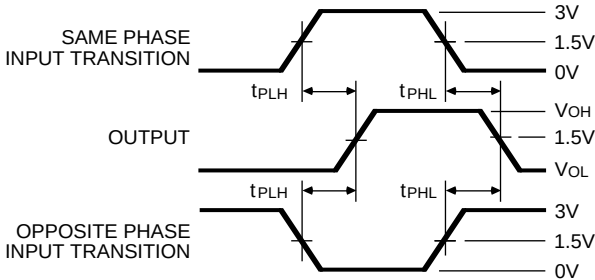
SET-UP, HOLD AND RELEASE TIMES



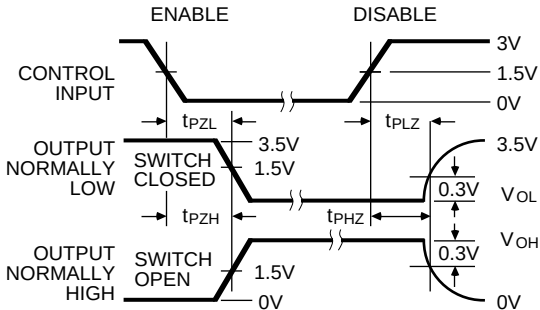
PULSE WIDTH



PROPAGATION DELAY



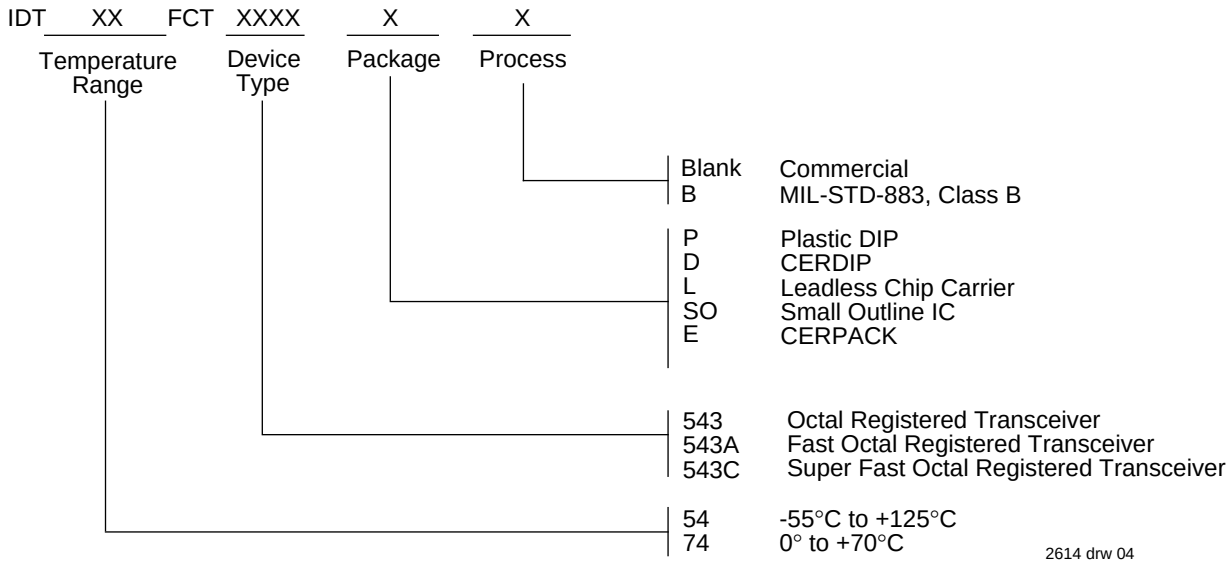
ENABLE AND DISABLE TIMES



- NOTES**
- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
 - Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; tr ≤ 2.5ns; tr ≤ 2.5ns.

2614 drw 05

ORDERING INFORMATION



2614 drw 04