June 24, 2009

LMH6654/LMH6655

Single/Dual Low Power, 250 MHz, Low Noise Amplifiers

General Description

The LMH6654/LMH6655 single and dual high speed, voltage feedback amplifiers are designed to have unity-gain stable operation with a bandwidth of 250 MHz. They operate from ±2.5V to ±6V and each channel consumes only 4.5 mA. The amplifiers feature very low voltage noise and wide output swing to maximize signal-to-noise ratio.

The LMH6654/LMH6655 have a true single supply capability with input common mode voltage range extending 150 mV below negative rail and within 1.3V of the positive rail.

LMH6654/LMH6655 high speed and low power combination make these products an ideal choice for many portable, high speed application where power is at a premium.

The LMH6654 is packaged in 5-Pin SOT-23 and 8-Pin SOIC. The LMH6655 is packaged in 8-Pin MSOP and 8-Pin SOIC.

The LMH6654/LMH6655 are built on National's Advance VIP10™ (Vertically Integrated PNP) complementary bipolar process.

Features

(V_S = ±5V, T_J = 25°C, Typical values unless specified).

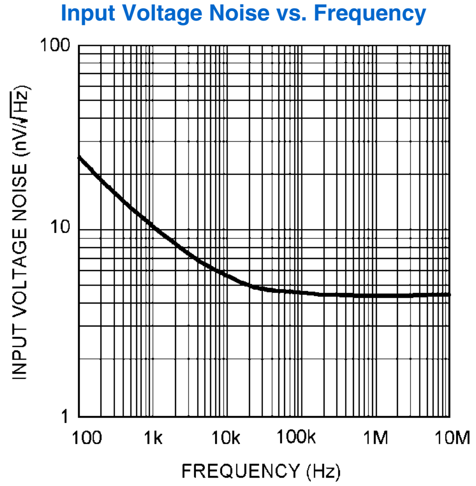
- Voltage feedback architecture
- Unity gain bandwidth 250 MHz
- Supply voltage range ±2.5V to ±6V
- Slew rate 200 V/µsec
- Supply current 4.5 mA/channel
- Input common mode voltage –5.15V to +3.7V
- Output voltage swing (R_L = 100Ω) –3.6V to 3.4V
- Input voltage noise 4.5 nV/√Hz
- Input current noise 1.7 pA/√Hz
- Settling Time to 0.01% 25 ns

Applications

- ADC drivers
- Consumer video
- Active filters
- Pulse delay circuits
- xDSL receiver
- Pre-amps

Typical Performance Characteristics

Input Voltage Noise vs. Frequency



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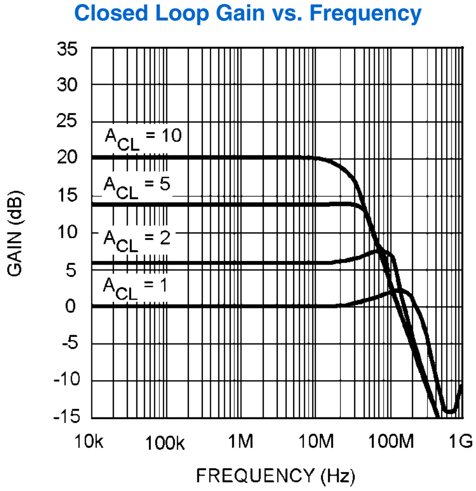
Closed Loop Gain vs. Frequency



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	2 kV
Machine Model	200V
V_{IN} Differential	±1.2V
Output Short Circuit Duration	(Note 3)
Supply Voltage ($V^+ - V^-$)	13.2V
Voltage at Input pins	V^+ +0.5V, V^- −0.5V
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	+150°C
Soldering Information	
Infrared or Convection (20 sec.)	235°C
Wave Soldering (10 sec.)	260°C

Operating Ratings (Note 1)

Supply Voltage (V^+ - V^-)	±2.5V to ±6.0V
Junction Temperature Range	−40°C to +85°C
Thermal Resistance (θ_{JA})	
8-Pin SOIC	172°C/W
8-Pin MSOP	235°C/W
5-Pin SOT-23	265°C/W

±5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = +5V, V^- = −5V, V_{CM} = 0V, A_V = +1, R_F = 25Ω for gain = +1, R_F = 402Ω for gain = ≥ +2, and R_L = 100Ω. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
Dynamic Performance						
f_{CL}	Close Loop Bandwidth	A_V = +1		250		MHz
		A_V = +2		130		
		A_V = +5		52		
		A_V = +10		26		
GBWP	Gain Bandwidth Product	A_V ≥ +5		260		MHz
	Bandwidth for 0.1 dB Flatness	A_V +1		18		MHz
φm	Phase Margin			50		deg
SR	Slew Rate (Note 8)	A_V = +1, V_{IN} = 2 V_{PP}		200		V/μs
t_S	Settling Time 0.01%	A_V = +1, 2V Step		25		ns
	0.1%			15		ns
t_r	Rise Time	A_V = +1, 0.2V Step		1.4		ns
t_f	Fall Time	A_V = +1, 0.2V Step		1.2		ns
Distortion and Noise Response						
e_n	Input Referred Voltage Noise	f ≥ 0.1 MHz		4.5		$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	f ≥ 0.1 MHz		1.7		$pA/\sqrt{Hz}$
	Second Harmonic Distortion	A_V = +1, f = 5 MHz		−80		dBc
	Third Harmonic Distortion	V_O = 2 V_{PP}, R_L = 100Ω		−85		
X_t	Crosstalk (for LMH6655 only)	Input Referred, 5 MHz, Channel-to-Channel		−80		dB
DG	Differential Gain	A_V = +2, NTSC, R_L = 150Ω		0.01		%
DP	Differential Phase	A_V = +2, NTSC, R_L = 150Ω		0.025		deg
Input Characteristics						
V_{OS}	Input Offset Voltage	V_{CM} = 0V	−3 **−4**	±1	3 **4**	mV
TC V_{OS}	Input Offset Average Drift	V_{CM} = 0V (Note 7)		6		μV/°C
I_B	Input Bias Current	V_{CM} = 0V		5	12 **18**	μA
I_{OS}	Input Offset Current	V_{CM} = 0V	−1 **−2**	0.3	1 **2**	μA
R_{IN}	Input Resistance	Common Mode		4		MΩ
		Differential Mode		20		kΩ

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
C_{IN}	Input Capacitance	Common Mode		1.8		pF
		Differential Mode		1		
CMRR	Common Mode Rejection Ration	Input Referred, V_{CM} = 0V to –5V	70 **68**	90		dB
CMVR	Input Common- Mode Voltage Range	CMRR ≥ 50 dB		–5.15	–5.0	V
			3.5	3.7		
Transfer Characteristics						
A_{VOL}	Large Signal Voltage Gain	V_O = 4 V_{PP}, R_L = 100Ω	60 **58**	67		dB
Output Characteristics						
V_O	Output Swing High	No Load	3.4 **3.2**	3.6		V
	Output Swing Low	No Load		–3.9	–3.7 **–3.5**	
	Output Swing High	R_L = 100Ω	3.2 **3.0**	3.4		
	Output Swing Low	R_L = 100Ω		–3.6	–3.4 **–3.2**	
I_{SC}	Short Circuit Current (Note 3)	Sourcing, V_O = 0V ΔV_{IN} = 200 mV	145 **130**	280		mA
		Sinking, V_O = 0V ΔV_{IN} = 200 mV	100 **80**	185		
I_{OUT}	Output Current	Sourcing, V_O = +3V		80		mA
		Sinking, V_O = –3V		120		
R_O	Output Resistance	A_V = +1, f <100 kHz		0.08		Ω
Power Supply						
PSRR	Power Supply Rejection Ratio	Input Referred, V_S = ±5V to ±6V	60	76		dB
I_S	Supply Current (per channel)			4.5	6 **7**	mA

5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = +5V, V^- = –0V, V_{CM} = 2.5V, A_V = +1, R_F = 25Ω for gain = +1, R_F = 402Ω for gain = ≥ +2, and R_L = 100Ω to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
Dynamic Performance						
f_{CL}	Close Loop Bandwidth	A_V = +1		230		MHz
		A_V = +2		120		
		A_V = +5		50		
		A_V = +10		25		
GBWP	Gain Bandwidth Product	A_V ≥ +5		250		MHz
	Bandwidth for 0.1 dB Flatness	A_V = +1		17		MHz
φm	Phase Margin			48		deg
SR	Slew Rate (Note 8)	A_V = +1, V_{IN} = 2 V_{PP}		190		V/μs
t_S	Settling Time 0.01%	A_V = +1, 2V Step		30		ns
	0.1%			20		ns
t_r	Rise Time	A_V = +1, 0.2V Step		1.5		ns
t_f	Fall Time	A_V = +1, 0.2V Step		1.35		ns

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
Distortion and Noise Response						
e_n	Input Referred Voltage Noise	f ≥ 0.1 MHz		4.5		$nV/\sqrt{Hz}$
i_n	Input Referred Current Noise	f ≥ 0.1 MHz		1.7		$pA/\sqrt{Hz}$
	Second Harmonic Distortion	A_V = +1, f = 5 MHz		−65		dBc
	Third Harmonic Distortion	V_O = 2 V_{PP}, R_L = 100Ω		−70		
X_t	Crosstalk (for LMH6655 only)	Input Referred, 5 MHz		−78		dB
Input Characteristics						
V_{OS}	Input Offset Voltage	V_{CM} = 2.5V	−5 **−6.5**	±2	5 **6.5**	mV
TC V_{OS}	Input Offset Average Drift	V_{CM} = 2.5V (Note 7)		**6**		μV/°C
I_B	Input Bias Current	V_{CM} = 2.5V		6	12 **18**	μA
I_{OS}	Input Offset Current	V_{CM} = 2.5V	−2 **−3**	0.5	2 **3**	μA
R_{IN}	Input Resistance	Common Mode		4		MΩ
		Differential Mode		20		kΩ
C_{IN}	Input Capacitance	Common Mode		1.8		pF
		Differential Mode		1		
CMRR	Common Mode Rejection Ration	Input Referred, V_{CM} = 0V to −2.5V	70 **68**	90		dB
CMVR	Input Common Mode Voltage Range	CMRR ≥ 50 dB		−0.15	0	V
			3.5	3.7		
Transfer Characteristics						
A_{VOL}	Large Signal Voltage Gain	V_O = 1.6 V_{PP}, R_L = 100Ω	58 **55**	64		dB
Output Characteristics						
V_O	Output Swing High	No Load	3.6 **3.4**	3.75		V
	Output Swing Low	No Load		0.9	1.1 **1.3**	
	Output Swing High	R_L = 100Ω	3.5 **3.35**	3.70		
	Output Swing Low	R_L = 100Ω		1	1.3 **1.45**	
I_{SC}	Short Circuit Current (Note 3)	Sourcing , V_O = 2.5V ΔV_{IN} = 200 mV	90 **80**	170		mA
		Sinking, V_O = 2.5V ΔV_{IN} = 200 mV	70 **60**	140		
I_{OUT}	Output Current	Sourcing, V_O = +3.5V		30		mA
		Sinking, V_O = 1.5V		60		
R_O	Output Resistance	A_V = +1, f <100 kHz		.08		Ω
Power Supply						
PSRR	Power Supply Rejection Ratio	Input Referred , V_S = ± 2.5V to ± 3V	60	75		dB
I_S	Supply Current (per channel)			4.5	6 **7**	mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Table.

Note 2: Human body model, 1.5 kΩ in series with 100 pF. Machine model: 0Ω in series with 100 pF.

Note 3: Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C.

Note 4: The maximum power dissipation is a function of $T_{J(MAX)}$, $θ_{JA}$ and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/θ_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 5: Typical Values represent the most likely parametric norm.

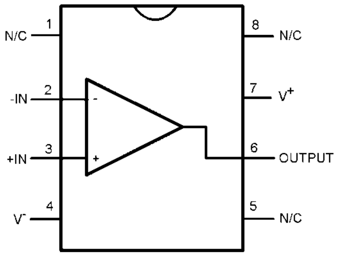
Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Offset voltage average drift is determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

Note 8: Slew rate is the slower of the rising and falling slew rates. Slew rate is rate of change from 10% to 90% of output voltage step.

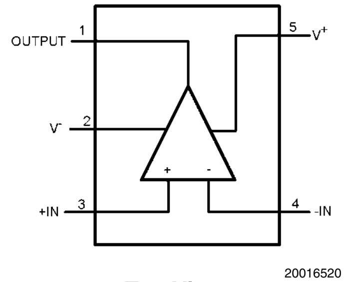
Connection Diagrams

8-Pin SOIC (LMH6654)



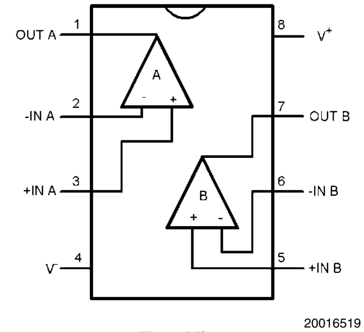
Top View

5-Pin SOT-23 (LMH6654)



Top View

8-Pin SOIC and MSOP (LMH6655)



Top View

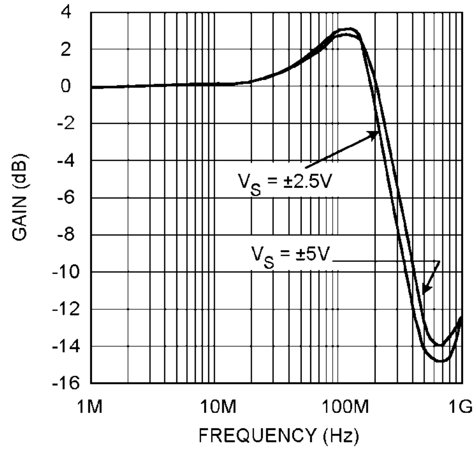
Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Pin SOIC	LMH6654MA	LMH6654MA	95 Units Rails	M08A
	LMH6654MAX		2.5k Units Tape and Reel	
	LMH6655MA	LMH6655MA	95 Units Rails	
	LMH6655MAX		2.5k Units Tape and Reel	
5-Pin SOT-23	LMH6654MF	A66A	1k Units Tape and Reel	MF05A
	LMH6654MFX		3K Units Tape and Reel	
8-Pin MSOP	LMH6655MM	A67A	1k Units Tape and Reel	MUA08A
	LMH6655MMX		3.5k Units Tape and Reel	

Typical Performance Characteristics

$T_J = 25°C$, $V^+ = \pm 5V$, $V^- = -5$, $R_F = 25\Omega$ for gain = +1, $R_F = 402\Omega$ and for gain ≥ +2, and $R_L = 100\Omega$, unless otherwise specified.

Closed Loop Bandwidth (G = +1)



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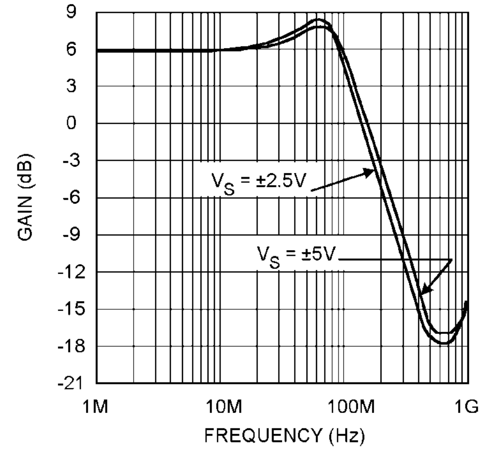
Closed Loop Bandwidth (G = +2)



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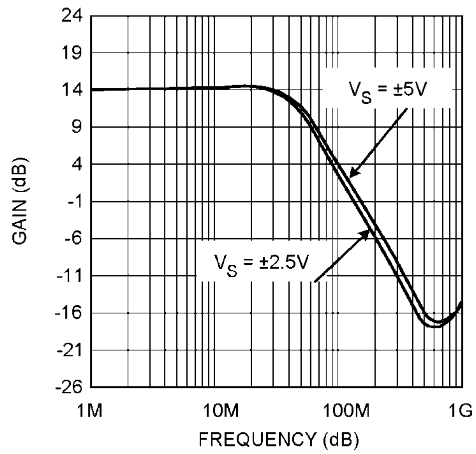
Closed Loop Bandwidth (G = +5)



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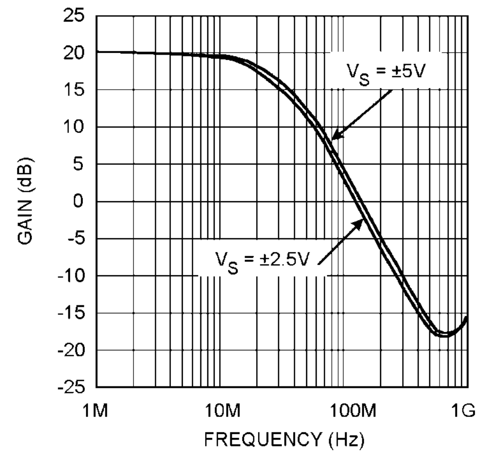
Closed Loop Bandwidth (G = +10)



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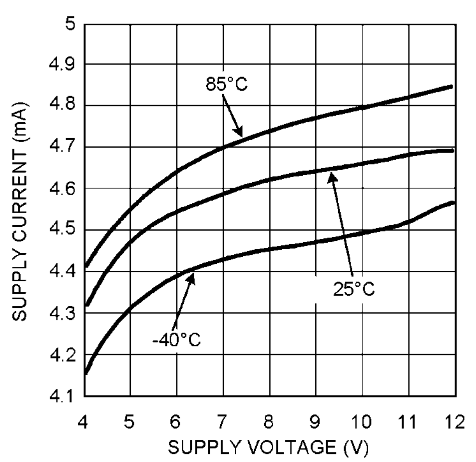
Supply Current per Channel vs. Supply Voltage



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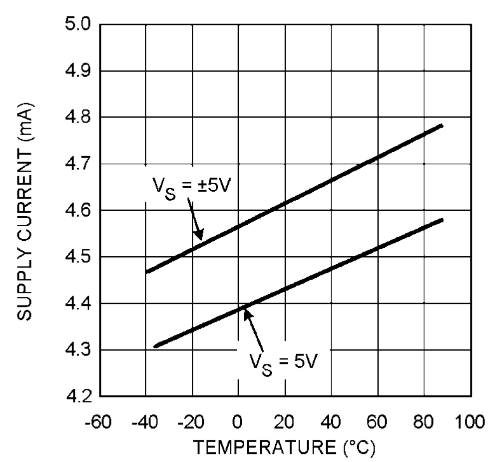
Supply Current per Channel vs. Temperature



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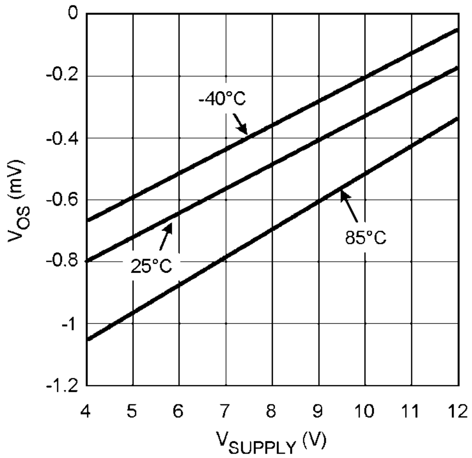
Offset Voltage vs. Supply Voltage (V_{CM} = 0V)



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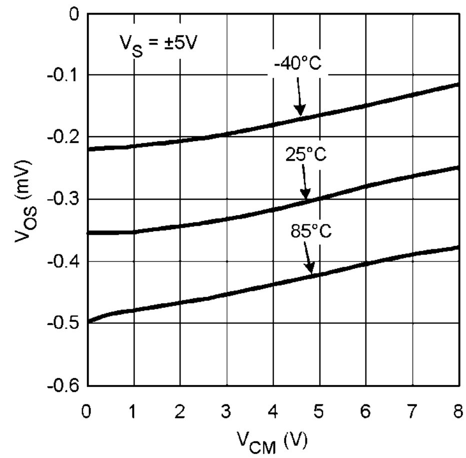
Offset Voltage vs. Common Mode



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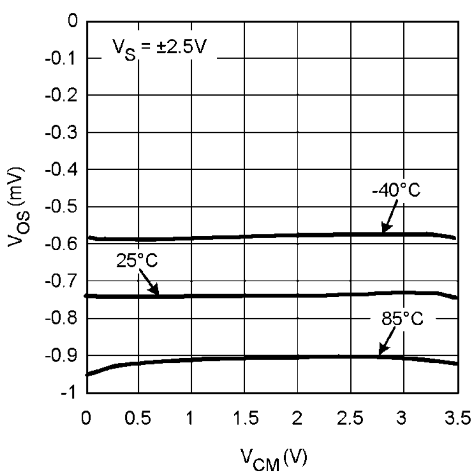
Offset Voltage vs. Common Mode



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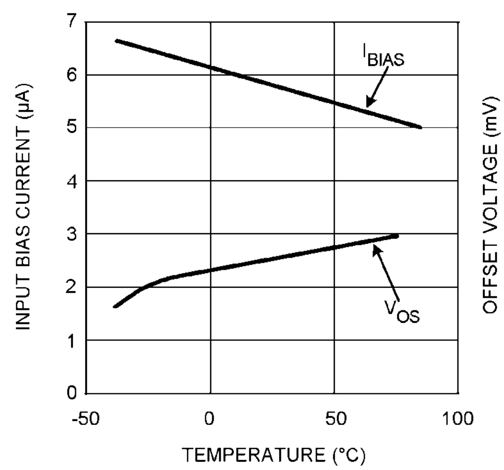
Bias Current and Offset Voltage vs. Temperature



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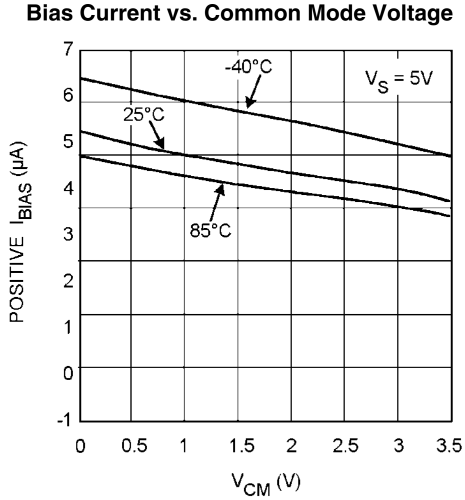
Bias Current vs. Common Mode Voltage



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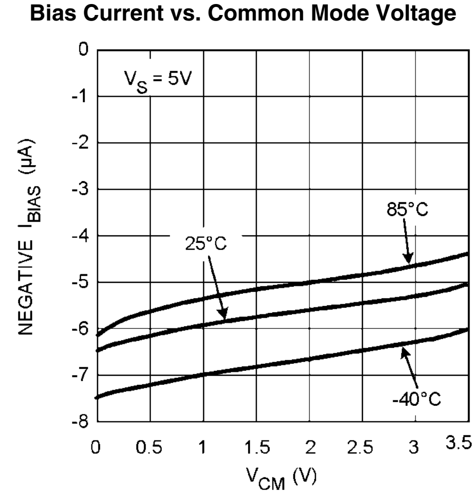
Bias Current vs. Common Mode Voltage



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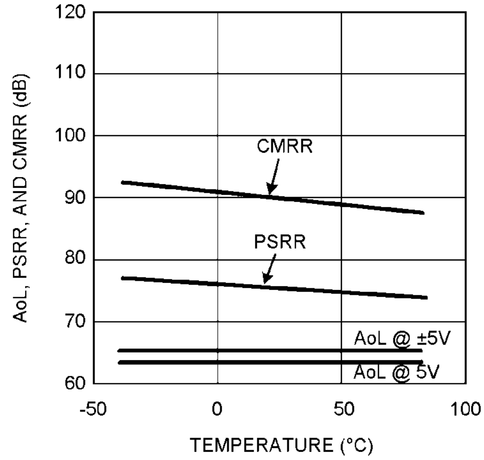
A_{OL}, PSRR and CMRR vs. Temperature



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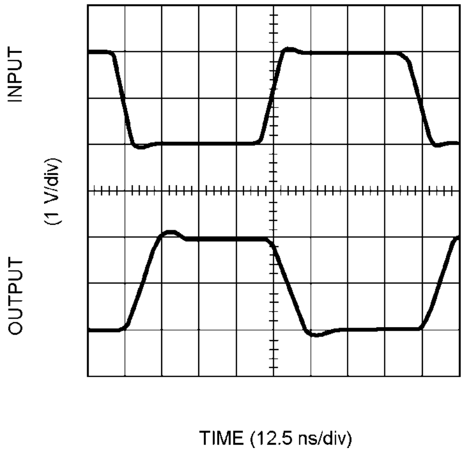
Inverting Large Signal Pulse Response (V_S = 5V)



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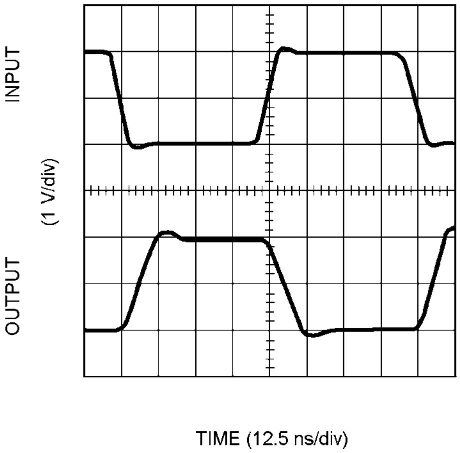
Inverting Large Signal Pulse Response (V_S = ±5V)



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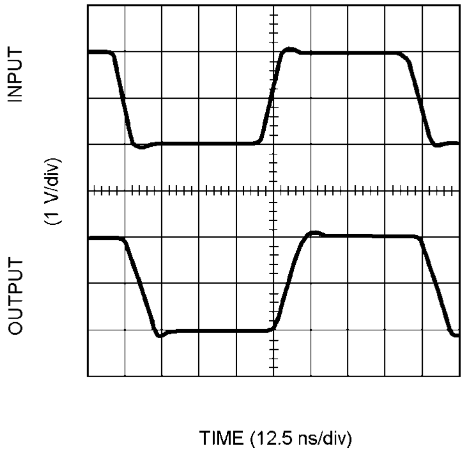
Non-Inverting Large Signal Pulse Response (V_S = 5V)



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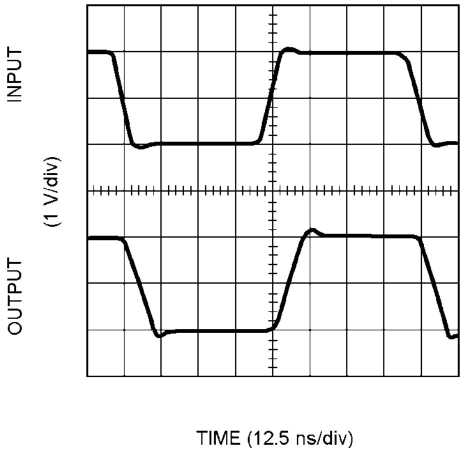
Non-Inverting Large Signal Pulse Response (V_S = ±5V)



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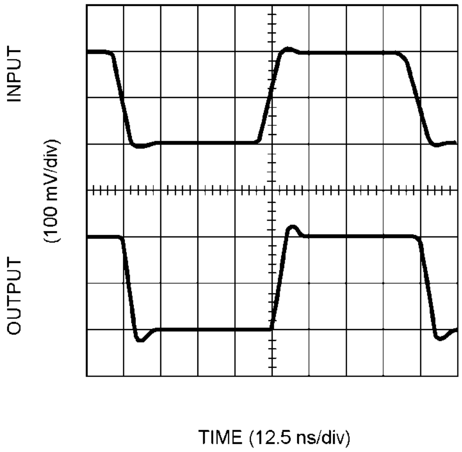
Non-Inverting Small Signal Pulse Response (V_S = 5V)



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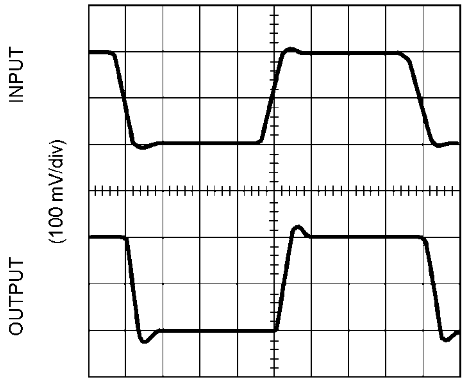
Non-Inverting Small Signal Pulse Response (V_S = ±5V)



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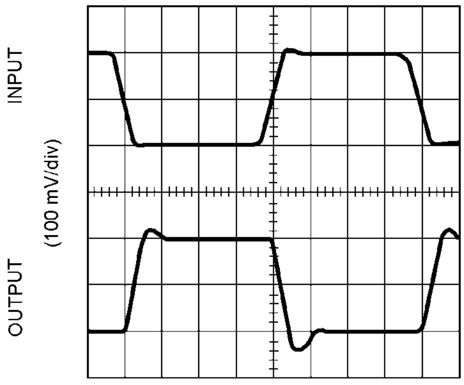
Inverting Small Signal Pulse Response (V_S = 5V)



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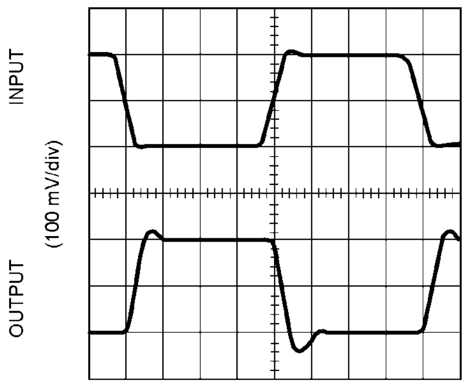
Inverting Small Signal Pulse Response (V_S = ±5V)



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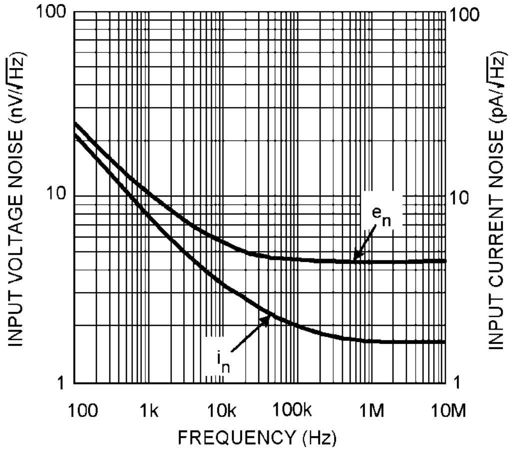
Input Voltage and Current Noise vs. Frequency (V_S = 5V)



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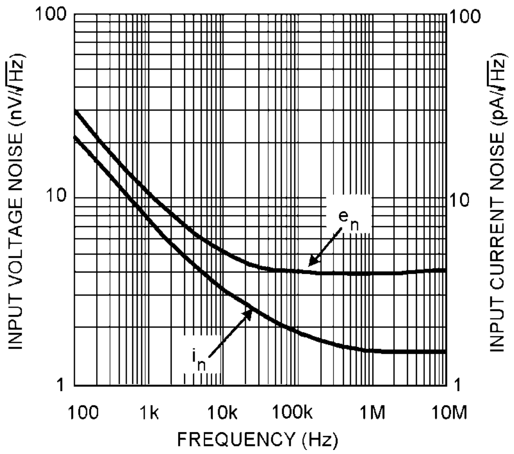
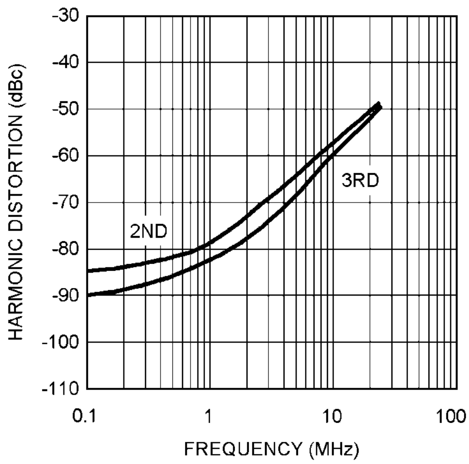
Input Voltage and Current Noise vs. Frequency (V_S = ±5V)



20016514

Harmonic Distortion vs. Frequency G = +1, V_O = 2 V_{PP}, V_S = 5V



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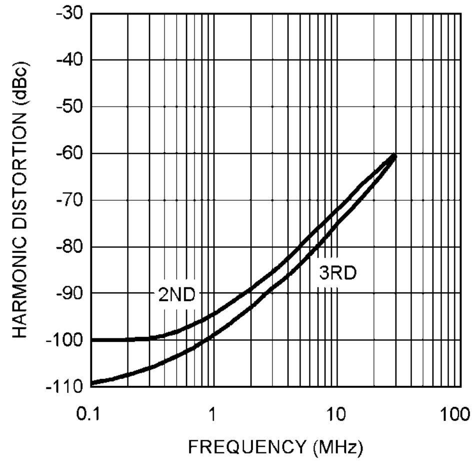
Harmonic Distortion vs. Frequency
G = +1, V_O = 2 V_{PP}, V_S = ±5V



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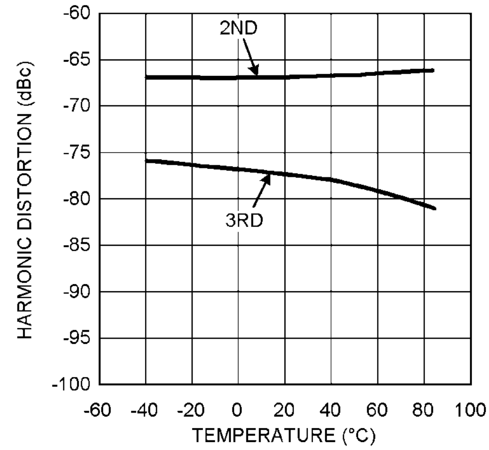
Harmonic Distortion vs. Temperature
V_S = 5V, f = 5 MHz, V_O = 2 V_{PP}



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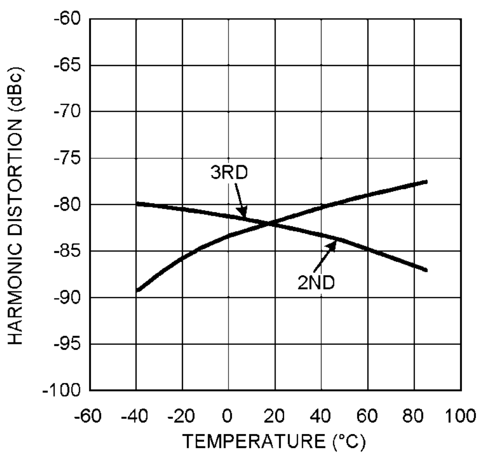
Harmonic Distortion vs. Temperature
V_S = ±5V, f = 5 MHz, V_O = 2 V_{PP}



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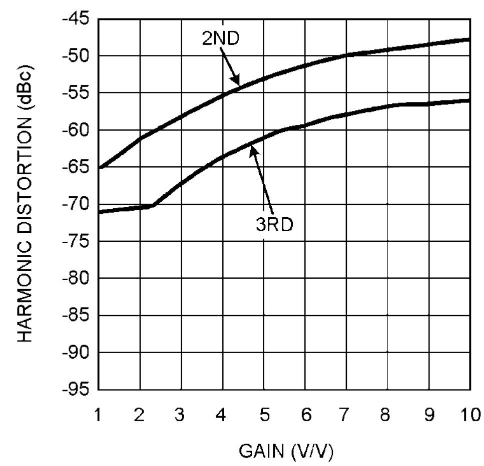
Harmonic Distortion vs. Gain
V_S = 5V, f = 5 MHz, V_O = 2 V_{PP}



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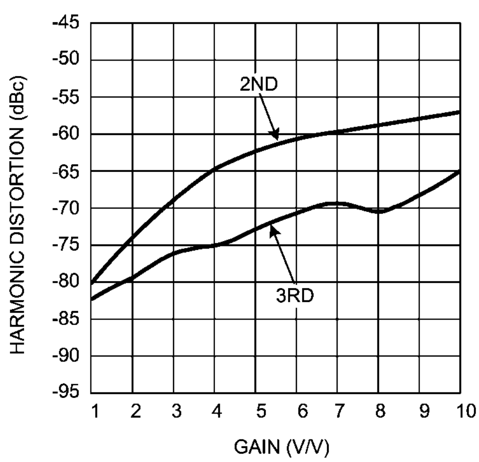
Harmonic Distortion vs. Gain
V_S = ±5V, f = 5 MHz, V_O = 2 V_{PP}



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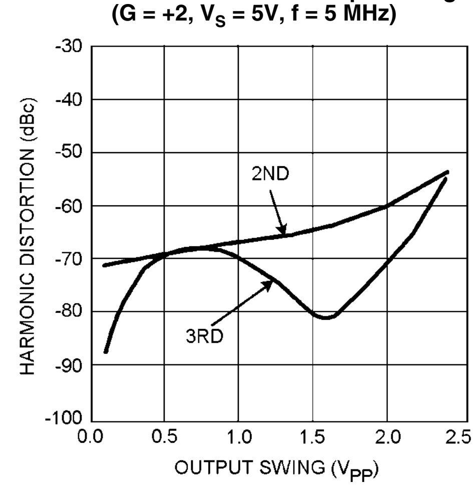
Harmonic Distortion vs. Output Swing
(G = +2, V_S = 5V, f = 5 MHz)



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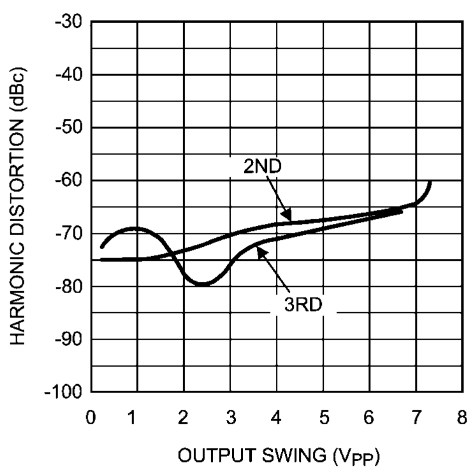
Harmonic Distortion vs. Output Swing ($G = +2$, $V_S = \pm 5V$, $f = 5$ MHz)



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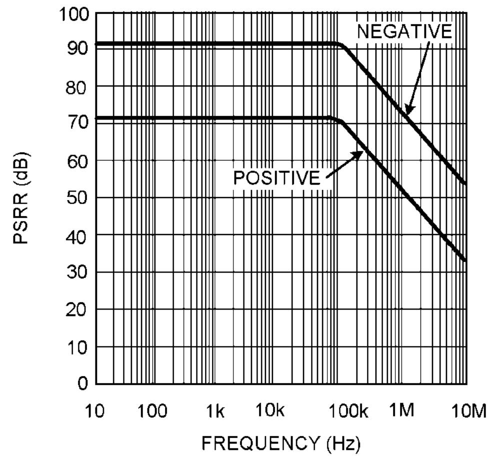
PSRR vs. Frequency



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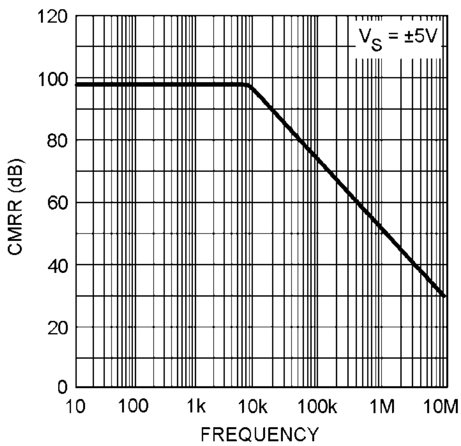
CMRR vs. Frequency



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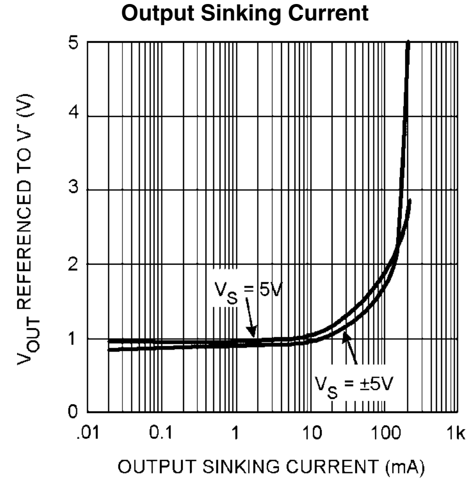
Output Sinking Current



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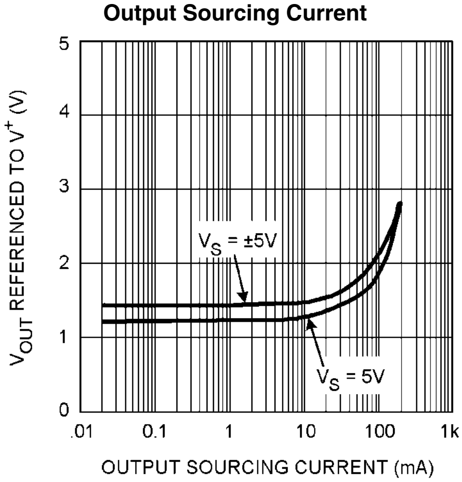
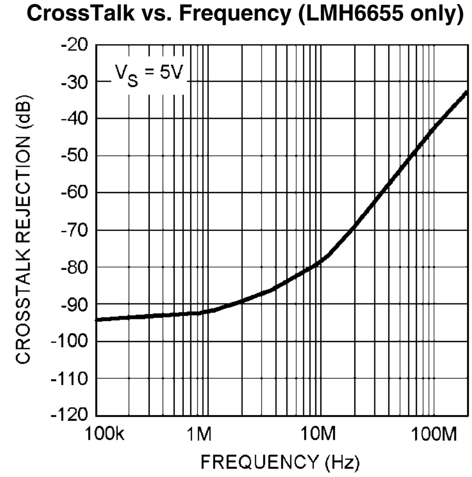
Output Sourcing Current



20016547

CrossTalk vs. Frequency (LMH6655 only)



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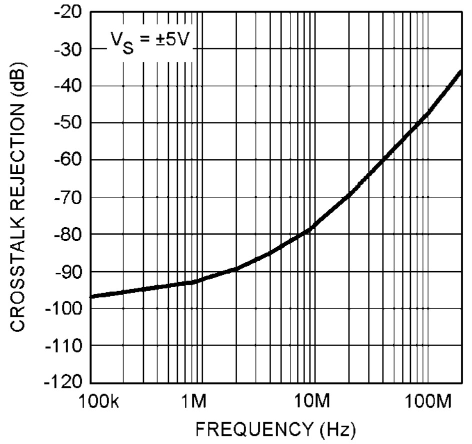
CrossTalk vs. Frequency (LMH6655 only)



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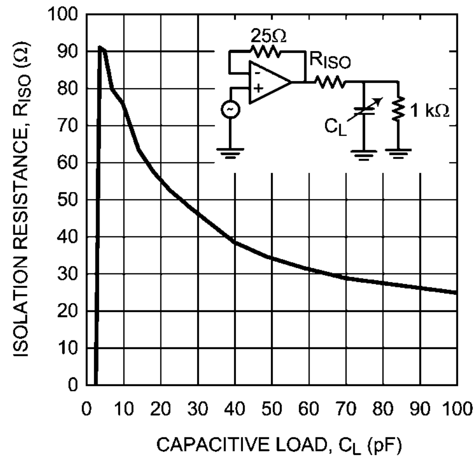
Isolation Resistance vs. Capacitive Load



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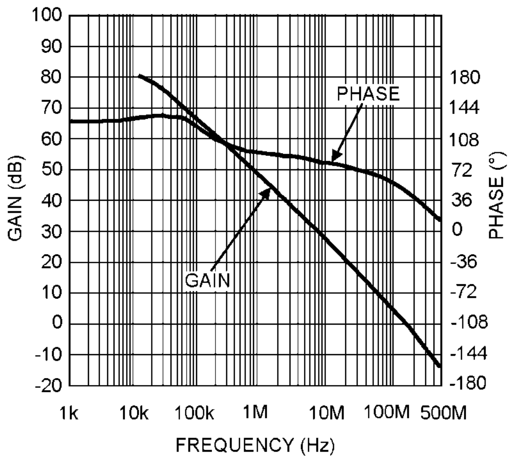
Open Loop Gain and Phase vs. Frequency



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Application Information

GENERAL INFORMATION

The LMH6654 single and LMH6655 dual high speed, voltage feedback amplifiers are manufactured on National Semiconductor's new VIP10 (Vertically Integrated PNP) complementary bipolar process. These amplifiers can operate from ±2.5V to ±6V power supply. They offer low supply current, wide bandwidth, very low voltage noise and large output swing. Many of the typical performance plots found in the datasheet can be reproduced if 50Ω coax and 50Ω $R_{IN}/_{ROUT}$ resistors are used.

CIRCUIT LAYOUT CONSIDERATION

With all high frequency devices, board layouts with stray capacitance have a strong influence on the AC performance. The LMH6654/LMH6655 are not exception and the inverting input and output pins are particularly sensitive to the coupling of parasitic capacitance to AC ground. Parasitic capacitances on the inverting input and output nodes to ground could cause frequency response peaking and possible circuit oscillation. Therefore, the power supply, ground traces and ground plan should be placed away from the inverting input and output pins. Also, it is very important to keep the parasitic capacitance across the feedback to an absolute minimum.

The PCB should have a ground plane covering all unused portion of the component side of the board to provide a low impedance path. All trace lengths should be minimized to reduce series inductance.

Supply bypassing is required for the amplifiers performance. The bypass capacitors provide a low impedance return current path at the supply pins. They also provide high frequency filtering on the power supply traces. It is recommended that a ceramic decoupling capacitor 0.1 µF chip should be placed with one end connected to the ground plane and the other side as close as possible to the power pins. An additional 10 µF tantalum electrolytic capacitor should be connected in parallel, to supply current for fast large signal changes at the output.

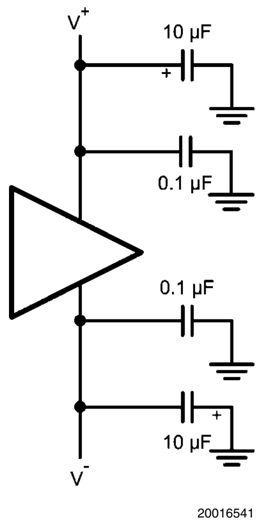

FIGURE 1.

EVALUATION BOARDS

National provides the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization.

Device	Package	Evalulation Board PN
LMH6654MF	5-Pin SOT-23	CLC730068
LMH6654MA	8-Pin SOIC	CLC730027
LMH6655MA	8-Pin SOIC	CLC730036
LMH6655MM	8-Pin MSOP	CLC730123

The free evaluation board are shipped automatically when a device sample request is placed with National Semiconductor.

The CLC730027 datasheet also contains tables of recommended components to evaluate several of National's high speed amplifiers. This table for the LMH6654 is illustrated below. Refer to the evaluation board datasheet for schematics and further information.

Components Needed to Evaluate the LMH6654 on the Evaluation Board:

- R_fR_g use the datasheet to select values.
- R_{IN}, R_{OUT} typically 50Ω (Refer to the Basic Operation section of the evaluation board datasheet for details)
- R_t is an optional resistor for inverting again configurations (select R_t to yield desired input impedance = $R_g||R_t$)
- C_1, C_2 use 0.1 µF ceramic capacitors
- C_3, C_4 use 10 µF tantalum capacitors

Components not used:

1. C_5, C_6, C_7, C_8
2. R1 thru R8

The evaluation boards are designed to accommodate dual supplies. The board can be modified to provide single operation. For best performance;

1) do not connect the unused supply.

2) ground the unused supply pin.

POWER DISSIPATION

The package power dissipation should be taken into account when operating at high ambient temperature and/or high power dissipative conditions. In determining maximum operable temperature of the device, make sure the total power dissipation of the device is considered; this power dissipated in the device with a load connected to the output as well as the nominal dissipation of the op amp.

DRIVING CAPACITIVE LOADS

Capacitive loads decrease the phase margin of all op amps. The output impedance of a feedback amplifier becomes inductive at high frequencies, creating a resonant circuit when the load is capacitive. This can lead to overshoot, ringing and oscillation. To eliminate oscillation or reduce ringing, an isolation resistor can be placed as shown in *Figure 2* below. At frequencies above

$$F = \frac{1}{2\pi R_{ISO} C_{LOAD}}$$

the load impedance of the Amplifier approaches R_{ISO}. The desired performance depends on the value of the isolation resistor. The isolation resistance vs. capacitance load graph in the typical performance characteristics provides the means for selection of the value of R_S that provides ≤ 3 dB peaking in closed loop A_V = 1 response. In general, the bigger the isolation resistor, the more damped the pulse response becomes. For initial evaluation, a 50Ω isolation resistor is recommended.

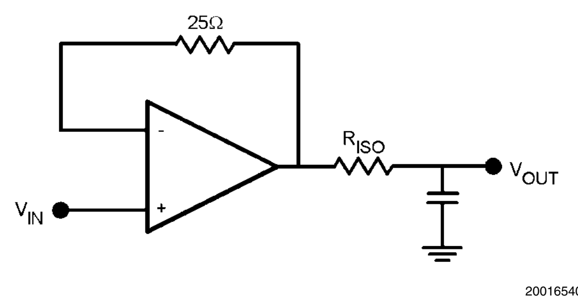

FIGURE 2.

COMPONENTS SELECTION AND FEEDBACK RESISTOR

It is important in high-speed applications to keep all component leads short since wires are inductive at high frequency. For discrete components, choose carbon composition axially leaded resistors and micro type capacitors. Surface mount components are preferred over discrete components for minimum inductive effect. Never use wire wound type resistors in high frequency applications.

Large values of feedback resistors can couple with parasitic capacitance and cause undesired effects such as ringing or oscillation in high-speed amplifiers. Keep resistors as low as possible consistent with output loading consideration. For a gain of 2 and higher, 402Ω feedback resistor used for the typical performance plots gives optimal performance. For unity gain follower, a 25Ω feedback resistor is recommended rather than a direct short. This effectively reduces the Q of what would otherwise be a parasitic inductance (the feedback wire) into the parasitic capacitance at the inverting input.

BIAS CURRENT CANCELLATION

In order to cancel the bias current errors of the non-inverting configuration, the parallel combination of the gain setting R_g and feedback R_f resistors should equal the equivalent source resistance R_{seq} as defined in *Figure 3*. Combining this constraint with the non-inverting gain equation, allows both R_f and R_g to be determined explicitly from the following equations:

$$R_f = A_V R_{seq} \text{ and } R_g = R_f/(A_V-1)$$

For inverting configuration, bias current cancellation is accomplished by placing a resistor R_b on the non-inverting input equal in value to the resistance seen by the inverting input $(R_f//(R_g+R_s))$. The additional noise contribution of R_b can be minimized through the use of a shunt capacitor.

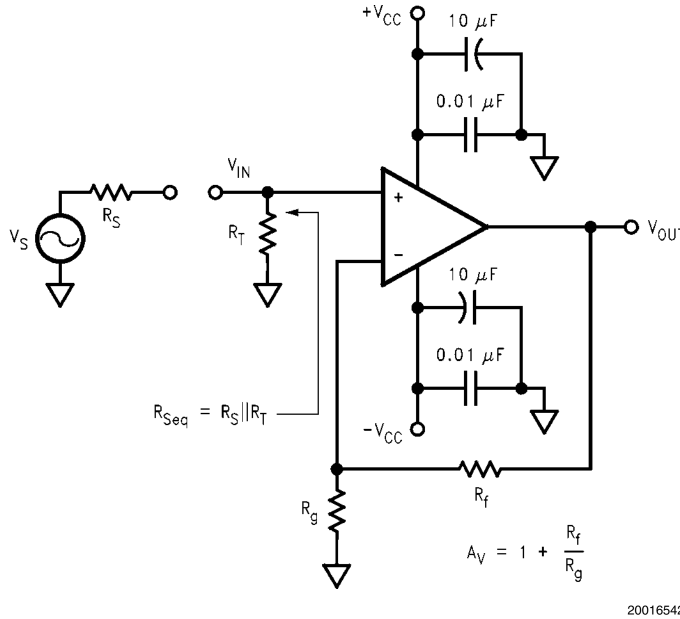

FIGURE 3. Non-Inverting Amplifier Configuration

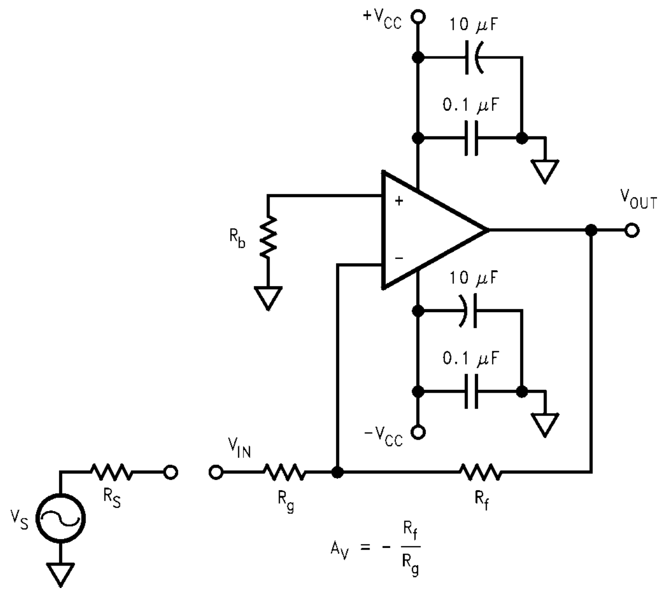

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FIGURE 4. Inverting Amplifier Configuration

TOTAL INPUT NOISE VS. SOURCE RESISTANCE

The noise model for the non-inverting amplifier configuration showing all noise sources is described in *Figure 5*. In addition to the intrinsic input voltage noise (e_n) and current noise ($i_n = i_{n+} = i_{n-}$) sources, there also exits thermal voltage noise $e_t = \sqrt{4kTR}$ associated with each of the external resistors. Equation 1 provides the general form for total equivalent input voltage noise density (e_{ni}). Equation 2 is a simplification of Equation 1 that assumes

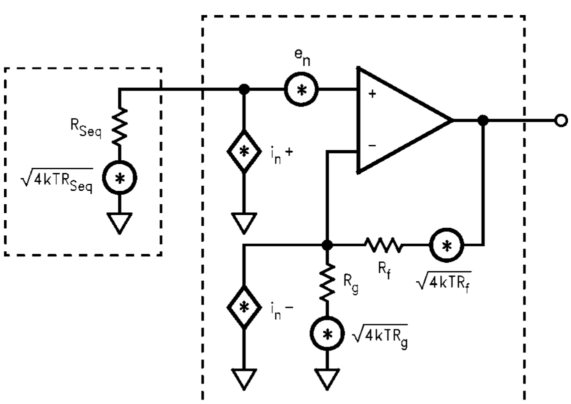

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FIGURE 5. Non-Inverting Amplifier Noise Model

$$e_{ni} = \sqrt{e_n^2 + (i_n + R_{seq})^2 + 4kTR_{seq} + (i_n - (R_f \,||\, R_g))^2 + 4kT(R_f \,||\, R_g)} \quad (1)$$

$R_f || R_g = R_{seq}$ for bias current cancellation. *Figure 6* illustrates the equivalent noise model using this assumption. The total equivalent output voltage noise (e_{no}) is e_{ni} * A_V.

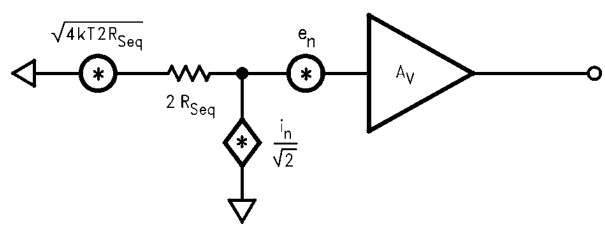

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FIGURE 6. Noise Model with $R_f || R_g = R_{seq}$

$$e_{ni} = \sqrt{e_n^2 + 2\,(i_n \; R_{seq})^2 + 4kT\,(2R_{seq})} \quad (2)$$

If bias current cancellation is not a requirement, then $R_f || R_g$ does not need to equal R_{seq}. In this case, according to Equation 1, $R_f R_g$ should be as low as possible in order to minimize noise. Results similar to Equation 1 are obtained for the inverting configuration on *Figure 2* if R_{seq} is replaced by R_b and R_g is replaced by $R_g + R_s$. With these substitutions, Equation 1 will yield an e_{ni} referred to the non-inverting input. Referring to e_{ni} to the inverting input is easily accomplished by multiplying e_{ni} by the ration of non-inverting to inverting gains.

Noise Figure

Noise Figure (NF) is a measure of the noise degradation caused by an amplifier.

$$NF = 10LOG\left[\frac{S_i/N_i}{S_o/N_o}\right] = 10LOG\left[\frac{e_{ni}^2}{e_t^2}\right] \quad (3)$$

The noise figure formula is shown is Equation 3. The addition of a terminating resistor R_T, reduces the external thermal noise but increases the resulting NF.

The NF is increased because the R_T reduces the input signal amplitude thus reducing the input SNR.

$$NF = 10\ LOG\left[\frac{e_n^{\,2} + i_n^{\,2}\,(R_{seq} + (R_f \,||\, R_g)^2 + 4KTR_{seq} + 4kt\,(R_f \,||\, R_g)}{4kTR_{seq}}\right] \quad (4)$$

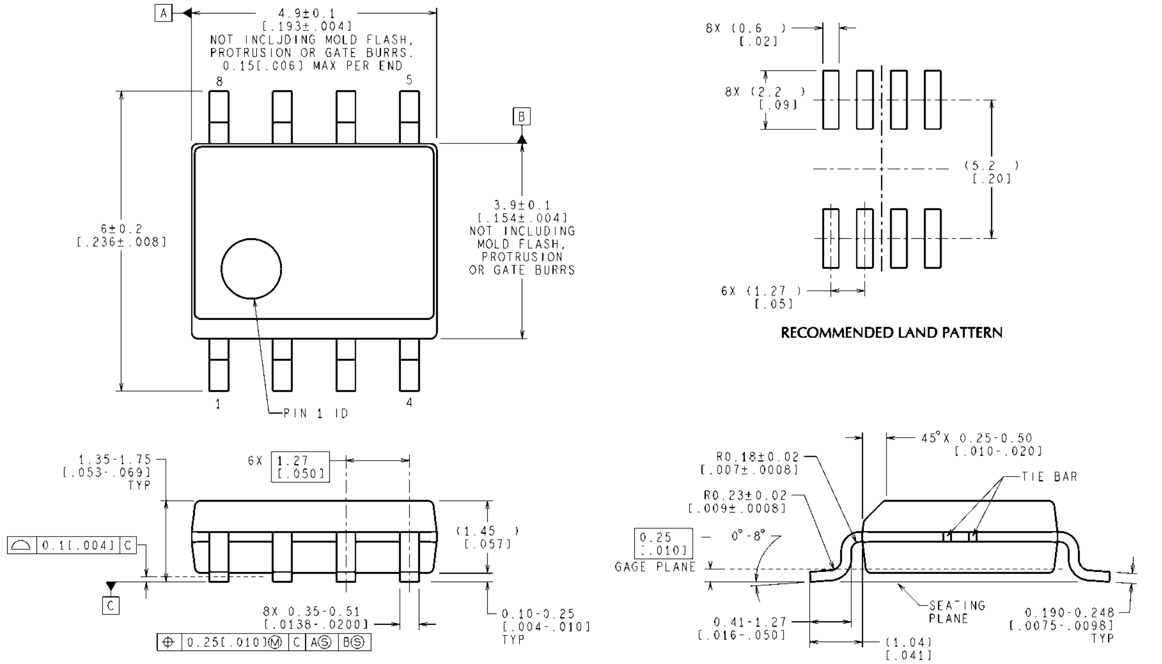
The noise figure is related to the equivalent source resistance (R_{seq}) and the parallel combination of R_f and R_g. To minimize noise figure, the following steps are recommended:

1. Minimize $R_f || R_g$
2. Choose the Optimum R_s (R_{OPT})

R_{OPT} is the point at which the NF curve reaches a minimum and is approximated by:

$R_{OPT} \approx (e_n/i_n)$

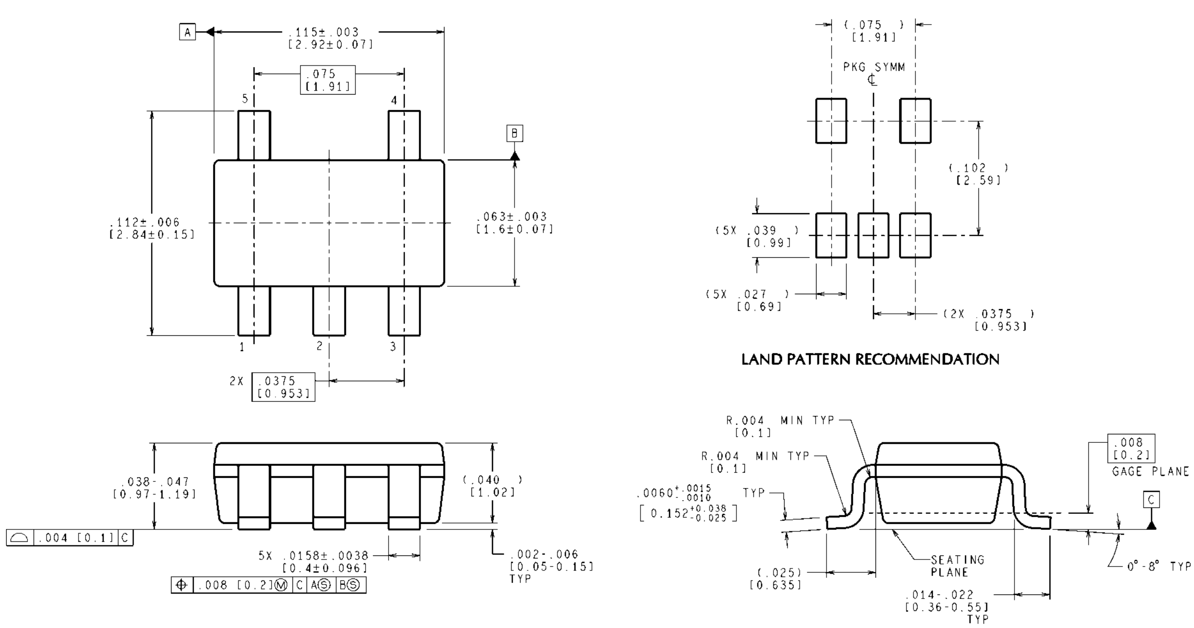
Physical Dimensions inches (millimeters) unless otherwise noted



CONTROLLING DIMENSION IS MILLIMETER
VALUES IN [ ] ARE INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

M08A (Rev M)

8-Pin SOIC
NS Package Number M08A



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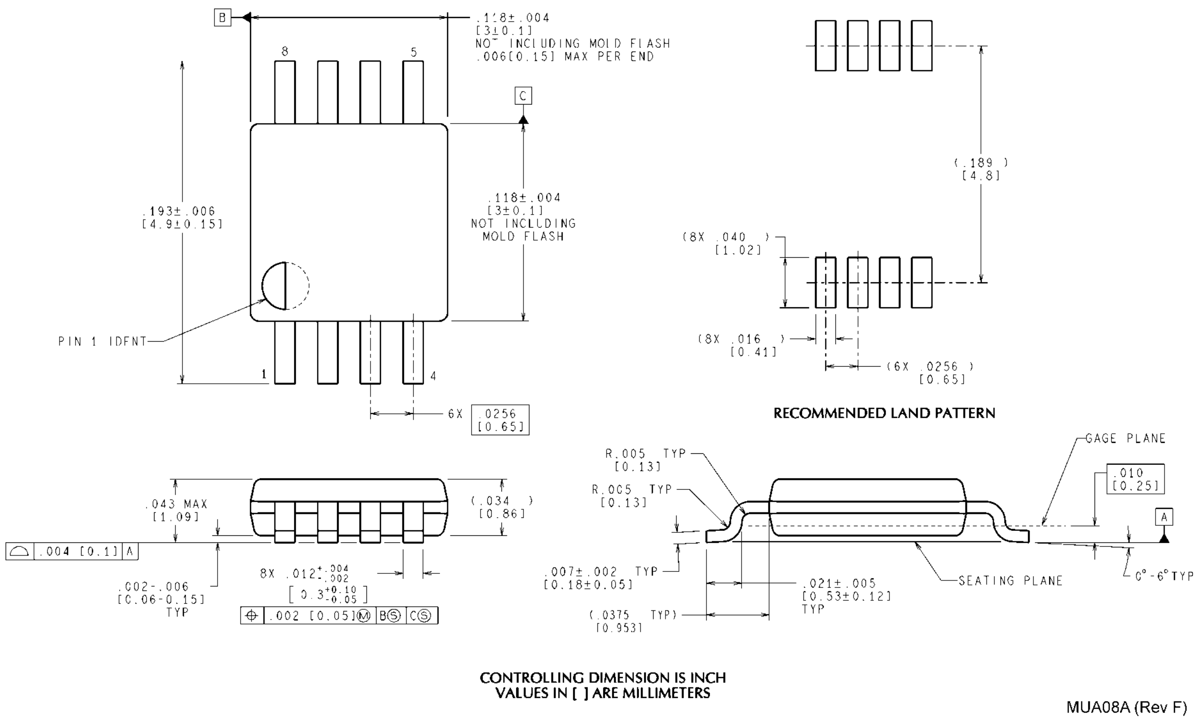
MF05A (Rev D)

5-Pin SOT-23
NS Package Number MF05A



MUA08A (Rev F)

8-Pin MSOP
NS Package Number MUA08A

Notes

Notes

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