

CYPRESS  
SEMICONDUCTORCY7C130/CY7C131  
CY7C140/CY7C1411024 x 8 Dual-Port  
Static RAM

## Features

- 0.8-micron CMOS for optimum speed/power
- Automatic power-down
- TTL compatible
- Capable of withstanding greater than 2001V electrostatic discharge
- Fully asynchronous operation
- Master CY7C130/CY7C131 easily expands data bus width to 16 or more bits using SLAVE CY7C140/CY7C141
- BUSY output flag on CY7C130/CY7C131; BUSY input on CY7C140/CY7C141
- INT flag for port-to-port communication

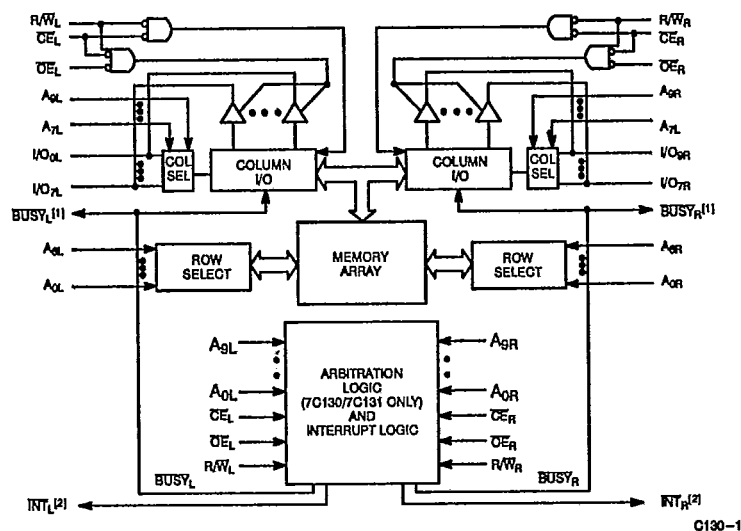
## Functional Description

The CY7C130/CY7C131/CY7C140/CY7C141 are high-speed CMOS 1K by 8 dual-port static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C130/CY7C131 can be utilized as either a standalone 8-bit dual-port static RAM or as a master dual-port RAM in conjunction with the CY7C140/CY7C141 slave dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data, such as cache memory for DSP, bit-slice, or multiprocessor designs.

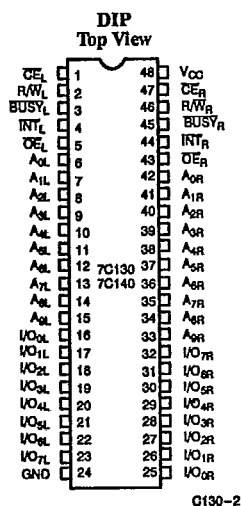
Each port has independent control pins; chip enable (CE), write enable (R/W), and output enable (OE). Two flags are provided on each port, BUSY and INT. BUSY signals that the port is trying to access the same location currently being accessed by the other port. INT is an interrupt flag indicating that data has been placed in a unique location (3FF for the left port and 3FE for the right port). An automatic power-down feature is controlled independently on each port by the chip enable (CE) pins.

The CY7C130 and CY7C140 are available in both 48-pin DIP and 48-pin LCC. The CY7C131 and CY7C141 are available in both 52-pin LCC and PLCC.

## Logic Block Diagram



## Pin Configurations



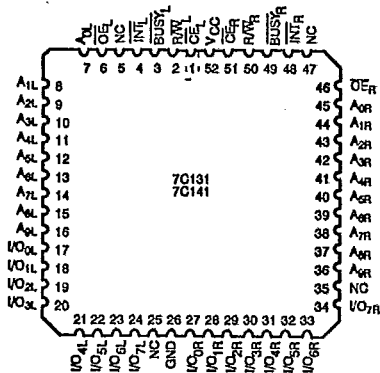
## Notes:

1. CY7C130/CY7C131 (Master): BUSY is open drain output and requires pull-up resistor. CY7C140/CY7C141 (Slave): BUSY is input.
2. Open drain outputs: pull-up resistor required.

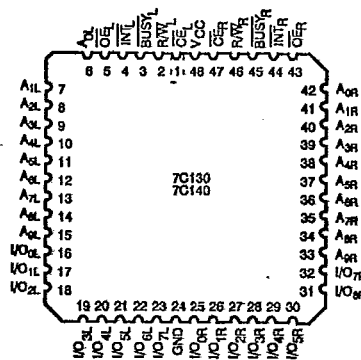


## Pin Configurations (continued)

T-46-23-12

52-Pin LCC/PLCC  
Top View

C130-3

48-Pin LCC/QFP  
Top View

C130-4



SRAMS

## Selection Guide

|                                |           | 7C130-25 <sup>[3]</sup><br>7C131-25<br>7C140-25<br>7C141-25 | 7C130-30<br>7C131-30<br>7C140-30<br>7C141-30 | 7C130-35<br>7C131-35<br>7C140-35<br>7C141-35 | 7C130-45<br>7C131-45<br>7C140-45<br>7C141-45 | 7C130-55<br>7C131-55<br>7C140-55<br>7C141-55 |
|--------------------------------|-----------|-------------------------------------------------------------|----------------------------------------------|----------------------------------------------|----------------------------------------------|----------------------------------------------|
| Maximum Access Time (ns)       |           | 25                                                          | 30                                           | 35                                           | 45                                           | 55                                           |
| Maximum Operating Current (mA) | Com'l/Ind | 170                                                         | 170                                          | 120                                          | 90                                           | 90                                           |
|                                | Military  |                                                             |                                              | 170                                          | 120                                          | 120                                          |
| Maximum Standby Current (mA)   | Com'l/Ind | 65                                                          | 65                                           | 45                                           | 35                                           | 35                                           |
|                                | Military  |                                                             |                                              | 65                                           | 45                                           | 45                                           |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... - 65°C to +150 °C

Ambient Temperature with

Power Applied ..... - 55°C to +125°C

Supply Voltage to Ground Potential

(Pin 48 to Pin 24) ..... - 0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State ..... - 0.5V to +7.0V

DC Input Voltage ..... - 3.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

Latch-Up Current ..... &gt;200 mA

## Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Industrial              | - 40°C to +85°C     | 5V ± 10%        |
| Military <sup>[4]</sup> | - 55°C to +125°C    | 5V ± 10%        |

## Notes:

3. 25-ns version available only in PLCC/LCC packages.

4. T<sub>A</sub> is the "instant on" case temperature.



T-46-23-12

CY7C130/CY7C131  
CY7C140/CY7C141Electrical Characteristics Over the Operating Range<sup>[5]</sup>

| Parameter        | Description                                    | Test Conditions                                                                                                                                                                                                  | 7C130-25, 30 <sup>[3]</sup><br>7C131-25,30<br>7C140-25,30<br>7C141-25,30 |       | 7C130-35<br>7C131-35<br>7C140-35<br>7C141-35 |       | 7C130-45,55<br>7C131-45,55<br>7C140-45,55<br>7C141-45,55 |       | Units |
|------------------|------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|-------|----------------------------------------------|-------|----------------------------------------------------------|-------|-------|
|                  |                                                |                                                                                                                                                                                                                  | Min.                                                                     | Max.  | Min.                                         | Max.  | Min.                                                     | Max.  |       |
| V <sub>OH</sub>  | Output HIGH Voltage                            | V <sub>CC</sub> = Min., I <sub>OH</sub> = - 4.0 mA                                                                                                                                                               | 2.4                                                                      |       | 2.4                                          |       | 2.4                                                      |       | V     |
| V <sub>OL</sub>  | Output LOW Voltage                             | I <sub>OL</sub> = 4.0 mA                                                                                                                                                                                         |                                                                          | 0.4   |                                              | 0.4   |                                                          | 0.4   | V     |
|                  |                                                | I <sub>OL</sub> = 16.0 mA <sup>[6]</sup>                                                                                                                                                                         |                                                                          | 0.5   |                                              | 0.5   |                                                          | 0.5   |       |
| V <sub>IH</sub>  | Input HIGH Voltage                             |                                                                                                                                                                                                                  | 2.2                                                                      |       | 2.2                                          |       | 2.2                                                      |       | V     |
| V <sub>IL</sub>  | Input LOW Voltage                              |                                                                                                                                                                                                                  |                                                                          | 0.8   |                                              | 0.8   |                                                          | 0.8   | V     |
| I <sub>IX</sub>  | Input Leakage Current                          | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                                                                                                                                                                           | - 5                                                                      | +5    | - 5                                          | +5    | - 5                                                      | +5    | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                         | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> ,<br>Output Disabled                                                                                                                                                      | - 5                                                                      | +5    | - 5                                          | +5    | - 5                                                      | +5    | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[7, 8]</sup> | V <sub>CC</sub> = Max.,<br>V <sub>OUT</sub> = GND                                                                                                                                                                |                                                                          | - 350 |                                              | - 350 |                                                          | - 350 | mA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current       | CE = V <sub>IL</sub> ,<br>Outputs Open,<br>f = f <sub>MAX</sub> <sup>[9]</sup>                                                                                                                                   | Com'l                                                                    | 170   |                                              | 120   |                                                          | 90    | mA    |
|                  |                                                |                                                                                                                                                                                                                  | Mil                                                                      |       |                                              | 170   |                                                          | 120   |       |
| I <sub>SB1</sub> | Standby Current Both Ports, TTL Inputs         | CE <sub>L</sub> and CE <sub>R</sub> ≥ V <sub>IH</sub> ,<br>f = f <sub>MAX</sub> <sup>[9]</sup>                                                                                                                   | Com'l                                                                    | 65    |                                              | 45    |                                                          | 35    | mA    |
|                  |                                                |                                                                                                                                                                                                                  | Mil                                                                      |       |                                              | 65    |                                                          | 45    |       |
| I <sub>SB2</sub> | Standby Current One Port, TTL Inputs           | CE <sub>L</sub> or CE <sub>R</sub> ≥ V <sub>IH</sub> ,<br>Active Port Outputs Open,<br>f = f <sub>MAX</sub> <sup>[9]</sup>                                                                                       | Com'l                                                                    | 115   |                                              | 90    |                                                          | 75    | mA    |
|                  |                                                |                                                                                                                                                                                                                  | Mil                                                                      |       |                                              | 115   |                                                          | 90    |       |
| I <sub>SB3</sub> | Standby Current Both Ports, CMOS Inputs        | Both Ports CE <sub>L</sub> and CE <sub>R</sub> ≥ V <sub>CC</sub> - 0.2V,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0                                                            | Com'l                                                                    | 15    |                                              | 15    |                                                          | 15    | mA    |
|                  |                                                |                                                                                                                                                                                                                  | Mil                                                                      |       |                                              | 15    |                                                          | 15    |       |
| I <sub>SB4</sub> | Standby Current One Port, CMOS Inputs          | One Port CE <sub>L</sub> or CE <sub>R</sub> ≥ V <sub>CC</sub> - 0.2V,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V,<br>Active Port Outputs Open,<br>f = f <sub>MAX</sub> <sup>[9]</sup> | Com'l                                                                    | 105   |                                              | 85    |                                                          | 70    | mA    |
|                  |                                                |                                                                                                                                                                                                                  | Mil                                                                      |       |                                              | 105   |                                                          | 85    |       |

Capacitance<sup>[8]</sup>

| Parameters       | Description        | Test Conditions                                             | Max. | Units |
|------------------|--------------------|-------------------------------------------------------------|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz,<br>V <sub>CC</sub> = 5.0V | 15   | pF    |
| C <sub>OUT</sub> | Output Capacitance |                                                             | 10   | pF    |

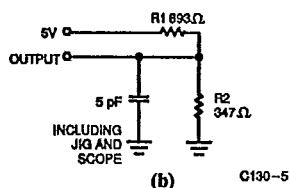
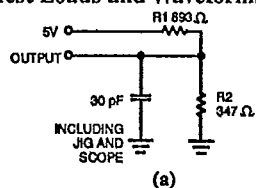
## Notes:

- See the last page of this specification for Group A subgroup testing information.
- BUSY and INT pins only.
- Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.
- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency of read cycle of 1/t<sub>RC</sub> and using AC Test Waveforms input levels of GND to 3V.
- AC Test conditions use V<sub>OH</sub> = 1.6V and V<sub>OL</sub> = 1.4V.
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub>, and 30-pF load capacitance.
- AC Test Conditions use V<sub>OH</sub> = 1.6V and V<sub>OL</sub> = 1.4V.
- t<sub>IZCE</sub>, t<sub>IZWE</sub>, t<sub>IZOE</sub>, t<sub>IZCE</sub> and t<sub>IZWE</sub> are tested with C<sub>L</sub> = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>IZCE</sub> is less than t<sub>IZWE</sub> for any given device.
- The internal write time of the memory is defined by the overlap of CS LOW and R/W LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

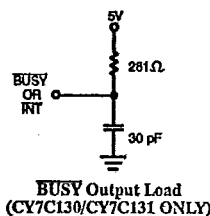


## AC Test Loads and Waveforms

T-46-23-12

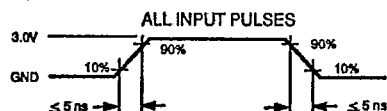


C130-5



C130-6

Equivalent to: THEVENIN EQUIVALENT  
OUTPUT — 250Ω — 1.40V

Switching Characteristics Over the Operating Range<sup>[5,11]</sup>

| Parameters                  | Description                                              | 7C130-25 <sup>[3]</sup> |      | 7C130-30 |      | 7C130-35 |      | 7C130-45 |      | 7C130-55 |      | Units |
|-----------------------------|----------------------------------------------------------|-------------------------|------|----------|------|----------|------|----------|------|----------|------|-------|
|                             |                                                          | Min.                    | Max. | Min.     | Max. | Min.     | Max. | Min.     | Max. | Min.     | Max. |       |
| READ CYCLE                  |                                                          |                         |      |          |      |          |      |          |      |          |      |       |
| t <sub>RC</sub>             | Read Cycle Time                                          | 25                      |      | 30       |      | 35       |      | 45       |      | 55       |      | ns    |
| t <sub>AA</sub>             | Address to Data Valid <sup>[12]</sup>                    |                         | 25   |          | 30   |          | 35   |          | 45   |          | 55   | ns    |
| t <sub>OHA</sub>            | Data Hold from Address Change                            | 0                       |      | 0        |      | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>ACE</sub>            | $\overline{\text{CE}}$ LOW to Data Valid <sup>[12]</sup> |                         | 25   |          | 30   |          | 35   |          | 45   |          | 55   | ns    |
| t <sub>DOE</sub>            | $\overline{\text{OE}}$ LOW to Data Valid <sup>[12]</sup> |                         | 15   |          | 20   |          | 20   |          | 25   |          | 25   | ns    |
| t <sub>LZOE</sub>           | $\overline{\text{OE}}$ LOW to Low Z                      | 3                       |      | 3        |      | 3        |      | 3        |      | 3        |      | ns    |
| t <sub>HZOE</sub>           | $\overline{\text{OE}}$ HIGH to High Z <sup>[13]</sup>    |                         | 15   |          | 15   |          | 20   |          | 20   |          | 25   | ns    |
| t <sub>LZCE</sub>           | $\overline{\text{CE}}$ LOW to Low Z <sup>[13,14]</sup>   | 5                       |      | 5        |      | 5        |      | 5        |      | 5        |      | ns    |
| t <sub>HZCE</sub>           | $\overline{\text{CE}}$ HIGH to High Z <sup>[13,14]</sup> |                         | 15   |          | 15   |          | 20   |          | 20   |          | 25   | ns    |
| t <sub>PU</sub>             | $\overline{\text{CE}}$ LOW to Power-Up                   | 0                       |      | 0        |      | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>PD</sub>             | $\overline{\text{CE}}$ HIGH to Power-Down                |                         | 25   |          | 25   |          | 35   |          | 35   |          | 35   | ns    |
| WRITE CYCLE <sup>[15]</sup> |                                                          |                         |      |          |      |          |      |          |      |          |      |       |
| t <sub>WC</sub>             | Write Cycle Time                                         | 25                      |      | 30       |      | 35       |      | 45       |      | 55       |      | ns    |
| t <sub>SCE</sub>            | $\overline{\text{CE}}$ LOW to Write End                  | 20                      |      | 25       |      | 30       |      | 35       |      | 40       |      | ns    |
| t <sub>AW</sub>             | Address Set-Up to Write End                              | 20                      |      | 25       |      | 30       |      | 35       |      | 40       |      | ns    |
| t <sub>HA</sub>             | Address Hold from Write End                              | 2                       |      | 2        |      | 2        |      | 2        |      | 2        |      | ns    |
| t <sub>SA</sub>             | Address Set-Up to Write Start                            | 0                       |      | 0        |      | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>PWE</sub>            | R/W Pulse Width                                          | 15                      |      | 25       |      | 25       |      | 30       |      | 30       |      | ns    |
| t <sub>SD</sub>             | Data Set-Up to Write End                                 | 15                      |      | 15       |      | 15       |      | 20       |      | 20       |      | ns    |
| t <sub>HD</sub>             | Data Hold from Write End                                 | 0                       |      | 0        |      | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>HZWE</sub>           | R/W LOW to High Z                                        |                         | 15   |          | 15   |          | 20   |          | 20   |          | 25   | ns    |
| t <sub>LZWE</sub>           | R/W HIGH to Low Z                                        | 0                       |      | 0        |      | 0        |      | 0        |      | 0        |      | ns    |

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T-46-23-12

CY7C130/CY7C131

CY7C140/CY7C141

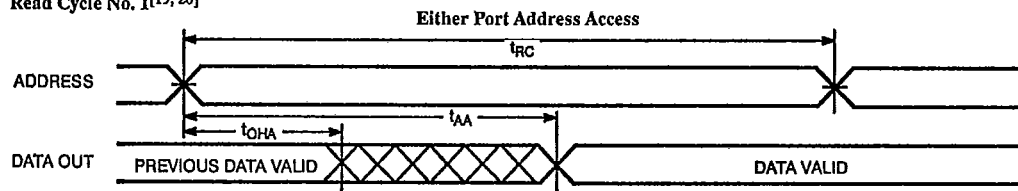
Switching Characteristics Over the Operating Range<sup>[5,11]</sup> (continued)

| Parameters                      | Description                                             | 7C130-25 <sup>[3]</sup> |         | 7C130-30 |         | 7C130-35 |         | 7C130-45 |         | 7C130-55 |         | Units |
|---------------------------------|---------------------------------------------------------|-------------------------|---------|----------|---------|----------|---------|----------|---------|----------|---------|-------|
|                                 |                                                         | Min.                    | Max.    | Min.     | Max.    | Min.     | Max.    | Min.     | Max.    | Min.     | Max.    |       |
| BUSY/INTERRUPT TIMING           |                                                         |                         |         |          |         |          |         |          |         |          |         |       |
| t <sub>BLA</sub>                | BUSY LOW from Address Match                             |                         | 20      |          | 20      |          | 20      |          | 25      |          | 30      | ns    |
| t <sub>BHA</sub>                | BUSY HIGH from Address Mismatch <sup>[16]</sup>         |                         | 20      |          | 20      |          | 20      |          | 25      |          | 30      | ns    |
| t <sub>BLC</sub>                | BUSY LOW from $\overline{CE}$ LOW                       |                         | 20      |          | 20      |          | 20      |          | 25      |          | 30      | ns    |
| t <sub>BHC</sub>                | BUSY HIGH from $\overline{CE}$ HIGH <sup>[16]</sup>     |                         | 20      |          | 20      |          | 20      |          | 25      |          | 30      | ns    |
| t <sub>PS</sub>                 | Port Set Up for Priority                                | 5                       |         | 5        |         | 5        |         | 5        |         | 5        |         | ns    |
| t <sub>WB</sub> <sup>[17]</sup> | R/W LOW after BUSY LOW                                  | 0                       |         | 0        |         | 0        |         | 0        |         | 0        |         | ns    |
| t <sub>WH</sub>                 | R/W HIGH after BUSY HIGH                                | 20                      |         | 30       |         | 30       |         | 35       |         | 35       |         | ns    |
| t <sub>BDD</sub>                | BUSY HIGH to Valid Data                                 |                         | 25      |          | 30      |          | 35      |          | 45      |          | 45      | ns    |
| t <sub>DDD</sub>                | Write Data Valid to Read Data Valid                     |                         | Note 18 |          | Note 18 |          | Note 18 |          | Note 18 |          | Note 18 | ns    |
| t <sub>WDD</sub>                | Write Pulse to Data Delay                               |                         | Note 18 |          | Note 18 |          | Note 18 |          | Note 18 |          | Note 18 | ns    |
| INTERRUPT TIMING                |                                                         |                         |         |          |         |          |         |          |         |          |         |       |
| t <sub>WINS</sub>               | R/W to INTERRUPT Set Time                               |                         | 25      |          | 25      |          | 25      |          | 35      |          | 45      | ns    |
| t <sub>EINS</sub>               | $\overline{CE}$ to INTERRUPT Set Time                   |                         | 25      |          | 25      |          | 25      |          | 35      |          | 45      | ns    |
| t <sub>INS</sub>                | Address to INTERRUPT Set Time                           |                         | 25      |          | 25      |          | 25      |          | 35      |          | 45      | ns    |
| t <sub>OINR</sub>               | $\overline{OE}$ to INTERRUPT Reset Time <sup>[16]</sup> |                         | 25      |          | 25      |          | 25      |          | 35      |          | 45      | ns    |
| t <sub>EinR</sub>               | $\overline{CE}$ to INTERRUPT Reset Time <sup>[16]</sup> |                         | 25      |          | 25      |          | 25      |          | 35      |          | 45      | ns    |
| t <sub>INR</sub>                | Address to INTERRUPT Reset Time <sup>[16]</sup>         |                         | 25      |          | 25      |          | 25      |          | 35      |          | 45      | ns    |

## Notes:

16. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
17. CY7C140/CY7C141 only.
18. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
  - A. BUSY on Port B goes HIGH.
  - B. Port B's address is toggled.
  - C.  $\overline{CE}$  for Port B is toggled.
  - D. R/W for Port B is toggled during valid read.
19. R/W is HIGH for read cycle.
20. Device is continuously selected,  $\overline{CE} = V_{IL}$  and  $\overline{OE} = V_{IL}$ .
21. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
22. If  $\overline{OE}$  is LOW during a R/W controlled write cycle, the write pulse width must be the larger of  $t_{PWG}$  or  $t_{HZWB} + t_{SD}$  to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required  $t_{SD}$ .
23. If the  $\overline{CE}$  LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in the high-impedance state.

## Switching Waveforms

Read Cycle No. 1<sup>[19, 20]</sup>

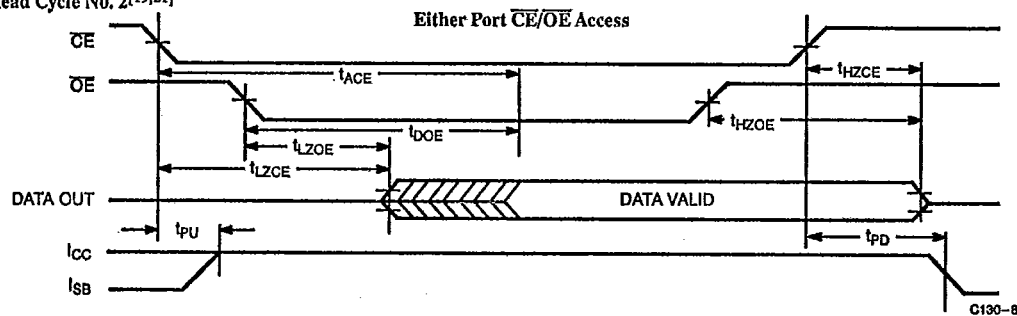
C130-7



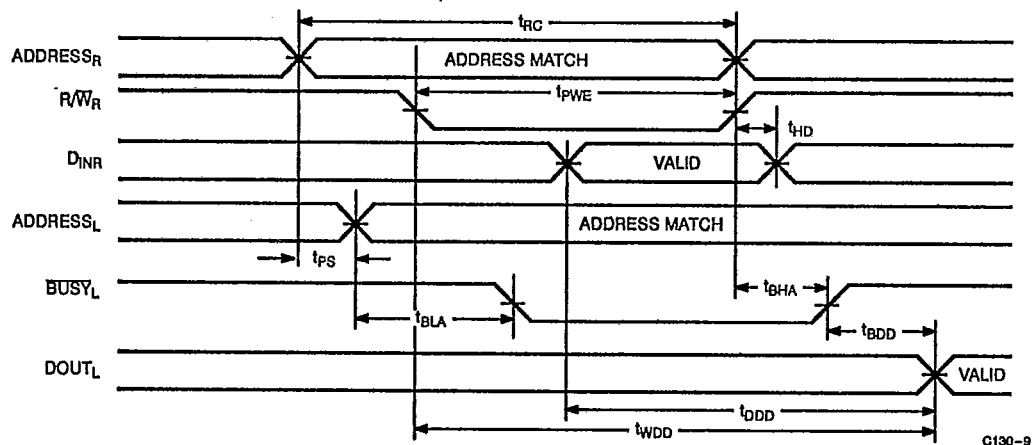
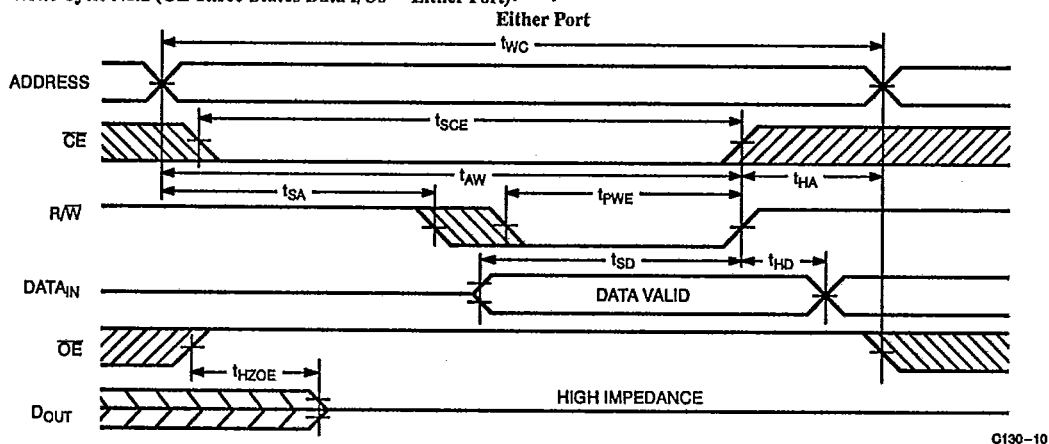
CY7C130/CY7C131  
CY7C140/CY7C141

## Switching Waveforms (continued)

T-46-23-12

Read Cycle No. 2<sup>[19,21]</sup>

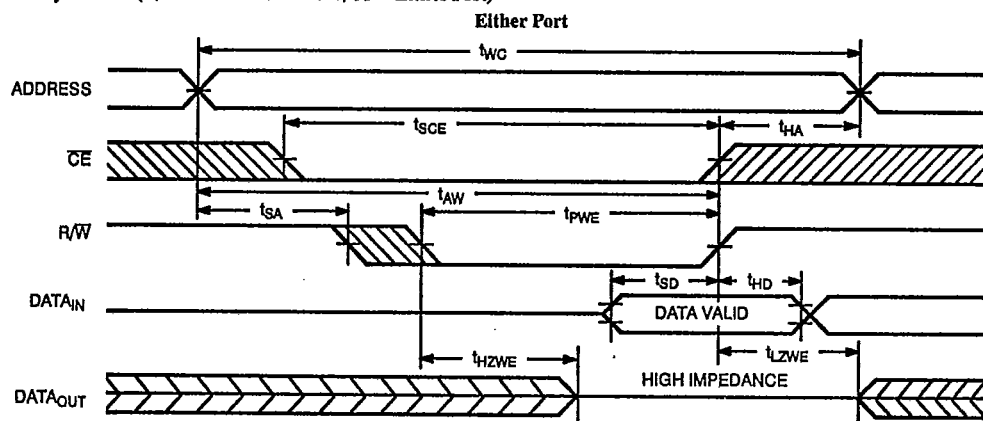
SRAMs

Read Cycle No. 3<sup>[20]</sup>Read with  $\overline{BUSY}$ , Master: CY7C130 and CY7C131Write Cycle No. 1 ( $\overline{OE}$  Three-States Data I/Os - Either Port)<sup>[15,22]</sup>

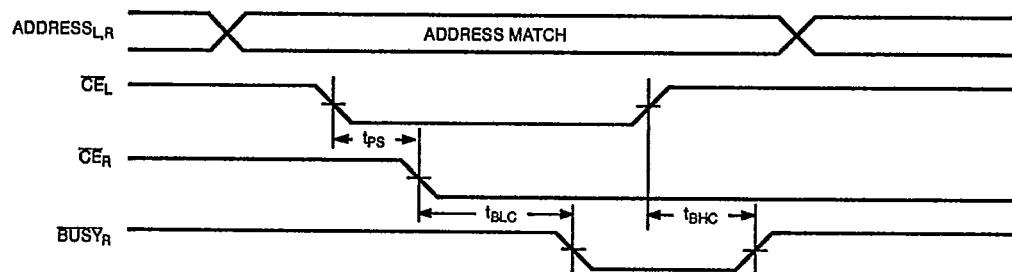
CYPRESS  
SEMICONDUCTORCY7C130/CY7C131  
CY7C140/CY7C141

## Switching Waveforms (continued)

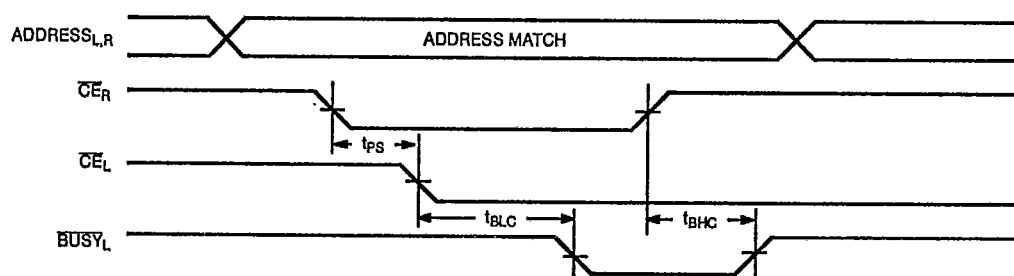
T-46-23-12

Write Cycle No. 2 (R/W Three-States Data I/Os - Either Port)<sup>[15,23]</sup>

C130-11

Busy Timing Diagram No. 1 ( $\overline{CE}$  Arbitration) $\overline{CE}_L$  Valid First:

C130-12

 $\overline{CE}_R$  Valid First:

C130-13



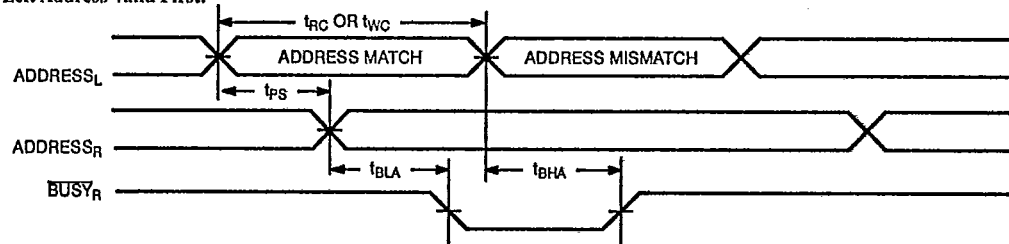
CY7C130/CY7C131  
CY7C140/CY7C141

## Switching Waveforms (continued)

## Busy Timing Diagram No. 2 (Address Arbitration)

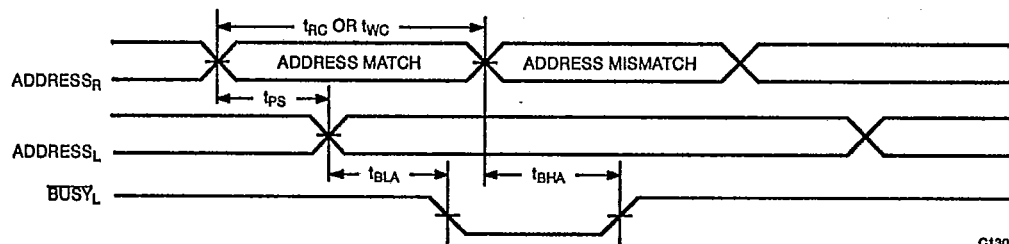
T-46-23-12

## Left Address Valid First:



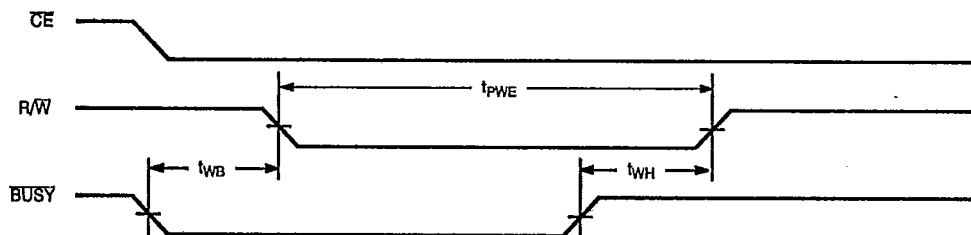
C130-14

## Right Address Valid First:



C130-15

## Busy Timing Diagram No. 3

Write with  $\overline{BUSY}$  (Slave: CY7C140/CY7C141)

C130-16



SRAMS

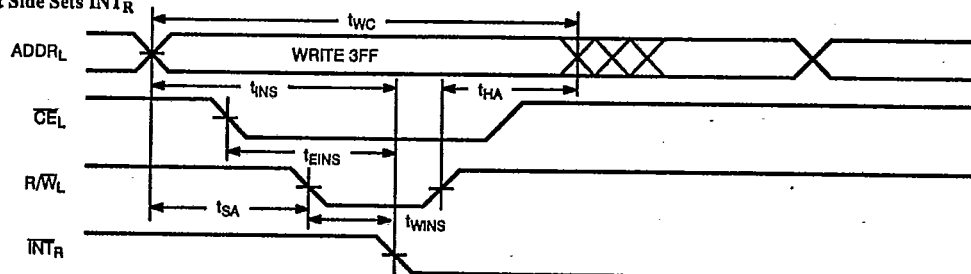


T-46-23-12

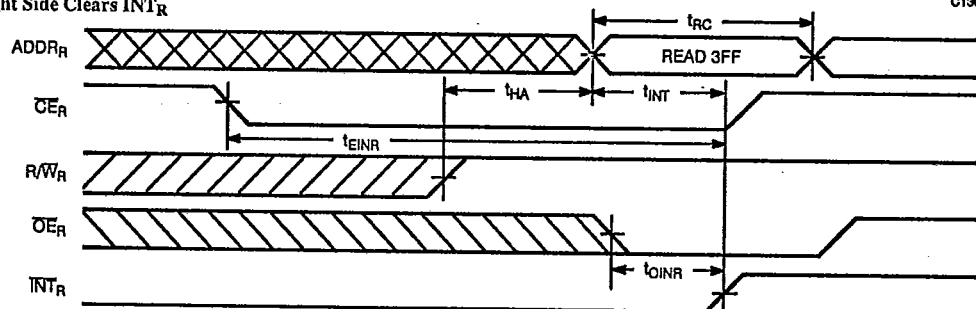
CY7C130/CY7C131  
CY7C140/CY7C141

## Switching Waveforms (continued)

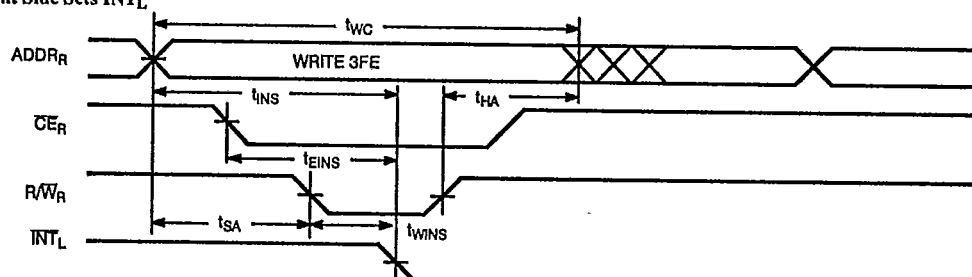
## Interrupt Timing Diagrams

Left Side Sets  $\overline{INT}_R$ 

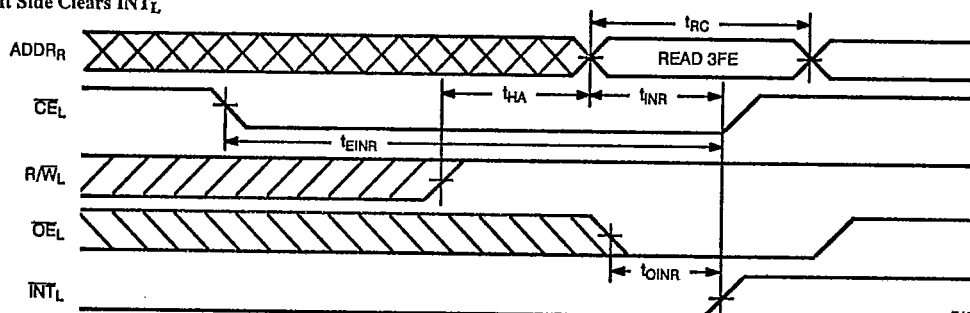
C130-17

Right Side Clears  $\overline{INT}_R$ 

C130-18

Right Side Sets  $\overline{INT}_L$ 

C130-19

Left Side Clears  $\overline{INT}_L$ 

C130-20



CY7C130/CY7C131  
CY7C140/CY7C141

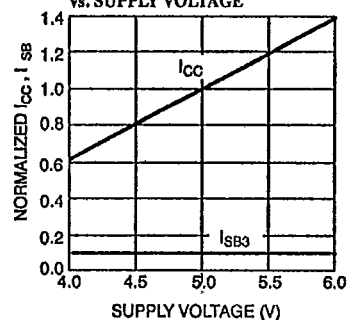
## Typical DC and AC Characteristics

T-46-23-12

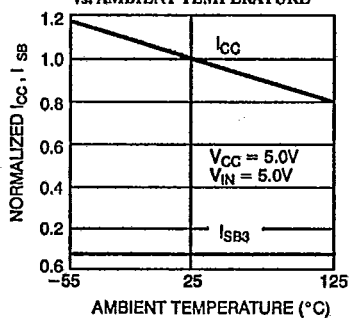


SRAMS

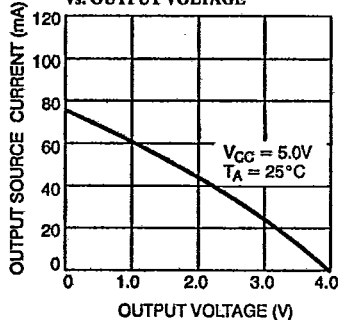
NORMALIZED SUPPLY CURRENT  
vs. SUPPLY VOLTAGE



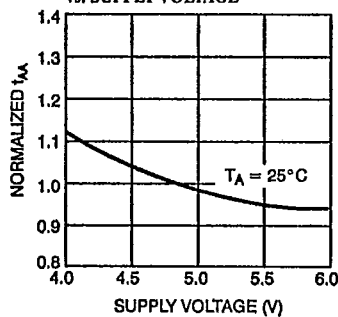
NORMALIZED SUPPLY CURRENT  
vs. AMBIENT TEMPERATURE



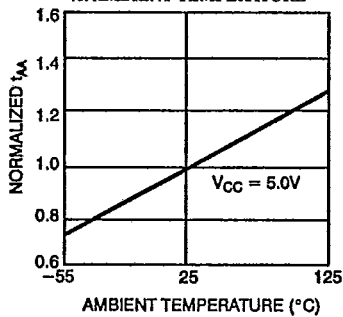
OUTPUT SOURCE CURRENT  
vs. OUTPUT VOLTAGE



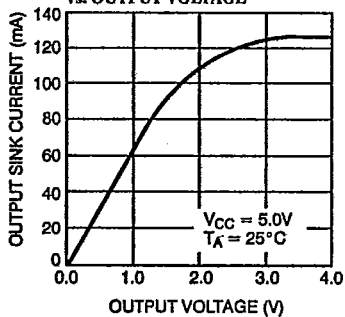
NORMALIZED ACCESS TIME  
vs. SUPPLY VOLTAGE



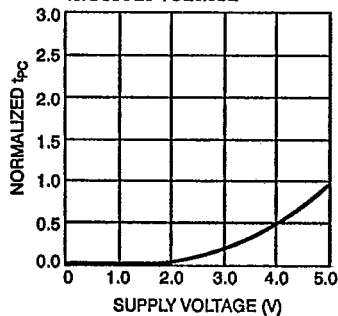
NORMALIZED ACCESS TIME  
vs. AMBIENT TEMPERATURE



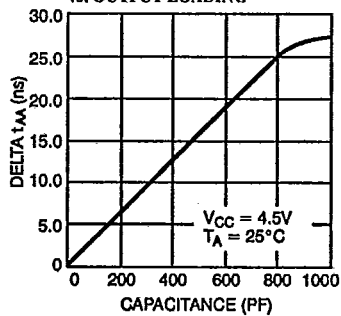
OUTPUT SINK CURRENT  
vs. OUTPUT VOLTAGE



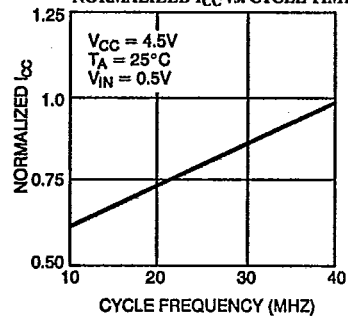
TYPICAL POWER-ON CURRENT  
vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE  
vs. OUTPUT LOADING



NORMALIZED ICC vs. CYCLE TIME



CYPRESS  
SEMICONDUCTOR

T-46-23-12

CY7C130/CY7C131

CY7C140/CY7C141

## Ordering Information

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 25         | CY7C130-25LC  | L68          | Commercial      |
| 30         | CY7C130-30DC  | D26          | Commercial      |
|            | CY7C130-30LC  | L68          |                 |
|            | CY7C130-30PC  | P25          |                 |
|            | CY7C130-30DI  | D26          | Industrial      |
|            | CY7C130-30PI  | P25          |                 |
| 35         | CY7C130-35DC  | D26          | Commercial      |
|            | CY7C130-35LC  | L68          |                 |
|            | CY7C130-35PC  | P25          |                 |
|            | CY7C130-35DI  | D26          | Industrial      |
|            | CY7C130-35PI  | P25          |                 |
|            | CY7C130-35DMB | D26          | Military        |
|            | CY7C130-35FMB | F78          |                 |
|            | CY7C130-35LMB | L68          |                 |
| 45         | CY7C130-45DC  | D26          | Commercial      |
|            | CY7C130-45LC  | L68          |                 |
|            | CY7C130-45PC  | P25          |                 |
|            | CY7C130-45DI  | D26          | Industrial      |
|            | CY7C130-45PI  | P25          |                 |
|            | CY7C130-45DMB | D26          | Military        |
|            | CY7C130-45FMB | F78          |                 |
|            | CY7C130-45LMB | L68          |                 |
| 55         | CY7C130-55DC  | D26          | Commercial      |
|            | CY7C130-55LC  | L68          |                 |
|            | CY7C130-55PC  | P25          |                 |
|            | CY7C130-55DI  | D26          | Industrial      |
|            | CY7C130-55PI  | P25          |                 |
|            | CY7C130-55DMB | D26          | Military        |
|            | CY7C130-55FMB | F78          |                 |
|            | CY7C130-55LMB | L68          |                 |

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 25         | CY7C131-25JC  | J69          | Commercial      |
|            | CY7C131-25LC  | L69          |                 |
| 30         | CY7C131-30JC  | J69          | Commercial      |
|            | CY7C131-30LC  | L69          |                 |
|            | CY7C131-30JI  | J69          | Industrial      |
| 35         | CY7C131-35JC  | J69          | Commercial      |
|            | CY7C131-35LC  | L69          |                 |
|            | CY7C131-35JI  | J69          | Industrial      |
|            | CY7C131-35FMB | F78          | Military        |
|            | CY7C131-35LMB | L69          |                 |
| 45         | CY7C131-45JC  | J69          | Commercial      |
|            | CY7C131-45LC  | L69          |                 |
|            | CY7C131-45JI  | J69          | Industrial      |
|            | CY7C131-45FMB | F78          | Military        |
|            | CY7C131-45LMB | L69          |                 |
| 55         | CY7C131-55JC  | J69          | Commercial      |
|            | CY7C131-55LC  | L69          |                 |
|            | CY7C131-55JI  | J69          | Industrial      |
|            | CY7C131-55FMB | F78          | Military        |
|            | CY7C131-55MB  | L69          |                 |



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CY7C130/CY7C131

CY7C140/CY7C141

## Ordering Information (continued)

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 25         | CY7C140-25LC  | L68          | Commercial      |
| 30         | CY7C140-30DC  | D26          | Commercial      |
|            | CY7C140-30LC  | L68          |                 |
|            | CY7C140-30PC  | P25          |                 |
|            | CY7C140-30DI  | D26          | Industrial      |
|            | CY7C140-30PI  | P25          |                 |
| 35         | CY7C140-35DC  | D26          | Commercial      |
|            | CY7C140-35LC  | L68          |                 |
|            | CY7C140-35PC  | P25          |                 |
|            | CY7C140-35DI  | D26          | Industrial      |
|            | CY7C140-35PI  | P25          |                 |
|            | CY7C140-35DMB | D26          | Military        |
|            | CY7C140-35FMB | F78          |                 |
| 45         | CY7C140-35LMB | L68          |                 |
|            | CY7C140-45DC  | D26          |                 |
|            | CY7C140-45LC  | L68          | Commercial      |
|            | CY7C140-45PC  | P25          |                 |
|            | CY7C140-45DI  | D26          |                 |
|            | CY7C140-45PI  | P25          | Industrial      |
|            | CY7C140-45DMB | D26          |                 |
|            | CY7C140-45FMB | F78          | Military        |
| 55         | CY7C140-45LMB | L68          |                 |
|            | CY7C140-55DC  | D26          | Commercial      |
|            | CY7C140-55LC  | L68          |                 |
|            | CY7C140-55PC  | P25          |                 |
|            | CY7C140-55DI  | D26          | Industrial      |
|            | CY7C140-55PI  | P25          |                 |
|            | CY7C140-55DMB | D26          | Military        |
|            | CY7C140-55FMB | F78          |                 |
|            | CY7C140-55LMB | L68          |                 |

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 25         | CY7C141-25JC  | J69          | Commercial      |
|            | CY7C141-25LC  | L69          |                 |
| 30         | CY7C141-30JC  | J69          | Commercial      |
|            | CY7C141-30LC  | L69          |                 |
|            | CY7C141-30JI  | J69          | Industrial      |
| 35         | CY7C141-35JC  | J69          | Commercial      |
|            | CY7C141-35LC  | L69          |                 |
|            | CY7C141-35JI  | J69          | Industrial      |
|            | CY7C141-35FMB | F78          | Military        |
|            | CY7C141-35LMB | L69          |                 |
| 45         | CY7C141-45JC  | J69          | Commercial      |
|            | CY7C141-45LC  | L69          |                 |
|            | CY7C141-45JI  | J69          | Industrial      |
|            | CY7C141-45FMB | F78          | Military        |
|            | CY7C141-45LMB | L69          |                 |
| 55         | CY7C141-55JC  | J69          | Commercial      |
|            | CY7C141-55LC  | L69          |                 |
|            | CY7C141-55JI  | J69          | Industrial      |
|            | CY7C141-55FMB | F78          | Military        |
|            | CY7C141-55LMB | L69          |                 |



SRAMS

**MILITARY SPECIFICATIONS****Group A Subgroup Testing****DC Characteristics**

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1, 2, 3   |
| V <sub>OL</sub>      | 1, 2, 3   |
| V <sub>IH</sub>      | 1, 2, 3   |
| V <sub>IL</sub> Max. | 1, 2, 3   |
| I <sub>Ix</sub>      | 1, 2, 3   |
| I <sub>OZ</sub>      | 1, 2, 3   |
| I <sub>CC</sub>      | 1, 2, 3   |
| I <sub>SB1</sub>     | 1, 2, 3   |
| I <sub>SB2</sub>     | 1, 2, 3   |
| I <sub>SB3</sub>     | 1, 2, 3   |
| I <sub>SB4</sub>     | 1, 2, 3   |

**Switching Characteristics**

| Parameters         | Subgroups       |
|--------------------|-----------------|
| <b>READ CYCLE</b>  |                 |
| t <sub>RC</sub>    | 7, 8, 9, 10, 11 |
| t <sub>AA</sub>    | 7, 8, 9, 10, 11 |
| t <sub>ACE</sub>   | 7, 8, 9, 10, 11 |
| t <sub>DOE</sub>   | 7, 8, 9, 10, 11 |
| <b>WRITE CYCLE</b> |                 |
| t <sub>WC</sub>    | 7, 8, 9, 10, 11 |
| t <sub>SCE</sub>   | 7, 8, 9, 10, 11 |
| t <sub>AW</sub>    | 7, 8, 9, 10, 11 |
| t <sub>HA</sub>    | 7, 8, 9, 10, 11 |
| t <sub>SA</sub>    | 7, 8, 9, 10, 11 |
| t <sub>PWE</sub>   | 7, 8, 9, 10, 11 |
| t <sub>SD</sub>    | 7, 8, 9, 10, 11 |
| t <sub>HD</sub>    | 7, 8, 9, 10, 11 |

| Parameters                      | Subgroups       |
|---------------------------------|-----------------|
| <b>BUSY/INTERRUPT TIMING</b>    |                 |
| t <sub>BLA</sub>                | 7, 8, 9, 10, 11 |
| t <sub>BHA</sub>                | 7, 8, 9, 10, 11 |
| t <sub>BLC</sub>                | 7, 8, 9, 10, 11 |
| t <sub>BHC</sub>                | 7, 8, 9, 10, 11 |
| t <sub>PS</sub>                 | 7, 8, 9, 10, 11 |
| t <sub>WINS</sub>               | 7, 8, 9, 10, 11 |
| t <sub>EINS</sub>               | 7, 8, 9, 10, 11 |
| t <sub>INS</sub>                | 7, 8, 9, 10, 11 |
| t <sub>OINR</sub>               | 7, 8, 9, 10, 11 |
| t <sub>EINR</sub>               | 7, 8, 9, 10, 11 |
| t <sub>INR</sub>                | 7, 8, 9, 10, 11 |
| <b>BUSY TIMING</b>              |                 |
| t <sub>WB</sub> <sup>[24]</sup> | 7, 8, 9, 10, 11 |
| t <sub>WH</sub>                 | 7, 8, 9, 10, 11 |
| t <sub>BDD</sub>                | 7, 8, 9, 10, 11 |

Note:

24. CY7C140/CY7C141 only.

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