TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS101C – Revised September 2003

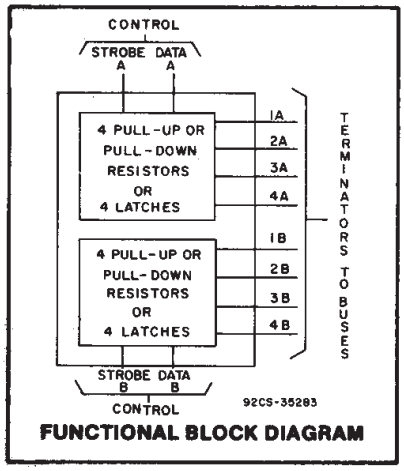
NOT RECOMMENDED FOR NEW DESIGNS

CD40117B Types

Programmable Dual 4-Bit Terminator

High-Voltage Types (20-Volt Rating)

Features:
- *One standard "B" output will drive eight terminator circuits.*
- *Will terminate a CMOS data bus with up to 40 B-series inputs inputs or 3-state outputs connected at VDD of 5 V.*
- *Input terminals protected by standard "B" series ESD protection network.*
- *Preserves final logic state.*
- *Output after switching is closer to VDD or VSS rail than with a resistor.*
- *Requires only one solder connection.*
- *Open circuited terminator not used will not affect performance.*
- *Can be connected to any CMOS I/O line.*
- *Draws current only when logic state is changing.*
- *Can be preset.*



FUNCTIONAL BLOCK DIAGRAM

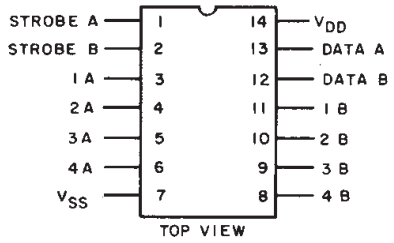
■ CD40117B is a dual 4-bit terminator that can be programmed by means of STROBE and DATA control bits to function as pull-up or pull-down resistors. The CD40117B can also be programmed to function as latches to terminate any open or unused CMOS logic when used with 3-state logic or during a power-down condition. Considerable savings in power and board space can be realized when this device is used to replace pull-up or pull-down resistors. When the STROBE is in the logic "1" state, the terminator functions as a pull-up resistor if the DATA input is a logic "1" or as a pull-down resistor if the DATA input is a logic "0".

When the STROBE is in the logic "0" state, the terminator performs the latch function, i.e., it follows the changing states of the bus. If the bus goes into the high-Z state or into a power-down condition, the latched terminator retains the data ("1" or "0") that the bus carried before it switched to the high-Z or power-down state. If and when the bus changes from the high-Z state to the state opposite to that which the latch is storing, the bus will override the latch and the terminator will reflect the state on the bus. The small geometries chosen for the inverters in the latch allow this override mode. When checking the data bus whose last state is being preserved by the terminator, a resistor should be used in series with the probe whose input capacitance could trip the small latches. The resistance should be in excess of the output impedance of the latch, i.e., R should be > 30 KΩ at V_{DD} =10 V.

The STROBE and DATA inputs in each section can be paralleled allowing this device to be used as an 8-bit bus terminator.

The CD40117B types are supplied in 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Applications:
- *Error state identification.*
- *Replaces pull-up or pull-down resistors*
- *Avoids floating inputs in modular systems*
- *Sharpens transistors (hysteresis)*
- *Anti-bounce circuit*



TERMINAL DIAGRAM

TRUTH TABLE

STROBE	DATA	1A(B)	2A(B)	3A(B)	4A(B)
1	0	0^{Δ}	$\frac{0^{\Delta}}{1^{+}}$	$\frac{0^{\Delta}}{1^{+}}$	$\frac{0^{\Delta}}{1^{+}}$
1	1	1^{+}			
0	X	*	*	*	*

1 = High, 0 = Low, X = Don't Care

Δ Equivalent to pull-down resistor.
+ Equivalent to pull-up resistor.
*Equivalent to a latch.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		MIN.	TYP.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)	—	3	18	V

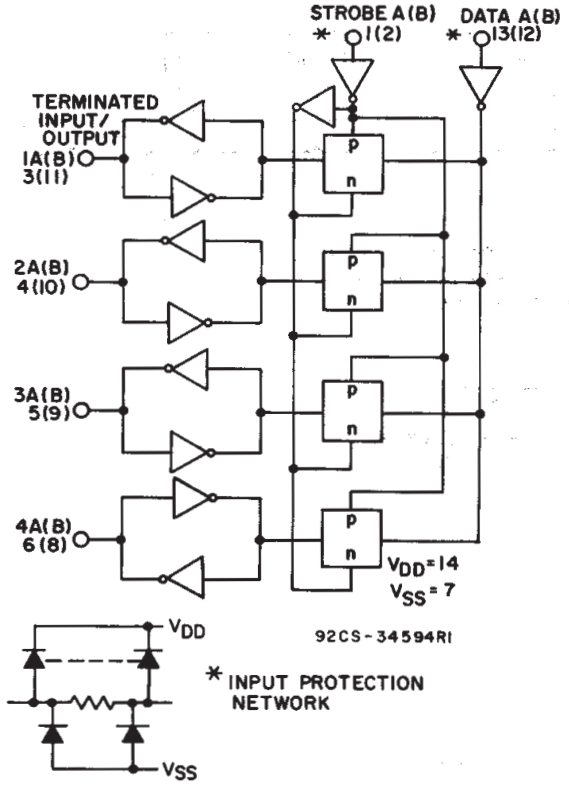
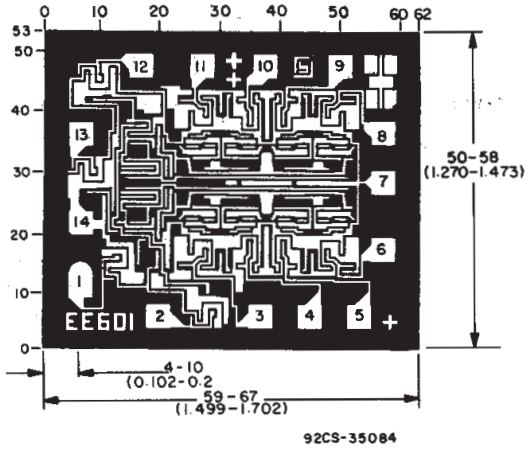


Fig. 1 - Logic diagram (½ of CD40117B)



Dimensions and pad layout for CD40117B.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

TYPICAL APPLICATIONS

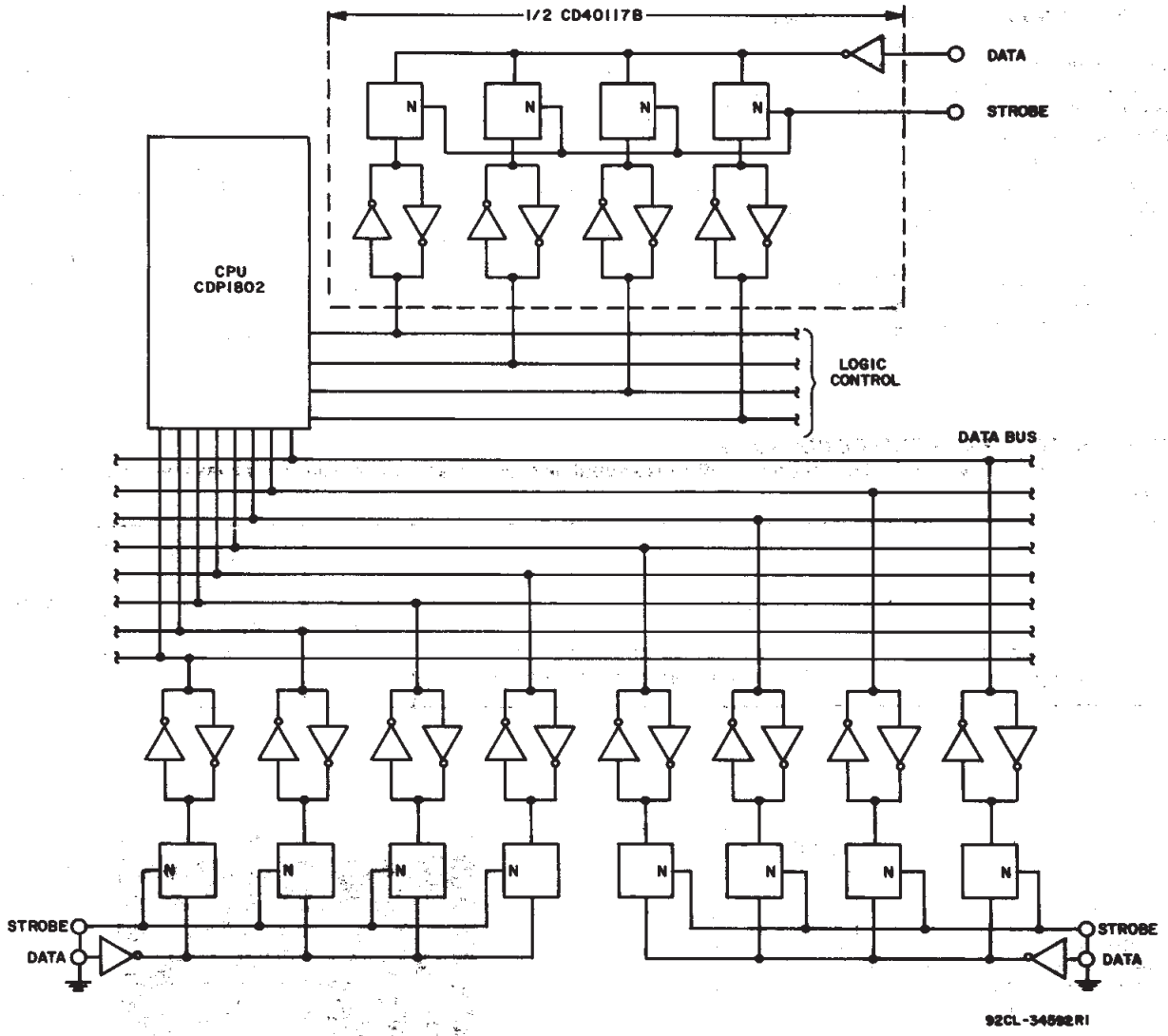


Fig. 2 - Schematic of CD40117B interfacing with microprocessor terminating an 8-bit bus line and 1/2 of CD40117B as a programmable pull-up/pull down logic controller.

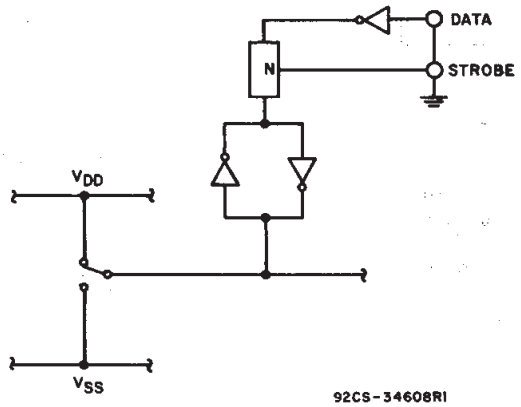


Fig. 3 - Schematic of CD40117B in anti-bounce circuit application.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current Max.	I_{DD}	—	0, 5	5	0.25	0.25	7.5	7.5	—	0.01	0.25	μA
		—	0, 10	10	0.5	0.5	15	15	—	0.01	0.5	
		—	0, 15	15	1	1	30	30	—	0.01	1	
		—	0, 20	20	5	5	150	150	—	0.02	5	
Output Low Sink Current Min.	I_{OL}	0.4	0, 5	5	—	—	—	—	—	25	—	μA
		0.5	0, 10	10	—	—	—	—	—	60	—	
		1.5	0, 15	15	—	—	—	—	—	250	—	
Output High (Source) Current Min.	I_{OH}	4.6	0, 5	5	—	—	—	—	—	-25	—	
		2.5	0, 5	5	—	—	—	—	—	—	—	
		9.5	0, 10	10	—	—	—	—	—	-60	—	
		13.5	0, 15	15	—	—	—	—	—	-250	—	
Output Voltage: Low-Level Max.	V_{OL}	—	0, 5	5	0.05				—	0	0.05	V
		—	0, 10	10	0.05				—	0	0.05	
		—	0, 15	15	0.05				—	0	0.05	
Output Voltage: High-Level Min.	V_{OH}	—	0, 5	5	4.95				4.95	5	—	
		—	0, 10	10	9.95				9.95	10	—	
		—	0, 15	15	14.95				14.95	15	—	
Input Low Voltage Max.	V_{IL}	0.5, 4.5	—	5	1.5				—	—	1.5	V
		1, 9	—	10	3				—	—	3	
		1.5, 13.5	—	15	4				—	—	4	
Input High Voltage Min.	V_{IH}	0.5, 4.5	—	5	3.5				3.5	—	—	
		1, 9	—	10	7				7	—	—	
		1.5, 13.5	—	15	11				11	—	—	
Input Current Max.	I_{IN}	—	0, 18	18	±0.1	±0.1	±1	±1	—	$±10^{-5}$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C; Input t_r, t_f=20 ns, C_L=50 pF, R_L=200 kΩ

CHARACTERISTIC		TEST CONDITIONS V_{DD} (V)	LIMITS All Packages MIN.	TYP.	MAX.	UNITS
Propagation Delay Time Strobe, Data to Outputs	t_{PHL}	5	—	1.7	—	μs
		10	—	850	—	ns
		15	—	575	—	ns
	t_{PLH}	5	—	1.5	—	μs
		10	—	625	—	ns
		15	—	500	—	ns
Transition Time	t_{THL}, t_{TLH}	5	—	3.3	—	μs
		10	—	1.6	—	
		15	—	1.1	—	
Minimum Strobe Pulse Width	t_W	5	—	1.5	—	μs
		10	—	600	—	ns
		15	—	475	—	ns
Minimum Data Pulse Width	t_{WH}, t_{WL}	5	—	1.6	—	μs
		10	—	700	—	ns
		15	—	500	—	ns
Minimum Terminator Input/Output Pulse Width	t_W	5	—	10	—	ns
Minimum Data Setup Time Data to Strobe	t_{SU}	5	—	0	—	ns
		10	—	0	—	
		15	—	0	—	
Input Capacitance	C_{IN}	Any Input	—	5	—	pF

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD40117BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD40117BE	Samples
CD40117BEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD40117BE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

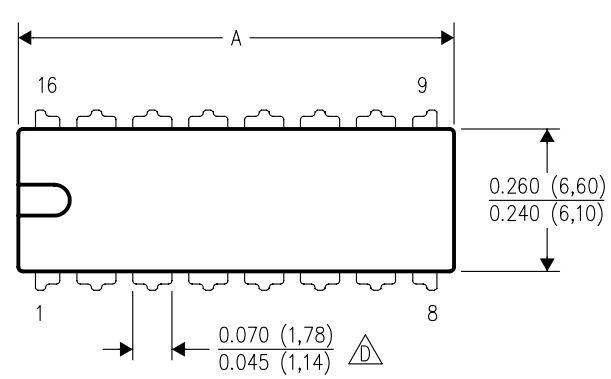
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

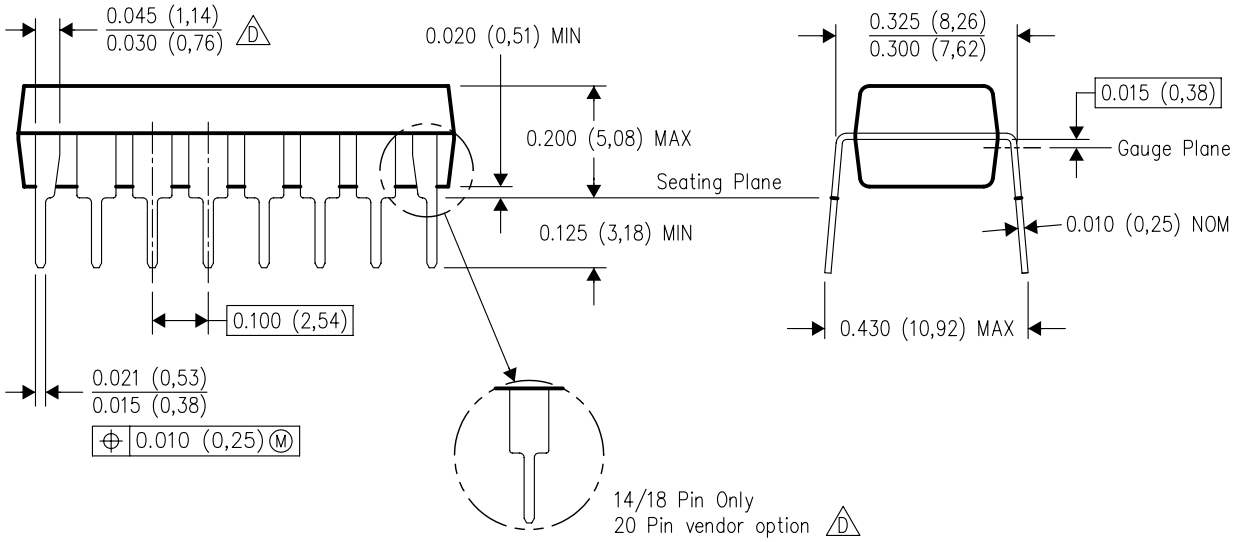
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265