

LOW SKEW, 1-TO-2 DIFFERENTIAL-TO-LVHSTL FANOUT BUFFER

ICS85211I

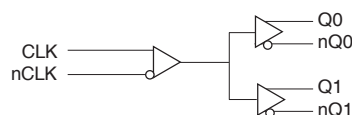
GENERAL DESCRIPTION

The ICS85211I is a low skew, high performance 1-to-2 Differential-to-LVHSTL Fanout Buffer. The CLK, nCLK pair can accept most standard differential input levels. The ICS85211I is characterized to operate from a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the ICS85211I ideal for those clock distribution applications demanding well defined performance and repeatability. For optimal performance, terminate all outputs.

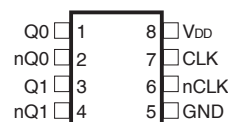
FEATURES

- Two differential LVHSTL compatible outputs
- One differential CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency: 700MHz
- Translates any single-ended input signal to LVHSTL levels with resistor bias on nCLK input
- Output skew: 30ps (maximum)
- Part-to-part skew: 250ps (maximum)
- Propagation delay: 1ns (maximum)
- Output duty cycle: 49% - 51% up to 266.6MHz
- $V_{OH} = 1.2V$ (maximum)
- 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Available in both standard and lead-free RoHS compliant packages

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS85211I
8-Lead SOIC

3.90mm x 4.90mm x 1.37mm package body

M Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. LVHSTL interface levels.
3, 4	Q1, nQ1	Output		Differential output pair. LVHSTL interface levels.
5	GND	Power		Power supply ground.
6	nCLK	Input	$V_{DD}/2$	Inverting differential clock input. $V_{DD}/2$ default when left floating.
7	CLK	Input	Pulldown	Non-inverting differential clock input.
8	V_{DD}	Power		Positive supply pin.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		k Ω
$R_{PULLDOWN}$	Input Pulldown Resistor			51		k Ω

TABLE 3. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
CLK	nCLK	Q0, Q1	nQ0, nQ1		
0	0	LOW	HIGH	Differential to Differential	Non Inverting
1	1	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section, "Wiring the Differential Input to Accept Single Ended Levels".

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_{DD}	-0.5V to $V_{DD} + 0.5$ V
Outputs, V_{DD}	-0.5V to $V_{DD} + 0.5$ V
Package Thermal Impedance, θ_{JA}	112.7°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				50	mA

TABLE 4B. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK	$V_{DD} = V_{IN} = 3.465\text{V}$		150	μA
		CLK	$V_{DD} = V_{IN} = 3.465\text{V}$		150	μA
I_{IL}	Input Low Current	nCLK	$V_{DD} = 3.465\text{V}, V_{IN} = 0\text{V}$	-150		μA
		CLK	$V_{DD} = 3.465\text{V}, V_{IN} = 0\text{V}$	-5		μA
V_{PP}	Peak-to-Peak Input Voltage		0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2		0.5		$V_{DD} - 0.85$	V

NOTE 1: For single ended applications the maximum input voltage for CLK and nCLK is $V_{DD} + 0.3\text{V}$.

NOTE 2: Common mode voltage is defined as V_{IH} .

TABLE 4C. LVHSTL DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		1.0		1.2	V
V_{OL}	Output Low Voltage; NOTE 1		0		0.4	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6	0.9	1.2	V

NOTE 1: All outputs must be terminated with 50 Ω to ground.

TABLE 5. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				700	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq 600\text{MHz}$	0.7		1.0	ns
$tsk(o)$	Output Skew; NOTE 2, 4				30	ps
$tsk(pp)$	Part-to-Part Skew; NOTE 3, 4				250	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		600	ps
odc	Output Duty Cycle		47		53	%
		$f \leq 266.6\text{MHz}$	49		51	%

All parameters measured at 600MHz unless noted otherwise.

The cycle-to-cycle jitter on the input will equal the jitter on the output. The part does not add jitter.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

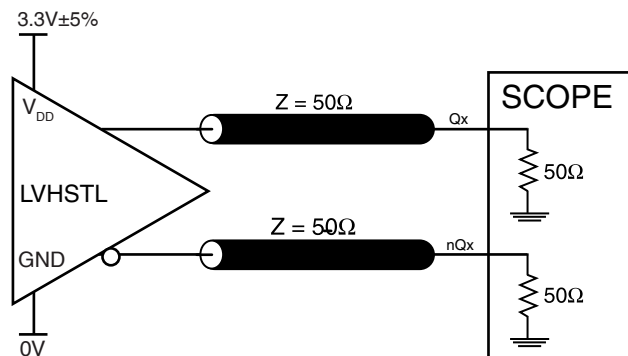
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at output differential cross points.

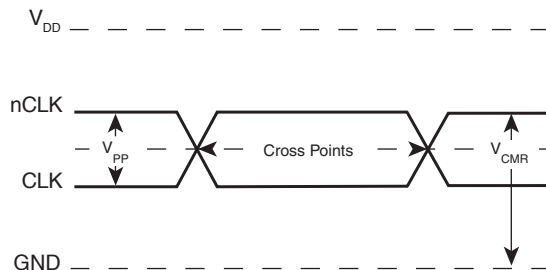
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

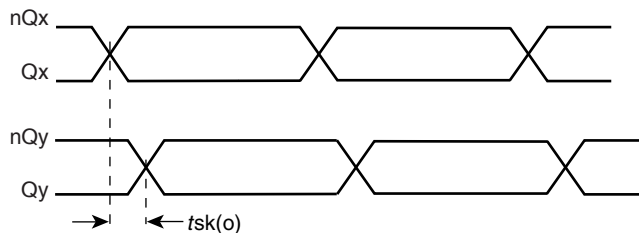
PARAMETER MEASUREMENT INFORMATION



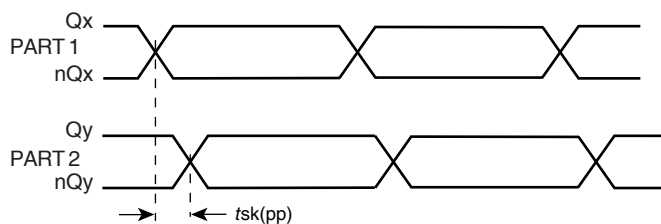
3.3V Output Load AC Test Circuit



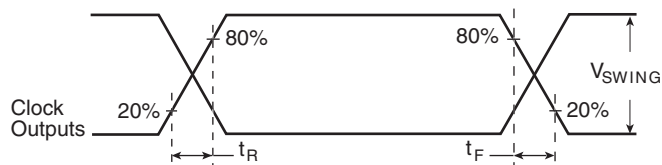
DIFFERENTIAL INPUT LEVEL



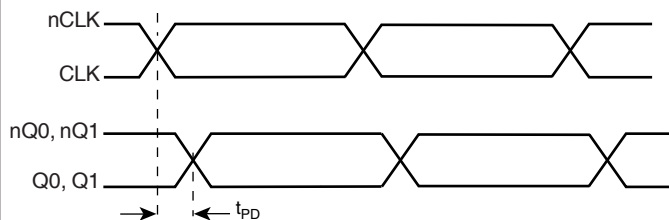
OUTPUT SKEW



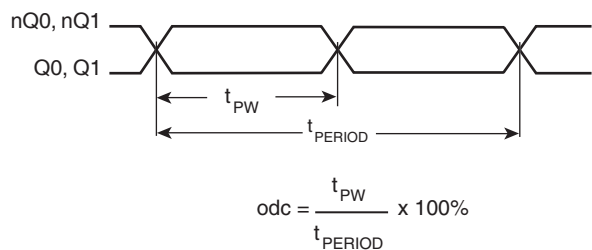
PART-TO-PART SKEW



OUTPUT RISE/FALL TIME



PROPAGATION DELAY



OUTPUT DUTY CYCLE PULSE WIDTH/PERIOD

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio

of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{DD} = 3.3V$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.

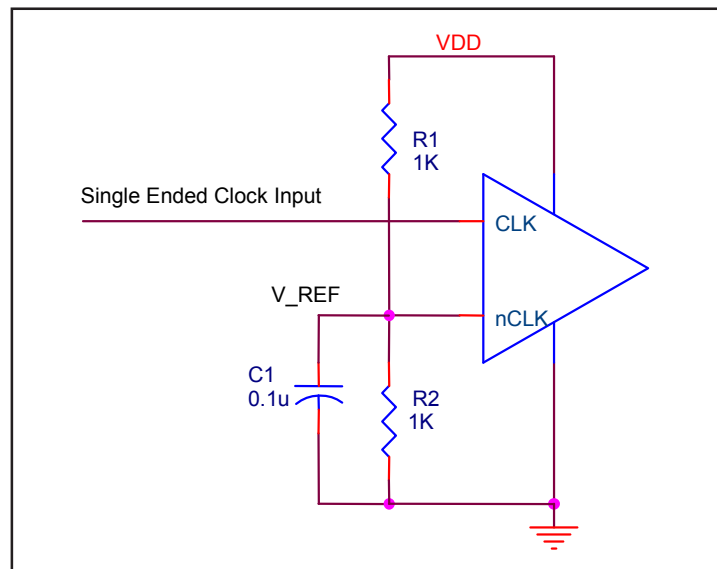


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

RECOMMENDATIONS FOR UNUSED OUTPUT PINS

OUTPUTS:

LVHSTL OUTPUT

All unused LVHSTL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

CLOCK INPUT INTERFACE

The CLK /nCLK accepts differential input signals of both V_{SWING} and V_{OH} to meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2D* show interface examples for the ICS85211I clock input driven by most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the

driver components to confirm the driver termination requirement. For example in *Figure 2A*, the input termination applies for LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

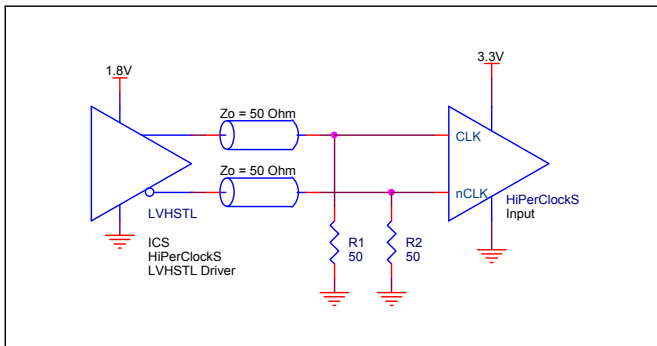


FIGURE 2A. ICS85211I CLK/nCLK INPUT DRIVEN BY LVHSTL DRIVER

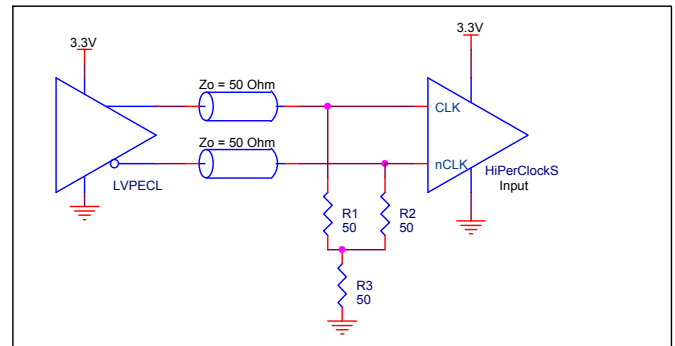


FIGURE 2B. ICS85211I CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER (INTERFACE 1)

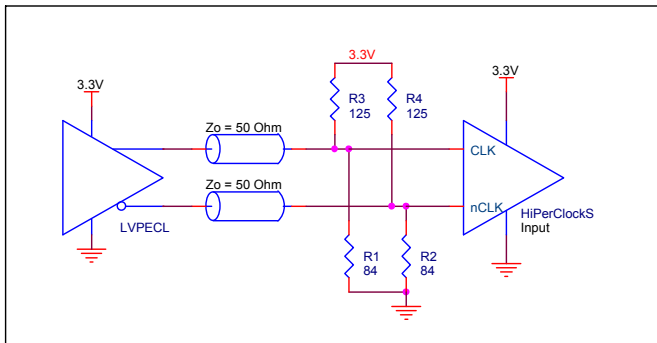


FIGURE 2C. ICS85211I CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER (INTERFACE 2)

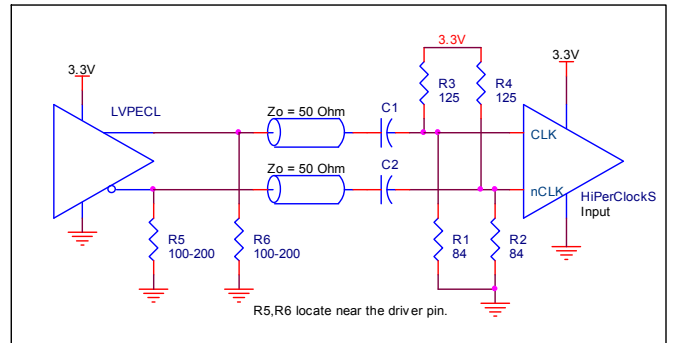


FIGURE 2D. ICS85211I CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE

SCHEMATIC EXAMPLE

Figure 3 shows a schematic example of ICS85211I. In this example, the input is driven by an ICS LVHSTL driver. The decoupling capacitors should be physically located near the

power pin. For ICS85211I, the unused outputs need to be terminated.

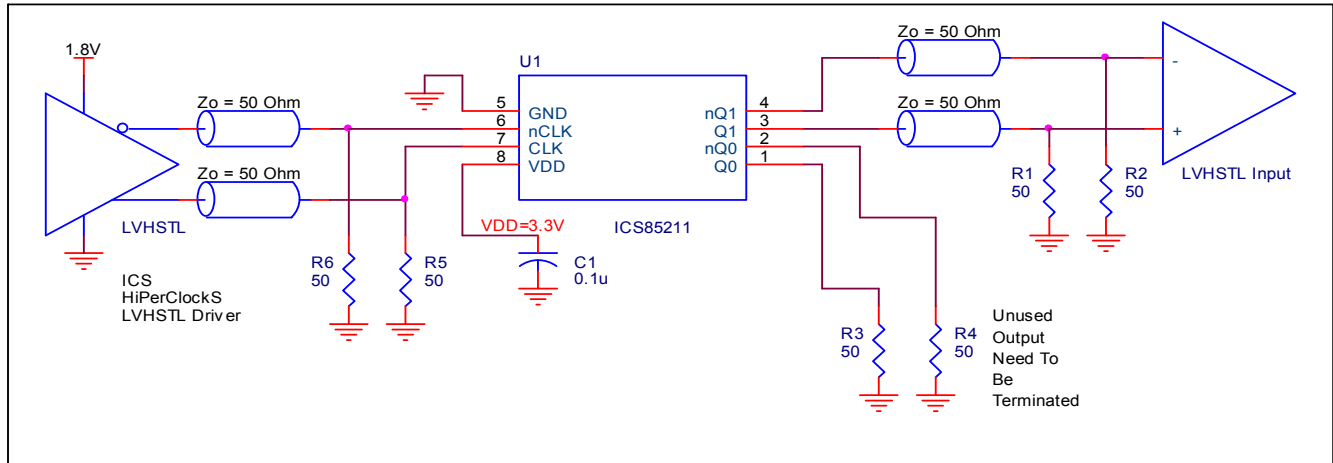


FIGURE 3. ICS85211I LVHSTL BUFFER SCHEMATIC EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS85211I. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS85211I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{DD_MAX} * I_{DD_MAX} = 3.465V * 50mA = 173.3mW$
- Power (outputs)_{MAX} = **78.88mW/Loaded Output pair**
If all outputs are loaded, the total power is $2 * 78.88mW = 157.8mW$

Total Power_{MAX} (3.465V, with all outputs switching) = $173.3mW + 157.8mW = 311.1mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for the devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 103.3°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.311W * 103.3^\circ C/W = 117.1^\circ C. \text{ This is well below the limit of } 125^\circ C.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 8-PIN SOIC, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVHSTL output driver circuit and termination are shown in *Figure 4*.

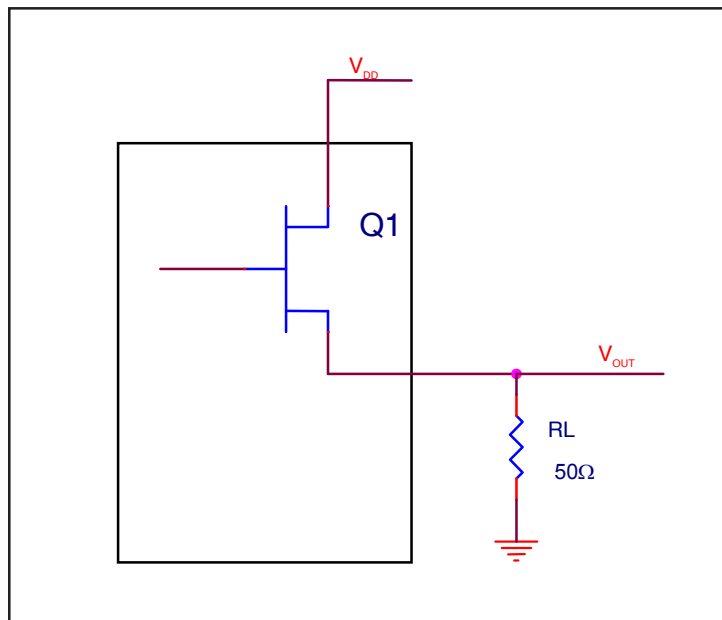


FIGURE 4. LVHSTL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = (V_{OH_MAX} / R_L) * (V_{DD_MAX} - V_{OH_MAX})$$

$$Pd_L = (V_{OL_MAX} / R_L) * (V_{DD_MAX} - V_{OL_MAX})$$

$$Pd_H = (1.2V / 50\Omega) * (3.465V - 1.2V) = 54.36mW$$

$$Pd_L = (0.4V / 50\Omega) * (3.465V - 0.4V) = 24.52mW$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = \mathbf{78.88mW}$$

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD SOIC

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

TRANSISTOR COUNT

The transistor count for ICS85211I is: 411

PACKAGE OUTLINE - M SUFFIX FOR 8 LEAD SOIC

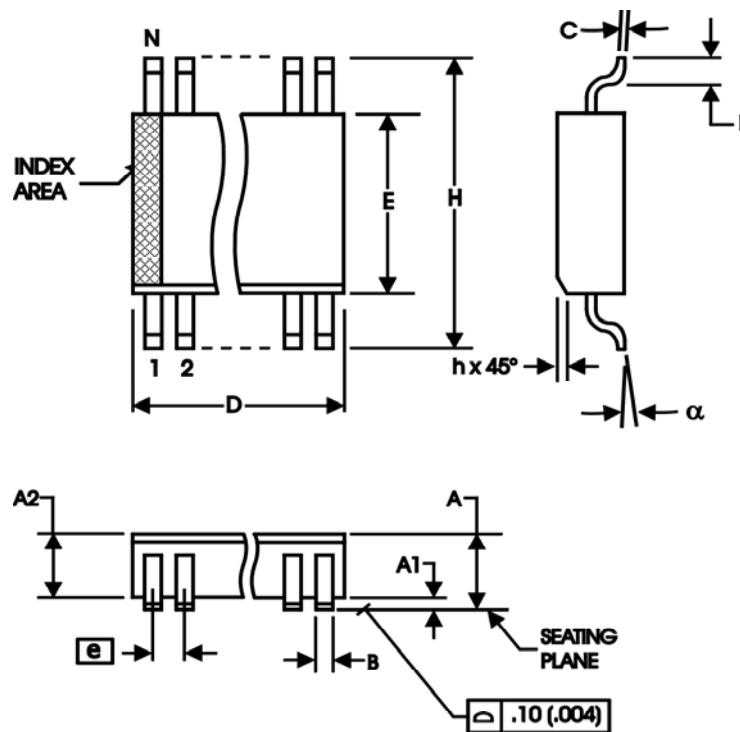


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MINIMUM	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
I85211AMI	85211AMI	8 lead SOIC	tube	-40°C to 85°C
85211AMIT	85211AMI	8 lead SOIC	2500 tape & reel	-40°C to 85°C
85211AMILF	85211AIL	8 lead SOIC	tube	-40°C to 85°C
85211AMILFT	85211AIL	8 lead SOIC	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology, Inc. (IDT) assumes no responsibility for either its use or for infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial and industrial applications. Any other applications such as those requiring high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

REVISION HISTORY SHEET

Rev	Table	Page	Description of Change	Date
B	T4A	3	Power Supply table, changed maximum I_{DD} spec to 50mA from 40mA.	4/8/03
		7	Power Considerations, changed I_{DD_MAX} to 50mA from 40mA and recalculated equations.	
C	T2	1	Features Section - added lead-free bullet.	7/12/06
		2	Pin Characteristics - changed CIN 4pF max. to 4pF typical.	
		5	Added <i>Recommendations for Unused Output Pins</i> .	
D	T9	12	Ordering Information Table - added lead-free part number, marking and note.	7/26/10
		14	Updated datasheet's header/footer with IDT from ICS. Removed ICS prefix from Part/Order Number column. Added Contact Page.	

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales

800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support

netcom@idt.com
480-763-2056

Corporate Headquarters

Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Asia Pacific and Japan

Integrated Device Technology
Singapore (1997) Pte. Ltd.
Reg. No. 199707558G
435 Orchard Road
#20-03 Wisma Atria
Singapore 238877
+65 6 887 5505

Europe

IDT Europe, Limited
321 Kingston Road
Leatherhead, Surrey
KT22 7TU
England
+44 (0) 1372 363 339
Fax: +44 (0) 1372 378851



www.IDT.com