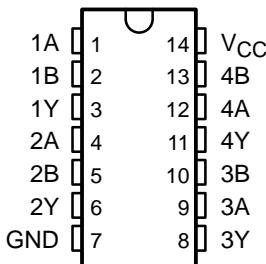


- AC Types Feature 1.5-V to 5.5-V Operation and Balanced Noise Immunity at 30% of the Supply
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Balanced Propagation Delays
- $\pm 24$ -mA Output Drive Current
  - Fanout to 15 F Devices
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015

E OR M PACKAGE  
(TOP VIEW)



### description/ordering information

The CD74AC86 is a quadruple 2-input exclusive-OR gate. This device performs the Boolean function  $Y = A \oplus B$  or  $Y = \overline{A}B + A\overline{B}$  in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	PDIP – E	Tube	CD74AC86E	CD74AC86E
	SOIC – M	Tube	CD74AC86M	AC86M
		Tape and reel	CD74AC86M96	

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

### FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# CD74AC86

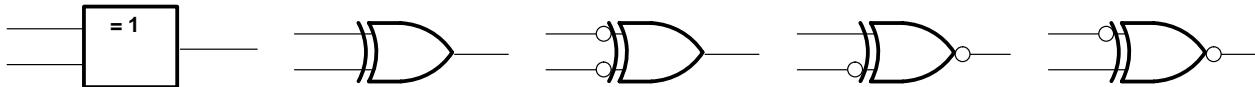
## QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

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### exclusive-OR logic

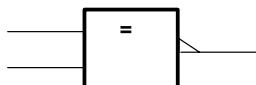
An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE OR



These are five equivalent exclusive-OR symbols valid for an CD74AC86 gate in positive logic; negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT



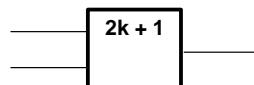
The output is active (low) if all inputs stand at the same logic level (i.e.,  $A = B$ ).

EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ .....	-0.5 V to 6 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1) .....	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 100$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): E package .....	80°C/W
	M package .....
Storage temperature range, $T_{STG}$ .....	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JEDEC 51-7.

recommended operating conditions (see Note 3)

			$T_A = 25^\circ\text{C}$		$-55^\circ\text{C} \text{ to } 125^\circ\text{C}$		$-40^\circ\text{C} \text{ to } 85^\circ\text{C}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage		1.5	5.5	1.5	5.5	1.5	5.5	V
V <sub>IH</sub>	High-level input voltage		V <sub>CC</sub> = 1.5 V		1.2		1.2		V
			V <sub>CC</sub> = 3 V		2.1		2.1		
			V <sub>CC</sub> = 5.5 V		3.85		3.85		
V <sub>IL</sub>	Low-level input voltage		V <sub>CC</sub> = 1.5 V		0.3		0.3		V
			V <sub>CC</sub> = 3 V		0.9		0.9		
			V <sub>CC</sub> = 5.5 V		1.65		1.65		
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		V <sub>CC</sub> = 4.5 V to 5.5 V		-24		-24		mA
I <sub>OL</sub>	Low-level output current		V <sub>CC</sub> = 4.5 V to 5.5 V		24		24		mA
$\Delta t/\Delta v$	Input transition rise or fall rate		V <sub>CC</sub> = 1.5 V to 3 V		50		50		ns/V
			V <sub>CC</sub> = 3.6 V to 5.5 V		20		20		

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	$T_A = 25^\circ\text{C}$		$-55^\circ\text{C} \text{ to } 125^\circ\text{C}$		$-40^\circ\text{C} \text{ to } 85^\circ\text{C}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 $\mu\text{A}$	1.5 V	1.4	1.4		1.4		V
			3 V	2.9	2.9		2.9		
			4.5 V	4.4	4.4		4.4		
		I <sub>OH</sub> = -4 mA	3 V	2.58	2.4		2.48		
		I <sub>OH</sub> = -24 mA	4.5 V	3.94	3.7		3.8		
		I <sub>OH</sub> = -50 mA <sup>†</sup>	5.5 V		3.85				
		I <sub>OH</sub> = -75 mA <sup>†</sup>	5.5 V				3.85		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 $\mu\text{A}$	1.5 V	0.1	0.1		0.1		V
			3 V	0.1	0.1		0.1		
			4.5 V	0.1	0.1		0.1		
		I <sub>OL</sub> = 12 mA	3 V	0.36	0.5		0.44		
		I <sub>OL</sub> = 24 mA	4.5 V	0.36	0.5		0.44		
		I <sub>OL</sub> = 50 mA <sup>†</sup>	5.5 V			1.65			
		I <sub>OL</sub> = 75 mA <sup>†</sup>	5.5 V				1.65		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		5.5 V		$\pm 0.1$		$\pm 1$		$\mu\text{A}$
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0		5.5 V		4		80		$\mu\text{A}$
C <sub>i</sub>					10		10		pF

<sup>†</sup> Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50- $\Omega$  transmission-line drive capability at 85°C and 75- $\Omega$  transmission-line drive capability at 125°C.

# CD74AC86

## QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

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**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 1.5$  V,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C TO 85°C		UNIT
			MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	Y		135		123	ns
$t_{PHL}$				135		123	

**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3$  V  $\pm 0.3$  V,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C TO 85°C		UNIT
			MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	Y	3.8	15.1	3.9	13.7	ns
$t_{PHL}$			3.8	15.1	3.9	13.7	

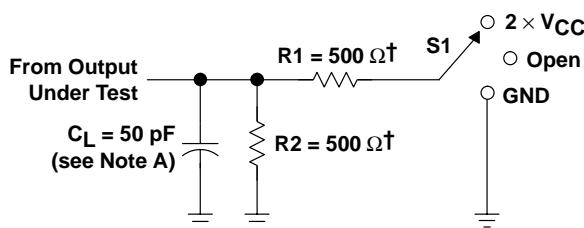
**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5$  V  $\pm 0.5$  V,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C TO 85°C		UNIT
			MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	Y	2.7	10.8	2.8	9.8	ns
$t_{PHL}$			2.7	10.8	2.8	9.8	

**operating characteristics,  $T_A = 25^\circ\text{C}$**

PARAMETER			TYP	UNIT
$C_{pd}$	Power dissipation capacitance		57	pF

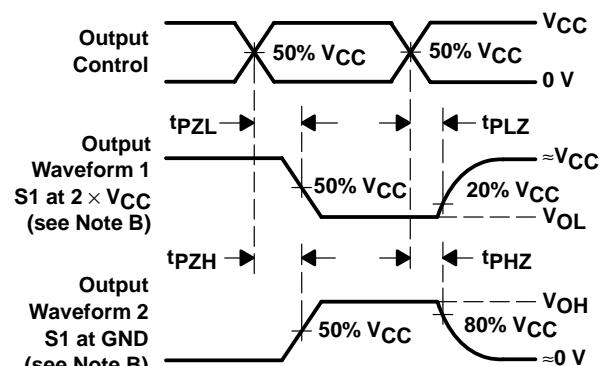
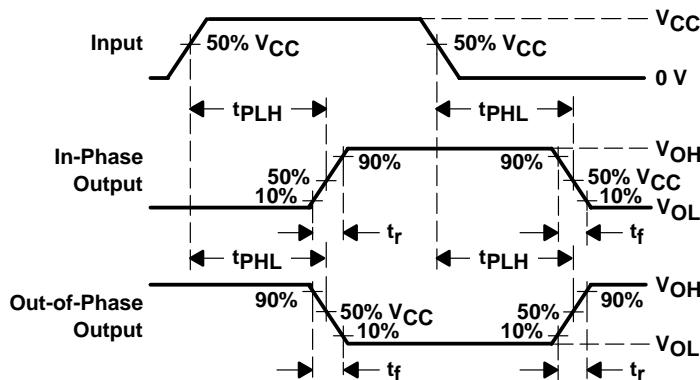
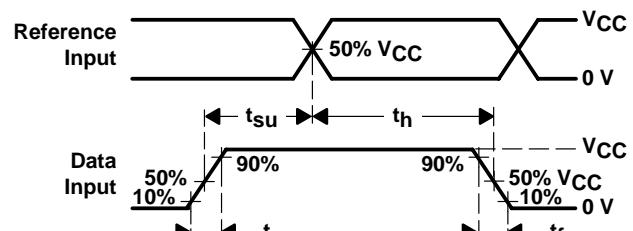
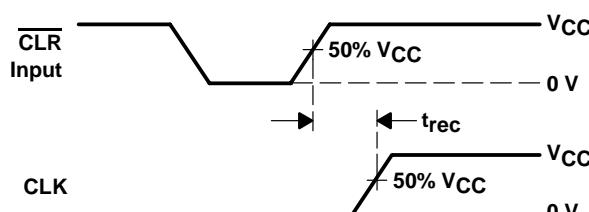
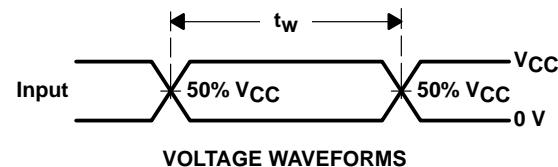
PARAMETER MEASUREMENT INFORMATION



$\dagger$  When  $V_{CC} = 1.5 \text{ V}$ ,  $R1 = R2 = 1 \text{ k}\Omega$

LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



NOTES:

- $C_L$  includes probe and test-fixture capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ . Phase relationships between waveforms are arbitrary.
- For clock inputs,  $f_{max}$  is measured with the input duty cycle at 50%.
- The outputs are measured one at a time with one input transition per measurement.
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD74AC86E	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74AC86EE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74AC86M	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC86M96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC86M96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC86M96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC86ME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC86MG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

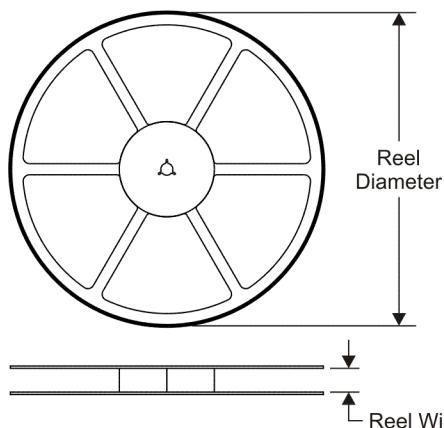
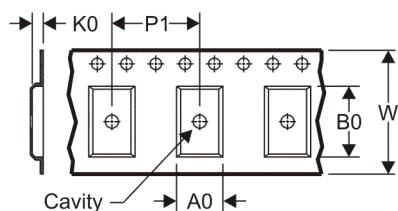
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

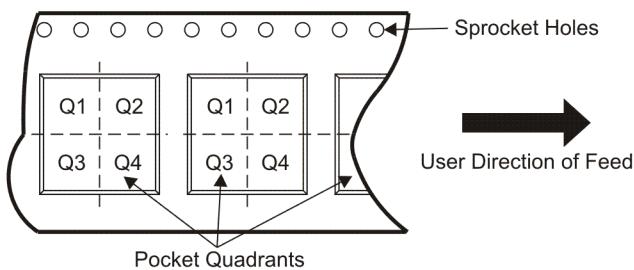
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


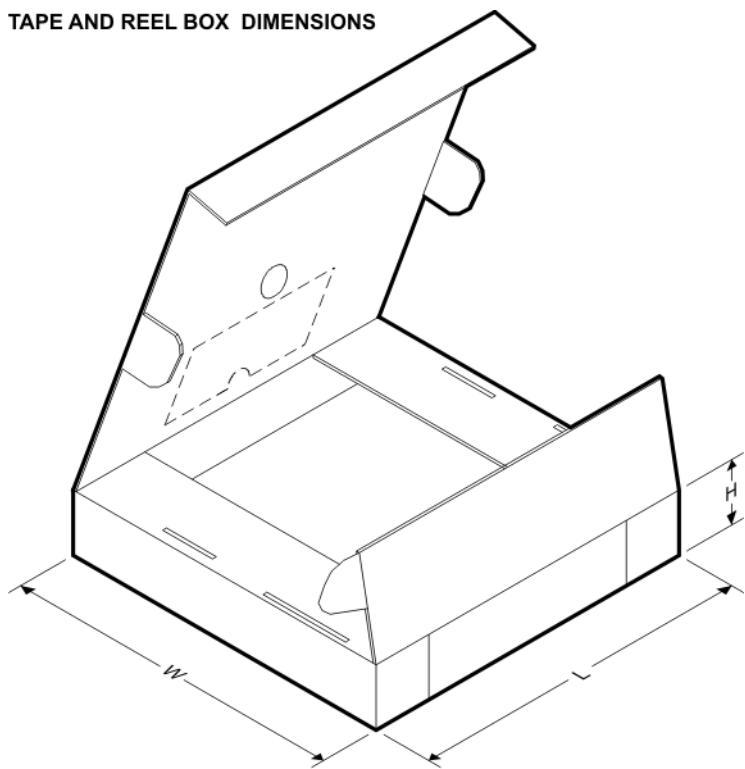
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC86M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



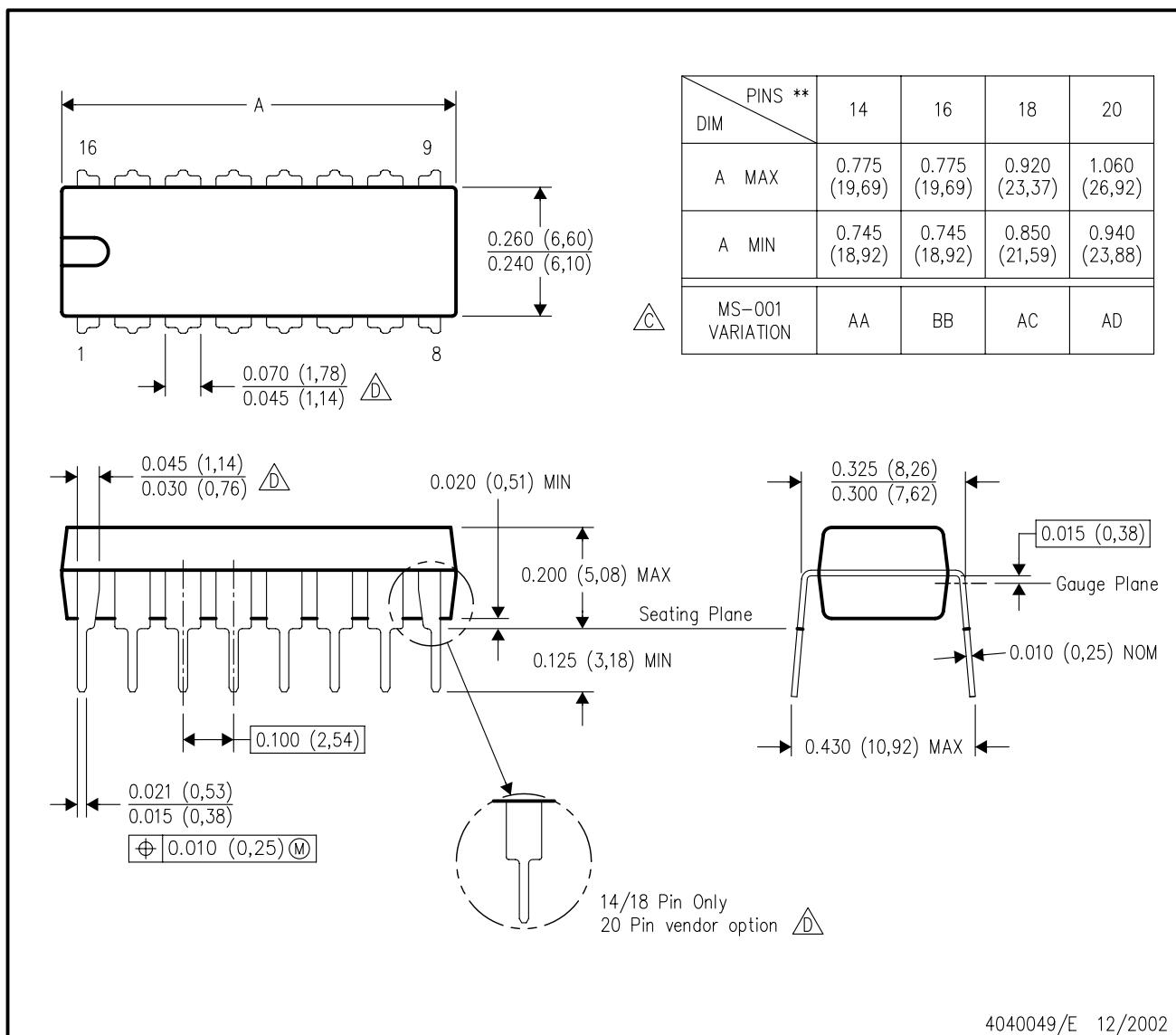
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC86M96	SOIC	D	14	2500	346.0	346.0	33.0

## N (R-PDIP-T\*\*)

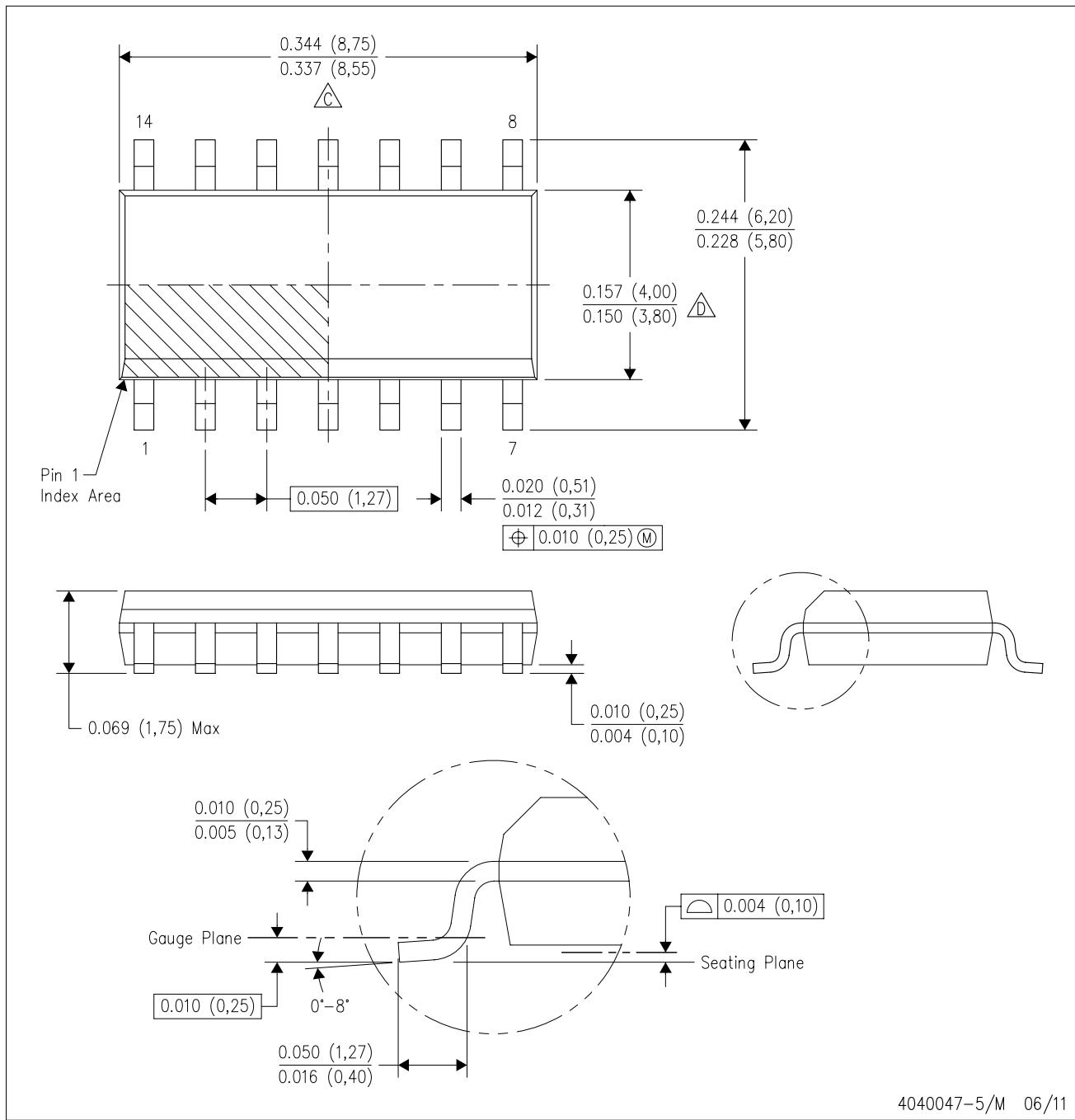
16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

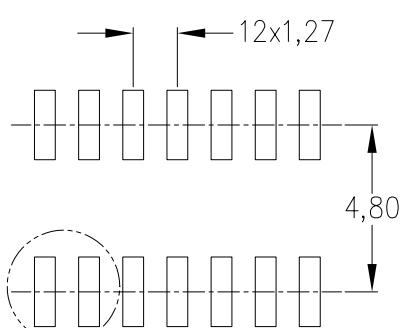
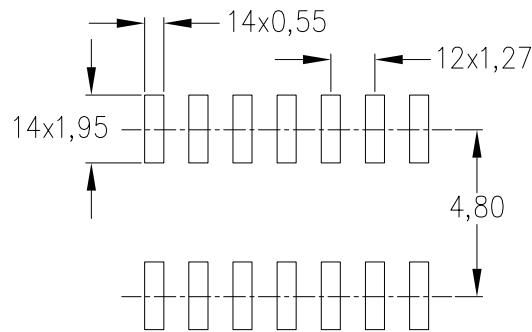
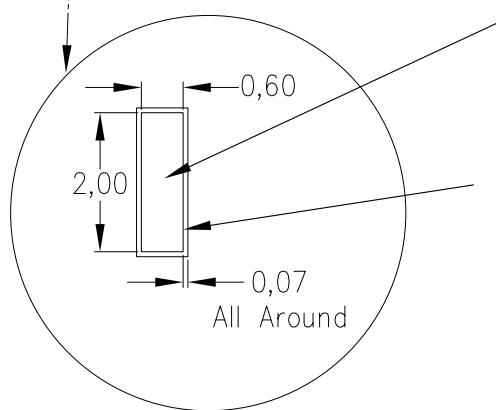
C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Solder Mask Opening  
(See Note E)

4211283-3/D 06/11

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
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RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>

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