



STD85N3LH5 STP85N3LH5, STU85N3LH5

N-channel 30 V, 0.0042 Ω , 80 A, DPAK, TO-220, IPAK
STripFET™ V Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)} max	I _D
STD85N3LH5	30 V	< 0.005 Ω	80 A
STP85N3LH5	30 V	< 0.0054 Ω	80 A
STU85N3LH5	30 V	< 0.0054 Ω	80 A

- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- High avalanche ruggedness
- Low gate drive power losses

Application

- Switching applications

Description

This product utilizes the 5th generation of design rules of ST's proprietary STripFET™ technology. The lowest available R_{DS(on)} * Q_g, in the standard packages, makes this device suitable for the most demanding DC-DC converter applications, where high power density is to be achieved.

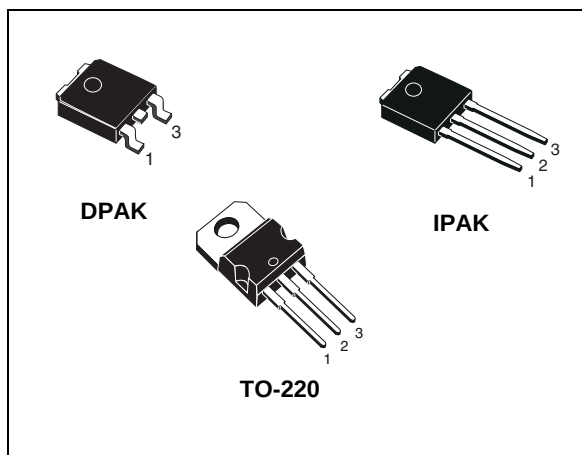


Figure 1. Internal schematic diagram

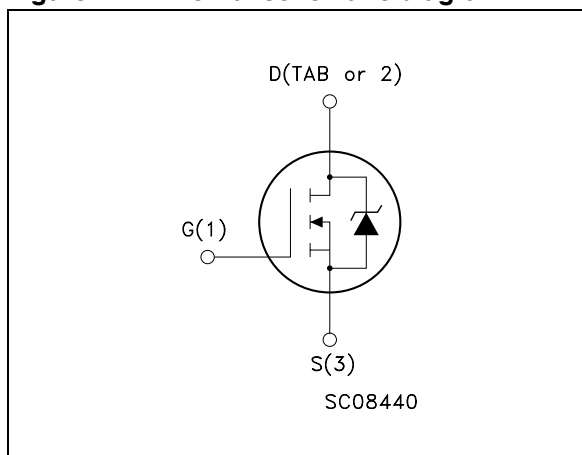


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD85N3LH5	85N3LH5	DPAK	Tape and reel
STP85N3LH5	85N3LH5	TO-220	Tube
STU85N3LH5	85N3LH5	IPAK	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	30	V
V_{DS}	Drain-source voltage ($V_{GS} = 0$) @ T_{JMAX}	35	V
V_{GS}	Gate-source voltage	± 22	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	80	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	55	A
$I_{DM}^{(2)}$	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	70	W
	Derating factor	0.47	W/ $^{\circ}\text{C}$
$E_{AS}^{(3)}$	Single pulse avalanche energy	165	mJ
T_{stg}	Storage temperature	-55 to 175	$^{\circ}\text{C}$
T_j	Max. operating junction temperature	175	$^{\circ}\text{C}$

1. Limited by wire bonding
2. Pulse width limited by safe operating area
3. Starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = 40\text{ A}$, $V_{DD} = 25\text{ V}$

Table 3. Thermal resistance

Symbol	Parameter	Value			Unit
		TO-220	DPAK	IPAK	
$R_{thj-case}$	Thermal resistance junction-case max	2.14			$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-amb max	62.5		100	$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}$	Thermal resistance junction-pcb max		100		$^{\circ}\text{C}/\text{W}$
T_L	Maximum lead temperature for soldering purpose	275			$^{\circ}\text{C}$

2 Electrical characteristics

($T_{CASE} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 20\text{ V}$ $V_{DS} = 20\text{ V}$, $T_c = 125\text{ }^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 22\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1		2.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 40\text{ A}$ SMD version		0.042	0.005	Ω
		$V_{GS} = 10\text{ V}$, $I_D = 40\text{ A}$		0.0046	0.0054	Ω
		$V_{GS} = 5\text{ V}$, $I_D = 40\text{ A}$ SMD version		0.0052	0.0065	Ω
		$V_{GS} = 5\text{ V}$, $I_D = 40\text{ A}$		0.0058	0.0071	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		1850 380 58		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 15\text{ V}$, $I_D = 80\text{ A}$ $V_{GS} = 5\text{ V}$ Figure 16		14 6.8 4.7		nC nC nC
Q_{gs1} Q_{gs2}	Pre V_{th} gate-to-source charge Post V_{th} gate-to-source charge	$V_{DD} = 15\text{ V}$, $I_D = 80\text{ A}$ $V_{GS} = 5\text{ V}$ Figure 16		2.3 4.5		nC nC
R_G	Gate input resistance	$f = 1\text{ MHz}$ gate bias Bias = 0 test signal level = 20 mV open drain		1.2		Ω

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD} = 15\text{ V}$, $I_D = 40\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 5\text{ V}$ Figure 15		6 14		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD} = 15\text{ V}$, $I_D = 40\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 5\text{ V}$ Figure 15		23.6 10.8		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				80 320	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 40\text{ A}$, $V_{GS} = 0$			1.1	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 80\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 20\text{ V}$ Figure 17		31.8 26.1 1.6		ns nC A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

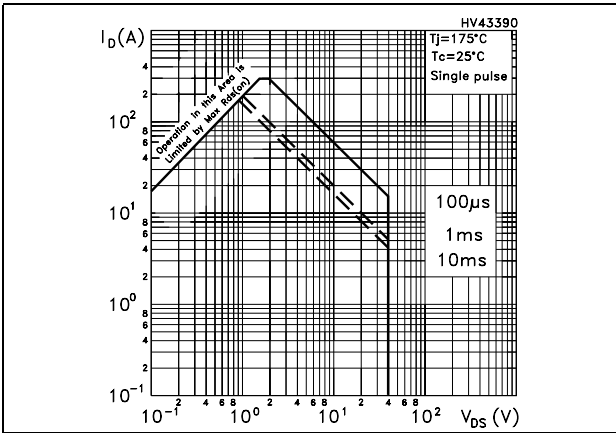


Figure 3. Thermal impedance

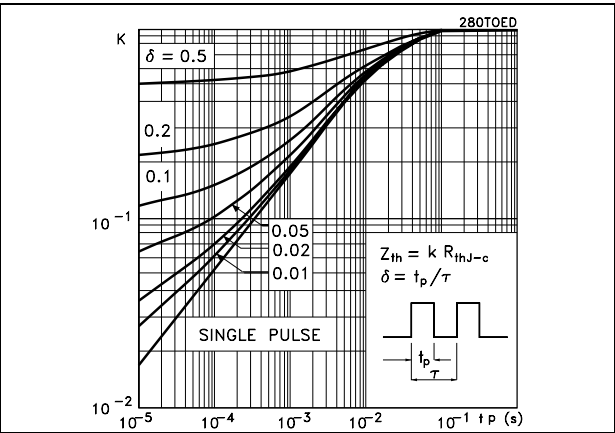


Figure 4. Output characteristics

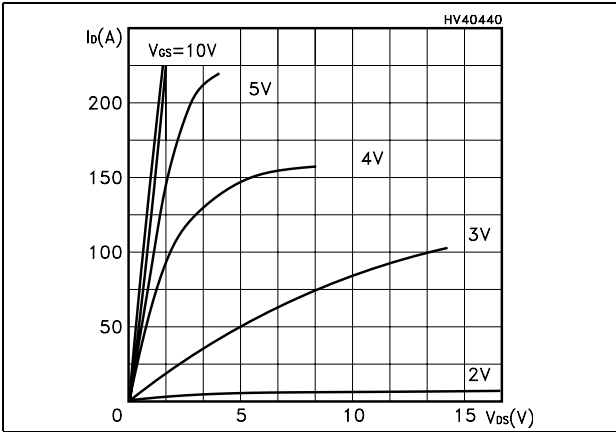


Figure 5. Transfer characteristics

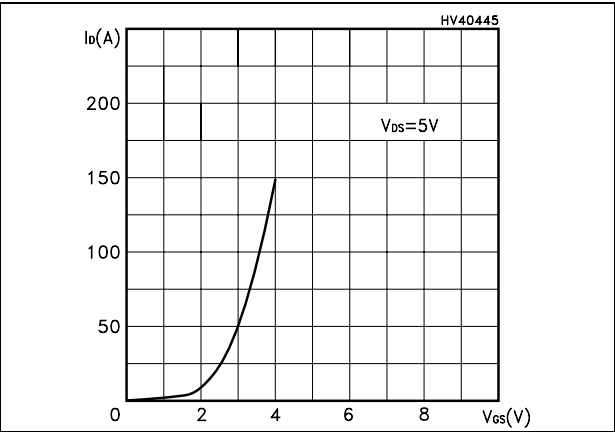


Figure 6. Normalized B_VDSS vs temperature

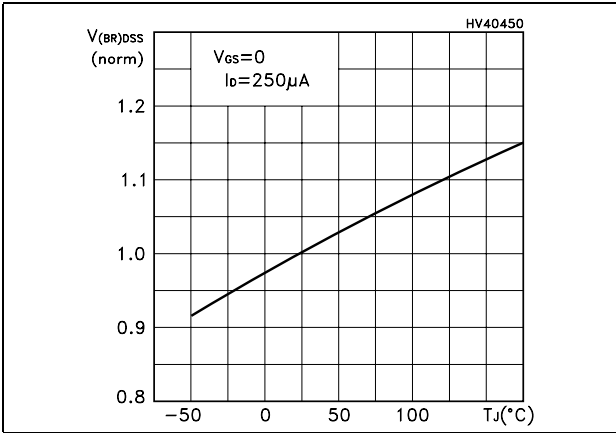


Figure 7. Static drain-source on resistance

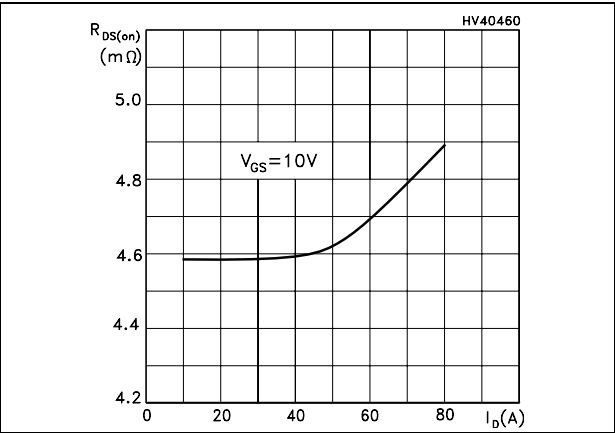


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

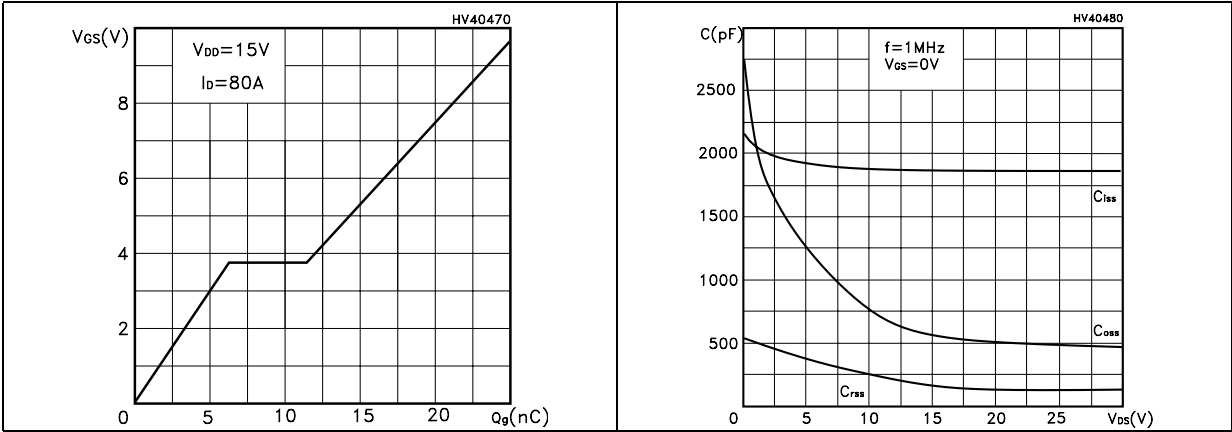


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

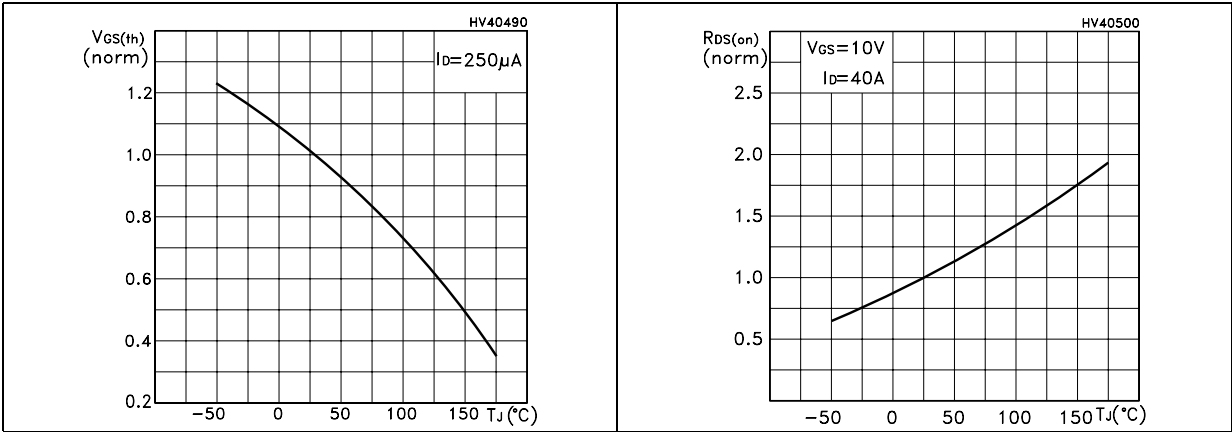
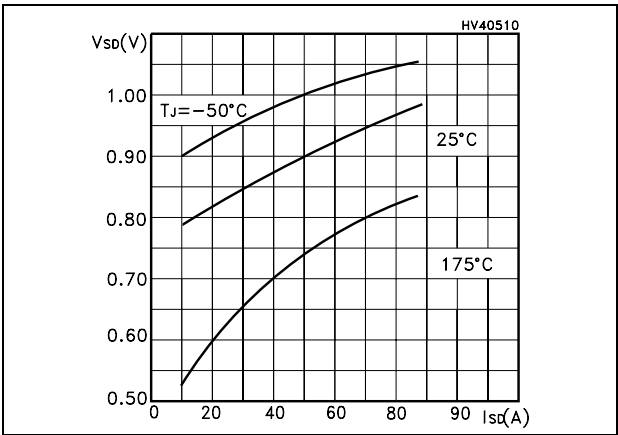


Figure 12. Source-drain diode forward characteristics



3 Test circuit

Figure 13. Switching times test circuit for resistive load

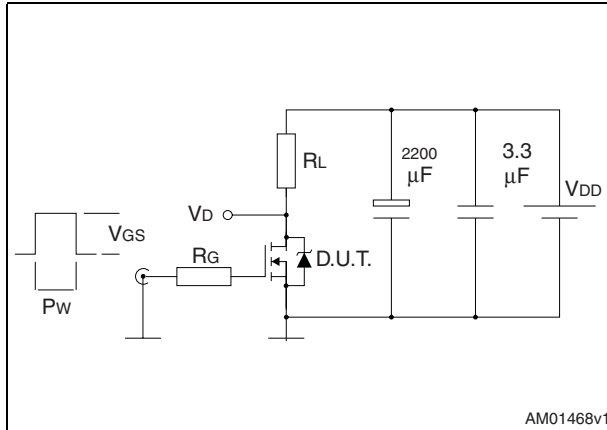


Figure 14. Gate charge test circuit

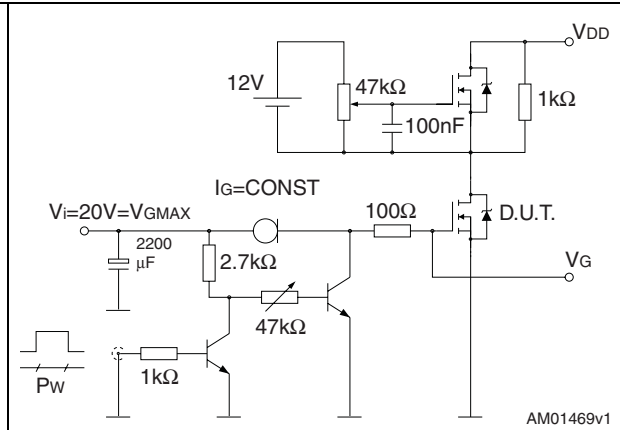


Figure 15. Test circuit for inductive load switching and diode recovery times

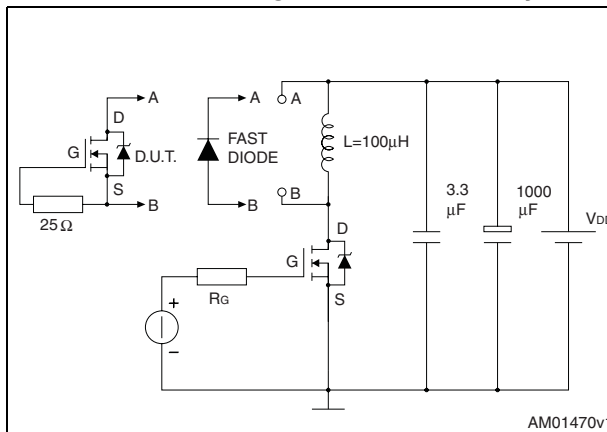


Figure 16. Unclamped inductive load test circuit

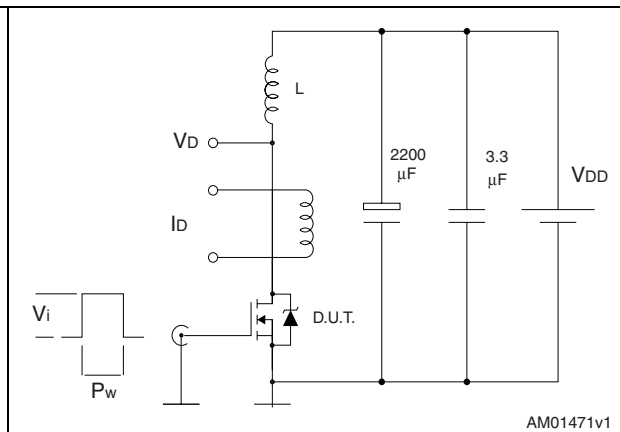


Figure 17. Unclamped inductive waveform

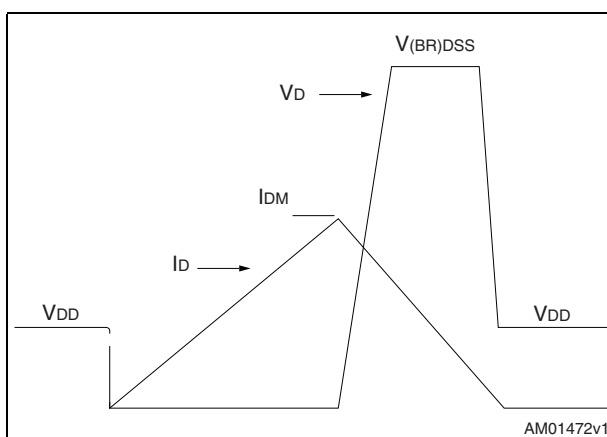


Figure 18. Switching time waveform

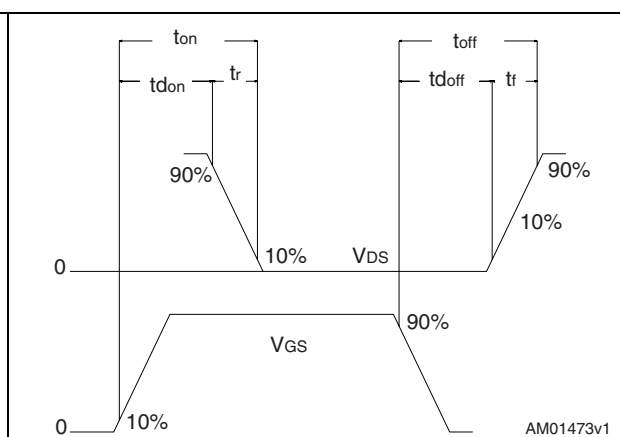
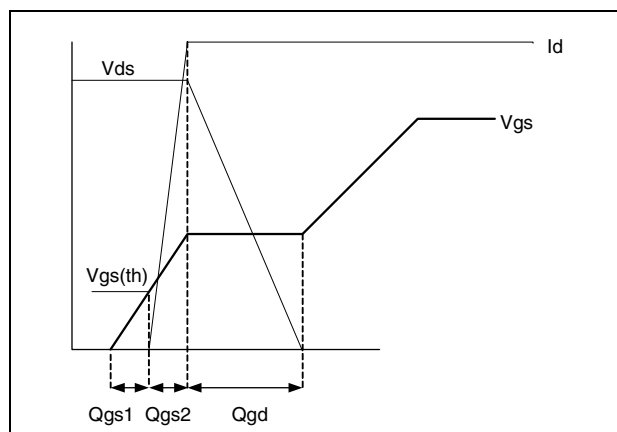


Figure 19. Gate charge waveform

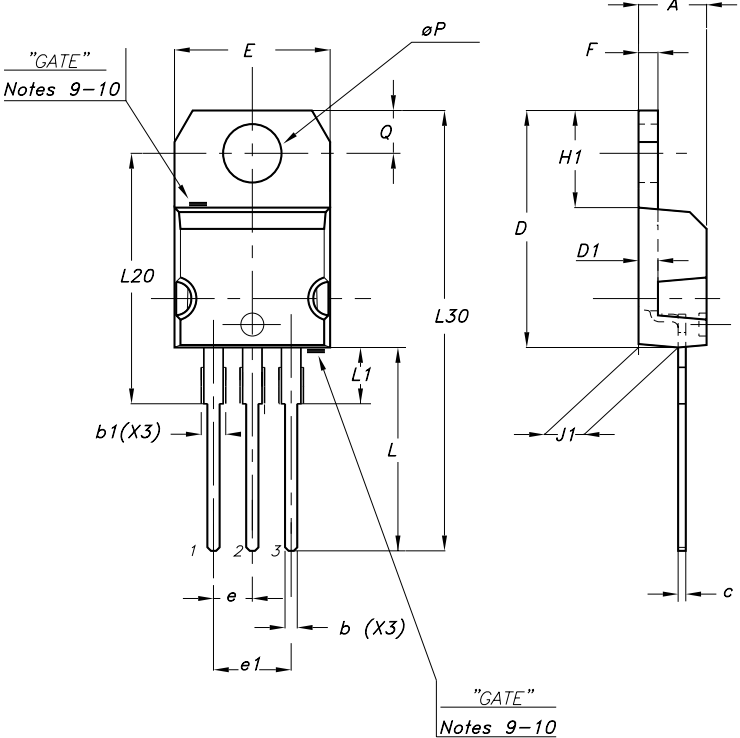


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

TO-220 mechanical data

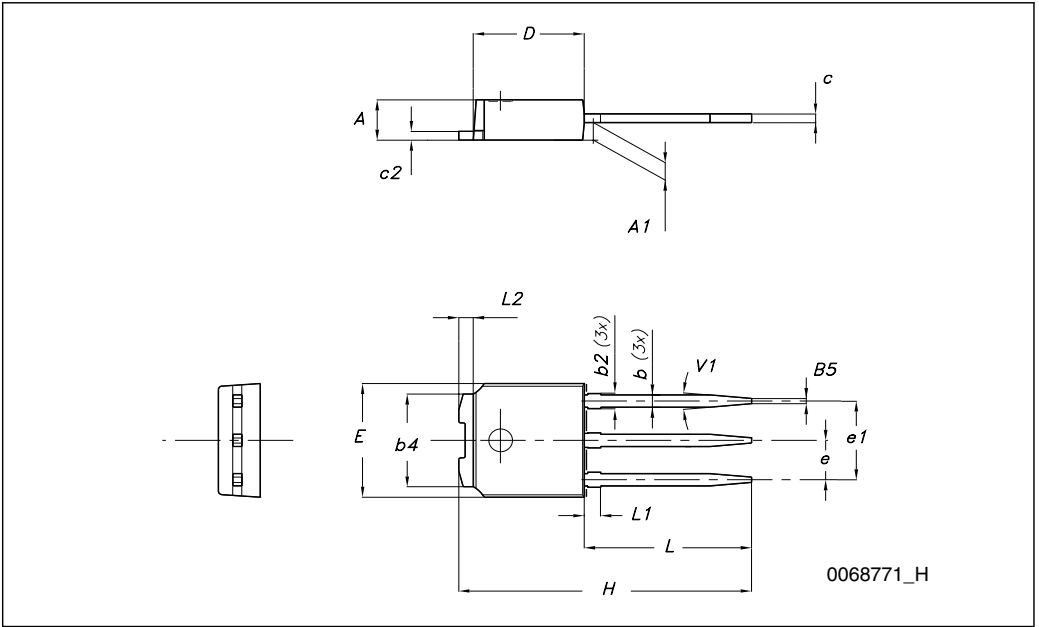
Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
ØP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



0015988_Rev_R

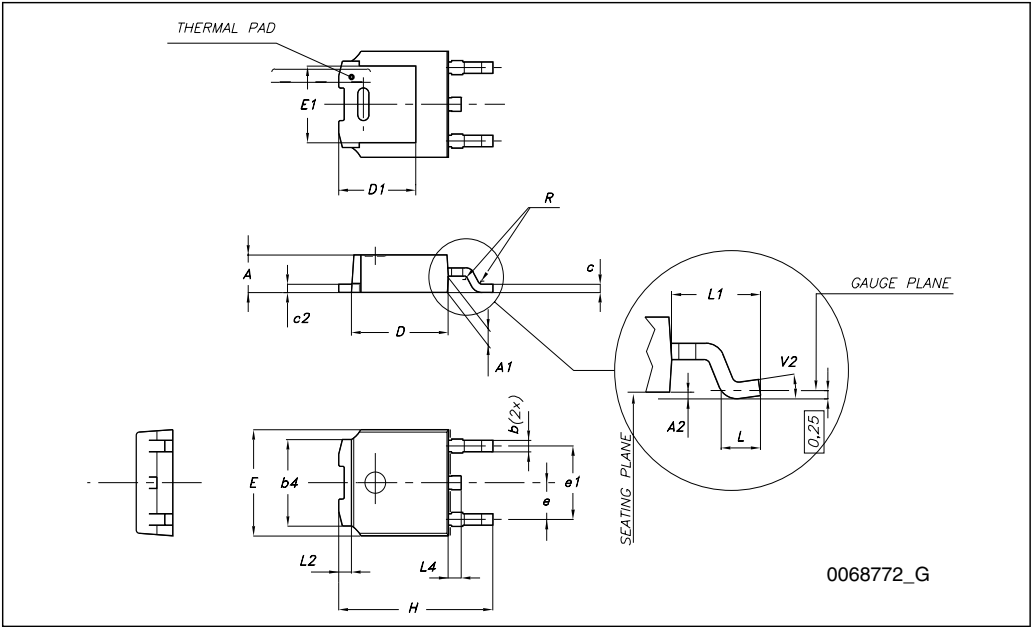
TO-251 (IPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
(L1)	0.80		1.20
L2		0.80	
V1		10°	



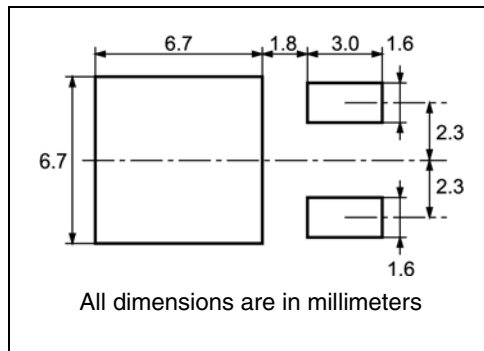
TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

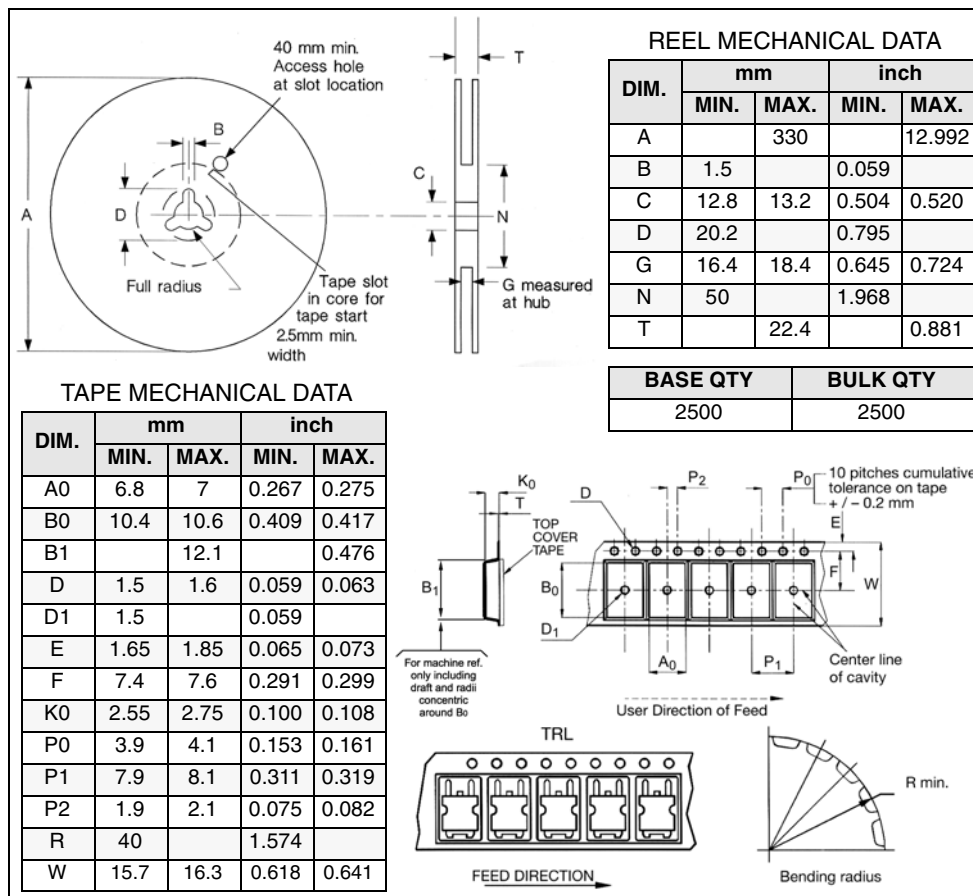


5 Packaging mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT



6 Revision history

Table 8. Document revision history

Date	Revision	Changes
19-Oct-2007	1	First release
20-Feb-2008	2	Minor text changes to improve readability
21-Jul-2008	3	– Added new package, mechanical data: TO-220 – Figure 2: Safe operating area has been corrected – Figure 7: Static drain-source on resistance updated – New value on Table 2: Absolute maximum ratings
20-Aug-2008	4	Added max value on $V_{GS(th)}$ (Table 4)
25-Sep-2008	5	V_{GS} values has been changed on Table 2 and Table 4
22-Jan-2009	6	Corrected value on Table 3: Thermal resistance

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