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**JAPAN**: Motorola Japan, Ltd.; SPS, Technical Information Center, 3-20-1, Minami-Azabu, Minato-ku Tokyo 106-8573 Japan. 81-3-3440-3569

**ASIA/PACIFIC**: Motorola Semiconductors H.K. Ltd., Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate, 2 Tai Po, N.T., Hong Kong. 852-26668334

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### About This Book

microprocessor, the third generation of the DragonBall family of products. It provides the details of how to initialize, configure, and program the MC68VZ328. The manual presumes basic knowledge of 68000 This user's manual describes the features and operation of the MC68VZ328 (DragonBall<sup>TM</sup> VZ)

## Audience

successfully integrate the MC68VZ328 into a wide variety of applications. It is assumed that the reader has a good working knowledge of the 68000 CPU. For programming information about the 68000, see the documents listed in the Suggested Reading section of this preface. The MC68VZ328 user's manual is intended to provide a design engineer with the necessary data to

## Organization

the DragonBall VZ device. Summaries of the chapters follow. The MC68VZ328 user's manual is organized into 20 chapters that cover the operation and programming of

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Chapter 2 Chapter 3 Chapter 4	Introduction: This chapter contains a device overview, system block diagrams, and an operational overview of 68000 CPU operation.  Signal Descriptions: This chapter contains listings of the MC68VZ328 input and output signals, organized into functional groups.  Memory Map: This chapter summarizes the memory organization, programming information, and registers' addresses and reset values.  Clock Generation Module and Power Control Module: This chapter provides detailed information about the operation and programming of the clock generation module as well as the recommended circuit schematics for external
Chapter 3	<b>Memory Map</b> : This chapter summarizes the memory organization, programming information, and registers' addresses and reset values.
Chapter 4	Clock Generation Module and Power Control Module: This chapter provides detailed information about the operation and programming of the clock generation module as well as the recommended circuit schematics for external clock circuits. It also describes and provides programming information about the operation of the power control module and the system power states.
Chapter 5	<b>System Control:</b> This chapter describes the operation of and programming models for the system control, peripheral control, ID, and I/O drive control registers.
Chapter 6	<b>Chip-Select Logic:</b> This chapter describes the operation and programming of the chip-select logic. It includes information related to the operation of the DRAM controller and other memory-related applications.



Chapter 8

LCD controller, which provides display data for external LCD drivers or for an LCD Controller: This chapter describes the operation and programming of the 16-bit DRAM supporting EDO RAM, Fast Page Mode, and synchronous DRAM described in this chapter. This module provides a glueless interface to 8-bit or **DRAM Controller**: The operation and programming of the DRAM controller is

LCD panel.

Chapter 7

Chapter 16

Chapter 17

Chapter 15 Pulse-Width Modulator 1 and 2: This chapter describes both pulse-width	Chapter 14 Universal Asynchronous Receiver/Transmitter 1 and 2: The two universal asynchronous receiver/transmitter (UART) ports allow the incorporation of serial communication in existing and new designs. This section describes how data is transported in character blocks using the standard "start-stop" format. It also discusses how to configure and program the UART modules.	Chapter 13 Serial Peripheral Interface 1 and 2: This chapter describes the features of the DragonBall VZ's two serial peripheral interfaces and how they are used to communicate with external devices.	Chapter 12 <b>General-Purpose Timers</b> : This chapter describes the two 16-bit timers that can be used as both watchdogs and alarms. It also describes how the timers can be combined into a single 32-bit timer.	Chapter 11  Real-Time Clock: This chapter describes the operation of the real-time clock (RTC) module, which is composed of a prescaler, time-of-day (TOD) clock, TOD alarm, programmable real-time interrupt, watchdog timer, and minute stopwatch as well as control registers and bus interface hardware.	Chapter 10 I/O Ports: This chapter covers all 76 GPIO lines found in the MC68VZ328.  Because each pin is individually configurable, a detailed description of the operation of and programming information for each pin is provided.	Chapter 9 Interrupt Controller: This chapter provides a description and operational considerations for interrupt controller operation. It includes a description of the vector generator and pen and keyboard interrupts.	
using the standard "start-stop" format. It also program the UART modules.	<b>eiver/Transmitter 1 and 2:</b> The two universal tter (UART) ports allow the incorporation of serial new designs. This section describes how data is	and 2: This chapter describes the features of the ripheral interfaces and how they are used to vices.	is chapter describes the two 16-bit timers that can lalarms. It also describes how the timers can be imer.	sed of a prescaler, time-of-day (TOD) clock, TOI interrupt, watchdog timer, and minute stopwatch bus interface hardware.	all 76 GPIO lines found in the MC68VZ328. ly configurable, a detailed description of the information for each pin is provided.	apter provides a description and operational atroller operation. It includes a description of the eyboard interrupts.	

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a new design. It as to get started with the design processor.

Lechanical Data and Ordering Information: This chapter provides mechanical data, including illustrations, and ordering information.

Chapter 19

Chapter 20

Mechanical Data and Ordering Information: This chapter provides

Electrical Characteristics: This chapter describes the electrical characteristics

Development System (ADS) board to get started with the design process

Chapter 18

integration of the MC68VZ328 into an existing or a new design. It includes a design checklist and instructions for using the MC68VZ328 Application

Application Guide: This chapter contains information that will assist during the

system's RAM using the UART 1 or UART 2 controller.

system to initialize a target system and download a program or data to the target chapter. This chapter describes programming information necessary to allow a Bootstrap Mode: The operation of bootstrap models is described in detail in this

MC68VZ328 microprocessor.

module and how it is used to support low-cost emulator designs for the In-Circuit Emulation: This chapter describes the in-circuit emulation (ICE)

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## Suggested Reading

design properly with the part. Especially for those not familiar with the 68000 CPU, the following documents will be helpful when used in conjunction with this manual. The following documents are required for a complete description of the MC68VZ328 and are necessary to

M68000 Family Programmer's Reference Manual (order number M68000PM/AD)

M68000 User's Manual (order number M68000UM/D)

M68000 User's Manual Addendum (order number M68000UMAD/AD)

MC68EZ328 User's Manual (order number MC68EZ328UM/D)

MC68EZ328 User's Manual Addendum (order number MC68EZ328UMA/D)

MC68VZ328 Product Brief (order number MC68VZ328P/D)

documents may be downloaded from the Web site, or a printed version may be obtained from a local sales office. The Web site also may have useful application notes. The manuals may be found at the Motorola Web site at http://www.Motorola.com/DragonBall. These

## Conventions

This user's manual uses the following conventions:

- OVERBAR is used to indicate a signal that is active when pulled low: for example, RESET
- Logic level one is a voltage that corresponds to Boolean true (1) state.
- Logic level zero is a voltage that corresponds to Boolean false (0) state
- To set a bit or bits means to establish logic level one.
- To clear a bit or bits means to establish logic level zero
- A signal is an electronic construct whose state conveys or changes in state convey information.

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- A pin is an external physical connection. The same pin can be used to connect a number of signals
- Asserted means that a discrete signal is in active logic state.
- Active low signals change from logic level one to logic level zero.
- Active high signals change from logic level zero to logic level one

Negated means that an asserted discrete signal changes logic state

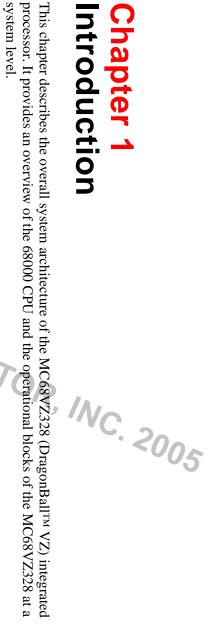
- Active low signals change from logic level zero to logic level one.
- Active high signals change from logic level one to logic level zero
- low and high bytes or words are spelled out. LSB means least significant bit or bits, and MSB means most significant bit or bits. References to
- Numbers preceded by a percent sign (%) are binary. Numbers preceded by a dollar sign (\$) or 0xARCHIV



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## Chapter 1 ntroduction



designers with more performance—the capability of running at higher speed while achieving lower power consumption using a true static core. Additionally, the new DragonBall VZ integrates the logic needed to monitors, games, smart toys, depth finders, navigation systems, and smart phones. the most popular PDA designs, and it can be used in a wide variety of other applications including exercise 68000 core that utilizes an advanced process technology. Thus, the DragonBall VZ can provide system support color LCD panels on-chip. The DragonBall VZ is the integrated processor of choice for some of The MC68VZ328 builds on the success of the earlier DragonBall processors and features a synthesizable

essential signals are brought out to the pins, allowing the MC68VZ328's primary packages (TQFP and MAPBGA) to occupy the smallest possible footprint on the circuit board Its functionality and glue logic are all optimally connected and timed with the same clock. Also, only the All these features combine to make the MC68VZ328 microprocessor attractive to many system designers

modules and typical system interface logic. The architecture of the MC68VZ328, shown in Figure 1-1 on implementation, the MC68VZ328 combines a powerful FLX68000 processor with intelligent peripheral page 1-2, consists of the following blocks: To improve total system throughput and reduce component count, board size, and the cost of system

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- **FLX68000 CPU**
- Chip-select logic and 8-/16-bit bus interface
- Clock generation module (CGM) and power control
- Interrupt controller
- 76 GPIO lines grouped into 10 ports
- Two pulse-width modulators (PWM 1 and PWM 2)
- Two general-purpose timers
- Two serial peripheral interfaces (SPI 1 and SPI 2)
- Two UARTs (UART 1 and UART 2) and infrared communication support
- LCD controller
- Real-time clock
- DRAM controller that supports EDO RAM, Fast Page Mode, and SDRAM
- In-circuit emulation module
- Bootstrap mode



Figure 1-1. MC68VZ328 Block Diagram

# eatures of the MC68VZ328

Static FLX68000 CPU-

- The features of the DragonBall VZ include the following: identical to the MC68EC000 microprocessor
- Full compatibility with MC68000 and MC68EC000
- 32-bit internal address bus
- Static design that allows processor clock to be stopped to provide power savings
- 5.4 MIPS performance at 33 MHz processor clock
- External M68000 bus interface with selectable bus sizing for 8-bit and 16-bit data ports
- array logic, reducing parts counts in design, with functions that include the following: System integration module (SIM) that incorporates many functions typically related to external
- System configuration and programmable address mapping
- Glueless interface to SRAM, DRAM, SDRAM, EPROM, and flash memory
- Eight programmable chip-selects with wait-state generation logic
- Four programmable interrupt I/Os, with keyboard interrupt capability



# Freescale Semiconductor, Incatures of the MC68VZ328

- Five general-purpose, programmable edge/level/polarity interrupt IRQs
- Other programmable I/O, multiplexed with peripheral functions of up to 76 GPIO lines
- Programmable interrupt vector response for on-chip peripheral modules
- Low-power mode control
- DRAM controller
- Support for  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycles and self-refresh mode DRAM
- Support for 8-bit and 16-bit port DRAM and synchronous DRAM
- EDO RAM or automatic Fast Page Mode for LCD access
- Programmable refresh rate
- Support for up to two banks of DRAM and EDO RAM
- 76 GPIO lines grouped into 10 ports
- Two UART ports
- Two serial peripheral interface (SPI) ports
- Two 16-bit general-purpose counters/timers

- Real-time clock/sampling timer

- Sampling timer with selectable frequency (4 Hz, 8 Hz, 16 Hz, 32 Hz, 64 Hz, 256 Hz, 512 Hz.

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- Interrupt generation for digitizer sampling or keyboard debouncing
- LCD controller
- Software-programmable screen size (up to  $640\times512$ ) to support single (nonsplit) monochrome and color STN panels
- Toshiba, and numerous other manufacturers Capability of directly driving popular LCD drivers and modules from Motorola, Sharp, Hitachi
- Support for up to 16 gray levels out of a palette of 16 density levels
- Utilization of system memory as display memory
- LCD contrast control using 8-bit PWM
- Two pulse-width modulator (PWM) modules
- Audio effects support
- 16- and 8-bit resolution
- 5-byte FIFO that provides more flexibility on performance
- Sound and melody generation



Built-in emulation function

CPU

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- Dedicated memory space for emulator debug monitor with chip-select
- Dedicated interrupt (interrupt level 7) for in-circuit emulation (ICE)
- single or multiple hardware execution One address-signal comparator and one control-signal comparator, with masking to support
- Breakpoint
- One breakpoint instruction insertion unit
- Bootstrap mode function
- Capability to initialize system and download programs and data to system memory through
- Acceptance of execution command to run program stored in system memory
- 8-byte-long instruction buffer for 68000 instruction storage and execution
- Power management
- Fully static HCMOS technology
- frequency control Programmable clock synthesizer using 32.768 kHz or 38.4 kHz external crystal for full
- Low-power stop capabilities
- Modules that can be individually shut down
- Operation from DC to 33 MHz (processor clock)
- Operating voltage of 2.7 V to 3.3 V
- Compact 144-lead thin quad flat pack (TQFP) and MAPBGA

architecture. The main features of the CPU are the following: The FLX68000 CPU in the MC68VZ328 is an updated implementation of the 68000 32-bit microprocessor

- Low-power, fully static HCMOS implementation
- 32-bit address bus and 16-bit data bus
- Sixteen 32-bit data and address registers
- 56 powerful instruction types that support high-level development languages
- 14 addressing modes and 5 main data types
- Seven priority levels for interrupt control

access to a broad base of established real-time kernels, operating systems, languages, applications, and The CPU is completely code compatible with other members of the M68000 families, which means it has



# .2.1 CPU Programming Mode

status register. The D7-D0 and A6-A0 registers can be used as index registers. address registers. These registers can be used for word and long-word operations, but they do not affect the registers (D7-D0) are data registers that are used for byte (8-bit), word (16-bit), and long-word (32-bit) seven registers (A6–A0) and the user stack pointer (USP) can function as software stack pointers and base operations. When being used to manipulate data, the data registers affect the status register (SR). The next The CPU has 32-bit registers and a 32-bit program counter, which are shown in Figure 1-2. The first eight

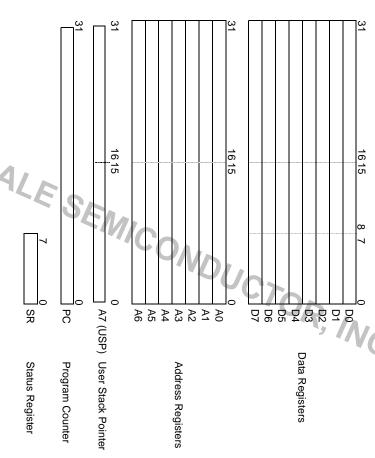


Figure 1-2. User Programming Model

In supervisor mode, the upper byte of the status register and the supervisor stack pointer (SSP) can also be programmed, as shown in Figure 1-

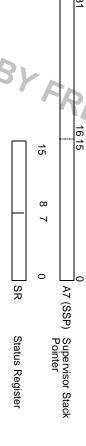


Figure 1-3. Supervisor Programming Model Supplement

is in trace mode, and the S bit indicates when it is in supervisor or user mode negative (N), zero (Z), overflow (V), and carry (C) condition code. The T bit indicates when the processor The status register contains the interrupt mask with seven available levels, as well as an extend (X),

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# 1.2.2 Data and Address Mode Types

shown in Table 1-1. binary-coded decimal (BCD) digits, bytes, words, and long words. The six types of address modes are The CPU supports five types of data and six main types of address modes. The five types of data are bits.

Table 1-1. Address Modes

Address Mode	Syntax
Register direct address	Vo
<ul><li>Data register direct</li><li>Address register direct</li></ul>	An An
Absolute data address	
Absolute short	xxx.W
Absolute long	xxx.L
Program counter relative address	- j
Relative with offset	d <sub>16</sub> (PC)
Relative with index offset	d <sub>8</sub> (PC, Xn)
Register indirect address	
Register indirect	(An)
Postincrement register indirect	(An)+
Register indirect with offset	H(An)
<ul> <li>Indexed register indirect with offset</li> </ul>	d <sub>8</sub> (An, Xn)
Immediate data address	
Immediate     Ouick immediate	#XXX #1_#8
E	
<ul><li>Implied address</li><li>Implied register</li></ul>	SR/USP/SP/PC
Note:	
Dn = Data register	
An = Address register Xn = Address or data register used as index register	
SR = Status register	
PC = Program counter	
SP = Stack pointer	
( ) = Effective address	
d <sub>8</sub> = 8-bit offset (displacement)	
d <sub>16</sub> = 16-bit offset (displacement)	
#xxx = Immediate data	

# 1.2.3 FLX68000 Instruction Set

every instruction operates on bytes, words, and long words, and most of them can use any of the 14 address divide, quick arithmetic operations, binary-coded decimal (BCD) arithmetic, and expanded operations instructions. These instructions, shown in Table 1-2 on page 1-7, include signed and unsigned multiply and modes. Combining instruction types, data types, and address modes provides access to over 1,000 possible The FLX68000 CPU instruction set supports high-level languages that facilitate programming. Almost (through traps).



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Set conditional	Scc	Exclusive OR	EOR
Subtract decimal with extend	SBCD	Unsigned divide	DIVU
Return from subroutine	RTS	Signed divide	DIVS
Return and restore	RTR	Test conditionally, decrement, and branch	DBcc
Return from exception	RTE	Compare immediate	CMPI
Rotate right with extend	ROXR	Compare memory	CMPM
Rotate left with extend	ROXL	Compare address	CMPA
Rotate right without extend	ROR	Compare	CMP
Rotate left without extend	ROL	Clear operand	CLR
Reset external devices	RESET	Check register against bounds	CHK
Push effective address	PEA	Bit test	BTST
OR immediate to status register	ORI to SR	Branch to subroutine	BSR
OR immediate to condition codes	ORI to CCR	Bit test and set	BSET
OR immediate	ORI	Branch always	BRA
Logical OR	OR	Bit test and clear	BCLR
One's-complement	NOT	Bit test and change	BCHG
No operation	NOP	Branch conditionally	Всс
Negate with extend	NEGX	Arithmetic shift right	ASR
Negate	NEG	Arithmetic shift left	ASL
Negate decimal with extend	NBCD	AND immediate to status register	ANDI to SR
Unsigned multiply	MULU	AND immediate to condition codes	ANDI to CCR
Signed multiply	MULS	AND immediate	ANDI
Move user stack pointer	MOVE USP	Logical AND	AND
Move to condition codes	MOVE to CCR	Add with extend	ADDX
Move to status register	MOVE to SR	Add immediate	ADDI
Move from status register	MOVE from SR	Add quick	ADDQ
Move quick	MOVEQ	Add address	ADDA
Move peripheral data	MOVEP	Add	ADD
Move multiple registers	MOVEM	Add decimal with extend	ABCD
Description	Mnemonic	Description	Mnemonic

### Modules of the MC68VZ32Freescale Semiconductor, Inc.

Table 1-2. Instruction Set (Continued)

Mnemonic	Description	Mnemonic	Description
EORI	Exclusive OR immediate	STOP	Stop
EORI to CCR	Exclusive OR immediate to condition codes	SUB	Subtract
EORI to SR	Exclusive OR immediate to status register	SUBA	Subtract address
EXG	Exchange registers	SUBI	Subtract immediate
EXT	Sign extend	SUBQ	Subtract quick
JMP	dwnr	SUBX <b>?</b>	Subtract with extend
JSR	Jump to subroutine	SWAP	Swap data register halves
LEA	Load effective address	TAS	Test and set operand
LINK	Link stack	TRAP	Trap
LSL	Logical shift left	TRAPV	Trap on overflow
LSR	Logical shift right	TST	Test
MOVE	Move	UNLK	Unlink
MOVEA	Move address		

## .3 Modules of the MC68VZ328

how they operate. interface and control modules. The following subsections provide brief descriptions of these modules and In addition to the powerful 68000 processor, the DragonBall VZ contains a wide variety of peripheral

### .3.1 Memory Controller

one or two banks of DRAM may be used, and each bank can be a maximum of 32 Mbyte. For a more complete explanation of how memory is configured and controlled, see Chapter 3, "Memory Map." ROM, SRAM, different DRAM types (EDO RAM and Fast Page Mode), and synchronous DRAM. Either The memory controller provides a glueless interface to most memory chips on the market. It supports flash,

# Clock Generation Module and Power Control Module

optimize power consumption. The power control module offers three power-saving modes: normal, doze, shut down the system clock divider chain for maximum power saving, while the real-time clock (RTC) and frequency can be adjusted by writing to the CGM frequency select register. The CGM can be disabled to oscillator to provide a stable clock source for the internal clock generation module (CGM). The output The module containing the clock synthesizer operates with either an external crystal or an external DRAM controller remain active. The power control module can be configured to control the CPU cycles to



# Freescale Semiconductor, Incodules of the MC68VZ328

and sleep. When in sleep mode, the CGM wakes up automatically when any unmasked external or internal interrupt occurs. See Chapter 4, "Clock Generation Module and Power Control Module," for more detailed information.

### 1.3.3 System Control

current of the GPIO lines. See Chapter 5, "System Control," for more information. modules in the DragonBall VZ. These registers grant permission for access to many of the internal the bus time-out control and status (bus error generator). System control also is used to program the drive peripheral registers. In addition, the module controls address space of the internal peripheral registers and The primary function of the system control module is to provide configuration control of several other

### 1.3.4 Chip-Select Logic

detailed information about using the chip-select logic, see Chapter 6, "Chip-Select Logic." option, internal and external DTACK generation, and 8-bit and 16-bit data port size selection. For more of a wide variety of memory or external peripherals. Each chip-select signal provides a write-protect The MC68VZ328 provides eight programmable general-purpose chip-select signals to allow the selection

### 1.3.5 DRAM Controller

to controlling DRAM, the DRAM controller supports access for LCD controller burst accesses. See The DRAM controller provides a glueless interface for either 8-bit or 16-bit DRAM. It supports EDO RAM, Fast Page Mode, and synchronous DRAM. The DRAM controller provides row address strobe Chapter 7, "DRAM Controller," for more information about this module.  $(\overline{RAS})$  and column address strobe  $(\overline{CAS})$  signals for up to a maximum of two banks of DRAM. In addition

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### 1.3.6 LCD Controller

this reason, an understanding of the DRAM controller is recommended. For more information, please refer controller fetches display data directly from system memory through periodic DMA transfer cycles. For to Chapter 7, "DRAM Controller," as well as Chapter 8, "LCD Controller." The LCD controller provides display data for external LCD drivers or for an LCD panel. The LCD

## 1.3.7 Interrupt Controller

vector generation, and unique vector number generation for each interrupt level. For additional information about this module, see Chapter 9, "Interrupt Controller." interrupt controller features prioritized interrupts, a fully nested interrupt environment, programmable routine of a lower-priority interrupt may be suspended by a higher-priority interrupt request. The on-chip during the CPU interrupt-acknowledge cycle. Interrupt nesting is also provided so that an interrupt service The interrupt controller prioritizes internal and external interrupt requests and generates a vector number



# Modules of the MC68VZ32Freescale Semiconductor, Inc.

# General-Purpose I/O (GPIO) Lines

independently programmed as a GPIO pin even when other pins related to that on-chip peripheral are used as dedicated pins. For detailed information about programming these GPIO lines, see Chapter 10, "I/O These ports can be configured as GPIO pins or dedicated peripheral interface pins. Each pin can be The MC68VZ328 supports a maximum of 76 GPIO lines grouped together in ports A-G, J, K, and M

### **Real-Time Clock**

software watchdog logic resets or interrupts the CPU. For detailed information about configuring and does reach its time-out value, the watchdog timer assumes that a system failure has occurred and the of escape from unexpected input conditions, external events, or programming errors. Once started, this it is in sleep or doze mode. The watchdog clock timer protects against system failures by providing a way A real-time clock provides the time of day with 1-second resolution. Using an external crystal (either 32.768 kHz or 38.4 kHz) as a clock source, it keeps time as long as power is applied to the chip, even when programming this module, refer to Chapter 11, "Real-Time Clock." timer must be cleared by software on a regular basis so that it never reaches its time-out value. When it

## **General-Purpose Timer**

derived from the system clock. The two timers can also be cascaded together as one 32-bit timer. This module is described in detail in Chapter 12, "General-Purpose Timers." external events. Each timer has an 8-bit prescaler to allow a programmable clock input frequency to be an external event, to trigger an external event or interrupt when the timer reaches a set value, or to count The MC68VZ328 has two 16-bit timers that can be used in various modes to capture the timer value with

# .3.11 Serial Peripheral Interfaces (SPI)

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and 2," provides detailed information about the configuration and operation of the SPIs other SPI (SPI 1) may be configured as either master or slave. Chapter 13, "Serial Peripheral Interface 1 only operates in master mode, which initiates SPI transfers from the MC68VZ328 to the peripheral. The with the SPI clock, and it is transmitted and received with the same SPI clock. One SPI module (SPI 2) peripheral interfaces are mainly used for controlling external peripherals. The passed data is synchronized The MC68VZ328 contains two serial peripheral interface (SPI) modules, SPI 1 and SPI 2. The serial

## 1.3.12 Universal Asynchronous Receiver/Transmitter (UART) Modules

The two UART ports in the MC68VZ328 may be used to communicate with external serial devices. UART 1 is identical to the UART in the DragonBall EZ processor, while UART 2 represents an enhanced input frequency, which is 33.16 MHz, doubling the 16.58 MHz frequency of the MC68EZ328. For a information about the programming and configuration of these two modules, see Chapter 14, "Universal unless the divider and prescaler are adjusted to compensate for the increased clock speed. For more 33.16 MHz system clock, software written for the MC68EZ328 version of the chip is not compatible TxFIFO to reduce the number of software interrupts. An improvement to both UARTs is the system clock version of UART 1. One of the enhancements to the UART 2 design consists of an enlarged RxFIFO and Asynchronous Receiver/Transmitter 1 and 2."



# 1.3.13 Pulse-Width Modulators (PWM)

Freescale Semiconductor, Infodules of the MC68VZ328

quality. Users can enable both PWMs at the same time to generate a mixed PWMO signal. See Chapter 15 reducing the number of interrupts to the CPU. The 16-bit PWM provides higher resolution for better sound into analog waveforms. The 8-bit PWM contains a 5-byte FIFO that enhances the system performance by these devices. "Pulse-Width Modulator 1 and 2," for more detailed information about the configuration and operation of PWM can be used to play back high-quality digital sounds, produce simple tones, or convert digital data modes of operation—playback, tone, and digital-to-analog (D/A) conversion. Using these three modes, the The MC68VZ328 has two pulse-width modulators (PWMs). Each of the pulse-width modulators has three

## 1.3.14 In-Circuit Emulation Module

The in-circuit emulation module is designed for low-cost emulator development purposes. System memory space, which is 0xFFFC0000 to 0xFFFCFFFF, is covered by the EMUCS signal and primarily dedicated to system I/O port. Keep in mind that if the monitor ROM is selected, the system must boot up in emulator the emulator debug monitor. However, the EMUCS signal can be used to select the monitor ROM or mode. Refer to Chapter 16, "In-Circuit Emulation," for more details.

### **Bootstrap Mode**

stored in flash memory. Simple hardware debug functions may be performed on the target system using the bootstrap utility program BBUGV.EXE, which is available on the following World Wide Web site: programming the UART controllers. Once a program is downloaded to the MC68VZ328, it can be http://www.Motorola.com/DragonBall. See Chapter 17, "Bootstrap Mode," for more information about executed, providing a simple debugging environment for failure analysis and a channel to update programs Chapter 14, "Universal Asynchronous Receiver/Transmitter 1 and 2," for information on operating and programs or data to the target system RAM using either the UART 1 or UART 2 controller. See The bootstrap mode is designed to allow the initialization of a target system and the ability to download ARCHIVED BY FREESC/

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## Signal

groups, as illustrated in Figure 2-1 on page 2-2. The MC68VZ328 uses a standard M68000 bus to chip. CPU read cycles to internal memory-mapped registers of the device are invisible on the external bus communicate with on-chip and external peripherals. This single continuous bus exists both on and off the This chapter describes the MC68VZ328's input and output signals, which are organized into functional but write cycles to internal or external memory-mapped locations are visible <sup>INC.</sup> 2005





### PF[6:3]/A[23:20] PG2/EMUIRQ PG3/HIZ/P/D PG4/EMUCS PG5/EMUBRK PA[7:0]/D[7:0] < PF2/CLKO PD0/INT0 PD5/IRQ2 PD4/<u>IRQ</u> PF1/IRΩ5 PD3/INT3 PK[2:1]/UDS/LDS/RW PG0/BUSW/DTACK PG1/A0 LWE/LB UWE/UB MA[15:0/A[16:1] A[19:17] D[15:8] RESET EXTAL XTAL Port G Port D Port F Port A Figure 2-1. Synthesizer & System Integration Module FLX68000 Static CPU Bootstrap Real-Time Clock Interrupt Controller Emulation Processor Interface 8/16-Bit 68000 Bus Control Power Control Clock **Signals Grouped by Function** 68000 Internal Bus UART with IRDA1.0 M/S SPI with FIFO Chip-Select Memory Controller Voltage Regulator Controller 8/16-Bit PWM Master SPI 16-Bit Timer UART Timer 16-Bit VSS LVDD Ports J & K Ports C, F, & K Port B Port E PB0/CSB0 PB1/CSB1/SDWE PB2/CSC0/RAS0 PB3/CSC1/RAS1 PB4/CSD0/CAS0 PB5/CSD1/CAS1 PC6/LCLK PC7/LACD PF0/LCONTRAST PJ4/RXD2 PJ5/TXD2 PJ6/<u>RTS2</u> PJ7/<u>CTS</u>2 PJ2/<u>SP</u>ICLK1 PJ3/SS PE2/SPICLK2 PE3/DWE/UCLK PJ0/MISO PJ1/MOSI CSA<u>0</u> PF7/CSA1 PM0/SDCLK PM1/SDCE PM2/DQMH PM3/DQML PM4/SDA10 PK0/DATA\_READY/PWMO2 PE0/SPITXD PB7/PWM01 PE4/RXD1 PE1/SPIRXD PK[7:4]/LD[7:4] PB6/TOUT/TIN PM5/DM0E PC4/LFLM PC[3:0]/LD[3:0]

Table 2-1 on page 2-3 groups the MC68VZ328 signals according to their function

# Semiconductor, speas Grouped by Function

ble 2-1. Signal Function Groups

Finction Group	Signals	Number of Pins	of Pins
- dioxidi	Cigirais	TQFP	PBGA
Power	V <sub>DD</sub>	9	Ŋ
Ground	Vss	16	28
Regulator output	LV <sub>DD</sub>	Ŋ	_
Clocks/PCIO	XTAL, EXTAL, CLKO/PF2	З	ω
System control	RESET	_	_
Address bus/PFIO	PF[3:6]/A[23:20], A[19:14], A0/PG1, MA[15:0]/A[16:1]	24	24
Lower data bus/PAIO	PA[7:0]/D[7:0]	&	8
Upper data bus	D[15:8]	8	8
Bus control/PCIO/PEIO/ PKIO	BUS <u>W/DTACK/</u> PG0, <u>OE, LWE/LB, UWE/UB,</u> PE3/DWE/UCLK, PK2/LDS, PK3/UDS, PK1/RW	8	8
Interrupt controller/PMIO	NT0/PD0, NT1/PD1, NT2/PD2, NT3/PD3, RQ1/PD4, RQ2/PD5, RQ3/PD6, RQ6/PD7, RQ5/PF1	9	9
LCD controller/PCIO	LACD/PC7, LCLK/PC6, LLP/PC5, LFLM/PC4, LD[7:4]/PK[7:4], LD[3:0]/PC[3:0], LCON- TRAST/PF0	13	13
UART1/PEIO, UART2/PJIO	PE4/RXD1, PE5/TXD1, PE6 <u>/RTS1,</u> PE7 <u>/CTS1,</u> PJ4/RXD2, PJ5/TXD2, PJ6/RTS2, PJ7/CTS2	8	8
Timer/PBIO	TOUT/TIN/PB6	_	_
Pulse-width modulator/PBIO	PWMO1/PB7 (PM5/DATA_READY/PWMO2)	1	1
Master SPI/PEIO, config- urable SPI/PJIO/PKIO	SPITXD/PE0, SPIRXD/PE1, SPICLK2/PE2, PJ0/MOSI, PJ1/MISO, PJ2/SPICLK1, PJ3/SS, PK0/DATA_READY/PWMO2	8	8
Chip-select, EDO RAM/PBIO, PMIO	CSA[1:0]/PF7, CSB[1:0]/PB[1:0]/SDWE, CSC[1:0]/PB[3:2]/RAS[1:0], CSD[1:0]/PB[5:4]/CAS[1:0], PM5/DMOE	9	9
SDRAM/PMIO	PM0/SDCLK, PM1/SDCE, PM2/DQMH, PM3/DQML, PM4/SDA10, (SDWE, SDCAS[1:0], SDRAS[1:0])—multiplexed with chip-select signals	S	5
Emulator pins	EMUIRQ/PG2, EMUBRK/PG5, HIZ/P/D/PG3, EMUCS/PG4	4	4
No connect pins	NC	4	0

# Clock and System Control Stansscale Semiconductor, Inc.

## 2.2 Power and Ground Signals

The MC68VZ328 microprocessor has three types of power pins. They are  $V_{DD}$ ,  $V_{SS}$ , and  $LV_{DD}$ .

- recommended to place a 0.1 µF bypass capacitor close to each of these pins. V<sub>DD</sub>—External power supply to drive all I/O pins and for the internal voltage regulator. It is
- V<sub>SS</sub>—Signal return pin for both digital and analog circuits.
- single LV<sub>DD</sub> pin (M1) requiring only a 270 nF and a 0.0001 µF bypass capacitor. pins, except pin 35, which requires a 270 nF and a 0.0001 uF bypass capacitor. The PBGA has a by pass capacitor circuit of  $0.01 \,\mu\text{F}$  and  $0.0001 \,\mu\text{F}$  (in parallel) be placed close to each of the LV<sub>DD</sub> package has unique bypass capacitor requirements. The TQFP package requires that an external should not be used as an external circuit power supply due to current supply limitations. Each  $LV_{DD}$ —Internal voltage regulator output signal that is used by the internal circuitry. The  $LV_{DD}$  pins

### NOTE:

placed as close to the pins as possible. For maximum noise immunity, ensure that external bypass capacitors are

# Clock and System Control Signals

There are four clock and system control signals.

design values, see Figure 4-2 on page 4-4 Figure 2-2 illustrates how a crystal is usually connected to the MC68VZ328. For specific circuit For a 32.768 kHz input, the internal phase-locked loop generates a PLLCLK signal that passes through two prescalers, and the resulting output (DMACLK and SYSCLK) clock is 16.58 MHz. The MC68VZ328 microprocessor supports both a 32.768 kHz and a 38.4 kHz crystal frequency. -External Clock/Crystal. This input signal connects to the external low frequency crystal

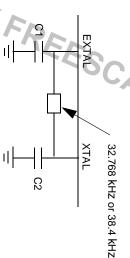


Figure 2-2. Typical Crystal Connection

- -Crystal. This output signal connects the on-chip oscillator output to an external crystal.
- detailed information, refer to Section 10.4.7.3, "Port F Dedicated I/O Functions," on page 10-26. page 4-8 for more information. The CLKO/PF2 signal defaults to the Port F pin 2 input signal. For power consumption and electromagnetic emission. See Section 4.4.1, "PLL Control Register," on provided for external reference. The output can be disabled in the PLL control register to reduce oscillator and is internally connected to the clock output of the internal CGM. This signal is CLKO/PF2--Clock Out or bit 2 of Port F. This output clock signal is derived from the on-chip clock
- 0.8 V low. After the MC68VZ328 powers up, this reset input signal should be driven low for at least processor (CPU and peripherals). The threshold of this Schmitt trigger device is 1.2 V high and RESET--Reset. This active low, Schmitt trigger input signal resets the entire MC68VZ328



## Freescale Semiconductor, Inc.

**Data Bus Signals** 

This signal is inactive while the CPU is executing the RESET instruction. See Section 4.3.1, "CLK32 Clock Signal," on page 4-4 for details about selecting circuit values. 1.2 s before its voltage is higher than 1.2 V to ensure that the crystal oscillator starts and stabilizes

### NOTE:

MC68VZ328, When an R/C circuit is being used to generate the RESET signal to the the R/C circuit must be placed as close to the chip as

## Address Bus Signals

The address bus pins A[23:0] are the address lines driven by the CPU or LCD controller for panel refresh DMA. In sleep mode, all address signals are in an active state of the last bus cycle. Refer to Section 4.5.1.4, "Sleep Mode," on page 4-12 for more detailed information.

- A0/PG1—Address 0 or Port G bit 1. After system reset, this signal defaults to A0
- on DRAM access cycles. lines are multiplexed with the DRAM row and column address signals. The MA signal is selected MA[15:0]/A[16:1]—Multiplexed DRAM bits 15-0 or Address bits 16-1. These address output
- -Address lines 19–17.
- Port F. These signals default to address functions after reset. A[23:20]/PF[6:3]—Address bits 23–20 or Port F bits 6–3. These address lines are multiplexed with

## Data Bus Signals

Section 4.5.1.4, "Sleep Mode," on page 4-12 for more detailed information. lower byte of the data bus (in an 8-bit-only system) to operate as general-purpose I/O signals. In sleep mode, all of the data bus pins (D15–D0) are individually pulled up with 1-megaohm resistors. Refer to The flexible data bus interface design of the MC68VZ328 microprocessor allows programming of the

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- peripherals should be connected to this bus. In pure 8-bit systems, this is the data bus. In mixed 8- and 16-bit systems, 8-bit memory blocks or D[15:8]—Data bits 15–8. The upper byte of the data bus is not multiplexed with any other signal.
- register (0xFFF000) should be set to 1 by software before the port can be used. See Section 5.2.1, I/O. In pure 8-bit systems, this bus can serve as a general-purpose I/O. The WDTH8 bit in the SCR D[7:0]/PA[7:0]—Data bits 7–0 or Port A bits 7–0. This bus is the lower data byte or general-purpose "System Control Register," on page 5-2 for details on setting this bit. In 16-bit or mixed 8-16-bit systems, these pins must function as the lower data byte. ARCHIVE



# Interrupt Controller Signal Freescale Semiconductor, Inc.

### Bus **Control Signals**

following descriptions provide detailed information about programming the signals and their use. The bus control signals are used for both the configuration and operation of the MC68VZ328 bus. The

- of the 16-bit memory chip pins are UB and LB. These two data strobe signals are normally used to connect to UDS and LDS two pins are LWE and UWE and function as previously described. If the SR16 bit is set, these two DWE should be used. For CSB[1:0] cycles, if the SR16 bit is clear in the CSCTRL1 register, these be used as a DRAM write-enable if DRAM refresh does not require that UWE stay high. Otherwise set to 8-bit port (the BSW bit is clear), use only the UWE signal for write-enable control. UWE can UWE. They are used as lower and upper write-enable signals to a 16-bit port. If the chip-select is Upper Byte data strobes. For all chip-select cycles except  $\overline{\text{CSB}}[1:0]$ , these two pins are  $\overline{\text{LWE}}$  and LWE/LB, UWE/UB—Lower Byte Write-Enable and Upper Byte Write-Enable, or Lower Byte and
- Interface Signals," on page 14-3. This pin defaults to GPIO input pulled high. to the UART module. For a description of the UCLK signal, refer to Section 14.2.3, "Serial bit of the DRAMC register, which is described in Section 7.3.2, "DRAM Control Register," on UWE. This signal stays high during refresh cycles. This pin defaults to a PE3 input signal. To select the DWE function, program Port E to DWE and enable the DWE signal by writing a 1 to the DWE DRAM, which requires an independent write-enable signal rather than one that is shared with page 7-14. If this bit is not enabled, the UCLK signal function is selected, which is an input clock  $\overline{\mathrm{DWE}}/\mathrm{UCLK/PE3}$ —DRAM Write-Enable, UART Clock, or Port E bit 3. Use the  $\overline{\mathrm{DWE}}$  signal with
- pulled up, externally. system reset. For a 16-bit CSA0-selected memory device, it is recommended that this signal be cycles of internal DTACK will gnore the input status. This pin can be configured to GPIO after If it is input, only those chip-select cycles using external DTACK will be affected. Chip-select on reset means that CSA0 connects to a T6-bit memory device. After reset, this pin defaults to the of BUSW on reset means that CSA0 connects to an 8-bit memory device, and a logic high of BUSW RESET signal. Its mode will determine the default bus width for CSAO. For example, a logic low signal. The MC68VZ328 microprocessor will latch the BUSW signal at the rising edge of the default bus width for the CSAO signal. The DTACK signal is the external input data acknowledge BUSW/DTACK/PG0—Bus Width, Data Transfer Acknowledge, or Port G bit 0. BUSW is the  $\overline{\mathrm{DTACK}}$  input signal.  $\overline{\mathrm{DTACK}}$  can be configured as output by programming the Port G DIR register

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- OE—Output Enable. This active low signal is asserted during a read cycle of the MC68VZ328 microprocessor, which enables the output of either ROM or SRAM.
- UDS/PK3, LDS/PK2—Data strobes or GPIO. UDS and LDS are 68000 CPU data strobe signals These pins default to GPIO input pulled high.
- $\overline{\text{RW}}/\text{PK1}$ —Read/Write or Port K bit 1.  $\overline{\text{RW}}$  is the 68000 CPU read/write signal. This pin defaults to GPIO input pulled high

## Interrupt Controller Signals

This section describes signals that are used by the MC68VZ328 interrupt controller.

described in Chapter 9, "Interrupt Controller." These pins default to GPIO input pulled high support keyboard applications, the I/O function can be used with interrupt capabilities, which are INT[3:0], IRQ[3:1], IRQ6/PD[7:0]—Interrupt bits 3-0, Interrupt Request bits 3-1, or Port D bits  $-0.\overline{\text{INT}}[3:0], \overline{\text{IRQ}}[3:1],$  and  $\overline{\text{IRQ}6}$  can be configured as edge or level trigger interrupt signals. To



2-6

# Freescale Semiconductor, Inc. LCD Controller Signals

- or level low trigger interrupt. This pin defaults to GPIO input pulled high. interrupt input. When configured as an interrupt input, the signal may be programmed as a level high IRQ5/PF1—Interrupt Request 5 or Port F bit 1. This signal can be programmed as GPIO or as an
- from EMUIRO, which is an active low, edge-sensitive interrupt. To clear this interrupt, read the EMIQ—Emulator Interrupt Status. This bit indicates that the in-circuit emulation module or ICEMSR. See Section 9.6.4, "Interrupt Status Register," on page 9-12 for more information ICEMSR register to identify the interrupt source and write a 1 to the corresponding bit in the EMUIRQ pin is requesting a level 7 interrupt. This bit can be generated from three interrupt two breakpoint interrupts from the in-circuit emulation module and an external interrupt

## **Controller Signals**

The MC68VZ328 contains all necessary circuitry to support an external LCD display panel. This section describes the signals used by the LCD controller. It also provides some programming information about the use of these signals.

Panel interfaces of 1, 2, 4, or 8 bits are supported LD[3:0]/PC[3:0], LD[7:4]/PK[7:4]—LCD Data Bus bits 7–0, or Port C bits 3–0 and Port K bits The pixel data is arranged to accommodate the programmable panel mode data width selection. -4. LD signals output bus transfers of pixel data to the LCD panel to which it will be displayed

### NOTE:

type, connect the MC68VZ328's LD0 signal to the LCD panel's data bit 3, connection between the MC68VZ328's LCD data bus and the LCD panel's pixel 0,0. Some LCD panel manufacturers program their LCD panel data K pulled high. These signals default as GPIO input with Port C being pulled low and Port data 0. The four pins can also be programmed as I/O ports from Port C and then connect LD1 to LCD data 2, LD2 to LCD data 1, and LD3 to LCD data bus may have a reversed bit significance. For a 4-bit LCD panel of this bus so that the MSB of the panel displays pixel 0,0. For these panels, the The MC68VZ328's LCD interface data bus uses the LSB (LD0) to display

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- This pin defaults to GPIO input pulled low. programmed to be an active high or an active low signal. It can also be programmed as an I/O port frame. LFLM becomes active after the first line pulse of the frame and remains active until the next line pulse, at which point it deasserts and remains inactive until the next frame. LFLM can be LFLM/PC4 -First Line Marker or Port C bit 4. This signal indicates the start of a new display
- software. See Section 8.3.10, "LCD Polarity Configuration Register," on page 8-16 for more onto an LCD panel. The LLP can be programmed to be an active high or active low signal in LLP/PC5 LCD Line Pulse or Port C bit 5. The LLP signal is used to latch a line of shifted data
- the LCD panel is synchronized. LCLK can be programmed to be either an active high or an active LCLK/PC6—LCD Shift Clock or Port C bit 6. This is the clock output to which the output data to low signal. This pin can also be programmed as an I/O port. This pin defaults to GPIO input pulled
- the crystal polarization on the panel. This signal can be programmed to toggle at a period of 1 to LACD/PC7—LCD Alternate Crystal Direction or Port C bit 7. This output is toggled to alternate input pulled low 128 frames or lines. This pin also can also be programmed as an I/O port. This pin defaults to GPIO



pin can also be programmed as an I/O port. This pin defaults to GPIO input pulled high. modulator (PWM) inside the LCD controller to adjust the supply voltage to the LCD panel. This LCONTRAST/PF0—LCD Contrast and Port F bit 0. This output is generated by the pulse-width

# **UART 1 and UART 2 Controller Signals**

section describes the signals that are used to interface with external serial devices. There are two Universal Asynchronous Receive Transmit (UART) modules in the MC68VZ328. This

- receiver to convert voltage levels. These pins default to GPIO input pulled high. used to convert the IrDA signal to an electrical signal. RS-232 applications need an external RS-232 narrow pulse of 1.6 µs minimum is expected for each zero bit received. External circuitry must be is the receiver serial input. During normal operation, NRZ data is expected, but in IrDA mode, a RXD1/PE4, RXD2/PJ4--UART 1 and UART 2 Receive Data or Port E bit 4 and Port J bit 4. RXD
- default to GPIO input pulled high. RS-232 transmitter. For IrDA applications, this pin can directly drive an IrDA LED. These pins period for each zero bit transmitted. For RS-232 applications, this pin must be connected to an mode, they output a selectable pulse width of three-sixteenths bit period or 1.6 µs minimum bit is the transmitter serial output. During normal operation, they output NRZ data signals. In IrDA TXD1/PE5, TXD2/PJ5—UART 1 and UART 2 Transmit Data or Port E bit 5 and Port J bit 5. TXD
- These pins default to GPIO input pulled high. the far-end transmitter's CTS pin. When the receiver detects a pending overrun, it negates this pin indicates that it is ready to receive data by asserting this pin (low). This pin would be connected to RTS1/PE6, RTS2/PJ6-–UART 1 and UART 2 Request to Send or Port E bit 6 and Port J bit 6.  $\overline{\text{RTS}}$
- character whenever a character is ready to transmit. These pins default to GPIO input pulled high character is transmitted. If the NOCTSx bit is set in the UTX register, the transmitter sends a controls the transmitter. Normally, the transmitter waits until this signal is active (low) before a CTS1/PE7, CTS2/PJ7--UART 1 and UART 2 Clear to Send or Port E bit 7 and Port J bit 7. CTS

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently

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### Timer Signals

describes the signals and how they are programmed There are several external timer and clock signal functions available using the MC68VZ328. This section

- defaults to GPIO input pulled high. toggle or generate a pulse of 1-system-clock duration when the timer/counter reaches a reference value. TIN is used as the external clock source of Timer 1 or used as a capture function. This pin TOUT/TIN/PB6 -Timer 1 Output, Timer 1 Input, or Port B bit 6. TOUT can be programmed to
- defaults to GPIO input pulled high peripheral control register selects the clock output signal from UART 1 or UART 2 controlled by the UCLKDIR bit of UART 1 and UART 2. For UCLK output, the UCLK bit of UCLK/DWE/PE3—UART Clock input/output, DRAM Write-Enable, or Port E bit 3. The UCLK function is selected when  $\overline{\text{DWE}}$  is disabled and PESEL3 is written 0. The direction of UCLK is



# **Pulse-Width Modulator Signals**

signals available to communicate with these PWM modules. There are two pulse-width modulator (PWM) modules in the MC68VZ328. This section describes the

Freescale Semiconductors Interface 2 Signals

- GPIO input pulled high. the logical operation (AND or OR) of both the PWM 1 and PWM 2 modules. This pin defaults to PWMO1/PB7--Pulse-Width Modulator Output 1 or Port B bit 7. PWMO1 is an output signal from
- (DATA\_READY) is selected. This pin defaults to GPIO input pulled high. function and PKDIR0 is 1, the PWMO2 signal is selected. If PKDIR0 is 0, SPI Data Ready PWMO2 is an output signal from the PWM 2 module. If this pin is configured for dedicated PWMO2/DATA\_READY/PK0—Pulse-Width Modulator Output 2, SPI Data Ready, or Port K bit 0

### Serial Peripheral Interface 1 Signals

signals that are used with SPI 1 to interface with external devices. There are two serial peripheral interface (SPI) modules in the MC68VZ328. This section describes the

- SPI shift register. This pin defaults to GPIO input pulled high. MOSI/PJ0—SPI Transmit Data or Port J bit 0. MOSI is the master output/slave input signal for the
- SPI shift register. This pin defaults to GPIO input pulled high. MISO/PJ1--SPI Receive Data or Port J bit 1. MISO is the master input/slave output signal for the
- idle. In polarity = 1 mode, this signal is high during idle. This pin defaults to GPIO input pulled signal for SPI. In polarity = 0 mode, this signal is low while the serial peripheral interface master is SPICLK1/PJ2—SPI Clock or Port J bit 2. SPICLK1 is the master clock output/slave clock input
- SS/PJ3 pin defaults to GPIO input pulled high. -SPI Slave Select or Port J bit  $3.\overline{\text{SS}}$  is the master output/slave input chip-select signal. This

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PKDIR0 and PKSEL0 bits are written 0. This pin defaults to GPIO input pulled high master mode to signal the SPI master to clock out data. To select the DATA\_READY function, the \_READY/PWMO2/PK0—SPI Data Ready or Port K bit 0. DATA\_READY can be used

## Serial Peripheral Interface Signals

This section describes the signals that are used with SPI 2, the second serial peripheral interface (SPI) module in the MC68VZ328, to interface with external devices.

- output signal. This pin defaults to GPIO input pulled high. SPITXD/PE0--SPI Master Transmit Data or Port E bit 0. SPITXD is the master SPI shift register
- register. This pin defaults to GPIO input pulled high. SPIRXD/PE1—SPI Master Receive Data or Port E bit 1. SPIRXD is the input to the master SPI shift
- defaults to GPIO input pulled high peripheral interface master is idle. In polarity = 1 mode, this signal is high during idle. This pin peripheral interface master is enabled. In polarity = 0 mode, this signal is low while the serial SPICLK2/PE2—SPI Master Clock or Port E bit 2. SPICLK2 is the clock output when the serial



# SDRAM Interface Signals Freescale Semiconductor, Inc.

### Chip-Select and **EDO RAM Interface** Signals

SDRAM, and EDO RAM. section and Section 2.15, "SDRAM Interface Signals," describe the signals used to interface with RAM Chip-select logic is used to provide maximum compatibility with a wide variety of memory logic. This

- of the BUSW signal. space (0xFFFC0000–0xFFFFFFFFF). It can be reprogrammed during the boot sequence to another address range or different wait states. The default data bus width for CSAO is determined by the state and decodes all address ranges, except internal register address space, emulator space, and bootstrap Chip-Select A bit 0. CSAO is a default chip-select signal after reset. It is set to 6 wait states
- and RAS signals. These pins default to GPIO input pulled high. general-purpose I/O. In addition, CSC[1:0] and CSD[1:0] are designed to support DRAM as CAS individually programmable. Pins that are not needed as chip-selects can be programmed as signals. These pins comprise the remainder of the Group A, B, C, and D chip-selects and are CSA1/PF7, CSB[1:0]/PB[1:0], CSC[1:0]/PB[3:2]/RAS[1:0], CSD[1:0]/PB[5:4]/CAS[1:0]-Chip-Select A, B, C, and D bits 0 and 1, Port F bit 7, Port B bits 5–0, or row and column select
- access. This pin defaults to GPIO input pulled high. continuous page mode is enabled. Using this mode will minimize the number of clocks per DRAM contention. Therefore, a dedicated output enable, DMOE, is required, connecting to DRAM if and if OE is used to enable the DRAM data output, DRAM will drive data, producing bus memory read cycles. In continuous page mode, RAS is held low until a page-miss, refresh required, or RAS duration time out. During an RAS low period there may be other memory access cycles, the OE signal. However, DMOE only goes active on DRAM read cycles, while OE is active for all PM5/DMOE -Port M bit 5 or DRAM Continuous Page Mode Output Enable. DMOE is similar to

## ..15 SDRAM Interface Signals

- "Chip-Select Logic," for more details. CSD0, CSD1—These two signals are multiplexed with SDRAM CSO and CSI. When SDRAM is enabled, CSD0 and CSD1 are SDRAM bank 1 and bank 2 chip-select signals. Also see Chapter 6,
- "Chip-Select Logic." becomes an SDRAM RAS signal. For additional information about this subject, see Chapter 6, -This signal is multiplexed with SDRAM RAS. When SDRAM is enabled, this signal
- becomes an SDRAM RAS signal. For more details, see Chapter 6, "Chip-Select Logic." This signal is multiplexed with SDRAM CAS. When SDRAM is enabled, this signal
- signal. There is additional programming information about this subject in Chapter 6, "Chip-Select SDWE—SDRAM WE. When SDRAM is enabled, this signal becomes an SDRAM Write-Enable
- PM0/SDCLK--Port M bit 0 or SDRAM Clock. This pin defaults to GPIO input pulled low
- PM1/SDCE--Port M bit 1 or SDRAM Clock Enable. This pin defaults to GPIO pulled low.
- PM2/DQMH, PM3/DQML—Port M bits 2-3 or SDRAM input/output mask. These pins default to GPIO pulled low.
- PM4/SDA10—Port M bit 4 or SDRAM Address A10. This pin defaults to GPIO input pulled low



# In-Circuit Emulation (ICE) Signals

Freescale Semiconductors#®Remulation (ICE) Signals

The ICE module is designed to support low-cost emulator designs using the MC68VZ328 microprocessor There are four interface signals that are extended to external pins.

- or in data space during emulation mode. the P/D function. P/D is a status signal that shows whether the current bus cycle is in program space reset or left unconnected. This pin defaults to GPIO input pulled high, but can be programmed as three-stated after reset release. For normal operation, this pin must be pulled high during system of this input signal will put the MC68VZ328 into Hi-Z mode, in which all MC68VZ328 pins are HIZ/P/D/PG3--High Impedance, Program/Data, or Port G bit 3. During system reset, a logic low
- emulation mode. EMUIRQ is an active low, level 7 interrupt input signal. "In-Circuit Emulation." For normal operation, this pin must be pulled high during system reset or input signal will put the MC68VZ328 into emulation mode, which is described in Chapter 16, left unconnected. After system reset, this pin defaults to an EMUIRQ function in normal or EMUIRQ/PG2--Emulator Interrupt Request or Port G bit 2. During system reset, a logic low of this
- used in emulation mode for breakpoint control. unconnected. After system reset, this pin defaults to the EMUBRK function, which is an I/O signal "Bootstrap Mode." For normal operation, this pin must be pulled high during system reset or left input signal will put the MC68VZ328 into bootstrap mode, which is described in Chapter 17, EMUBRK/PG5--Emulator Breakpoint or Port G bit 5. During system reset, a logic low of this
- but in normal and bootstrap modes as well. See Chapter 16, "In-Circuit Emulation," used to select 16-bit data bus memory devices. EMUCS is not only activated in emulation mode signal that selects the dedicated memory space from 0xFFFC0000 to 0xFFFDFFFF. It cannot be information about EMUCS operation. This pin defaults to an EMUCS signal EMUCS/PG4-ARCHIVED BY FREESCALE -Emulator Chip-Select or Port G bit 4. EMUCS is an 8-bit data bus width chip-select

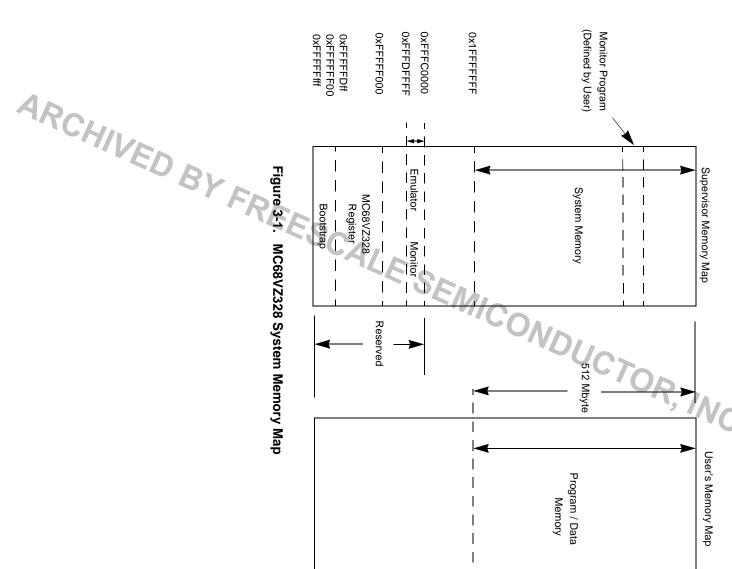




## Freescale Semiconductor, Inc.

### Memory Map Chapter

The memory map is a guide to all on-chip resources. When you configure your chip, refer to Figure 3-1 and either Table 3-1 on page 3-2, which is sorted by address, or Table 3-2 on page 3-8, which is sorted alphabetically by register name.



# Programmer's Memory Mafreescale Semiconductor, Inc.

## 3.1 Programmer's Memory Map

a double-mapped bit is cleared in the system control register, then the base address is 0xFFFFF000 only. Unpredictable results occur if you write to any 4K register space not documented in Table 3-1 or Table 3-2 On reset the base address used in the table is 0xFFFFF000 (or 0xXXFFF000, where XX is "don't care"). If

able 3-1. Programmer's Memory Map (Sorted by Address)

Address	Name	Width	Description	Reset Value	Page Number
0xFFFFF000	SCR	8	System control register	0x1C	5-2
0xFFFFF003	PCR	8	Peripheral control register	0x00	5-4
0xFFFFF004	IDR	32	Silicon ID register	0x56000000	5-5
0xFFFFF008	IODCR	16	I/O drive control register	0x1FFF	5-6
0xFFFFF100	CSGBA	16	Chip-select group A base register	0x0000	6-4
0xFFFFF102	CSGBB	16	Chip-select group B base register	0x0000	6-4
0xFFFFF104	CSGBC	16	Chip-select group C base register	0x0000	6-4
0xFFFFF106	CSGBD	16	Chip-select group D base register	0x0000	6-4
0xFFFFF108	CSUGBA	16	Chip-select upper group address register	0000x0	6-6
0xFFFFF10A	CSCR	16	Chip-select control register	0x0000	6-16
0xFFFFF110	CSA	16	Group A chip-select register	0x00B0	6-8
0xFFFFF112	CSB	16	Group B chip-select register	0x0000	6-8
0xFFFFF114	CSC	16	Group C chip-select register	0000x0	6-8
0xFFFFF116	CSD	16	Group D chip-select register	0x0200	6-8
0xFFFFF118	EMUCS	16	Emulation chip-select register	0x0060	6-16
0xFFFFF200	PLLCR	16	PLL control register	0x24B3	4-8
0xFFFFF202	PLLFSR	16	PLL frequency select register	0x0347	4-10
0xFFFFF204	RES	ļ	Reserved	I	I
0xFFFFF207	PCTLR	8	Power control register	0x1F	4-14
0xFFFFF300	IVR	8	Interrupt vector register	0x00	9-7
0xFFFFF302	ICR	16	Interrupt control register	0x0000	9-8
0xFFFFF304	MR	32	Interrupt mask register	0x00FFFFFF	9-10
0xFFFFF308	RES	32	Reserved	-	I
0xFFFFF30C	ISR	32	Interrupt status register	0x00000000	9-12

Table 3-1. Programmer's Memory Map (Sorted by Address) (Continued)

10-25	0xFF	Port F data register	8	PFDATA	0xFFFFF429
10-24	00x0	Port F direction register	8	PFDIR	0xFFFFF428
10-21	0xFF	Port E select register	8	PESEL	0xFFFFF423
10-21	0xFF	Port E pull-up enable register	8	PEPUEN	0xFFFFF422
10-21	93x0	Port E data register	8	PEDATA	0xFFFFF421
10-21	00x0	Port E direction register	8	PEDIR	0xFFFFF420
10-16	00x0	Port D interrupt request edge register	8	PDIRQEG	0xFFFFF41F
10-16	00x0	Port D keyboard enable register	8	PDKBEN	0xFFFFF41E
10-16	0x00	Port D interrupt request enable register	8	PDIRQEN	0xFFFFFF41D
10-16	00x0	Port D polarity register	8	PDPOL	0xFFFFF41C
10-16	0Ax0	Port D select register	8	PDSEL	0xFFFFF41B
10-16	33×0	Port D pull-up enable register	8	PDPUEN	0xFFFFFF41A
10-16	0xFF	Port D data register	8	PDDATA	0xFFFFF419
10-16	00x0	Port D direction register	8	PDDIR	0xFFFFF418
10-11	93×0	Port C select register	8	PCSEL	0xFFFFF413
10-11	0xFF	Port C pull-down enable register	8	PCPDEN	0xFFFFF412
10-11	00x0	Port C data register	8	PCDATA	0xFFFFF411
10-11	00x0	Port C direction register	8	PCDIR	0xFFFFF410
10-8	JJX0	Port B select register	8	PBSEL	0xFFFFF40B
10-8	33x0	Port B pull-up enable register	8	PBPUEN	0xFFFFF40A
10-8	33x0	Port B data register	8	PBDATA	0xFFFFF409
10-8	00x0	Port B direction register	8	PBDIR	0xFFFFF408
I	I	Reserved	8	RES	0xFFFFF403
10-6	94x0	Port A pull-up enable register	8	PAPUEN	0xFFFFF402
10-6	33x0	Port A data register	8	PADATA	0xFFFFF401
10-6	00x0	Port A direction register	8	PADIR	0xFFFFF400
9-19	2859x0	Interrupt level control register	16	ILCR	0xFFFFF314
9-16	0000000000	Interrupt pending register	32	IPR	0xFFFFF310
Page Number	Reset Value	Description	Width	Name	Address

### Table 3-1.

# Programmer's Memory Map (Sorted by Address) (Continued)

15-10	0x0000	PWM unit 2 counter register	16	PWMCNT2	0xFFFFF516
15-10	0x0000	PWM unit 2 width register	16	PWMW2	0xFFFFF514
15-9	0x0000	PWM unit 2 period register	16	PWMP2	0xFFFFF512
15-8	0x0000	PWM unit 2 control register	16	PWMC2	0xFFFFF510
	I	Reserved	16	RES	0xFFFFF506
15-7	0x00	PWM unit 1 counter register	8	PWMCNT1	0xFFFFF505
15-7	0xFE	PWM unit 1 period register	8	PWMP1	0xFFFFF504
15-6	0xxxxx	PWM unit 1 sample register	16	PWMS1	0xFFFFF502
15-4	0x0020	PWM unit 1 control register	91	PWMC1	0xFFFFF500
10-40	0x3F	Port M select register	8	PMSEL	0xFFFFF44B
10-39	0x3F	Port M pull-up/pull-down enable regis- ter	8	PMPUEN	0xFFFFFF44A
10-38	0x20	Port M data register	8	PMDATA	0xFFFFF449
10-37	0x00	Port M direction register	8	PMDIR	0xFFFFF448
10-36	0xFF	Port K select register	8	PKSEL	0xFFFFF443
10-36	0xFF	Port K pull-up/pull-down enable register	8	PKPUEN	0xFFFFFF442
10-35	0x0F	Port K data register	8	PKDATA	0xFFFFF441
10-34	0x00	Port K direction register	8	PKDIR	0xFFFFF440
10-33	0xEF	Port J select register	8	PJSEL	0xFFFFFF43B
10-33	0xFF	Port J pull-up enable register	8	PJPUEN	0xFFFFF43A
10-32	0xFF	Port J data register	8	PJDATA	0xFFFFF439
10-31	0x00	Port J direction register	8	PJDIR	0xFFFFF438
10-31	0x08	Port G select register	8	PGSEL	0xFFFFF433
10-30	0x3D	Port G pull-up enable register	8	PGPUEN	0xFFFFF432
10-28	0x3F	Port G data register	8	PGDATA	0xFFFFF431
10-28	0x00	Port G direction register	8	PGDIR	0xFFFFFF430
10-27	0x87	Port F select register	8	PFSEL	0xFFFFFF42B
10-27	0×FF	Port F pull-up/pull-down enable register	8	PFPUEN	0xFFFFF42A
Page Number	Reset Value	Description	Width	Name	Address

Table 3-1.

Address  0xFFFFF600  0xFFFFF602  0xFFFFF604  0xFFFFF606  0xFFFFF608	Name TCTL1 TPRER1 TCMP1 TCR1 TCN1	Width  16  16  16  16	Timer unit 1 control register Timer unit 1 prescaler registe Timer unit 1 compare register Timer unit 1 compare register Timer unit 1 capture register Timer unit 1 counter register	Description  Timer unit 1 control register  Timer unit 1 prescaler register  Timer unit 1 compare register  Timer unit 1 capture register  Timer unit 1 counter register	VC. 2005
0xFFFFF60A 0xFFFFF610	TSTAT1 TCTL2	16	Timer unit 1 status register Timer unit 2 control register	ster	ster 0x0000 lister 0x0000
0xFFFFF612	TPRER2	16	Timer unit 2 prescaler register	egister	egister 0x0000
0xFFFFF614	TCMP2	16	Timer unit 2 compare register	egister	egister 0xFFFF
0xFFFFF616	TCR2	16	Timer unit 2 capture register	gister	gister 0x0000
0xFFFFF618	TCN2	16	Timer unit 2 counter register	gister	gister 0x0000
0xFFFFF61A	TSTAT2	16	Timer unit 2 status register	ster	ster 0x0000
0xFFFFF700	SPIRXD	16	SPI unit 1 receive data register	register	register 0x0000
0xFFFFFF702	SPITXD	16	SPI unit 1 transmit data register	a register	a register 0x0000
0xFFFFF704	SPICONT1	16	SPI unit 1 control/status register	ıs register	ıs register 0x0000
0xFFFFFF706	SPIINTCS	16	SPI unit 1 interrupt control/status register	ntrol/status	ntrol/status 0x0000
0xFFFFF708	SPITEST	16	SPI unit 1 test register		0x0000
0xFFFFF70A	SPISPC	16/	SPI unit 1 sample period control register	d control	d control 0x0000
0xFFFFF800	SPIDATA2	16	SPI unit 2 data register		
0xFFFFF802	SPICONT2	16	SPI unit 2 control/status register	s register	s register 0x0000
0xFFFFF900	USTCNT1	16	UART unit 1 status/control register	trol register	<u> </u>
0xFFFFF902	UBAUD1	16	UART unit 1 baud control register	ol register	jister
0xFFFFF904	URX1	16	UART unit 1 receiver register	gister	gister 0x0000
0xFFFFF908	UMISC1	16	UART unit 1 miscellaneous register	ous register	
V0644444×0	NIPR1	16	UART unit 1 non-integer prescaler register	r prescaler	r prescaler 0x0000
0xFFFFF910	USTCNT2	16	UART unit 2 status/control register	rol register	rol register 0x0000

Programmer's Memory Map (Sorted by Address) (Continued)

Address	Name	Width	Description	Reset Value	Page Number
0xFFFFF912	UBAUD2	16	UART unit 2 baud control register	0x003F	14-12
0xFFFFF914	URX2	16	UART unit 2 receiver register	0x0000	14-13
0xFFFFF916	UTX2	16	UART unit 2 transmitter register	0x0000	14-14
0xFFFFF918	UMISC2	16	UART unit 2 miscellaneous register	0x0000	14-16
0xFFFFF91A	NIPR2	16	UART unit 2 non-integer prescaler register	0x0000	14-18
0xFFFFF91C	HMARK	16	UART unit 2 FIFO half mark register	0x0102	14-29
0xFFFFFA00	LSSA	32	LCD screen starting address register	0x00000000	8-10
0xFFFFFA05	LVPW	8	LCD virtual page width register	0xFF	8-11
0xFFFFFA08	LXMAX	16	LCD screen width register	0x03F0	8-12
0xFFFFFA0A	LYMAX	16	LCD screen height register	0x01FF	8-12
0xFFFFFA18	LCXP	16	LCD cursor X position register	0x0000	8-12
0xFFFFFA1A	LCYP	16	LCD cursor Y position register	0x0000	8-13
0xFFFFFA1C	LCWCH	16	LCD cursor width and height register	0x0101	8-14
0xFFFFFA1F	LBLKC	8	LCD blink control register	0x7F	8-14
0xFFFFFA20	LPICF	8	LCD panel interface configuration register	0x00	8-15
0xFFFFFA21	LPOLCF	8	LCD polarity configuration register	0x00	8-16
0xFFFFFA23	LACDRC	8	LACD rate control register	0x00	8-16
0xFFFFFA25	LPXCD	8	LCD pixel clock divider register	0x00	8-17
0xFFFFFA27	LCKCON	8	LCD clocking control register	0x00	8-18
0xFFFFFA29	LRRA	8	LCD refresh rate adjustment register	0xFF	8-18
0xFFFFFA2B	RES 👩	8	Reserved	-	I
0xFFFFFA2D	LPOSR	8	LCD panning offset register	0x00	8-19
0xFFFFFA31	LFRCM	œ	LCD frame rate control modulation register	0x00	8-19
0xFFFFFA33	LGPMR	8	LCD gray palette mapping register	0x84	8-20
0xFFFFFA36	PWMR	16	PWM contrast control register	0x0000	8-20
0xFFFFFA38	RMCR	8	Refresh mode control register	0x00	8-21
0xFFFFFA39	DMACR	8	DMA control register	0x62	8-22

ble 3-1.
Programmer's Memory Map (Sorted by Address) (Continued)
Map
(Sorted by
Address)
(Continued)

г		1	<u> </u>			<u> </u>												Т		T	Г	
	0xFFFFFExx	0xFFFFFD0E	0xFFFFFD0C	0xFFFFFD0A	0xFFFFFD08	0xFFFFFD04	0xFFFFFD00	0xFFFFFC80	0xFFFFFC06	0xFFFFFC04	0xFFFFFC02	0xFFFFFC00	0xFFFFFB1C	0xFFFFFB1A	0xFFFFFB12	0xFFFFFB10	0xFFFFFB0E	0xFFFFFB0C	0xFFFFFB0A	0xFFFFFB04	0xFFFFFB00	Address
ARCHIVEDBY	Bootloader	ICEMSR	ICEMCR	ICEMCMR	ICEMCCR	ICEMAMR	ICEMACR	RES	SDPWDN	SDCTRL	DRAMC	DRAMMC	DAYALARM	DAYR	STPWCH	RTCIENR	RTCISR	RTCCTL	WATCHDOG	RTCALRM	RTCTIME	Name
	1	16	16	16	16	32	32		16	16	16	16	16	16	8	16	16	8	16	32	32	Width
	Bootloader microcode space	ICEM status register	ICEM control register	ICEM control mask register	ICEM control compare register	ICEM address mask register	ICEM address compare register	Reserved	SDRAM power down register	SDRAM control register	DRAM control register	DRAM memory configuration register	RTC day alarm register	RTC day count register	Stopwatch minutes register	RTC interrupt enable register	RTC interrupt status register	RTC control register	Watchdog timer register	RTC alarm register	RTC time of day register	Description
	1	0000x0	0000x0	0000x0	0000x0	00000000x0	00000000x0	_	0000x0	0£00x0	0000x0	0000x0	0000x0	xxx0x0	JE00x0	0000x0	0000x0	0800x0	1000x0	00000000x0	XX00XXXx0	Reset Value
	1	16-10	16-8	16-6	16-6	16-4	16-4		7-18	7-16	7-14	7-12	11-8	11-6	11-14	11-12	11-10	11-10	11-4	11-3	11-3	Page Number

Programmer's Memory Map (Sorted by Register Name)

9-10	0x00FFFFFF	Interrupt mask register	32	0xFFFFF304	IMR
9-19	0x6533	Interrupt level control register	16	0xFFFFF314	ILCR
5-5	0x56000000	Silicon ID register	32 8	0xFFFFF004	IDR
9-8	0x0000	Interrupt control register	16	0xFFFFF302	ICR
16-10	0x0000	ICEM status register	16	0xFFFFFD0E	ICEMSR
16-8	0x0000	ICEM control register	16	0xFFFFFFD0C	ICEMCR
16-6	0000x0	ICEM control mask register	16   1	0xFFFFFD0A	ICEMCMR
16-6	0x0000	ICEM control compare register	16	0xFFFFFD08	ICEMCCR
16-4	00000000000	ICEM address mask register	32	0xFFFFFD04	ICEMAMR
16-4	0000000000	ICEM address compare register	32	0xFFFFFD00	ICEMACR
14-29	0x0102	UART unit 2 FIFO half mark register	16 ر	0xFFFFF91C	HMARK
6-16	0x0060	Emulation chip-select register	16 E	0xFFFFF118	SOUME
7-12	0x0000	DRAM memory configuration register	16	0xFFFFFC00	DRAMMC
7-14	0000x0	DRAM control register	1 91	0xFFFFFC02	DRAMC
8-22	0x62	DMA control register	1 8	0xFFFFFA39	DMACR
11-6	0x0xxx	RTC day count register	16 F	0xFFFFFB1A	DAYR
11-8	0x0000	RTC day alarm register	16 F	0xFFFFFB1C	DAYALARM
6-6	0x0000	Chip-select upper group address register	16	0xFFFFF108	CSUGBA
6-4	0000x0	Chip-select group D base register	16	0xFFFFF106	CSGBD
6-4	0000x0	Chip-select group C base register	16	0xFFFFF104	CSGBC
6-4	0000x0	Chip-select group B base register	16	0xFFFFF102	GSGBB
6-4	0x0000	Chip-select group A base register	16	0xFFFFF100	CSGBA
6-8	0x0200	Group D chip-select register	16 (	0xFFFFF116	CSD
6-16	0x0000	Chip-select control register	16 (	0xFFFFF10A	CSCR
6-8	0x0000	Group C chip-select register	16	0xFFFFF114	080
6-8	0x0000	Group B chip-select register	16	0xFFFFF112	CSB
6-8	0x00B0	Group A chip-select register	16	0xFFFFF110	CSA
I	I	Bootloader microcode space		0xFFFFFExx	Bootloader
Page Number	Reset Value	Description	Width	Address	Name

Programmer's Memory Map (Sorted by Register Name) (Continued)

10-8	0xFF	Port B data register	00	0xFFFFF409	PBDATA
10-6	0xFF	Port A pull-up enable register	8	0xFFFFF402	PAPUEN
10-6	0000	Port A direction register	8	0xFFFFF400	PADIR
10-6	34x0	Port A data register	8	0xFFFFF401	PADATA
14-18	0000x0	UART unit 2 non-integer prescaler register	16	0xFFFFF91A	NIPR2
14-18	0000x0	UART unit 1 non-integer prescaler register	16	0xFFFFF90A	NIPR1
8-12	0x01FF	LCD screen height register	16	0xFFFFFA0A	LYMAX
8-12	0x03F0	LCD screen width register	16	0xFFFFFA08	LXMAX
8-11	0xFF	LCD virtual page width register	8	0xFFFFFA05	LVPW
8-10	0x00000000	LCD screen starting address register	32	0xFFFFFA00	LSSA
8-18	0xFF	LCD refresh rate adjustment register	8	0xFFFFFA29	LRRA
8-17	0x00	LCD pixel clock divider register	8	0xFFFFFA25	LPXCD
8-19	0x00	LCD panning offset register	8	0xFFFFFA2D	LPOSR
8-16	0x00	LCD polarity configuration register	8	0xFFFFFA21	LPOLCF
8-15	00x0	LCD panel interface configuration register	8	0xFFFFFA20	LPICF
8-20	0x84	LCD gray palette mapping register	8	0xFFFFFA33	LGPMR
8-19	0x00	LCD frame rate control modulation register	8	0xFFFFFA31	LFRCM
8-13	0x0000	LCD cursor Y position register	16	0xFFFFFA1A	LCYP
8-12	0x0000	LCD cursor X position register	16	0xFFFFFA18	LCXP
8-14	0x0101	LCD cursor width and height register	16	0xFFFFFA1C	LCWCH
8-18	00x0	LCD clocking control register	8	0xFFFFFA27	LCKCON
8-14	0x7F	LCD blink control register	8	0xFFFFFA1F	LBLKC
8-16	0x00	LACD rate control register	8	0xFFFFFA23	LACDRC
9-7	0x00	Interrupt vector register	8	0xFFFFF300	IVR
9-12	0x00000000	Interrupt status register	32	0xFFFFF30C	ISR
9-16	0x00000000	Interrupt pending register	32	0xFFFFF310	IPR
5-6	0x1FFF	I/O drive control register	16	0xFFFFF008	IODCR
Page Number	Reset Value	Description	Width	Address	Name

Programmer's Memory Map (Sorted by Register Name) (Continued)

Name	Address	Width	Description  Port B direction register	Reset Value
PBPUEN	0xFFFFF40A	8	gist	0xFF
PBSEL	0xFFFFF40B	&	Port B select register	0xFF
PCDATA	0xFFFFF411	&	Port C data register	0x00
PCDIR	0xFFFFFF410	8	Port C direction register	0x00
PCPDEN	0xFFFFF412	8	Port C pull-down enable register	0xFF
PCR	0xFFFFF003	8	Peripheral control register	0x00
PCSEL	0xFFFFF413	8	Port C select register	0xFF
PCTLR	0xFFFFF207	8	Power control register	0x1F
PDDATA	0xFFFFF419	8	Port D data register	0xFF
PDDIR	0xFFFFF418	8	Port D direction register	0x00
PDIRQEG	0xFFFFFF41F	8	Port D interrupt request edge register	0x00
PDIRQEN	0xFFFFF41D	8	Port D interrupt request enable register	0x00
PDKBEN	0xFFFFF41E	8	Port D keyboard enable register	0x00
PDPOL	0xFFFFF41C	8	Port D polarity register	0x00
PDPUEN	0xFFFFF41A	8	Port D pull-up enable register	0xFF
PDSEL	0xFFFFF41B	8	Port D select register	0xF0
PEDATA	0xFFFFFF421	8	Port E data register	0xFF
PEDIR	0xFFFFF420	8	Port E direction register	0x00
PEPUEN	0xFFFFF422	8	Port E pull-up enable register	0xFF
PESEL	0xFFFFF423	8	Port E select register	0xFF
PFDATA	0xFFFFF429	8	Port F data register	0xFF
PFDIR	0xFFFFF428	8	Port F direction register	0x00
NBUPAH	0xFFFFF42A	8	Port F pull-up/pull-down enable register	0xFF
PFSEL	0xFFFFFF42B	8	Port F select register	0x87
PGDATA	0xFFFFF431	8	Port G data register	0x3F
PGDIR	0xFFFFFF430	8	Port G direction register	0x00
PGPUEN	0xFFFFF432	8	Port G pull-up enable register	0x3D

Programmer's Memory Map (Sorted by Register Name) (Continued)

		Reserved	16	0xFFFFF506	RES
		Reserved	8	0xFFFFFF403	RES
		Reserved	32	0xFFFFF308	RES
		Reserved		0xFFFFF204	RES
0x0000		PWM unit 2 width register	16	0xFFFFF514	PWMW2
0xxxxx		PWM unit 1 sample register	16	0xFFFFF502	PWMS1
0x0000		PWM contrast control register	16	0xFFFFFA36	PWMR
0x0000		PWM unit 2 period register	16	0xFFFFF512	PWMP2
0xFE		PWM unit 1 period register	8	0xFFFFF504	PWMP1
0x0000		PWM unit 2 counter register	16	0xFFFFF516	PWMCNT2
0x00		PWM unit 1 counter register	8	0xFFFFF505	PWMCNT1
0x0000		PWM unit 2 control register	16	0xFFFFF510	PWMC2
0x0020		PWM unit 1 control register	16	0xFFFFF500	PWMC1
0x3F		Port M select register	8	0xFFFFF44B	PMSEL
0x3F		Port M pull-up/pull-down enable register	8	0xFFFFF44A	PMPUEN
0x00		Port M direction register	8	0xFFFFF448	PMDIR
0x20		Port M data register	8	0xFFFFFF449	PMDATA
0x0347		PLL frequency select register	16	0xFFFFF202	PLLFSR
0x24B3		PLL control register	16	0xFFFFF200	PLLCR
0xFF		Port K select register	8	0xFFFFFF443	PKSEL
0xFF		Port K pull-up/pull-down enable register	8	0xFFFFF442	PKPUEN
0x00		Port K direction register	8	0xFFFFF440	PKDIR
0x0F		Port K data register	8	0xFFFFF441	PKDATA
0xEF		Port J select register	8	0xFFFFF43B	PJSEL
0xFF		Port J pull-up enable register	8	0xFFFFF43A	PJPUEN
0x00	*	Port J direction register	8	0xFFFFF438	PJDIR
OxFF	<	Port J data register	8	0xFFFFFF439	PJDATA
0x08	20	Port G select register	8	0xFFFFFF433	PGSEL
Reset Value	_	Description	Width	Address	Name

Programmer's Memory Map (Sorted by Register Name) (Continued)

12-6	0x0000	Timer unit 2 control register	16	0xFFFFF610	TCTL2
12-6	0x0000	Timer unit 1 control register	16	0xFFFFF600	TCTL1
12-10	0x0000	Timer unit 2 capture register	16	0xFFFFF616	TCR2
12-10	0000x0	Timer unit 1 capture register	16	0xFFFFF606	TCR1
12-10	0000x0	Timer unit 2 counter register	16	0xFFFFF618	TCN2
12-11	0000x0	Timer unit 1 counter register	16	0xFFFFF608	TCN1
12-9	0xFFFF	Timer unit 2 compare register	16	0xFFFFF614	TCMP2
12-9	0xFFFF	Timer unit 1 compare register	16	0xFFFFF604	TCMP1
11-14	0x003F	Stopwatch minutes register	8	0xFFFFFB12	STPWCH
13-5	0000x0	SPI unit 1 transmit data register	16	0xFFFFF702	SPITXD
13-10	0000x0	SPI unit 1 test register	16	0xFFFFF708	SPITEST
13-11	0000×0	SPI unit 1 sample period control register	91	0xFFFFF70A	SPISPC
13-4	0x0000	SPI unit 1 receive data register	16	0xFFFFF700	SPIRXD
13-8	0000x0	SPI unit 1 interrupt control/status register	16	0xFFFFF706	SPIINTCS
13-14	0x0000	SPI unit 2 data register	16	0xFFFFF800	SPIDATA2
13-15	0000x0	SPI unit 2 control/status register	16	0xFFFFF802	SPICONT2
13-6	0x0000	SPI unit 1 control/status register	16	0xFFFFF704	SPICONT1
7-18	0000x0	SDRAM power down register	16	0xFFFFFC06	SDPWDN
7-16	0x003C	SDRAM control register	16	0xFFFFFC04	SDCTRL
5-2	0x1C	System control register	8	0xFFFFF000	SCR
11-3	0xXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	RTC time of day register	32	0xFFFFFB00	RTCTIME
11-10	0x0000	RTC interrupt status register	16	0xFFFFFB0E	RTCISR
11-12	0000x0	RTC interrupt enable register	16	0xFFFFFB10	RTCIENR
11-10	0x0080	RTC control register	8	0xFFFFFB0C	RTCCTL
11-3	0x00000000	RTC alarm register	32	0xFFFFFB04	RTCALRM
8-21	0x00	Refresh mode control register	8	0xFFFFFA38	RMCR
I	I	Reserved	I	0xFFFFFC80	RES
I	I	Reserved	8	0xFFFFFA2B	RES
Page Number	Reset Value	Description	Width	Address	Name

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	WATCHDOG	UTX2	UTX1	USTCNT2	USTCNT1	URX2	URX1	UMISC2
ARCHIVED BY FREESCAL	0xFFFFFB0A	0xFFFFF916	0xFFFFF906	0xFFFFF910	0xFFFFF900	0xFFFFF914	0xFFFFF904	0xFFFFF918
FREESO	16	16	16	16	16	16	16	16
42	Watchdog timer register	UART unit 2 transmitter register	UART unit 1 transmitter register	UART unit 2 status/control register	UART unit 1 status/control register	UART unit 2 receiver register	UART unit 1 receiver register	UART unit 2 miscellaneous registe

Reset Value Number

UBAUD2

0xFFFFF912

16

UART unit 2 baud control register

UMISC1

0xFFFFF908

16

UART unit 1 miscellaneous register

UBAUD1

0xFFFFF902

16

UART unit 1 baud control register

TSTAT2

0xFFFFF61A

16

Timer unit 2 status register

TPRER2

0xFFFFF612

16

Timer unit 2 prescaler register

TSTAT1

0xFFFFF60A

16

Timer unit 1 status register

TPRER1

0xFFFFF602

16

Timer unit 1 prescaler register

0x0001

0x0000

0x0000

0x0000

14-10

0x0000

14-10

0x0000

0x0000

0x0000

0x0000

0x003F

0x003F

0x0000

12-12

0x0000

12-12

0x0000

12-8

0x0000

12-8



## Freescale Semiconductor, Inc.

### Control Module Clock Generation Module and Power hapter 4 C. 2005

description of both modules comprises a single chapter because their operation is so closely integrated. MC68VZ328 and its associated peripherals. The programmability of the individual clock signals makes the CGM a flexible clock source for the This chapter describes the clock generation module (CGM) and power control module (PCM). The

clock signals used throughout the MC68VZ328 integrated processor. The frequency of all clock signals MC68VZ328 has four different power modes to provide optimum power efficiency. The CGM uses a low-frequency oscillator in conjunction with a multiplier/divider chain to produce the (except the low-frequency reference) are individually selectable through software control. The

clocks (except for the low-frequency clock) are disabled. burst widths. For maximum power savings, the MC68VZ328 can be placed in sleep mode in which all The PCM controls the power consumption of the CPU by applying clock signals to the CPU at reduced

### NOTE:

ARCHIVED BY FREES! the DragonBall family. The nomenclature changed from PLL to CGM to be consistent with Motorola naming and standards conventions. The term The CGM module is designated as the PLL module in earlier versions of

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are not available from Freescale for import or sale in the United States prior to September 2010; MC68VZ328 Product Family



### 4-2

## For More Information On This Product, Go to: www.freescale.com

Introduction to the Clock JeksessaleuSemiconductor, Inc.

Introduction to the **Clock Generation Module** 

The CGM produces four clock signals:

- DMACLK-CLK32--A low-frequency reference clock used by almost every module -Used to create the remaining two clocks, and serves as DMA clock for the LCD
- SYSCLK--Used by most modules, including the CPU
- -Used as reference by the LCD

the CLK32 signal, the frequency of the clock signals can be individually programmed The distribution of the clock signals generated by the CGM is shown in Table 4-1. With the exception of

**CGM Clock Signal Distribution** 

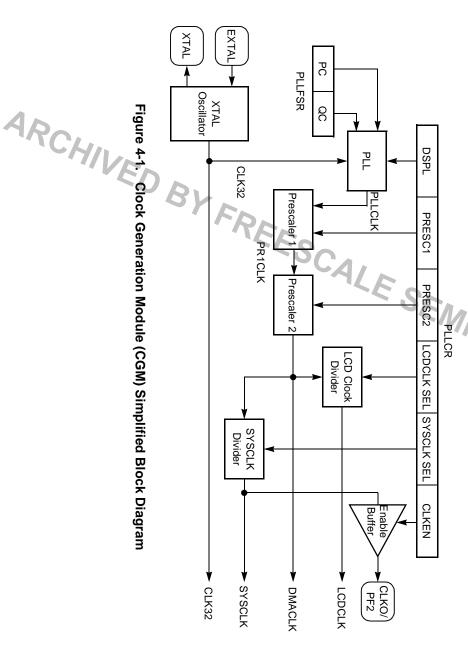
## CGM Operational Overview

Freescale Semiconductor, Incom Operational Overview

determined by the frequency of the external crystal. The CLK32 clock signal serves as a source for the PLL and many other modules within the MC68VZ328. XTAL oscillator circuit. The output of the XTAL oscillator is the CLK32 signal, whose frequency is source for the CGM is a crystal oscillator that is comprised of an external crystal connected to the internal The CGM consists of six major parts, as shown in the simplified block diagram in Figure 4-1. The clock

select 2 (PRESC2) bit in the PLLCR. The DMACLK signal is applied to the LCD controller in the of the PC and QC fields of the PLL frequency select register (PLLFSR). The output of the PLL is applied MC68VZ328 and also serves as the clock source for the LCD clock divider and the SYSCLK divider. frequency is selected by the prescaler select 1 (PRESC1) bit in the PLLCR. The output of the prescaler 1 to a divider chain composed of two prescalers. The PLLCLK clock is first input into prescaler 1. Its output The output frequency of the PLL (PLLCLK) is determined by the frequency of CLK32 and by the values (PR1CLK) is applied to prescaler 2, whose output frequency (DMACLK) is controlled by the prescaler

enabled and bit 2 in the Port F select register (PFSEL) is cleared. clock out/Port F bit 2 pin (CLKO/PF2). See Section 10.4.7.3, "Port F Dedicated I/O Functions," on also used as the CPU clock signal (CPUCLK) by the internal FLX68000 CPU. SYSCLK is the only selection (LCDCLK) field in the PLLCR. The LCDCLK signal is only used by the LCD controller. The page 10-26 for more information. The output is available when the clock enable bit of the PLLCR is CGM-generated clock signal that can be made available to external devices via the buffered output of the SYSCLK divider produces a SYSCLK clock signal that is used throughout the MC68VZ328. SYSCLK is The output of the LCD clock divider is LCDCLK, whose frequency is controlled by the LCD clock



# Detailed CGM Clock Descriptions Scale Semiconductor, Inc.

### Detailed **CGM Clock Descriptions**

Section 4.3.1, "CLK32 Clock Signal," and Section 4.3.2, "PLLCLK Clock Signal," describe in detail the operation of each clock signal produced by the CGM.

## CLK32 Clock Signal

frequency of the external crystal. The CGM supports either a 32.768 kHz or a 38.4 kHz crystal after initial power is applied to the circuit. The frequency of the CLK32 signal is determined by the The low-frequency output of the XTAL oscillator (CLK32) is available within a few hundred milliseconds

### NOTE:

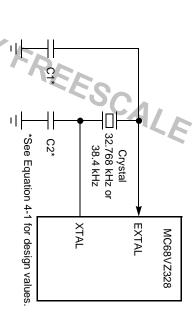
Regardless of the crystal frequency used, the output is always labeled

Figure 4-2 represents a suggestion of how a crystal may be connected to the MC68VZ328. The values of following formula: C1 and C2 in Figure 4-2 are determined by using the crystal load capacitance (CL), PCB stray capacitance, Cstray (measured or approximated), and DragonBall input capacitance (Cdbvz << 1.0 pf) according to the

$$CL = Cstray + Cdbvz + (C1 * C2) / (C1 + C2)$$

appropriate circuit layout and circuit values. Typical design values are C1 = C2 = 20 pf. The user should consult the crystal manufacturer for

"Sleep Mode," for detailed information on sleep mode is placed in sleep mode, the CLK32 clock is available as long as power is applied. See Section 4.5.1.4, The CLK32 clock signal is unique in that while the other clock sources are disabled when the MC68VZ328



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Figure 4-2. **Example of External Crystal Connection** 

## PLLCLK Clock Signal

input frequency and the values in the PC and QC fields of the PLLFSR. Section 4.3.2.2, The PLL output frequency, PLL clock (PLLCLK), is determined by a combination of the CLK32 signal's Selection," describes the procedure for frequency selection "PLL Frequency



## **PLLCLK Initial Power-up Sequence**

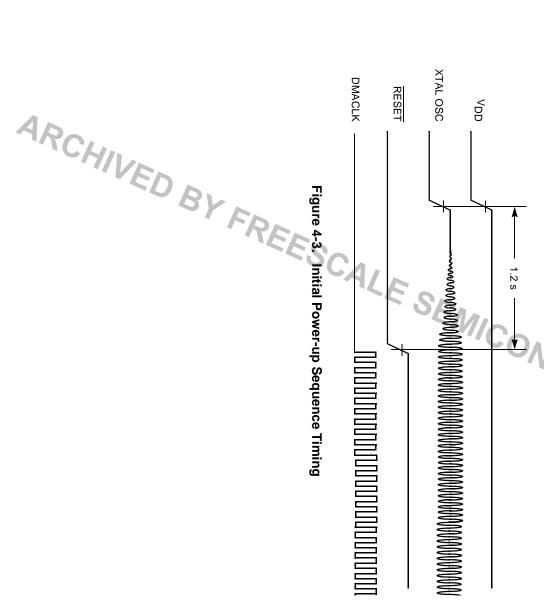
Freescale Semiconductorealecan Clock Descriptions

approximate value and should only be used as a starting point. The RESET pin (input) is a Schmitt trigger device with a threshold of 1.4 V high and 1.0 V low. ensure that the crystal oscillator starts and stabilizes. This is a significant change from the 250 ms required low-power design on the oscillator pads, the RESET signal must be asserted (low) for at least 1.2 s to power is initially applied to the MC68VZ328, the XTAL oscillator begins to oscillate. Due to the Refer to Figure 4-3 for a graphical representation of the following power-up sequence description. with the previous DragonBall and DragonBall EZ processors. The length of the delay  $(1.2~{
m s})$  is an

#### NOTE:

optimum value will be determined experimentally. Due to the inherent energized and its output has stabilized, as shown in Figure 4-3. While most nature of crystals, refer to manufacturers documentation for optimum crystal oscillators typically operate with a value of 1.2 seconds, the On power up, the RESET signal should be deasserted after the crystal has circuit design information.

availability of DMACLK from prescaler 2 After RESET is deasserted, the PLLCLK signal is available to the divider chain, resulting in the



# Detailed CGM Clock Descriptions Scale Semiconductor, Inc.

#### 4.3.2.2 PLL Frequency Selection

settings produce a 77.722 MHz PLLCLK. The PLLCLK clock is phase locked to the CLK32 clock input 32.768 kHz produces a PLLCLK output of 66.322 MHz. For a 38.400 kHz crystal, the same default Using the default settings for the PC and QC fields of the PLLFSR and a CLK32 input frequency of

#### WARNING:

DMACLK and SYSCLK from operating beyond their design limits The value of prescaler 1 must always be set to divide-by-two to prevent

overall multiplication ratio depends on two separate values, PC and QC. and the rest of the divider chain. Dual-modulus counters operate differently from other counters in that the The PLL uses a dual-modulus counter to multiply the CLK32 frequency before it is input to the prescaler

 $P \ge Q + 1$ . In the following equation, the value of Q is defined as  $1 \le Q \le 14$ , and the value of P is defined as

Multiplier = 
$$2(14(P+1)+Q+1)$$

Eqn. 4-2

For example, if Q = 3 and P = 71, then the following equations obtain:

Multiplier = 
$$2 * (14 (71 + 1) + 3 + 1) = 2 * (1008 + 4) = 2024$$

2024 \* 32.768 kHz = 66.322432 MHz

changing the PLLCLK in 32.768 kHz or 38.4 kHz steps. The minimum PC and QC values are P = 0x1Band Q = 0x04 (which produce a multiplier of 794 decimal). The default multiplier value is 2024. Using any multiplier equal to or greater than 794 (decimal) allows

# **PLLCLK Frequency Selection Programming Example**

Example 4-1 on page 4-7 demonstrates the recommended sequence of events to change the PLLCLK frequency. The assumptions are:

- All peripherals have been disabled using chip-select. See Chapter 6, "Chip-Select Logic," for
- SYSCLK is operating at the highest possible frequency (SYSCLK SEL = 100).

should only be changed during an early phase of the boot-up sequence In Example 4-1, the variable NEWFREQ is the new frequency value (P and Q values) to be programmed the temporary timer interrupt should clear the timer interrupt and then return. In addition, the PLLCLK CLK32 periods. When the PLL wakes up, it will be at the new frequency. The interrupt service routine for for detailed information about sleep modes. This routine enables the timer to wake up the PLL after 96 The MC68VZ328 is placed in sleep mode before the stop command. See Section 4.5.1.4, "Sleep Mode,"

#### NOTE:

Example 4-1 is designed for clarity, and is not necessarily efficient.



# Freescale Semiconductorealecan Clock Descriptions

xample 4-1.

**Configuring the PLLCLK Frequency** 

```
SYNC1
                                                                                                                                                                                                                                            NEWFREQ equ somevalue
PLLCONTROL equ $FFFFF200
PLLFREQ equ $FFFFF202
                                                                                                                                                                                                                      TCOMPARE equ $FFFFF604
TCONTROL equ $FFFFF600
                                                                                                              SYNC2
                                                                                                                                                                                                                                 TCOMPARE
                                  the PLL sr
interrupt
 The
                                                                                                                                                                                                          equ $FFFFFF304
 PLE
has
                                                shuts down here
                                    service
                                                                                                                                   move.w
btst.b
                                                                                                                                                                    move.1
                                                                                                                                                                                move.1
                       move.w
                                                                                                                      beq.s
                                                                                                                                                                                                                                 $FFFFF604
                                                          stop #$2000
                                                                                     move.w
                                                                                                                                                           move.w
                                                                        ori.b
                                                                                                bne.s
                                                                                                              btst.b
reacquired lock
                                                                                                SYNC2
                                                                                                                       SYNC1
                                                                       #$8, PLLCONTROL+1
                                                                                                                                            IMR,-(SP)
#$fffffffd,IMR
#$0001,TCOMPARE
#$0119,TCONTROL
                       for Timer (SP)+,IMR
                                                                                                            #$7,PLLFREQ
                                                                                                                                    #$7,PLLFREQ
                                                and
                                                waits
;PLL is now and SYSCLK is stable
                                    occurs
                                                for
                                      here
                                              the Timer interrupt
                                                                                                                                                                                                                                             ;PLL Frequency
                                                                                              synchronize to CLK32 lov CLK32 is still not low,
                                                            stop,
                                                                       disable the
                                                                                                                      synchronize to CLK32 is still
                                                                                                                                                                                                          Interrupt Mask Register
                                                                                                                                                                                                                                 Timer Compare Value
                                                                                                                                                                       enable ONLY
                                                                                                                                                                                                                      Timer Control Register
                                                                                                                                             ble ONLY Timer interrupt compare value to 2 ble Timer 2 with CLK32 so
                                                                                     the
                                                                                                                                                                                   the Interrupt
                                                          le the PLL (in 30 clocks)-sleep mode enable all interrupts
                                                                                    new
             at
                                                                       w frequency
PLL (in 30
                                                                                                                                   to CLK32 high
                                                                                                                                                                                                                                             Register
Cy Control Register
                       Interrupt
             the
                                                                                                                       not
                                                                                                            CLK32 low
             new
                                                                                                             high, go back
32 low level
                                                                                                                                                                                   Mask register
                                                                                                                                                                                                                                 Register
                                                                                                                                                                                                                                                                     frequency
            Mask Register frequency
                                                                                               go back
                                                                                                                                    level
                                                                                                                                               source
```

#### **Programming Considerations** When Changing Frequencies

The following information is provided to assist the user in programming the MC68VZ328

- When programming the SYSCLK frequency, ensure that it does not exceed 33.161216 MHz at any
- approximately 16 MHz. Since the PRESC1 and PRESC2 bits are set to %1 by default, the DMACLK output is

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- should not be changed during system operation. overall system timing (except for CLK32). Therefore, once a PLLCLK frequency is selected, it SYSCLK for bit-rate generation, changing the PLLCLK frequency will also change SYSCLK and Because most of the modules--such as the UART, SPI, general-purpose timers, and PWM-—use the
- startup time is not a factor PLLCR. Unlike the initial power-up sequence, the crystal oscillator is already on, so the crystal output (PLLCLK) is available after a delay determined by the setting in the WKSEL field of more details. When the MC68VZ328 is awakened from sleep mode by a wake-up event, the PLL PLL control register, which places the chip in sleep mode. See Section 4.5.1.4, "Sleep Mode," for To reduce power consumption, the output of the PLL can be disabled using the DISPLL bit in the



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# CGM Programming Model Freescale Semiconductor, Inc.

## 4.4 CGM Programming Model

This section describes the two registers that enable and control the frequency of the CGM clocks.

#### 4.4.1 PLL Control Register

each bit and field in the register are described in Table 4-2. DMACLK. It also enables the output of the PLL and clock out/Port F pin 2 (CLKO/PF2). The settings for The PLL control register (PLLCR) controls the frequency selection of the LCDCLK, SYSCLK, and

#### **PLLCR** RESET TYPE 15 BH 0 4 0 ₹ LCDCLK SEL 0 ₹ 0 10 ₹ SYSCLK PLL Control Register ₹ 9 0 SEL ₹ 0 PRESC1 PRESC2 CLKEN ₹ DISPLL ₹ 0 0xFFFFF200 0 ₹ WKSEL 0 BH

#### Table 4-2. PLL Control Register Description

Name	Description	Setting
Reserved Bits 15–14	Reserved	These bits are reserved and should be set to 0.
LCDCLK SEL Bits 13–11	LCD Clock Select—This field controls the divide ratio used by the LCD clock divider to	000 = DMACLK ÷ 2. 001 = DMACLK ÷ 4.
	convert DMACLK to LCDCLK. This field can be changed at any time.	010 = DMACLK ÷ 8. 011 = DMACLK ÷ 16. 1xx = DMACLK ÷ 1 (%100 after reset).
SYSCLK SEL Bits 10-8	System Clock Select—This field controls the divide ratio used by the SYSCLK divider to	000 = DMACLK ÷ 2. 001 = DMACLK ÷ 4.
	be changed at any time.	010 = DWACLK ÷ 8. 011 = DMACLK ÷ 16. 1xx = DMACLK ÷ 1 (%100 after reset).
PRESC1 Bit 7	Prescaler 1 Select—This bit selects the divide ratio of the prescaler 1.	$0 = PLLCLK \div 1$ . $1 = PLLCLK \div 2$ (default).
Reserved Bit 6	Reserved 20	This bit is reserved and should be set to 0.
PRESC2 Bit 5	Prescaler 2 Select—This bit selects the divide ratio used by the prescaler 2 to divide the output of prescaler 1, producing DMACLK. This field can be changed at any time.	0 = PR1CLK ÷ 1. 1 = PR1CLK ÷ 2 (default).
CLKEN Bit 4	Clock Enable—This bit enables the buffered output of the SYSCLK at the CLKO/PF2 pin when bit 2 of the PFSEL register is also cleared.	0 = CLKO enabled. 1 = CLKO disabled (default).

Name	Description	Setting
DISPLL Bit 3	<b>Disable PLL</b> —This bit, when set, disables the output of the PLL, placing the chip in sleep mode, its lowest power state.	0 = PLL enabled (default). 1 = PLL disabled.
Reserved Bit 2	Reserved	This bit is reserved and should be set to 0.
WKSEL Bits 1–0	Wake-up Clock Select—This field selects the delay of the PLL output from the initiation of the wake up until an output is available. Since the delay time is calculated by counting CLK32 cycles, the frequency of the crystal oscillator will determine the amount of delay that each setting produces.	See Table 4-3 for delay settings.

Г						
ARCHI	1	10	01	00	Bits 1–0	
ARCHIVED BY FREESCALE	96	64	48	32	CLK32 Periods	I dbie 4-5. W
SCALE	2.93 (default)	1.953	1.465	0.976	Delay in Milliseconds (32.768 kHz)	WKSEL Fleid (FLECK) Delay Settings
	2.500 (default)	1.667	1.250	0.833	Delay in Milliseconds (38.4 kHz)	Serings

# Introduction to the Power Etraesscale Semiconductor, Inc.

## 4.4.2 PLL Frequency Select Register

contains the write-protect bit for the QC and PC counters and the CLK32 status bit. Although PLLFSR field in the register is described in Table 4-4 register can be accessed in bytes, it should always be written as a 16-bit word. The settings for each bit and The PLL frequency select register (PLLFSR) controls the two dividers of the dual-modulus counter. It also

PLLFS	FSR		D	LL Frequency Select I	eque	ncy (	Sele	Ω R	Register		*		0	×(F	Ŧ	F202
	BIT 15	14	13	12	1	10	9	œ	7	6	Ŋ	4	ω	2	_	ВІТ 0
	CLK32	PROT				ည္က							РС			
TYPE	Г	rw*			W	W	W	W	V	W	w w w w	W	W	W	W	۲W
7 7 7	0	0	0	0	0	0	_	_	0	_	0	0	0	_	_	_

U

Table 4-4. PLL Frequency Select Register Settings

Name	Description	Setting
<b>CLK32</b> Bit 15	Clock32 Status—This read-only bit indicates the status of the CLK32 clock signal. The bit switches with each cycle of the CLK32 clock.	0 = CLK32 low. 1 = CLK32 high.
PROT Bit 14	Protect Bit—This bit write protects the QC and PC fields of the PLLFSR. After this bit is set by software, the register is write protected until a reset clears this bit.	0 = PLLFSR is not protected. 1 = PLLFSR is write protected.
Reserved Bits 13–12	Reserved	These bits are reserved and must remain at their default value.
<b>QC</b> Bits 11–8	<b>Q Counter</b> —This field contains the Q value that is used by the PLL to produce the PLLCLK.	Field value range is 1 ≤ Q ≤ 14.
PC Bits 7–0	P Counter—This field contains the P value that is used by the PLL to produce the PLLCLK.	Field value range is P ≥ Q + 1.

#### Introduction to the **Power Control Module**

can disable the CPU clock or apply the clock in bursts. When the MC68VZ328 is in one of these immediately enabled, allowing the CPU to service the request. The DMA controller is not affected by the than any component in the MC68VZ328, so to conserve power while the CPU is relatively idle, the PCM The purpose of the power control module (PCM) is to optimize the power consumption of the FLX68000 CPU by turning the CPU off for a programmed number of clock pulses. The CPU consumes more power PCM having full access to the bus while the CPU is idle, keeping the LCD screen refreshed. reduced-power modes, it is restored to normal operation by a wake-up event. When this occurs, the clock is



<sup>\*</sup>This bit can be set by software but is cleared only by reset.

Freescale Semiconductorontose Power Control Module

#### **Operating the PCM**

sleep mode. It is entered by setting the disable PLL (DISPLL) bit in the PLLCR, which disables the PLL and thus disables every clock signal in the CGM except CLK32. Section 4.5.1.1, "Normal Mode," through controls the burst width of the CPUCLK signal to the CPU. If the burst width of the CPU clock is reduced PCM is off. The MC68VZ328 enters burst mode when the PCM is enabled. In burst mode, the PCM Section 4.5.1.4, "Sleep Mode," give detailed information about each of the four power modes. to zero, CPUCLK is disabled and the MC68VZ328 is in doze mode. The lowest power mode setting is The power control module has four modes of operation: normal, burst, doze and sleep. In normal mode, the

#### **Normal Mode**

maximum power. This is normal mode After reset, the PCM is disabled, the CPU clock runs continuously, and the MC68VZ328 consumes

#### **Burst Mode**

Setting the PCEN bit in the power control register (PCTRL) enables the PCM, causing the clock burst and 100 percent in incremental steps of 3 percent. effectively produces a system clock with a variable burst width (and power dissipation) between 3 percent programmed for burst widths of any value between zero thirty-firsts and thirty-one thirty-firsts. This burst width to a lower value, and the clock is applied to the CPU in bursts. The burst-width register can be (one thirty-first of a cycle). Initially, the burst width is set to 100 percent. Software can then change the width of the CPU clock to be under the control of the PCTLR WIDTH settings in increments of 3 percent

continuous CPU clock. It is the responsibility of the wake-up service routine to reenable the PCM. When the PCM is enabled, if a wake-up event is received, the PCM is immediately disabled, restoring the

#### Doze Mode

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MC68VZ328 to enter doze mode. As with burst mode, the CPUCLK is immediately enabled when it Setting the width field of PCTLR to %00000 reduces the burst width of the CPU clock to zero, causing the event or hardware reset will reenable it. %00000, putting the CPU back into doze mode. Once the CPU is placed in doze mode, only a wake-up receives a wake-up event. At the end of the service routine, the PCM can be reenabled with a width of

#### NOTE:

affected by the PCM. events. The peripheral devices, including the LCD controller, are not possible moment, but allows the CPU to immediately respond to wake-up writing 0x80 into the PCTLR. This disables the CPU clock at the earliest mode until CPU action is not needed and then to enter doze mode by The most effective power-control strategy is to run the CPU in normal



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# Introduction to the Power Edicale Semiconductor, Inc.

#### 4.5.1.4 Sleep Mode

activate the PLL, and the system clock starts operating after a delay determined by the WKSEL setting in the PLLCR register. Only the 32 kHz clock works to keep the real-time clock operational. Wake-up events the PLLCR. the CLK32. The output of the PLL in the CGM is disabled in sleep mode through setting the DISPLL bit in Unlike burst or doze mode, sleep mode disables all of the clocks in the MC68VZ328 with the exception of

Other events that occur during sleep mode include:

- All Address Bus signals are in the active state of the last bus cycle
- All data bus pins (D15-D0) are individually pulled up with 1-megaohm resistors
- in sleep mode. If CLK32 is selected as the clock source, the general-purpose timer operates even while the PLL is
- The RTC interrupt status register can post interrupts while the system clock is in doze or sleep mode

## **CGM Operation During Sleep Mode**

divider chain of the CGM. The CPU executes an interrupt service routine for the level of the wake-up determined by the WKSEL setting in the PLLCR, the PLLCLK begins, as do as the rest of the clocks in the shutting the PLL down, make sure that all peripheral devices are prepared for shutdown. The PLL shuts execute the stop instruction. When a wake-up event occurs, the PLL is enabled, and after a delay down 30 clock cycles of SYSCLK after the DISPLL bit is set in the PLLCR, allowing sufficient time to frequency. The difference is that the system can be awakened only by a wake-up event or reset. Before Shutting down the PLL to place the system in sleep mode is similar to the process used to change the

After the rte instruction in the wake-up service routine, the CPU returns and starts execution on the instruction following the stop instruction. Example 4-2 illustrates a typical shutdown sequence. It assumes that all peripherals have been shut down before the PLL is stopped.

Example 4-2. Shutdown Example

```
ori.b
                                                                                                                            IRQMASK equ wake-up_mask_level
                          interrupt
                                                                                  #IRQMASK
                                                                                                  #$8, PLLCONTROL+1
                          shuts down here
has reacquired lock a
pt service occurs here
                                           and
                                                                                  ;disable the PLL
;stop, enable wal
                                         SYSCLK is stable
 ; the
 system
                                                                                  enable wake-up
 z-
operating
                                                                                                  (in 30 clocks)
                                                                                   events
```

#### 4.5.3 Burst Mode Operation

through to the clock control until the CPU clock's time slot has expired and is to be disabled. At that time SYSCLK input is unaffected by burst-width control appearing as CPUCLK from the clock control. When a to the DMA controller is asserted, allowing the DMA controller complete access to the bus. the clock control requests the bus from the CPU. After the bus is granted, the CPUCLK stops. A bus grant value has been placed in the width field of the PCTLR, the burst-width control allows the SYSCLK signal Figure 4-4 on page 4-13 shows a simplified block diagram of the PCM. When operating at 100 percent, the



# Freescale Semiconductorontose Power Control Module

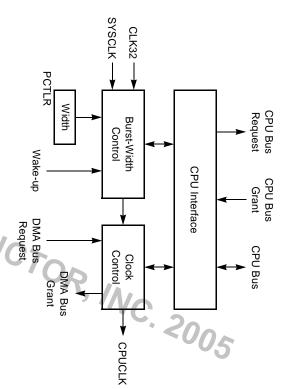


Figure 4-4. Power Control Module Block Diagram

If a wake-up event occurs while CPUCLK is disabled, the PCM is disabled and CPUCLK is immediately (master clock to all peripherals) is continuously active. access is in progress, the CPU will wait until the DMA controller has completed its access before servicing the wake-up routine. Note that the LCD DMA controller has access to the bus at all times and the SYSCLK restored, allowing the CPU to process the event. The DMA controller always has priority, so if a DMA

mode. When a wake-up event occurs, CPUCLK immediately returns to 100 percent so the CPU can service time, making the CPU active about 10 percent of the time. The remainder of the time, the CPU is in doze 00011. The clock bursts are applied at a burst width of three thirty-firsts, or approximately at 10 percent on represents 31 periods of CLK32, or approximately 1 ms. In this example, the width setting in the PCTLR is Figure 4-5 illustrates how the PCM operates. As described previously, a width setting of %11111 the wake-up event interrupt.

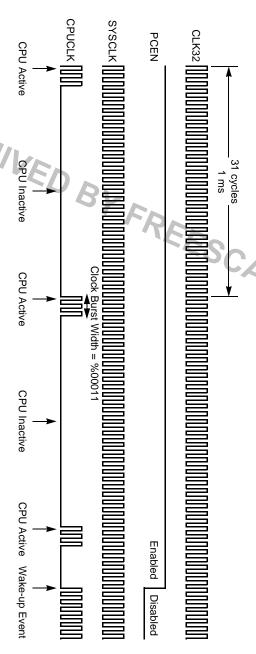


Figure 4-5. Power Control Operation in Burst Mode

# Introduction to the Power Ethers scale Semiconductor, Inc.

#### 4.5.4 Power Control Register

signal is applied to the CPU. The settings for each bit and field in the register are described in Table 4-5. The power control register (PCTLR) enables the power control module and determines when the CPUCLK

PCTLR		Pov	ver Con	Power Control Register	ster	:0	0x(FF	)FFF207
	BIT 7	თ	Сī	4	ω	2	_	BIT 0
	PCEN				C	WIDTH		
TYPE	ſW			۲W	W	W	W	rw
D II O II T	0	0	0	_	#/	_	_	_
7.00				0x	0x1F			

Table 4-5. Power Control Register Description

9		
Name	Description	Setting
PCEN Bit 7	Power Control Enable—This bit controls the operation of the power control module. While this bit is low, the CPU clock is on continuously. When this bit is high, the pulse-width comparator presents the clock to the CPU in bursts or disables it. When this bit is high, a masked interrupt can disable the power control module.	0 = Power control is disabled (default). 1 = Power control is enabled.
Reserved Bits 6–5	Reserved <b>S</b>	These bits are reserved and should remain set to 0.
WIDTH Bits 4-0	Width—This field controls the width of the CPU clock bursts in increments of one thirty-first. While this bit is set to 1 and the PCM is enabled, the clock is applied to the CPU in burst widths of one thirty-first (3 percent). When the width field is 0x1F, the clock is always on, and when it is 0, the clock is always off. You can immediately wake it up again without waiting for the PLL to reacquire lock. The contents of this field are not affected by the PCEN bit. When an interrupt disables the power control module, these bits are not changed.	00000 = 0/31 clock burst width. 00001 = 1/31 clock burst width. 00010 = 2/31 clock burst width.



### Freescale Semiconductor, Inc.

#### System Control Chapter 5



- Access permission from the internal peripheral registers
- Address space of the internal peripheral registers
- Bus time-out control and status (bus error generator)

## System Control Operation

cleared, the on-chip peripheral registers appear only at the top of the 4 Gbyte address range starting at reset. The DMAP bit in the system control register disables double mapping in a 32-bit system. If this bit is mapped beginning at location 0xFFFFF000 (32-bit) or 0xXXFFF000 (24-bit, where XX is "don't care") on 0xFFFFF000. The on-chip resources use a reserved 4,096-byte block of address space for their registers. This block is

The system control register provides control of system operation functions such as bus interface and watchdog protection. The system control register contains status bits that allow exception handler code to provide system protection. The bus time-out monitor generates a bus error when a bus cycle is not terminated by the DTACK signal after 128 clock cycles have elapsed. interrogate the cause of both exceptions and resets. The bus time-out monitor and the watchdog timer

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## **Bus Monitors and Watchdog Timers**

system control register. The BETO bit in the system control register is set after a bus time out, which may asserted until AS is deasserted. The bus error time-out logic consists of 1 control bit and 1 status bit in the The bus error time-out logic consists of a bus time-out monitor that, when enabled, begins to count clock cycles as the internal  $\overline{AS}$  pin is asserted for internal or external bus accesses. The deassertion of  $\overline{AS}$ indicate a write-protect violation or privilege normally terminates the count, but if the count reaches terminal count before AS is deasserted, BERR is

terminal count. The watchdog timer is enabled at reset. The watchdog timer resets the MC68VZ328 if it is enabled and not cleared or disabled before reaching



#### 5.2 Programming Mode

the other registers associated with its operation. The following sections provide detailed programming information about the system control register and

### 5.2.1 System Control Register

register display. The settings for the bits in the register are listed in Table 5-1. 68000's user mode if the SO bit is set to 1. The bit assignments for the register are shown in the following (where XX is "don't care") after reset. The SCR and all other internal registers cannot be accessed in the The 8-bit read/write system control register (SCR) resides at the address 0xFFFFF000 or 0xXXFFF000

-	В П О П П	TYPE			SCR
	0	W	ВЕТО	BIT 7	
	0	rw	WPV	6	Sys
	0	TW.	PRV	5	tem Cor
O/ 0x1C	4/	W	BETEN	4	System Control Register
C	_	W	so	З	ster
	_	W	DMAP	2	
	0			1	0x(FF)
	0	W	WDTH8	BIT 0	FF)FFF000

Table 5-1. System Control Register Description

Name	Description	Setting
вето	Bus Error Time Out—This status bit indicates	0 = A bus-error-timer time out did not occur.
Bit 7	whether or not a bus-error-timer time out has occurred. When a bus cycle is not terminated by	1 = A bus-error-timer time out has occurred because an undecoded address space has
	the DTACK signal after 128 clock cycles have elapsed, the BETO bit is set. However, the BETEN bit must be set for a bus error time out to	been accessed or because a write-protect or privilege violation has occurred.
	occur. This bit is cleared by writing a 1 (writing a 0 has no effect).	
WPV	Write-Protect Violation—This status bit indi-	0 = A write-protect violation did not occur.
Ç	If a write-protect violation occurs and the BETEN	/ with process violation has occarious
	nate. The BETEN bit must be set for a bus error	
	tion. This bit is cleared by writing a 1 (writing a 0 has no effect).	
<b>PRV</b> Bit 5	Privilege Violation—This status bit indicates that if a privilege violation occurs and the BETEN	<ul><li>0 = A privilege violation did not occur.</li><li>1 = A privilege violation has occurred.</li></ul>
	bit is not set, the cycle will not terminate. The BETEN bit must be set for a bus error exception to occur during a privilege violation. This bit is	
BETEN	Bus Error Time-Out Enable—This control bit	0 = Disable the bus error timer.
Bit 4	enables the bus error timer.	1 = Enable the bus error timer.
SO Bit 3	<b>Supervisor Only</b> —This control bit limits on-chip registers to supervisor accesses only.	0 = User and supervisor mode. 1 = Supervisor-only mode.

	WDTH8 Bit 0	Reserved Bit 1	DMAP Bit 2	Name	
ARCHIVED BY FREESCALE SEMICONDUCT	<b>8-Bit Width Select</b> —This control bit allows the D[7:0] pins to be used for Port A input/output.	Reserved	<b>Double Map</b> —This control bit controls the double-mapping function.	Description	Table 5-1. System Control Register
	0 = Not an 8-bit system. 1 = 8-bit system.	This bit is reserved and reads 0.	0 = The on-chip registers are mapped at 0xFFFFF000-0xFFFFFFFF.  1 = The on-chip registers are mapped at 0xFFFFF000-0xFFFFFFFF and 0xXXFFFF000-0xXXFFFFFF (XX = "don't care").	Setting	System Control Register Description (Continued)

### 5.2.2 Peripheral Control Register

signal. The bit assignments for the register are shown in the following register display. The settings for the bits in the register are listed in Table 5-2. This register controls the PWM logical block operation, timer TIN/TOUT signal, and UART UCLK

PCR		77	eriphera	Peripheral Control Register	egister		0x(FF)	x(FF)FFF003
	ВІТ 7	6	5	4	3	2	1	ВІТ 0
				UCLK	P[1:0]		η.	T[1:0]
TYPE				۲W	ΓW	W	ſW	W
D П О П	0	0	0	0	0,	0	0	0
Х П П				0x	0x00			

Table 5-2. Peripheral Control Register Description

Name	Description	Setting
Reserved Bits 7–5	Reserved	Do not use these bits.
DCLK Bit 4	UART Clock Pin Configuration—When UCLK of UART 1 and UART 2 is configured to output signal, this bit selects UART 1's or UART 2's UCLK for UCLK pin output. When UCLK of UART 1 and UART 2 is configured as input, this bit is "don't care," and UCLK pin is an input signal.	0 = UCLK pin is connected to UART 1. 1 = UCLK pin is connected to UART 2.
<b>P[1:0]</b> Bits 3–2	<b>PWM Outputs Logic Operation</b> —These bits select the logical combination for final PWM pin output.	00 = 8-bit PWM out only (default). 01 = 16-bit PWM out only. 10 = Logic OR of both PWM outputs. 11 = Logic AND of both PWM outputs.
<b>T[1:0]</b> Bits 1–0	TIN/TOUT Signal Configuration—These 2 bits are used to configure the external TIN/TOUT signal when pin PB6/TIN/TOUT is selected as TIN/TOUT function. For detailed information on using this function, see Section 12.1.4, "TOUT/TIN/PB6 Pin," on page 12-3.	00 = TIN/TOUT is connected to Timer 1. 01 = TIN/TOUT is connected to Timer 2. 10 = Timer 2 OUT -> Timer 1 IN; TIN -> Timer 2 (DIR6 = 0), or TOUT -> Timer 1 (DIR6 = 1). 11 = Timer 1 OUT -> Timer 2 IN; TIN -> Timer 1 (DIR6 = 0), or TOUT -> Timer 2 (DIR6 = 1).



**Programming Model** 

#### 5.2.3 ID Register

in the following register display. The settings for the bits in the register are listed in Table 5-3. This 32-bit read-only register shows the chip identification. The bit assignments for the register are shown

y	Setting	S							iption	Description					16	Name
						tion	scrip	er De	egist	. ID R	Table 5-3. ID Register Description	Та				
•	(	•	•	(	•	•	•	00000	) )	•	•	•	•	•	•	RESET
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
г	7	7	7	7	7	<b>-</b>	r	7	٦	Г	Г	Г	г	٢	r	TYPE
							J	SWID	S\							
BIT 0	_	2	ω	4	5	6	7	8	9	10	11	12	13	14	BIT 15	
						4	O									
						٠١,	P	0x5600	0x5							700
0	0	0	0	0	0	0	0	0	_	_	0	_	0	_	0	D F F F H
¬	¬	¬	¬	¬	¬	Ą	7	¬	¬	¬	¬	¬	¬	¬	7	TYPE
			MASKID	MAS	)	C					D	CHIPID				
17 BIT 16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	BIT 31	
0x(FF)FFF004	)FF	×(FF	0		300			ē	egist	ID Register						IDR

	<b>SWID</b> Bits 15–0	MASKID Bits 23–16	CHIPID Bits 31–24	Name	
ARCHIVED BY FREES	Software ID—This field contains the custom software ID. It is normally "0000."	Maskset ID Field—This field contains the maskset number for the silicon.	<b>Chip ID Field</b> —This field contains the chip identification number for the DragonBall series MPU.	Description	
	See description	See description	See description	Setting	

### I/O Drive Control Register

This register controls the driving strength of all I/O signals. By default, all pins are defaulted to 4 mA ot need ing

	TYPE			IODCR	display. The settings for the bits in the register are listed in Table 5-4.	high-current driving for power saving. The bit assignments for the register are shown in the following	driving current. After reset, system software should select 2 mA driving for those signals that do not need	This register condons the driving sucrigar of an 100 signats. By default, an plus are defaulted to 4 max
			BIT 15 14 13		The setti	ent driv	urrent. A	SIET COTT
0			14		ngs for	ing for	After re	TOTS UT
0			13		the bit	power	set, sys	OTTAIN C
_	V	AB	12 11 10 9 8 7 6 5 4 3 2 1 BITO	<u> </u>	s in the	saving.	tem sof	g sucm
_	W	DB CB PM PK PJ PG PF PE PD PC PB PA	11	I/O Drive Control Register	registe	The bi	îtware s	Sm or
_	TW TW TW TW TW TW TW TW TW	СВ	10	e Co	r are li	t assign	should	THE TO 3
_	V	PM	9	ntrol	sted i	nmeni	select	Signal
_	¥	PK	8	Rec	n Tab	ts for	2 m/	5. Ly
7	WI	PJ	7	jiste	le 5-4	the re	\ driv	deran
_	W	PG	6	<u>,                                     </u>	2	gister	ing fc	ш, ап
_	₹	PF	5	` <	<i>(0)</i>	are s	r thos	спп
_	¥	PE	4			hown	e sig	are as
_	V	PD	သ	0x		in th	nals ti	Tauto
_	8	PC	2	(FF)		e foll	hat do	כת וה
_	₹	PB	_	Ŧ		gniwc	not	4 1117
_	₹	PA	BIT 0	0x(FF)FFF008		09	need	•

	「able 5-4.
	<u></u>
	Drive (
	Control I
,	Regis
	ter [
	Description

	PM-PA Bits 9-0	CB Bit 10	<b>DB</b> Bit 11	<b>AB</b> Bit 12	Reserved Bits 15–13	Name
ARCHIVED BY FREE	Port M to Port A Group I/O Drive Control—Each bit controls the drive current for the lines in the respective port.	Control Bus Signals—Only those signals or functions not multiplexed with GPIO are controlled by this bit.	Upper Data Bus Signals I/O Drive Control—The lower data bus is controlled by the PA bit.	Address Bus Signals I/O Drive Control—It should be noted that A[23:20] are controlled by the PF bit.	Reserved	Description
	0 = I/O drive current for each pin is 2 mA. 1 = I/O drive current for each pin is 4 mA.	0 = I/O drive current for each pin is 2 mA. 1 = I/O drive current for each pin is 4 mA.	0 = I/O drive current for each pin is 2 mA. 1 = I/O drive current for each pin is 4 mA.	0 = I/O drive current for each pin is 2 mA. 1 = I/O drive current for each pin is 4 mA.	Do not use these bits.	Setting



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#### Chapter 6 Chip-Select Logic

information for controlling its operation. This chapter describes the chip-select logic's function and operation and provides programming <sup>1</sup>NC. 2005

#### Overview of the CSL

groups of twowhich are used to select external devices on the address and data bus. The signals are arranged in four The MC68VZ328 microprocessor contains eight general-purpose, programmable chip-select signals, CSA[1:0], CSB[1:0], CSC[1:0], and CSD[1:0].

mode all the addresses are mapped to CSA0 until such time that the group base address A is programmed the chip-select register. CSA0 does not decode globally and is only asserted when decoded from the programming information in and the chip-select enable (EN) bit is set in the appropriate chip-select register. From that point forward, CSA0 is a special-purpose chip-select signal, which is the boot device chip-select. After reset, in normal

Section 6.3.3, "Chip-Select Registers," in this chapter. programmed as row address strobe  $(\overline{RAS0}/\overline{RAS1})$  and column address strobe  $(\overline{CAS0}/\overline{CAS1})$  for the Group C (CSC0/CSC1) and Group D (CSD0/CSD1) chip-selects are unique in that they can also be DRAM interface. For details, refer to Section 7.3.2, "DRAM Control Register," on page 7-14 and

on cost and availability. Up to four different classes of devices and memory can be used in a system a programmable number of wait states. This feature saves board space that would otherwise be used as shown in Table 6-1 on page 6-2. of ROM, SRAM, flash memory and DRAM (EDO RAM, Fast Page Mode, or synchronous) are supported without the need for external decode or wait-state generation logic. Specifically, 8- or 16-bit combinations cycle-termination logic. Using CDL, the system designer can adopt a flexible memory configuration based Each memory area can be defined as an internally generated cycle-termination signal, called DTACK, with



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Table 6-1. Chip-Select and Memory Types

Chip-Select Signal	Memory Supported
CSA0	ROM, SRAM, flash memory chip
CSA1	ROM, SRAM, flash memory chip
CSB0	ROM, SRAM, flash memory chip
CSB1	ROM, SRAM, flash memory chip
CSC0/RAS0	DRAM, ROM, SRAM, flash memory chip-select
CSC1/RAS1	DRAM, ROM, SRAM, flash memory chip-select
CSD0/CAS0	DRAM, ROM, SRAM, flash memory chip-select
CSD1/CAS1	DRAM, ROM, SRAM, flash memory chip-select

memory sizes available on the market and apply to the registers CSB, CSC, and CSD. The CSA register size of the chip-select can be selected from a set of predefined ranges (32K, 64K, 128K, 256K, 512K, address match is described in terms of a group base address register and a chip-select register. The memory software without the necessity of programming a chip-select mask register. primarily supports ROM, which is usually 128K to 16 Mbyte. Using this scheme, it is easy to design The signals are asserted externally shortly after the internal Address Strobe (AS) signal goes low. The The basic chip-select model allows the chip-select output signal to assert in response to an address match. 1 Mbyte, 2 Mbyte, 4 Mbyte, 8 Mbyte, or 16 Mbyte). These memory ranges represent the most popular

The chip-select can be programmed to allow read-only or read/write accesses. Other parameters that can be DTACK signal is automatically generated for the chip-select logic. programmed include the number of wait states (from 0 to 13), data bus size selection, and whether a

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Freescale Semiconductor, Inc.

### 6.2 Chip-Select Operation

on a 64K boundary. Each chip-select is programmable, and the registers have read/write capability so that the programmed values can be read back. byte size of the matching block must be a power of two and the base address must be an integer multiple of base address and address mask registers are used in the compare logic to generate an address match. The A chip-select output signal is asserted when an address is matched and after the AS signal goes low. The Therefore, an 8K block size must begin on an 8K boundary, and a 64K block size can only begin

#### NOTE:

acknowledge (Function Code 7) cycles. The chip-select logic does not allow an address match during interrupt

#### **6.2.1 Memory Protection**

that control the crucial system data are usually programmed as supervisor-only and read-only so they can The chip-select range of the four chip-selects can be programmed as read-only or read/write. Chip-selects be protected from system misuse (for example, a low battery). However, a certain area of this



# Freescale Semiconductor, Inc. Chip-Select Operation

shown in Figure 6-1. This area can be defined by programming the UPSIZ bits in the CSB, CSC, and CSD chip-select-controlled area can be programmed as read/write, which provides optimal memory use, registers to between 32K and the entire chip-select area.

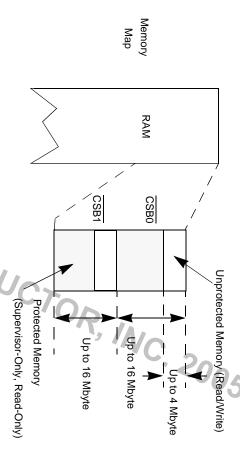


Figure 6-1. Size Selection and Memory Protection for CSB0 and CSB1

### Programmable Data Bus Size

system. The internal data bus is 16 bits wide. All internal registers can be read or written in a zero data bus width and connect to the D[7:0] pins. This balances the load of the two data bus halves in an 8-bit contiguous address locations (unused bytes on empty addresses), use a chip-select configured to a 16-bit next. A0 should be ignored in 16-bit data bus cycles even if only the upper or lower byte is being read or wait-state cycle. written. For an external peripheral that only needs an 8-bit data bus interface and does not require asserted until the end of the second 8-bit cycle. In this case, only the external CPU data bus upper byte 8-bit memory space, then two 8-bit cycles will occur. However, the address and data strobes remain memory devices can be mixed on a 16-bit data bus system. If the CPU performs a 16-bit data transfer in an Each chip-select can be configured to address an 8-or 16-bit space. Both 16- and 8-bit contiguous address (D[15:8]) is used, and the least significant bit of the address (A0) increments automatically from one to the

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ranges. The initial bus width for the boot chip-select can be selected by placing a logic 0 or 1 on the BUSW assumed to be a 16-bit device. This results in a single access performed for a 16-bit transfer. If it is applied in any given system. All external accesses that do not match one of the chip-select address ranges are field of the chip-select option register enables 16- and 8-bit data bus widths for each of the 16 chip-select Except for CSA0 and EMUCS, all chip-select signals are disabled by default. The data bus width (BSW) to an 8-bit port, the port is accessed every other byte. pin at reset to specify the width of the data bus. This allows a boot EPROM of the data bus width to be used

fetch the reset vector and execute the initialization code, which should set up the chip-select ranges space (0xFFFFF000 to 0xFFFFFFFF). This ensures that a chip-select to the boot ROM or EPROM will The boot chip-select is initialized from reset to assert in response to any address except the on-chip register

determined by the state of BUSW. The other chip-selects are initialized to be nonvalid, so they will not assert until they are programmed and the EN bit is set in the chip-select registers bits wide. At reset, the data bus port size for CSA0 and the data width of the boot ROM device are A logic 0 on the BUSW pin sets the boot device's data bus to be 8 bits wide, and a logic 1 sets it to be 16



## **Overlapping Chip-Select Registers**

**Programming Model** 

Freescale Semiconductor, Inc.

Unused chip-selects must be disabled. Map them to an unused space, if possible. Do not program group address and chip-select registers to overlap, or the chip-select signals will overlap

When the CPU tries to write to a read-only location that has already been programmed, the chip-select and function is enabled. DTACK signals will not be generated internally. BERR will be asserted internally if the bus error time-out

#### NOTE

acknowledge cycles. The chip-select logic does not allow an address match during interrupt

#### **Programming Model**

EN bit is set in the corresponding chip-select register. The only exception is the CSA0 signal, which is the memory. Chip-selects do not operate until the register in a particular group of devices is initialized and the The chip-select module contains registers that are programmed to control external devices, such as boot device chip-select.

# Chip-Select Group Base Address Registers

and so on. It cannot be set at  $0 \times 1$  Mbyte,  $0 \times 2$  Mbyte,  $0 \times 3$  Mbyte,  $0 \times 5$  Mbyte, and so on the group. For example, if CSA1 and CSA0 are each assigned a 2 Mbyte memory space, the CSGBA register must be set in a 4 Mbyte space boundary, such as system address  $0 \times 0$ ,  $0 \times 4$  Mbyte,  $0 \times 8$  Mbyte The chip-select base address must be set according to the size of the corresponding chip-select signals of The upper 15 bits of each base address register selects the starting address for the chip-select address The GBAx field is compared to the address on the address bus to determine if the group is decoded

CSGB	>		$\mathcal{C}_{L}$	ip-S	Chip-Select Group A Base Address Registe	Grou	Αdr	Base	Adc	ress	Reg	ister		0x(F	FF)FFF10	F100
	BIT 15	14	13	12	11	10	9	8	7	6	5	4	ы	2	1	ВІТ 0
	GB	GB	GB	GB	GB	GB	GB	GB		ВЭ	GB	GB	GB	GB	В	
	í	ŕ	í	í		í	ì	í	í			7117		3	1111	
TYPE	8	₹	V	rw rw	W	₹	₹	W	V	V	V	₹	V	W	₹	
D II O II	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7 6 6				31				0x(	)x0000							

Table 6-2. Chip-Select Group A Base Address Register Description

Name	Description	Setting
GBAx Bits 15–1	<b>Group A Base Address</b> —These bits select the high-order bits (28–14) of the starting address for the chip-select range.	The chip-select base address must be set according to the size of the corresponding chip-select signals of the group.
Reserved Bit 0	Reserved	This bit is reserved and should be set to 0.

CSGBC

Chip-Select Group C

Base Address Register

0x(FF)FFF104

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#### Semiconductor, Inc.

**Programming Model** 

B	
Chip-S	
elect Gro	
)up B Bas	
e Addres	
Chip-Select Group B Base Address Register	
0x(FF)FFF	
)FFF	

7 6	D II O II I	TYPE			CSGBI
	0	V	GB B28	BIT 15	w
	0	₹	GB B27	14	
	0	W	GB B26	13	Chi
	0	W	GB B25		Chip-Select Group B Base Address Register
	0	₹	GB B24	<u> </u>	lect (
	0	V	GB B23	10	Group
	0	V	GB B22		0 B B
0x0000	0	V	GB B21	&	ase
000	0	V	GB B20	7	Addr
	0	V	GB B19	6	ess F
	0	W	GB B18		₹egis
	0	¥	GB B17	4	iter
	0	₹	GB B16	ω	0
	0	₹	GB B15	8	×(FF
	0	₹	GB B14	_	)x(FF)FFF1
	0			0 B	102

Table 6-3. Chip-Select Group B Base Address Register Description

Name Description	าก	Setting
GBBx Group B Base Address—These bits select the high-order bits (28–14) of the starting address for the chip-select range.	These bits select of the starting ange.	The chip-select base address must be set according to the size of the corresponding chip-select signals of the group.
Reserved Reserved Bit 0		This bit is reserved and should be set to 0.

#### 0 0 0 ₹ 0 ₹ 0 ₹ 0 0 0 ₹ 0

RESET

TYPE

## Chip-Select Group C Base Address Register Description

	Reserved Bit 0	GBCx Bits 15–1	Name
ARCHIVE	Reserved 49	<b>Group C Base Address</b> —These bits select the high-order bits (28–14) of the starting address for the chip-select range.	Description
	This bit is reserved and should be set to 0.	The chip-select base address must be set according to the size of the corresponding chip-select signals of the group.	Setting

0

#### **Programming Model** Freescale Semiconductor, Inc.

CSGBD	ВІТ 15	G	D2		TYPE rw	DESET (	700
	3H 15					0	
_	4		D2	7	V	0	
) Hip	13		D2	6	W	0	
-Sel	12	GB	D2	5	W	0	
ect G	1	GB	D2	4	₹	0	
p-Select Group	10	GB	D2	3	8	0	
Ď	9	GB	D2	2	8	0	
Base /	œ	ВЭ	D2	1	V	0	)
Addr	7	ВЭ	D2	0	8	0	
Address	6	GB	7	9	₹	0	
Registe	5	gB	D1	8	W	0	
ster	4	В	<u> </u>	7	V	0	
0	ω	GB	7	6	8	0	
×(FF	2	GB	7	5	₹	0	
;)FFF	_	GB	<u>D</u>	4	₹	0	
FF106	0 BH					0	

Table 6-5. Chip-Select Group D Base Address Register Description

Name	Description	Setting
GBDx Bits 15–1	Group D Base Address—These bits select the high-order bits (28–14) of the starting address for the chip-select range.	The chip-select base address must be set according to the size of the corresponding chip-select signals of the group.
Reserved Bit 0	Reserved	This bit is reserved and should be set to 0.

# Chip-Select Upper Group Base Address Register

chip-select registers by the UGEN bit in the chip-select upper group base address register (CSUGBA). The The default setting for chip-select decoding limits addressing to A28. When the full address decode enable (UGEN) bit is set, it allows full address decoding. Full address decoding is enabled for all four of the fields in this register. The settings for this register are shown in Table 6-6. bit value of the MSB for each of the four chip-select registers can be written into each of the four MSB

CSUGBA	A	C	hip-	Selec	Chip-Select Upper Group Base Address Register	per C	roup	Bas	se Ac	dres	s Re	giste		0x(FF)FFF108	)FFF	<del>-</del> 108	
	BIT 15	14	13	12	12 11	10	9	8	7	6	5	4	3	2	1	BIT 0	
	EN	AG	AGBA[31:29]	29]	E	BG	BGBA[31:29]	29]		ce	CGBA[31:29]	29]		De	DGBA[31:29]	29]	
TYPE	V	₹	₹	8	E	₹	w w	V		V	₹	₹		₹	8	₹	
D D D D D D D D D D D D D D D D D D D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
7 7 6 7				•				0x0000	000								

Table 6-6. Chip-Select Upper Group Base Address Register Description

Name	Description	Setting
UGEN Bit 15	Full Address Decode Enable—This bit enables full address range decoding for all	0 = Ignores A31, A30, and A29. 1 = Decoding includes A31, A30, and A29.
i i	chip-select registers.	
AGBA[31:29]	MSB for Chip-Select A—The upper most sig-	Enter value for bits 31–29 of chip-select regis-
Bits 14–12	nificant bits for chip-select group A base	ter A.
	disabled.	

	<b>DGBA[31:29]</b> Bits 2–0	Reserved Bit 3	<b>CGBA[31:29]</b> Bits 6–4	Reserved Bit 7	<b>BGBA[31:29]</b> Bits 10-8	Reserved Bit 11	Name
ARCHIVED BY FREESCALE SEN	MSB for Chip-Select D—The upper most significant bits for chip-select group D base address. The value will be ignored if UGEN is disabled.	Reserved	<b>MSB for Chip-Select C</b> —The upper most significant bits for chip-select group C base address. The value will be ignored if UGEN is disabled.	Reserved	MSB for Chip-Select B—The upper most significant bits for chip-select group B base address. The value will be ignored if UGEN is disabled.	Reserved	Description
	Enter value for bits 31–29 of chip-select register D.	This bit is reserved and should be set to 0.	Enter value for bits 31–29 of chip-select register C.	This bit is reserved and should be set to 0.	Enter value for bits 31–29 of chip-select register B.	This bit is reserved and should be set to 0.	Setting

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	9

#### 6.3.3 Chip-Select Registers

the external DTACK signal. The settings for the registers are described in Table 6-7 through Table 6-10 on memory type and size of the memory range supported as well as to program the required wait states or use base address register. Each register controls two chip-select signals and can be configured to select the There are four 16-bit chip-select (CSA, CSB, CSC, and CSD) registers for each corresponding chip-select

- - -	D II O II O	TYPE			CSA
	0	V	RO	BIT 15	
	0			14	
	0			13	
	0			12	
	0			11	Chip
	0			10	Sel
	0			9	ect F
0x00B0	0	W	FLASH	8	Chip-Select Register /
	1	W	BSW	7/	er A
	0	₹	_	6	C
	_	rw rw rw rw rw	WS3-1	5	
	_	₹		4	
	0	₹		3	0×
	0	₹	SIZ	2	(FF
	0	8		1	)FF
	0	8	EN	BIT 0	x(FF)FFF110

able 6-7. Chip-Select Register A Description

**SIZ** Bits 3–1

Chip-Select Size—This field determines the memory range of the chip-select. For CSAx

and CSBx, the chip-select size is between 128K and 16 Mbyte. For CSCx and CSDx, the chip-select size is between 32K and 16 Mbyte.

000 = 128K (32K or 8 Mbyte\* for CSCx and CSDx).
001 = 256K (64K or 16 Mbyte\* for CSCx and CSDx).
010 = 512K (128K for CSCx and CSDx).
011 = 1 Mbyte (256K for CSCx and CSDx).
100 = 2 Mbyte (512K for CSCx and CSDx).
101 = 4 Mbyte (1 Mbyte for CSCx and CSDx).
110 = 8 Mbyte (2 Mbyte for CSCx and CSDx).
111 = 16 Mbyte (4 Mbyte for CSCx and CSDx).

DSIZ3 bit in the chip-select control register to be set. \* Note: Large DRAM size selection requires the

Chip-Select Enable

Name

	Bit 0
ARCHIVED BY FREESCALE SEMICONDUC	enables each chip-select.
NDUC	1 = Enabled.



7	D II O II I	TYPE		
	0	V	RO	BIT 15
	0	W	SOP	14
	0	W	ROP	13
	0	W	UP.	12
	0	<	UPSIZ	11
	0			10
	0			9
0x000C	0	W	FLASH	8
O	0	V	BSW	7
	0	₹		6
<	0	M	WS3-1	5
	0	₹		4
	0	¥		ω
	0	₹	SIZ	2
	0	₹		_
	0	\$	EN	8 0

able 6-8. Chip-Select Register B Description

Name	Description	Setting
RO Bit 15	Read-Only—This bit sets the chip-select to read-only. Otherwise, read and write accesses are allowed. A write to a read-only area will generate a bus error if the BETEN bit of the SCR is set. See Section 5.2.1, "System Control Register," on page 5-2 for more information.	0 = Read/write. 1 = Read-only.
SOP Bit 14	Supervisor-Use-Only Protected Memory Block—This bit sets the protected memory block to supervisor-only; otherwise, both supervisor and user accesses are allowed. Attempts to access the supervisor-only area result in a bus error if the BETEN bit of the SCR is set. See Section 5.2.1, "System Control Register," on page 5-2 for more information.	0 = Supervisor/user. 1 = Supervisor-only.
ROP Bit 13	Read-Only for Protected Memory Block—This bit sets the protected memory block to read-only. Otherwise, read and write accesses are allowed. If you write to a read-only area, you will get a bus error.	0 = Read/write. 1 = Read-only.
<b>UPSIZ</b> Bits 12–11	Unprotected Memory Block Size—This field determines the unprotected memory range of the chip-select.	00 = 32K. 01 = 64K. 10 = 128K. 11 = 256K.
Reserved Bits 10-9	Reserved 2	These bits are reserved and should be set to 0.
FLASH Bit 8	Flash Memory Support—When enabled, this bit provides support for flash memory by forcing the LWE/UWE signal to go active after chip-select.  Note: This bit is used for expanded memory size for CSD when the DRAM bit in the CSD register is enabled.	0 = The chip-select and LWE/UWE signals go active at the same clock edge. 1 = The chip-select signal goes low 1 clock before LWE/UWE.
BSW Bit 7	Data Bus Width—This bit sets the data bus width for this chip-select area.	0 = 8 bit. 1 = 16 bit.

Description	
Setting	•
	l

	Bit 0	WS3-1 Bits 6-4 Bits 3-1	Name
ARCHIVED BY FREESCAL	Chip-Select Enable—This write-only bit enables each chip-select.	Wait State—This field determines the number of wait states added before an internal DTACK signal is returned for this chip-select.  Note: When using the external DTACK signal, you must configure the BUSW/DTACK/PGO pin.  Chip-Select Size—This field determines the memory range of the chip-select. For CSAx and CSBx, the chip-select size is between 128K and 16 Mbyte. For CSCx and CSDx, the chip-select size is between 32K and 16 Mbyte.	Description
	0 = Disabled. 1 = Enabled.	000 = 0 + WS0 wait states. 001 = 2 + WS0 wait states. 010 = 4 + WS0 wait states. 011 = 6 + WS0 wait states. 101 = 10 + WS0 wait states. 101 = 10 + WS0 wait states. 111 = External DTACK.  When using the external DTACK signal, you must select DTACK function in Port G.  WS0 is the DWS0, CWS0, BWS0, or AWS0 bit in the CSCTRL1 register.  000 = 128K (32K or 8 Mbyte* for CSCx and CSDx). 010 = 512K (128K for CSCx and CSDx). 010 = 512K (128K for CSCx and CSDx). 110 = 2 Mbyte (256K for CSCx and CSDx). 110 = 8 Mbyte (1 Mbyte for CSCx and CSDx). 111 = 16 Mbyte (2 Mbyte for CSCx and CSDx). 111 = 16 Mbyte (2 Mbyte for CSCx and CSDx).  * Note: Large DRAM size selection requires the DSIZ3 bit in the chip-select control register to be set.	Setting

7	0 П 0 П 1	TYPE		
	0	۲W	RO	BIT 15
	0	V	SOP	14
	0	W	ROP	13
	0	W	UP	12
	0	>	UPSIZ	11
	0			10
	0			9
0x0000	0	W	FLASH	8
	0	V	BSW	7
	0	WI WI	1	6
	0	W	NS3-1	5
	0	₹		4
	0	W		з
	0	) rw rw rw	SIZ	2
	0	₹		_
	0	\$	EN	BIT 0

able 6-9. Chip-Select Register C Description

Name	Description	Setting
RO Bit 15	Read-Only—This bit sets the chip-select to read-only. Otherwise, read and write accesses are allowed. A write to a read-only area will generate a bus error if the BETEN bit of the SCR is set. See Section 5.2.1, "System Control Register," on page 5-2 for more information.	0 = Read/write. 1 = Read-only.
SOP Bit 14	Supervisor-Use-Only Protected Memory Block—This bit sets the protected memory block to supervisor-only; otherwise, both supervisor and user accesses are allowed. Attempts to access the supervisor-only area result in a bus error if the BETEN bit of the SCR is set. See Section 5.2.1, "System Control Register," on page 5-2 for more information.	0 = Supervisor/user. 1 = Supervisor-only.
ROP Bit 13	Read-Only for Protected Memory Block—This bit sets the protected memory block to read-only. Otherwise, read and write accesses are allowed. If you write to a read-only area, you will get a bus error.	0 = Read/write. 1 = Read-only.
<b>UPSIZ</b> Bits 12–11	Unprotected Memory Block Size—This field determines the unprotected memory range of the chip-select.	00 = 32K. 01 = 64K. 10 = 128K. 11 = 256K.
Reserved Bits 10-9	Reserved 💫	These bits are reserved and should be set to 0.
FLASH Bit 8	Flash Memory Support—When enabled, this bit provides support for flash memory by forcing the LWE/UWE signal to go active after chip-select.  Note: This bit is used for expanded memory size for CSD when the DRAM bit in the CSD register is enabled.	0 = The chip-select and LWE/UWE signals go active at the same clock edge. 1 = The chip-select signal goes low 1 clock before LWE/UWE.
BSW Bit 7	Data Bus Width—This bit sets the data bus width for this chip-select area.	0 = 8 bit. 1 = 16 bit.

	Bit O	<b>SIZ</b> Bits 3–1		WS3-1 Bits 6-4	Name
ARCHIVED BY FREESCAL	Chip-Select Enable—This write-only bit enables each chip-select.	Chip-Select Size—This field determines the memory range of the chip-select. For CSAx and CSBx, the chip-select size is between 128K and 16 Mbyte. For CSCx and CSDx, the chip-select size is between 32K and 16 Mbyte.		Wait State—This field determines the number of wait states added before an internal DTACK signal is returned for this chip-select.  Note: When using the external DTACK signal, you must configure the BUSW/DTACK/PG0 pin.	Description
	0 = Disabled. 1 = Enabled.	000 = 128K (32K or 8 Mbyte* for CSCx and CSDx). 001 = 256K (64K or 16 Mbyte* for CSCx and CSDx). 010 = 512K (128K for CSCx and CSDx). 011 = 1 Mbyte (256K for CSCx and CSDx). 100 = 2 Mbyte (512K for CSCx and CSDx). 101 = 4 Mbyte (1 Mbyte for CSCx and CSDx). 110 = 8 Mbyte (2 Mbyte for CSCx and CSDx). 111 = 16 Mbyte (4 Mbyte for CSCx and CSDx). * Note: Large DRAM size selection requires the DSIZ3 bit in the chip-select control register to be set.	When using the external DTACK signal, you must select DTACK function in Port G.  WS0 is the DWS0, CWS0, BWS0, or AWS0 bit in the CSCTRL1 register.	000 = 0 + WS0 wait states. 001 = 2 + WS0 wait states. 010 = 4 + WS0 wait states. 011 = 6 + WS0 wait states. 100 = 8 + WS0 wait states. 101 = 10 + WS0 wait states. 110 = 12 + WS0 wait states. 111 = External DTACK.	Setting

- - -	DE CET	TYPE		
	0	W	RO	BIT 15
	0	W		14
	0	W	SOP ROP	13
	0 0	W	UPSIZ	12 11
	0	V	COMB	10
	_	V	DRAM	9
0x0200	0	۲W	FLASH	8
١	0	W	BSW	7
, <	0	¥		6
	0	rw rw	WS3-	5
	0	8	1	4
	0	rw rw		з
	0	V	SIZ	2
	0	8		_
	0	\$	EN	BIT 0

Table 6-10. Chip-Select Register D Description

Name	Description	Setting
RO Bit 15	Read-Only—This bit sets the chip-select to read-only. Otherwise, read and write accesses are allowed. A write to a read-only area will generate a bus error if the BETEN bit of the SCR is set. See Section 5.2.1, "System Control Register," on page 5-2 for more information.	0 = Read/write. 1 = Read-only.
SOP Bit 14	Block—This bit sets the protected Memory block to supervisor-only; otherwise, both supervisor and user accesses are allowed. Attempts to access the supervisor-only area result in a bus error if the BETEN bit of the SCR is set. See Section 5.2.1, "System Control Register," on page 5-2 for more information.	0 = Supervisor/user. 1 = Supervisor-only.
ROP Bit 13	Read-Only for Protected Memory Block—This bit sets the protected memory block to read-only. Otherwise, read and write accesses are allowed. If you write to a read-only area, you will get a bus error.	0 = Read/write. 1 = Read-only.
<b>UPSIZ</b> Bits 12-11	Unprotected Memory Block Size—This field determines the unprotected memory range of the chip-select.	00 = 32K. 01 = 64K. 10 = 128K. 11 = 256K.
COMB Bit 10	Combining—This bit controls combining RAS0 and RAS1 memory space to generate RAS0. When this bit is set to 1, RAS1 can be used as a general-purpose I/O signal.	0 = RAS0 to RAS0 memory space. 1 = RAS0 covers both RAS0 and RAS1 memory space B.
DRAM Bit 9	DRAM Selection—This bit is used to enable RAS and CAS signals. Configuring the CSC register as a non-DRAM memory type requires clearing the DRAM bit of the CSD register.  Note: The DRAM bit overrides the flash bit.	0 = Select <u>CSC</u> [1:0] <u>and CSD</u> [1:0]. 1 = Select <u>CAS</u> and <u>RAS</u> .

Name	FLASH  Bit 8  Bit 8  forcing the l chip-select.  Note: Thi	~~~	WS3-1  Bits 6-4  Significant bits of The least significant control chip-select control these 4 bits deternance added to a DTACK is assert chip-select cycle.			Bits 3–1 memory range of t and CSBx, the chi 128K and 16 Mbyt chip-select size is 16 Mbyte.
Description	Flash Memory Support—When enabled, this bit provides support for flash memory by forcing the LWE/UWE signal to go active after chip-select.  Note: This bit is used for expanded memory size for CSD when the DBAM hit is enabled.	size for CSD when the DRAM bit is enabled.  Data Bus Width—This bit sets the data bus width for this chip-select area.	Wait State—This field contains the 3 most significant bits of the 4-bit wait-state value. The least significant bit is located in the chip-select control register 1. The value of these 4 bits determines the number of wait states added to a bus cycle before an internal DTACK is asserted to terminate the chip-select cycle.	COA	MI	Chip-Select Size—This field determines the memory range of the chip-select. For CSAx and CSBx, the chip-select size is between 128K and 16 Mbyte. For CSCx and CSDx, the chip-select size is between 32K and 16 Mbyte.
Setting	0 = The chip-select and LWE/UWE signals go active at the same clock edge. 1 = The chip-select signal goes low 1 clock before LWE/UWE.	0 = 8 bit. 1 = 16 bit.	000 = 0 + WS0 wait states. 001 = 2 + WS0 wait states. 010 = 4 + WS0 wait states. 011 = 6 + WS0 wait states. 100 = 8 + WS0 wait states. 101 = 10 + WS0 wait states. 110 = 12 + WS0 wait states. 111 = External DTACK.	When using the external DTACK signal, you must select DTACK function in Port G.  WS0 is the DWS0, CWS0, BWS0, or AWS0 bit in the CSCTRL1 register.		000 = 128K (32K or 8 Mbyte* for CSCx and CSDx). 001 = 256K (64K or 16 Mbyte* for CSCx and CSDx). 010 = 512K (128K for CSCx and CSDx). 011 = 1 Mbyte (256K for CSCx and CSDx). 100 = 2 Mbyte (512K for CSCx and CSDx). 101 = 4 Mbyte (1 Mbyte for CSCx and CSDx). 110 = 8 Mbyte (2 Mbyte for CSCx and CSDx). 111 = 16 Mbyte (4 Mbyte for CSCx and CSDx). * Note: Large DRAM size selection requires the DSIZ3 bit in the chip-select control register to be set.



## **Emulation Chip-Select Register**

register (EMUCS) that is specifically designed for the in-circuit emulation module. This register provides longer wait states. EMUCS is only valid for the 0xFFFC0000-0xFFFDFFFF memory location. wait states 12-0, depending on the type of chip used. External logic (DTACK) may also be used to have In addition to the eight general-purpose chip-select signals, the MC68VZ328 has an emulation chip-select

	RESET	TYPE			<b>EMUCS</b>
	0			BIT 15	O)
	0			14	
	0			14 13 12 11 10	
	0			12	Щ
	0			11	nula
	0			10	tion (
	0			9	Chip-
UXUUGU	0			8	Sele
00				7	ct Re
	Ų,	W		6	Emulation Chip-Select Register
	_	rw rw	WS3-1	21	76
	0	₹		4	
	0			3	0
	0			2	)x(FF)FFF118
	0			1	)FFF
	0			BIT 0	118

**Emulation Chip-Select Register Description** 

Name	Description	Setting
Reserved Bits 15–7	Reserved	These bits are reserved and should be set to 0.
<b>WS3-1</b> Bits 6-4	Wait State—This field contains the 3 most significant bits of the 4-bit wait-state value. The least significant bit is located in the chip-select control register 1. The value of these 4 bits determines the number of wait states added to a bus cycle before an internal DTACK is asserted to terminate the chip-select cycle.	000 = 0 + WS0 wait states. 001 = 2 + WS0 wait states. 010 = 4 + WS0 wait states. 011 = 6 + WS0 wait states. 100 = 8 + WS0 wait states. 101 = 10 + WS0 wait states. 110 = 12 + WS0 wait states. 111 = External DTACK.  When using the external DTACK signal, you must select DTACK function in Port G.  WS0 is the EWS0 bit in the CSCTRL1 register.
Reserved Bits 3–0	Reserved	These bits are reserved and should be set to 0.

## **Chip-Select Control Register 1**

page 6-17. memory space, and extended size for DRAM. See the following register display and Table 6-12 on features for chip-select logic. Control features include 16-bit SRAM support, extended size for unprotected wide variety of different memory types. The CSCTRL1 register provides supplemental memory-control The chip-select control register 1 (CSCTRL1) is one of three registers that provide features to control a



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Chin-Select Control Register	
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7 10 11	D II O II I	TYPE		
	0			BIT 15
	0	V	EUP	14
	0	8	SR 16	13
	0	₹	S0	12
	0	V	DW S0	11
	0	₹	CW S0	10
0×	0	₹	S0 BW	9
0x0000	0	₹	AW S0	8
	0			7
	0	8	DSI Z3	6
<	0		)6	5
	0	W	DUP S2	4
	0			ω
	0	V	CUP S2	2
	0			_
	0	V	BUP S2	ВІТ 0

 Fable 6-12.
 Chip-Select Control Register 1 Description

Name	Description	Setting
Reserved Bit 15	Reserved	This bit is reserved and should be set to 0.
EUPEN Bit 14	Extra UPSIZ Bit Enable—This bit enables the BUPS2, CUPS2, and DUPS2 bits to work with the corresponding UPSIZ configuration bits. Hence, it provides a larger dynamic range with smaller granularity for the unprotected memory sizing.	0 = EUPEN bit not set. 1 = EUPEN bit set.
<b>SR16</b> Bit 13	16-Bit SRAM Enable—This bit enables the use of 16-bit SRAM in chip-select group B memory space. It determines the functions of the LIME/LIB and LIME/LIB nine in CSR	0 = UWE and LWE are selected for all CSB  read/write cycles. 1 = UB and LB are selected for all CSB  read/write cycles
	read/write cycles.	
EWSO	Emulation Chip-Select Wait State  Rit 0.—This bit is the lowest significant bit of	Refer to Table 6-11 on page 6-16 on the emulation chin-select register for the wait state set.
	the EMU wait state register.	ting.
DWSO Bit 11	<b>CSD Wait State Bit 0</b> —This bit is the lowest significant bit of the CSD wait state register.	Refer to Table 6-10 on page 6-14 on the chip-select register D for the wait state setting.
CWSO Bit 10	CSC Wait State Bit 0—This bit is the lowest significant bit of the CSC wait state register.	Refer to Table 6-9 on page 6-12 on the chip-select register C for the wait state setting.
BWSO Bit 9	<b>CSB Wait State Bit 0</b> —This bit is the lowest significant bit of the CSB wait state register.	Refer to Table 6-8 on page 6-10 on the chip-select register B for the wait state setting.
AWS0 Bit 8	<b>CSA Wait State Bit 0</b> —This bit is the lowest significant bit of the CSA wait state register.	Refer to Table 6-7 on page 6-8 on the chip-select register A for the wait state setting.
Reserved Bit 7	Reserved 20	This bit is reserved and should be set to 0.
<b>DSIZ3</b> Bit 6	Size Bit 3 for DRAM Chip-Select Addressing Space—When set, this bit extends the DRAM size.	If SIZ[2:0] = 000, the CSD0 and CSD1 spaces are each 8 Mbyte. For 001, each space is 16 Mbyte. Only valid when the DRAM bit of the CSD register is set.
Reserved Bit 5	Reserved	This bit is reserved and should be set to 0.
DUPS2 Bit 4	<b>UPSIZ Bit 2 for CSD Register</b> —This is the most significant bit for UPSIZ[2:0] when the EUPEN bit is set.	For information on calculating unprotected memory size, see Example 6-1 on page 6-18.

#### Programming Model T

### Freescale Semiconductor, Inc

Table 6-12. **Chip-Select Control Register 1 Description (Continued)** 

Name	Description	Setting
Reserved Bit 3	Reserved	This bit is reserved and should be set to 0.
CUPS2 Bit 2	<b>UPSIZ Bit 2 CSC Register</b> —This is the most significant bit for UPSIZ[2:0] when the EUPEN bit is set.	For information on calculating unprotected memory size, see Example 6-1.
Reserved Bit 1	Reserved	This bit is reserved and should be set to 0.
BUPS2 Bit 0	UPSIZ Bit 2 CSB Register—This is the most significant bit for UPSIZ[2:0] when the EUPEN bit is set.	For information on calculating unprotected memory size, see Example 6-1.

The unprotected memory size is calculated according to the chip-select addressing space and the UPSIZ

### Example 6-1. Unprotected Memory Size Calculation

Unprotected Size = 
$$\frac{\text{Chip-Select Size}}{2^{(7-\text{UPSIZ})}}$$

follows: For example, if SIZ[2:0] in CSD = 111 and UPSIZ[2:0] = 011, the unprotected size is calculated

4 Mbyte / 
$$2^{(7-3)} = 256$$
K

## 6.3.6 Chip-Select Control Register 2

access performance by generally removing one CPU wait state or by relaxing the timing requirement for This register controls early cycle detection for both static and dynamic types of memory. It improves CPU

CSCTRL2	RL2			Chip-S	elect	Cor	p-Select Control Register 2	egist	er 2	. •			0×	(FE	)FF	x(FF)FFF10C
	BIT 15	14	13	12	11	10	9	8	7	6	5	4	6 5 4 3 2	2	1	BIT 0
	ECDD	ECDS	ECDS ECDT EASP	EASP			EASDLY[1:0]	_Y[1:0]								
TYPE	ſW	۲W	WI	rw			W	W								
D F C F T	0	0	0	_	0	0	0	0	0	0	0	0 0 0 0	0	0	0	0
7							0x1000	0								

## Table 6-13. Chip-Select Control Register 2 Description

Name	CA	Description	Setting
ECDD	Early Cycle	Early Cycle Detection for Dynamic	0 = Disabled.
Bit 15	Memory—T	<b>Memory</b> —This bit advances the timing, allow-	1 = Enabled.
	ing the CPU	ing the CPU to be used with dynamic memory	
	access. It re	access. It reduces wait states by one.	

						<u> </u>	
	Reserved Bits 7–0	EASDLY[1:0] Bits 9–8	Reserved Bits 11-10	EASP Bit 12	ECDT Bit 13	ECDS Bit 14	Name
ARCHIVED BY FREESO	Reserved	Early ASB Delay Value—When delay chain is chosen as the delay processing method for early ASB (that is, the EASP bit is clear), these bits select the level of the delay element for the early ASB to get through.	Reserved	<b>Memory Early Cycle Detection</b> —To prevent the early ASB signal from the CPU from being asserted before a valid address is present from the CPU, the early ASB can be programmed so it is delayed before going to the chip-select generator. This bit must be programmed appropriately when early ASB is chosen as the early cycle detection signal.	Early Cycle Detection Type—When the master enable for early cycle detection is on (that is, ECDD = 1), this bit selects what signal from the CPU is used to trigger the bus cycle.	Early Cycle Detection for Static Memory—This bit advances the chip-select signals for SRAM, ROM, or flash memory. It allows more setup time for slow memory with- out adding CPU wait states.	Description
	These bits are reserved and should be set to 0.	00 = No delay. 01 = 1 level. 10 = 2 levels. 11 = 3 levels.	These bits are reserved and should be set to 0.	0 = Use selectable delay chain as the delay processing method. 1 = Use negative CPU edge synchronization as the delay processing method (default setting).	0 = Use the early ASB from the CPU as the triggering signal for early cycle detection. 1 = Use the TSCAE from the CPU as the triggering signal for early cycle detection.	0 = Disabled. 1 = Enabled.	Setting



## **Chip-Select Control Register 3**

This register controls minor timing trims for static memory access

CSCTRL3

#### Chip-Select Control Register 3

0x(FF)FFF150

7 6	DESET	TYPE		
	_	rw	EWE	BIT 15
	0	ſW	WPEXT	14
	0	WI	LCWS AST	13
	_	W	AST	12
	_	W	DST	11
0x9	_	W	CST	10
0x9C00	0			9
	0			8
1	0			7
	0 0		<b>*</b>	6 5
	0			4
	0			ω
	0			2
	0			_
	_			Е
	0			3IT 0

#### Table 6-14. **Chip-Select Control Register 3 Description**

Name	Description	Setting
<b>EWE</b> Bit 15	End Write Early—When this bit is set, the RAM write-enable signal negates before the CS signal is negated.	0 = Disabled. 1 = Enabled.
WPEXT Bit 14	Write Pulse to CS Negation Margin Extension—When EWE is set, WPEXT is set to extend the WE negation to CS negation by one more clock.	0 = Disabled. 1 = Enabled.
LCWS Bit 13	Wait State Trim for LCD-SRAM  Access—When this bit is set, one additional wait state is added to the LCD-SRAM access cycle. For example, if the wait state is set to zero, all CPU accesses require 4 cycles to	<ul><li>0 = No additional wait state added.</li><li>1 = One additional wait state added.</li></ul>
	complete, the chip-select signal to SRAM lasts 2.5 CPU clock cycles, and 2 cycles are used for LCD access. When LCWS is enabled, the LCD access is delayed; the access is increased from 2 to 3 clock cycles.	
<b>AST</b> Bit 12	AS Toggle Enable—Enables AS toggling between two 8-bit transfers.	<ul><li>0 = Disable AS toggling between two 8-bit transfers.</li><li>1 = Enable AS toggling between two 8-bit transfers.</li></ul>
DST Bit 11	<b>DS Toggle Enable</b> —Enables DS toggling between two 8-bit transfers.	<ul><li>0 = Disable DS toggling between two 8-bit transfers.</li><li>1 = Enable DS toggling between two 8-bit transfers.</li></ul>
CST Bit 10	CS Toggle Enable—Enables CS toggling between two 8-bit transfers.	0 = Disable CS toggling between two 8-bit transfers. 1 = Enable CS toggling between two 8-bit transfers.
Reserved Bits 9–0	Reserved	These bits are reserved and should be set to 0.

configuration Example 6-2 on page 6-21 demonstrates how to initialize the chip-select with a particular memory



### Example 6-2. Programming Example

******** * Chip-S ************************************	****** %elect 1 ***** equ	**************************************
BASEB BASEB	egu egu	group A base register
BASEC	equ	C base
BASED	equ	D base register
CSA	equ	A chip-
CSB	equ	B chip-select
CSC	equ	C chip-select
CSD	equ	chip-select
*******	****	*****
* PORT c	control	PORT control registers
*******	****	**********
PORTBASE	egu	REGSBASE+0x400 port B registers base address
PBDir	equ	PORTBASE+0x08 port B direction register
PBData	equ	PORTBASE+0x09 port B data register
PBPU	equ	
PBSe1	equ	

move.w	move.w	move.w	move.w	move.w	move.w	START move.b	****************
W	₩ W	w.	₩	W.W	₩.	р.	****
#0x0000,CSD	#0x2040,BASEC #0x0191,CSC	#0x0093,CSB	#0x2000,BASEB	#0x8081,CSA	#0x0000,BASEA	#0x00,PBSel	************
config CSC,CSD as non-DRAM memory type	set base addrs 0x4080000 read/write,flash,16-bit,1 ws,32K	read/write,16-bit,1 wait state,256K	set base address 0x4000000	read-only,16-bit,0 wait state,128K	set base address 0x0000000	disable PortB, select chip-selects	*****

The preceding initialization will follows: configure the CSA and CSB chip-selects

32K 32K

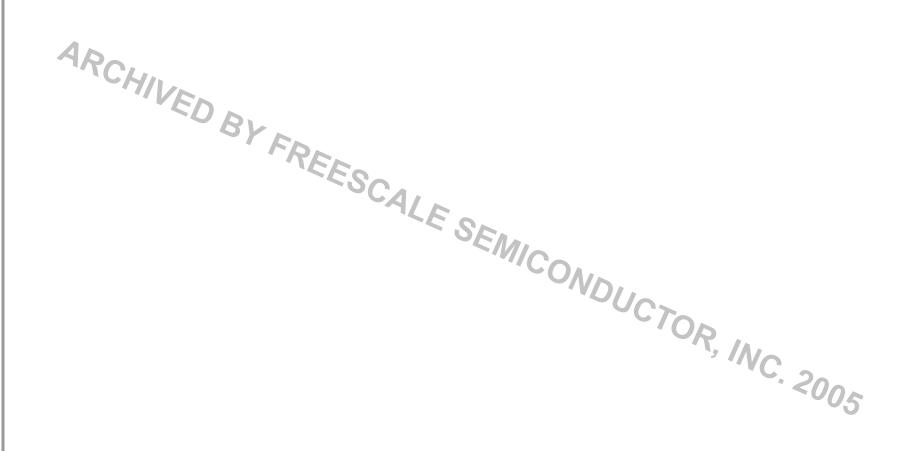
CSD1 disabled

CSD1 disabled

ARCHIE



CSAO CSA1 CSBO CSB1 CSCO CSCO CSCO 0x4088000-0x4080000-0x4040000-0-0x001ffff, read-only, 16-bit, 0 0-0x003ffff, read-only, 16-bit, 0 0-0x403ffff, read/write, 16-bit, 1 0-0x407ffff, read/write, 16-bit, 1 0-0x4087fff, read/write, flash, 16-0-0x408ffff, read/write, flash, 16state,128K state,256K state,256K state,256K 1 wait state, 1 wait state,



## Freescale Semiconductor, Inc.

### DRAM Controller Chapter 7

is closely linked to the chip-select logic. Please refer to Chapter 6, "Chip-Select Logic," for more details This chapter describes the DRAM controller for the MC68VZ328. The operation of the DRAM controller <sup>1</sup>NC. 2005

# Introduction to the DRAM Controller

addition to controlling DRAM, the DRAM controller provides support for LCD controller burst accesses RAM, Fast Page Mode, and synchronous DRAM. The DRAM controller provides Row Address Strobe  $(\overline{RAS})$  and Column Address Strobe  $(\overline{CAS})$  signals for up to a maximum of two banks of DRAM. In The DRAM controller provides a glueless interface for either 8-bit or 16-bit DRAM. It supports EDO

The DRAM controller has the following features:

- 68000 CPU zero wait-state operation support
- CAS-before-RAS refresh cycles and self-refresh mode DRAM support
- Fast Page Mode and EDO RAM modes or synchronous burst for LCD DMA access cycles

8- and 16-bit port DRAM support

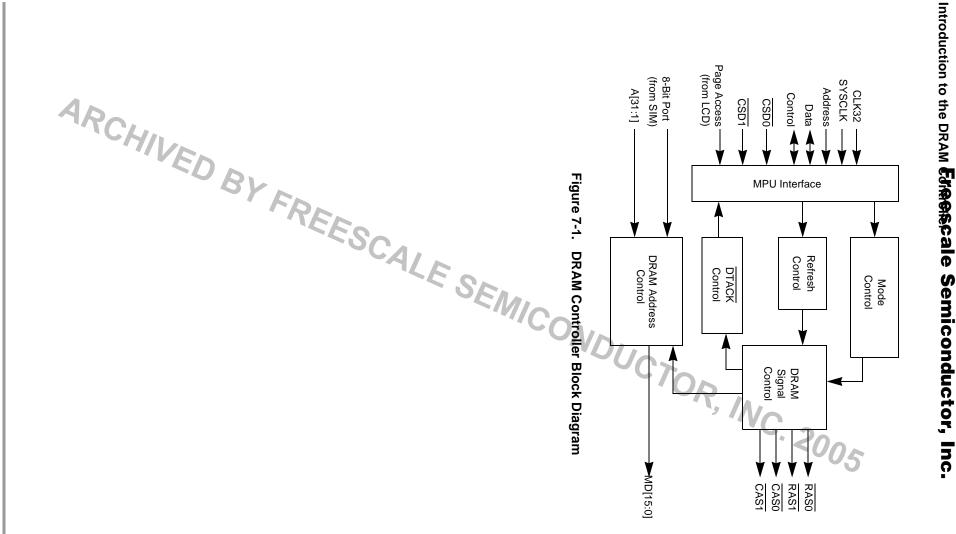
Programmable refresh rate

- Support for a maximum of two banks of DRAM
- Programmable row and column address size with symmetrical or asymmetrical addressing
- Support for up to 16 Mbyte  $\times$  16 or 32 Mbyte  $\times$  8 DRAM or SDRAM

A block diagram of the DRAM controller appears in Figure 7-1 on page 7-2







# Freescale Semiconductor, Incam Controller Operation

# DRAM Controller Operation

This section describes the DRAM controller's operation

7.2.1 Address Multiplexing

The address multiplexer can support a wide variety of memory devices in either 8- or 16-bit mode. The upper internal address lines from the CPIT or 1 CD controller and address lines from the CPIT or 1 CD controller and address lines from the CPIT or 1 CD controller and address lines from the CPIT or 1 CD controller and address lines from the CPIT or 1 CD controller and address lines from the CPIT or 1 CD controller and address lines from the CPIT or 1 CD controller and address lines from the CPIT or 1 CD controller and address lines from the CPIT or 1 CD controller and address lines from the CPIT or 1 CD controller and address lines from the CPIT or 1 CD controller and address lines from the CPIT or 1 CD controller and address lines from the CPIT or 1 CD controller and address lines from the CPIT or 1 CD controller and address lines from the CPIT or 1 CD controller and address lines from the CPIT or 1 CD controller and address lines from the CPIT or 1 CD controller and address lines from the CPIT or 1 CD controller and address lines from the CPIT or 1 CD controller and address lines from the controller and address lines from t columns and the data port size (8 or 16 bit) of the DRAM. supports different row and column configurations, depending on the arrangement of the DRAM rows and EDO RAM mode read accesses to the DRAM during LCD DMA cycles. The DRAM multiplexer also internal address lines are used as the column address. This scheme enables the use of Fast Page Mode or

addresses, the column addresses require PA[9:1], and PA[19:10] is used for the row addresses. used for row addresses. Similarly, if we use 16-bit DRAM with the same number of row and column configuration in 8-bit mode, the internal address bus PA[8:0] is used for column addresses, and PA[18:9] is For 4 Mbyte (512K × 8) DRAM, there are usually only 10 row addresses and 9 column addresses. For this

or PA9 for column address MD8. Similar address selection options are provided for MD9 and MD10 column addresses, the MD0 row address, and the row addresses MD8 through MD12 . controller uses PA[8:1] as the column addresses for MD[7:0] and then allows software to select either PA0 The address multiplexing options are provided in Table 7-1 on page 7-4. The MC68VZ328's DRAM

non-DRAM external accesses. Since the internal addresses (PA[13:1]) are present as the column address addresses A[13:1] for non-DRAM external accesses. This simplifies the overall multiplexing scheme for selection from the DRAM address multiplexer, these addresses may be used as the nonmultiplexed The MD[12:0] signals share the same address pins that output as nonmultiplexed addresses A[13:1] for

### // NOTE

The A0 signal is not used as a DRAM address pin connection.

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently

are not available from Freescale for import or sale in the United States prior to September 2010; MC68VZ328 Product Family

row labeled "Column Address Options" is used for Fast Page Mode and EDO RAM and is enabled when SDRAM control register is 1. the SDEN bit (bit 15) in the SDRAM control register (0xFFFFFC04) is 0. The row labeled "Column programmed in the DRAM memory configuration (DRAMMC) register except as noted in the table. Table 7-1 on page 7-4 contains the address multiplexing options for the VZ pins listed. All the options are Address Options Specific for SDRAM" is used for SDRAM and is enabled when the SDEN bit in the ARCHIVED BY FR



### DRAM Controller Operatio Freescale Semiconductor, Inc.

ble 7-1. DRAM Address Multiplexing Options

Row	<b>A1/MD0</b> PA23	<b>A2/MD1</b> PA12	<b>A3/MD2</b> PA13	<b>A4/MD3</b> PA14	<b>A5/MD4</b> PA15	<b>A6/MD5</b> PA16	<b>A7/MD6</b> PA17	
Row Address Options	PA23 PA22 PA11	PA12	PA13	PA14	PA15	PA16	P	A17
Column Address Options	PA1	PA2	PA3	PA4	PA5	PA6	ס <u>ר</u>	PA7
Column Address Options for SDRAM	PA1 <sup>1</sup> PA0	PA2	PA3	PA4	PA5	PA6	PA7	17
MD Address	MD0	MD1	MD2	MD3	MD4	MD5	MD6	)6
	A9/MD8	A10/MD9	A11/MD10	A12/MD11	A13/MD12	A14/MD13	A15/MD14	D14
Row Address Options	PA10 PA20	PA9 PA19	PA19 PA21	PA20 PA22	PA10 PA21 PA23	PA22	PA23	23
Column Address Options	PA0 (PA1) PA9	PA0 PA10	PA0 PA11	PA12	PA13	PA22	PA23	23
Column Address Options for SDRAM	PA1 <sup>2</sup> PA9	PA1	SCAL	PA20 <sup>3</sup> PA22	PA10 <sup>4</sup> PA21 PA23	PA22	PA23	13
MD Address	MD8	MD9	MID10	MD11	MD12	MD13	MD14	14

register (0xFFFFFC04) determines the selection. When SCOL = 0, PA1 is selected. When SCOL = 1, PA0 is se-1.Pin A1/MD0 has column address options of PA0 and PA1 for SDRAM. The SCOL bit (bit 6) of the SDRAM contro



<sup>2.</sup>Pin A9/MD8 has column address options of PA1 and PA9 for SDRAM. The COL8 bit (bit 5) of the DRAM memory configuration register (0xFFFFC00) determines the selection. When COL8 = 0, PA9 is selected. When COL8 = 1, PA1 is selected.

<sup>3.</sup>Pin A12/MD11 has column address options of PA20 and PA22 for SDRAM. The ROW11 bit (bit 11) of the DRAM memory configuration register (0xFFFFFC00) determines the selection. When ROW11 = 0, PA20 is selected. When ROW11 = 1, PA22 is selected.

<sup>4.</sup>Pin A13/MD12 has column address options of PA10, PA21, and PA23 for SDRAM. The ROW12 field (bits 15–14) of the DRAM memory configuration register (0xFFFFFC00) determines the selection. When ROW12 = 00, PA10 is selected. When ROW12 = 01, PA21 is selected. When ROW12 = 10, PA23 is selected.

### reescale Semiconductor, Incam Controller Operation

Table 7-2 through Table 7-5 on page 7-6 provide recommendations for MC68VZ328-to-SDRAM connections and for selecting multiplexing options for different types of SDRAM.

16 Mbit SDRAM—256 (16-Bit) and 512 (8-Bit) Page Size

Z	@ Q & C	2 9 8 C	O & _	S	_ 8
Note: ×=	Column Address Options (8-Bit)	Column Address Options (16-Bit)	Row Address Options	VZ Pins	SDRAM Pins
X = "don't care"	PA0	PA1	PA11	A1/ MD0	Α0
are"	PA2	PA2	PA12	A2/ MD1	A1
	PA3	PA3	PA13	A3/ MD2	A2
	PA4	PA4	PA14	A4/ MD3	А3
	PA5	PA5	PA15	A5/ MD4	Α4
111	PAG	PA6	PA16	A6/ MD5	A5
	PA7	UC 7A	PA17	A7/ MD6	A6
	PA8	PA8	PA18	A8/ MD7	A7
	PA1	×	PA10	A9/ MD8	A8
	×	×	PA9	A10/ MD9	A9
	0	0	PA19	A11/ MD10	A10
	PA20	PA20	PA20	A12/ MD11	BS

	Table 7-3.
	64 Mbit
	64 Mbit SDRAM-
	-256 (·
•	16-Bit) a
	16-Bit) and 512 (
•	8-Bit)
•	Page Size

Note: X=	Column Address Options (8-Bit)	Column Address Options (16-Bit)	Row Address Options	VZ Pins	SDRAM Pins
X = "don't care"	PA 0	PA 1	PA 11	A1/ MD	AO
care"	PA 2	PA 2	PA 12	A2/ MD	<u> 2</u>
	PA 3	PA 3	PA 13	A3/ MD 2	A2
	PA 4	PA 4	PA 14	A4/ MD 3	А3
	PA 5	PA 5	PA 15	A5/ MD 4	A4
	PA 6	PA 6	PA 16	A6/ MD 5	A5
	PA 7	PA 7	PA 17	A7/ MD 6	A6
	PA 8	PA 8	PA 18	A8/ MD 7	A7
	PA 1	×	PA 10	A9/ MD 8	A8
	×	X	PA 9	A10 /MD 9	A9
	0	0	PA 19	A11 /MD 10	A10
	×	×	PA 20	A12 /MD 11	A11
	PA21	PA21	PA21	A13/ MD 12	BS0
	PA22	PA22	PA22	A14/ MD 13	BS1

**VZ Pins** 

o M A1

**1** № 22

2 MD A3/

ω A4/

A5/

MD A6/

6 MD

A8/ 7 D

8 MD 8

A10 MD 9

A11 10

A12 /MD

A13 /MD 12

A15 /MD 14

A16 /MD 15

OI.

Address Options (16-Bit)

Column

2 P

 $\omega_{A}^{P}$ 

PA

6 P

7 PA

ωP

9 P

 $\times$ 

0

 $\times$ 

 $\times$ 

PA 23

24 24

Address Options

Row

1 PA

12

13 13

14 PA

15 P

16

PA 17

18 18

PA 20

21 21

PA 22

10 10

PA 23

PA 24

Note:

 $\times$ 

"don't care"

ARCHIV

Address Options (8-Bit)

Column

N ₽

ωΡ

4 PA

5 P

6 PA

7 PA

∞₽

9 P

0

 $\times$ 

 $\times$ 

23 23

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SDRAM Pins

z

VZ Pins	MD A1/	A2/ MD 1	A3/ MD 2	A4/ MD	A5/ MD	A6/ MD 5	A7/ MD 6	A8/ MD 7	A9/ MD 8	9 MD A10	A11 /MD 10	A12/ MD 11	A13 /MD 12
Row Address Options	11 11	PA 12	PA 13	PA 14	PA 15	PA 16	PA 17	PA 18	PA 20	PA 19	PA 21	PA22	10
Column Address Options (16-Bit)	PA 1	PA 2	PA 3	PA 4	PA 5	PA 6	PA 7	PA 8	PA 9	×	0	PA22	×
Column Address Options (8-Bit)	0 PA	PA 2	PA 3	4 PA	PA 5	PA 6	PA 7	8 8	9 9	1 PA	0	PA22	×
Note: X =	X = "don't care"	care"					C						

PA23

DRAM Controller Operatio Freescale Semiconductor, Inc.

SDRAM Pins

8

₹

₽2

₽3

₽4

8

₽

A9

A10

BS0

<u> 21</u>

BS1

PA23

A15/ MD 14

PA23

**Table 7-4.** 

128 Mbit SDRAM—512 (16-Bit) and 1024 (8-Bit) Page Size

ΑO	
<u>A</u>	Table
A2	7-5.
A3	256 Mk
A4	oit SDF
A5 A6	Table 7-5. 256 Mbit SDRAM—512 (16-Bit) and 1024 (8-Bit) Page Size
A7	6-Bit)
A8	and 10
A9	)24 (8-
A10	Bit) Pa
A10 A11 A12	age Sia
A12	že
BS 0	

MC68VZ328 User's Manual

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### **DTACK Generation**

Freescale Semiconductor, Incam Controller Operation

In a 16 MHz system frequency, 60 ns DRAM can support a zero wait state (4 clocks per access) for CPU bus cycles. Therefore, DTACK is only delayed for refresh operations that occur before a read/write access cycle. The value of N clocks (N is the number of system clock cycles required for refresh) will be inserted into a read or write cycle when the CPU cycle collides with a refresh cycle. Refresh, in this case, has a

### NOTE

the refresh cycle and CPU bus cycle. The value of N can be 1-4 clocks, depending on the collision overlap of

### **Refresh Contro**

n, the MC68 ,
te requirement may
λM configuration register ,
nples demonstrate refresh values u..

K32 = 32.768 kHz:

K = 0

RAMMC register value (REF) = 0
refresh period = 15.2 μs

SYSCLK = 16.58 MHz:

CLK = 1

DRAMMC register value (REF) = 7

refresh period = 15.44 μs REF field in the DRAM configuration register (DRAMMC) to select the required refresh frequency. The DRAM refresh rate requirement may vary between different DRAM chips. Users can program the During normal operation, the MC68VZ328 DRAM cycles are distributed evenly over the refresh period

The following examples demonstrate refresh values using two different settings and clock sources:

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# DRAM Controller Operatio Freescale Semiconductor, Inc.

### 7.2.4 LCD Interface

page bursting accesses. When the PAGE\_ACCESS signal is active and CSD[1:0] is active, Fast Page Figure 7-2 illustrates the LCD controller and DRAM controller interface. The DRAM controller supports Mode or EDO RAM mode will be initiated.

ellipsis and the final number: first clock-second clock-third clock-...-last clock. For example, the notation access cycle for the second and subsequent access cycles using the BC0 and BC1 bits of the DRAMC 4-2-2-...-2 represents 4 clocks for the first transfer and 2 clocks for the second and subsequent transfers. for the additional clock cycles is to display the first three numbers, separated by hyphens, followed by an register. One, two, three, and four additional clocks are supported by the DRAM controller. The notation In Fast Page Mode mode, the first access will always be 4 clocks. Additional clocks may be added to the The first access is always 4 clocks.

additional information about operation using an LCD display, see Chapter 8, "LCD Controller." transfers. However, in EDO RAM mode, the BC0 and BC1 bits are ignored by the DRAM controller. For Single clocks and transfers are only supported in EDO RAM mode, allowing the fastest LCD DMA

required for refresh). Therefore, in EDO RAM mode, for a 4-1-1-...-1 cycle, the access will become will go first, and N more clocks will be added to the first access (N is the number of system clock cycles When an LCD controller cycle and a refresh request collide before the LCD controller cycle starts, refresh

When consecutive LCD controller burst accesses cross a memory page boundary, the DRAM controller will hold the LCD controller that is negating the internal DTACK signal to change the row address and for 8 cycles, the deferred refresh cycle will not overlap with the next refresh request. refresh will be deferred until the end of the LCD controller cycle. Since the LCD controller cycle only lasts wait for a precharge time. When a refresh request occurs in the middle of an LCD controller cycle transfer,

transfer. If DTACK is asserted, the LCD controller will assume a fixed wait-state transfer per the setup within the LCD controller. The LCD controller will hold as long as  $\overline{DTACK}$  is not asserted. The DTACK signal is used to hold the LCD controller after the address changes on each word of an LCD

integration module that an LCD DMA burst transfer is about to begin. The associated chip-select signal will hold active throughout the LCD controller's access cycle. In this mode, the DRAM controller supports The PAGE\_ACCESS signal from the LCD controller indicates to the DRAM controller and system

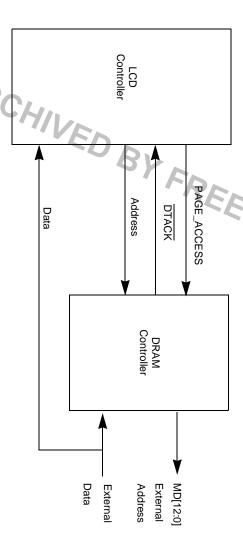


Figure 7-2. LCD Controller and DRAM Controller Interface



### 8-Bit Mode

Freescale Semiconductor, Incam Controller Operation

adjusted to fit the 8-bit operation of the selected DRAM device. RAS, CAS, and refresh signal functions as the least significant multiplexed address, and the remainder of the multiplexed address lines will be same time that CSDx is active. In 8-bit mode, the DRAM address multiplexer will use PA0 instead of PA1 port. If one of the  $\overline{\text{CSDx}}$  signals is programmed as 8-bit mode, the 8-bit mode signal will be active at the From the system integration module (SIM), 8-bit operation on the fly can be selected using the signal 8-bit address multiplexer options in the DRAMMC register. will remain the same. Depending on the DRAM type used, the system software may need to adjust the

## Low-Power Standby Mode

support self-refresh mode will enter self-refresh typically 100 µs after RAS and CAS are held in the operation will continue asserted state. After a wake up, one CAS-before-RAS refresh cycle will occur, and then normal-mode If DRAM that supports self-refresh mode is being used, the RM bit in the DRAMC register can be programmed to self-refresh mode before entering sleep mode. The DRAM controller will generate one CAS-before-RAS cycle, negate RAS and CAS for the required precharge time, then assert CAS-before-RAS, and continue to assert them until the mode is changed in the RM bit. DRAMs that

For DRAMs without self-refresh mode, ensure that the LPR bit in the DRAMC register is set for CAS-before-RAS refresh mode to continue while the processor is shut down and all other modules are



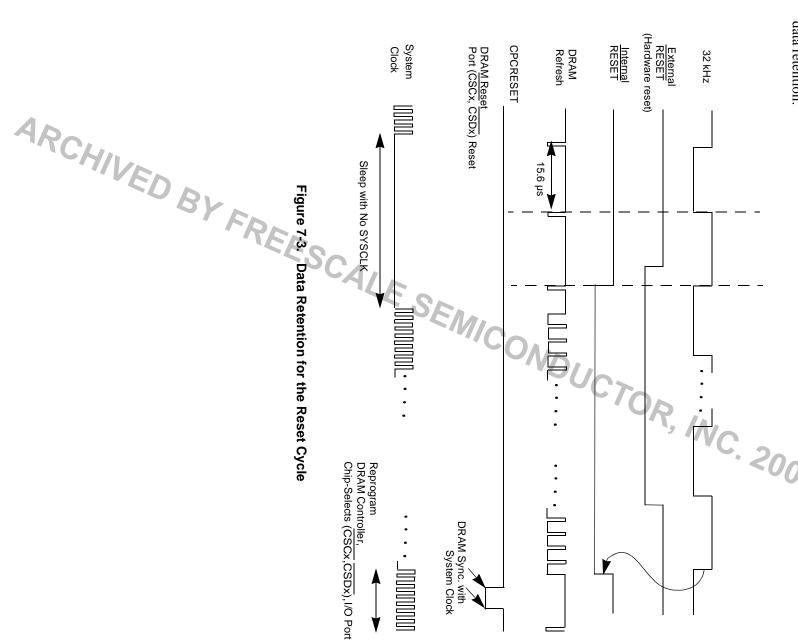
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## 2.7 Data Retention During Reset

DRAM Controller Operatio Freescale Semiconductor, Inc.

data retention. DRAM needs to retain data during reset, whether it is an external reset or an internal watchdog reset. The DRAM controller itself has a special design to support this feature. Figure 7-3 illustrates the timing for



### 2.8 Data Retention Sequence

Freescale Semiconductor, Incam Controller Operation

Data is retained in the following sequence:

- 1. The external RESET signal is sent to the MC68VZ328
- the CLK32 signal. The internal RESET signal is generated by synchronizing the external RESET signal with
- $\dot{\omega}$ operation and enter burst refresh mode, which is a consecutive CAS-before-RAS refresh When the internal RESET is asserted, the DRAM controller will stop the current refresh
- 4. The external RESET signal continues asserting
- 5. The external  $\overline{RESET}$  signal is negated
- 6. The internal RESET signal is negated.
- .7 The DRAM controller terminates the burst CAS-before-RAS refresh cycle
- $\infty$ and the  $\overline{CSCx}$  and  $\overline{CSDx}$  port signals. The internal CPCRESET signal is generated for 16 clocks to reset the DRAM controller
- The chip is now reset.

9.

The core processor programs the DRAM controller and the port pins after this reset to resume DRAM controller operation.

### NOTE

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### Programming Model

## Freescale Semiconductor, Inc.

### 7.3 Programming Mode

This section describes the programming model for the DRAM controller.

# **DRAM Memory Configuration Register**

configure the address multiplexer for the specific memory device being used. The bit position and values are shown in the following register display. The details about the register settings are described in The DRAM memory configuration register (DRAMMC) is used to set the DRAM refresh interval and

DRAM	MC			무	AM M	Memory (	Confi	y Configuration	/#	Register	Y	_	0x(F	÷F)F	FFF	FC00
	ВІТ 15	14	13	12	11	10	9	8	7	6	5	4	з	2	1	ВІТ
	ROW12	V12	ROWO	owo	ROW 11	ROW 10	ROW 9	ROW 8	10 LOC	COL 9	COL 8			REF		
TYPE	W	w w w	W	W	W	W	W	TW/	W	W	W	W	W	rw rw rw	M	W
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7 0 0								0x0000								

Table 7-6. DRAM Memory Configuration Register Description

Name	Description	Setting
<b>ROW12</b> Bits 15–14	Row Address MD12—This field selects the row address bit for multiplexed address MD12.	00 = PA10 01 = PA21 10 = PA23
<b>ROW0</b> Bits 13–12	Row Address MD0—This field selects the row address bit for multiplexed address MD0.	00 = PA11 01 = PA22 10 = PA23 11 = Not valid
ROW11 Bit 11	<b>Row Address MD11</b> —This bit selects the row address bit for multiplexed address MD11.	0 = PA20 1 = PA22
ROW10 Bit 10	<b>Row Address MD10</b> —This bit selects the row address bit for multiplexed address MD10.	0 = PA19 1 = PA21
ROW9 Bit 9	<b>Row Address MD9</b> —This bit selects the row address bit for multiplexed address MD9.	0 = PA9 1 = PA19
ROW8 Bit 8	<b>Row Address MD8</b> —This bit selects the row address bit for multiplexed address MD8.	0 = PA10 1 = PA20
COL10 Bit 7	<b>Column Address MD10—</b> This bit selects the column address bit for multiplexed address MD10.	0 = PA11 1 = PA0
COL9 Bit 6	<b>Column Address MD9</b> —This bit selects the column address bit for multiplexed address MD9.	0 = PA10 1 = PA0
COL8 Bit 5	Column Address MD8—This bit selects the column address bit for multiplexed address MD8.	0 = PA9 1 = PA0

Table 7-6. **DRAM Memory Configuration Register Description (Continued)** 

Name	Description	Setting
REF Bits 4–0	Refresh Cycle—This value determines the refresh rate for the DRAM controller. The refresh rate can be calculated using the equation shown in Example 7-1.	See description

The REF value is the time of 1 refresh cycle. Example 7-1. Calculating REF Field Values for Refresh Times

When CLK = 0, 32 kHz (or 34.8 kHz) is used for refresh control.

CLK = 1, the system clock is used for refresh control.

• The refresh rate = SYSCLK / (32 × (REF + 1)). D

ARCHIVED BY FREESCALE SEMICO If REF = (2 to 15), the refresh rate = 32 kHz / (REF + 1).

n CLK = 1, the system clock is used for refresh at



### 7.3.2 DRAM Control Register

described in Table 7-7. position and values are shown in the following register display. The details about the register settings are The DRAM control (DRAMC) register is used to control the operation of the DRAM controller. The bit

0x(FF)FFFC02

### DRAMC **DRAM Control Register**

7 0 1		TYPE			
	0	W	EN	BIT 15	
	0	W	RM	14	
	0	₹	ВС	13	
	0	V	BC1-0	12	
0x0000	0	8	CLK	11	
	0	W			
	0	₹	PGSZ	9	
	0	₹	SZ	8	
	0			7	
	0			6	
	9	W	MSW	5	
	0	₹	LSP	4	
	0	₹	SLW	3	
	0	₹	LPR	2	
	_	₹	RST	1	
	0	rw	DWE	BIT 0	

**Table 7-7. DRAM Control Register Description** 

RM       Refresh Mode—This bit sets the refresh mode.       0 = CAS-before-RAS refresh mode.       1 = Self-refresh mode.         Bit 14       Page Access Clock Cycle (Fast Page Bit 13–12 additional clocks of the second and subsequent accesses within a Fast Page Mode read cycle after the first data word.¹¹       00 = 1 additional clocks (2 clocks/transfer). 10 = 3 additional clocks (3 clocks/transfer). 10 = 3 additional clocks (3 clocks/transfer). 11 = 4 additional clocks (3 clocks/transfer). 10 = 3 additional clocks (4 clocks/transfer). 11 = 4 additional clocks (5 clocks/transfer). 11 = 4 additional clocks (6 clocks/transfer). 11 = 4 additional clocks (7 clocks/transfer). 11 = 4 additional clocks (5 clocks/transfer). 11 = 4 additional c	Name EN Bit 15
Page Access Clock Cycle (Fast Page Mode)—These bits determine the number of additional clocks for the second and subsequent accesses within a Fast Page Mode read cycle after the first data word.¹  Clock—This bit selects the clock that is provided to the refresh timer.  Extended Data Out—This bit selects the page access mode for LCD DMA DRAM accesses. This bit should only be set if the DRAM supports EDO RAM transfers. When the EDO bit is set, BCO and BC1 do not affect the number of clocks for LCD DMA DRAM accesses. EDO RAM mode is the fastest LCD DMA transfer mode.  Page Size—This field determines the page size in the word for Fast Page Mode mode access.  Slow Multiplexing—Setting this bit adds a sys- tem clock for DRAM address multiplexing, which allows for a heavily loaded A/DMA bus. Setting this bit causes an additional wait state for all core accesses and the first LCD DMA word access.	RM Bit 14
Clock—This bit selects the clock that is provided to the refresh timer.  Extended Data Out—This bit selects the page access mode for LCD DMA DRAM accesses. This bit should only be set if the DRAM supports EDO RAM transfers. When the EDO bit is set, BCO and BC1 do not affect the number of clocks for LCD DMA DRAM accesses. EDO RAM mode is the fastest LCD DMA transfer mode.  Page Size—This field determines the page size in the word for Fast Page Mode mode access.  Slow Multiplexing—Setting this bit adds a system clock for DRAM address multiplexing, which allows for a heavily loaded A/DMA bus. Setting this bit causes an additional wait state for all core accesses and the first LCD DMA word access.	<b>BC1–0</b> Bit 13–12
Extended Data Out—This bit selects the page access mode for LCD DMA DRAM accesses. This bit should only be set if the DRAM supports EDO RAM transfers. When the EDO bit is set, BC0 and BC1 do not affect the number of clocks for LCD DMA DRAM accesses. EDO RAM mode is the fastest LCD DMA transfer mode.  Page Size—This field determines the page size in the word for Fast Page Mode mode access.  ed Reserved  Slow Multiplexing—Setting this bit adds a system clock for DRAM address multiplexing, which allows for a heavily loaded A/DMA bus. Setting this bit causes an additional wait state for all core accesses and the first LCD DMA word access.	CLK Bit 11
Page Size—This field determines the page size in the word for Fast Page Mode mode access.  Page Mode mode access.  Fraction of the word for Fast Page Mode mode access.  Fraction of the word for Fast Page Mode mode access.  Fraction of the word for Fast Page Mode mode access.  Fraction of the word access.  Fraction of the word access.	EDO Bit 10
Reserved  Reserved  Slow Multiplexing—Setting this bit adds a system clock for DRAM address multiplexing, which allows for a heavily loaded A/DMA bus. Setting this bit causes an additional wait state for all core accesses and the first LCD DMA word access.	PGSZ Bits 9–8
this bit causes an additional wait state for all core accesses and the first LCD DMA word access.	Reserved Bits 7–6 MSW Bit 5
	Bit 5

Name	Description	Setting
Bit 4	Light Sleep—Setting this bit enables the core or LCD controller to access the DRAM when the RM bit is set (DRAM is in self-refresh mode). Self-refresh mode is temporarily interrupted for the DRAM access and automatically returns to self-refresh mode once the transfer is complete. Transfers in this mode are much slower than normal. Therefore, it is best to clear the RM bit if the DRAM is to be awake for extended periods of time. If this bit is clear, DRAM accesses will not occur when RM is set, and attempts will cause the bus to time out.	0 = Self-refresh is interrupted only by clearing the RM bit. 1 = Self-refresh is temporarily interrupted by core or LCD controller accesses to DRAM.
2	Constitution that the DAG	No work and the state of the st
Bit 3	precharge period for slower DRAM devices. This bit should be set if the RAS precharge time requirement for the device being used is greater than 60 ns (33 MHz system clock) or 120 ns (16.58 MHz system clock).	1 = Extended RAS precharge for slower DRAM devices (4 system clocks).
LPR	Low-Power Refresh Enable—This bit is used to	
Bit 2	control the refresh during low-power modes.	1 = Enable low-power refresh mode.
RST Bit 1	Reset Burst Refresh Enable—This bit controls the refresh type during RESET assertion.	<ul> <li>0 = Normal distributed refresh operation during DRAM reset function.</li> <li>1 = Continuous burst refresh operation during DRAM reset function.</li> </ul>
<b>DWE</b> Bit 0	DRAM Write-Enable—This bit is used to enable the DWE signal, which can be employed when a DRAM is being used that needs an independent write-enable signal, rather than sharing one with the UWE signal.	0 = Disable DWE. 1 = Enable DWE.

<sup>1.</sup>The first Fast Page Mode access will always be 4 clocks. When an LCD controller cycle and a refresh request collide before the LCD controller cycle starts, refresh will go first, and N more clocks will be added to the first ARCHIVED BY FRI



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## 7.3.3 SDRAM Control Register

following register display. The details about the register settings are described in Table 7-8 This register controls operation when SDRAM is being used. The bit position and values are shown in the

SDCTRL    BIT   14   13   12   11   10   9   8   7   6   5   4   3   2   1   BIT	7	D N	TYPE			SD
SDRAM Control Register   Ox(FF)FF	-	í T	PΕ			C
SDRAM Control Register   Ox(FF)FF		0	W	SDEN	ВІТ 15	~
SDRAM Control Register         0x(FF)FF           11         10         9         8         7         6         5         4         3         2         1           IP         MR         SCOL         BNKADDH         BNKADDL         CL           rw         rw         rw         rw         rw         rw         rw         rw           0         0         0         0         1         1         1         1         0		0	W	СРМ	14	
SDRAM Control Register         0x(FF)FF           11         10         9         8         7         6         5         4         3         2         1           IP         MR         SCOL         BNKADDH         BNKADDL         CL           rw         rw         rw         rw         rw         rw         rw         rw           0         0         0         0         1         1         1         1         0		0			13	
DX(FF)FF           5         4         3         2         1           BNKADDH         BNKADDL         CL           rw         rw         rw         rw         rw           1         1         1         1         0		0	W	RE	12	
DX(FF)FF           5         4         3         2         1           BNKADDH         BNKADDL         CL           rw         rw         rw         rw         rw           1         1         1         1         0		0	V	ПP	11	SDR/
DX(FF)FF           5         4         3         2         1           BNKADDH         BNKADDL         CL           rw         rw         rw         rw         rw           1         1         1         1         0		0	W	MR	10	AM C
DX(FF)FF           5         4         3         2         1           BNKADDH         BNKADDL         CL           rw         rw         rw         rw         rw           1         1         1         1         0		0			9	ontr
DX(FF)FF           5         4         3         2         1           BNKADDH         BNKADDL         CL           rw         rw         rw         rw         rw           1         1         1         1         0	0x00;	0			8	<u>o</u> F
DX(FF)FF           5         4         3         2         1           BNKADDH         BNKADDL         CL           rw         rw         rw         rw         rw           1         1         1         1         0	3C	0			7	γес
Ox(FF)FF           4         3         2         1           KADDH         BNKADDL         CL           rw         rw         rw         rw           1         1         1         0	P	0	W	SCOL	6	jister
0x(FF)FF 3 2 1 BNKADDL CL rw rw rw 1 1 0		_	8	BNK	5	20
F <b>)FF</b>		_	₹	ADDH	4	-0(
F <b>)FF</b>		_		BNK⊅	3	0
F)FFFC04  1 BIT 0  CL RACL  TW TW  0 0		_		DDL	2	×(F
BIT 0 RACL  O		0	₹	CL	_	F)FF
		0	W		ВІТ 0	FC04

## Table 7-8. SDRAM Control Register Description

Name	Description	Setting
SDEN Bit 15	SDRAM Enable—When this bit is set, together with the DRAM enable bit (bit 9 of the CSD register) being set and the EDO bit (DRAMC register bit 10) being cleared, the SDRAM operation is enabled.	<ul><li>0 = SDRAM disable.</li><li>1 = SDRAM enable (see description for other bits that must be set).</li></ul>
CPM Bit 14	Continuous Page Mode—This bit enables the DRAM to operate in continuous page mode. DRAM will only be precharged during a page-miss condition.	0 = SDRAM not in continuous page mode. 1 = SDRAM in continuous page mode.
Reserved Bit 13	Reserved	This bit is reserved and must be set to 0.
RE Bit 12	Refresh Enable—This bit enables the refresh cycle for SDRAM.	0 = SDRAM Refresh cycle not enabled. 1 = SDRAM refresh cycle enabled.
<b>IP</b> Bit 11	Initiate All Bank Precharge Command—Setting this bit triggers the precharge command for all banks of SDRAM.	0 = IP command to SDRAM disabled. 1 = IP command to SDRAM enabled.
MR Bit 10	Initiate Mode Register Set Command—Setting this bit triggers the load mode register command to SDRAM.	0 = MR command to SDRAM disabled. 1 = MR command to SDRAM enabled.
Reserved Bits 9–7	Reserved	These bits are reserved and should be set to 0.
SCOL Bit 6	<b>SDRAM Column Option</b> —This bit selects the SDRAM column address MD0.	0 = PA1 (normally for 16-bit SDRAM). 1 = PA0 (normally for 8-bit SDRAM).
Bits 5–4	SDRAM High Order Bank Address Line Selection—A 2-bit bank register selection address is generated by selecting the appropriate CPU address line. This register bit allows selection of the high order bit.	00 = PA20. 01 = PA22. 10 = PA24. 11 = Force this bank address line to 0. See Table 7-9 on page 7-17 for programming examples.

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Table 7-8. SDRAM Control Register Description (Continued)

Name	Description	Setting
BNKADDL Bits 3–2	SDRAM Low Order Bank Address Line Selection—A 2-bit bank register selection address is generated by selecting the appropriate CPU address	00 = PA19. 01 = PA21. 10 = PA23.
	line. This register bit allows selection of the low order bit.	<ul><li>11 = Force this bank address line to 0.</li><li>See Table 7-9 for programming examples.</li></ul>
CL Bit 1	<b>CAS Latency</b> —This bit selects the CAS latency for the SDRAM cycle. The bit must be programmed before the initialization sequence.	0 = CAS latency is 1 clock count. 1 = CAS latency is 2 clock counts.
RACL Bit 0	Refresh to Active Command Latency—This bit selects the latency for SDRAM from refresh to active cycle.	0 = 3 Clock counts. 1 = 6 Clock counts.

Table 7-9.
SDRAM E
Bank A
ddress Pro
gramming
Examples

Application	BNKADDH	BNKADDL	Remarks
Make all SDRAM appear as one single bank	1	Cô	None
Two banks of SDRAM—for example, 16 Mbyte	00		Choose PA20 as bank selection address
Four banks of SDRAM—for example, 64 Mbyte	01	10	Choose PA22 and PA21 as bank selection address
Four banks of SDRAM—for example, 128 Mbyte	01	10	Choose PA22 and PA23 as bank selection address
Four banks of SDRAM—for example, 256 Mbyte	SČ	10	Choose PA24 and PA23 as bank selection address
Note: Those bits are all set is fill	O D A M Or Flort	Dago Modo al	Note: Those his are all not in EDO DAM or East Dogo Mode allowing the use of only one page register.



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# 7.3.4 SDRAM Power-down Register

bit position and values are shown in the following register display. The details about the register settings are described in Table 7-10. This register controls how the SDRAM and the MC68VZ328 operate during a power-down operation. The

SDPWDN B 1 AP TYPE RESET	APEN O	BIT 14 15 APEN PDEN rw rw 0 0	0 13	SDF 12	SDRAM Po	10 PDTOL rw	<u> </u>	9r-dov 9 JT[3:0] rw	er-down R 9 8 0 173:0] 0 0	9 8 7 9 17[3:0] 7 7 7 7 8 7 9 7 9 7 9 7 9 7 9 9 9 7 9 9 9 7 9	SDRAM Power-down Register  12	9 8 7 6 5  7[3:0]	9 8 7 6 5 4 9 7 6 5 4 0 0 0 0 0 0	5 4 3 <b>9</b>	5 4 3 <b>9</b>	9 8 7 6 5 4 3 2 1 BIT 0 173:0]  Try rw rw 0 0 0 0 0 0 0 0 0 0 0
	BIT 15	14	13	12	<u> </u>	10	9	œ	7		0	5	6 5 4	6 5 4 3	6 5 4 3 2	6 5 4 3 2 1
	APEN	PDEN				РДТОПТ[3:0]	T[3:0]				4					
TYPE	W	W	,		₹		₹	W								
D II C II I	0	0	0	0	0	0	0	0	0	- 74	0	0 0	0 0 0	0 0 0 0	0 0 0 0 0	0 0 0 0 0 0
7 0 0							0x0000	000	O	-	4	4				

able 7-10. SDRAM Power-down Register Description

	Reserved Bits 7–0	PDTOUT [3:0] Bits 11–8	Reserved Bits 13–12	PDEN Bit 14	APEN Bit 15	Name
ARCHIVEDBY	Reserved	SDRAM Precharged Power-down Time Out—The bit is set to make the SDRAM Chip Enable signal go low when a time out occurs when the PDEN bit is set. Each binary unit represents a maximum of 128 clocks. When in power-down mode, SDRAM can be woken by a CPU or LCD access.	Reserved	SDRAM Precharged Power-down Enable—The bit is set to make the SDRAM Chip Enable signal go low when the DRAM controller is not sending a command after the SDRAM is precharged for a certain time. The time depends on the value in PDTOUT[3:0].	SDRAM Active Power-down Enable—The bit is set to make the SDRAM Chip Enable signal go low immediately when the DRAM controller is not sending a command, writing data, or reading data with the SDRAM.	Description
	These bits are reserved and should be set to 0.	See the description.	These bits are reserved and should be set to 0.	0 = PDEN disabled. 1 = PDEN enabled.	0 = APEN disabled. 1 = APEN enabled.	Settings



## Freescale Semiconductor, Inc.

### Chapter 8 \_CD Controller

directly from system memory through periodic DMA transfer cycles. For this reason, an understanding of Controller." The LCD controller uses very little bus bandwidth, giving the core sufficient processing time the DRAM controller is recommended. For more information, please refer to Chapter 7, "DRAM display data for external LCD drivers or for an LCD panel. The LCD controller fetches display data programming information necessary to implement it in design projects. The LCD controller provides This chapter describes the operation of the liquid crystal display (LCD) controller and supplies the <sup>INC.</sup> 2005

## LCD Controller Features

The following list describes the features of the LCD controller.

- Both system and display memory that is shared, so that dedicated video memory is not required
- Standard panel interface for industry-standard LCD drivers
- of image data with software Support for single (nonsplit) monochrome screen and color STN LCD panels through preprocessing

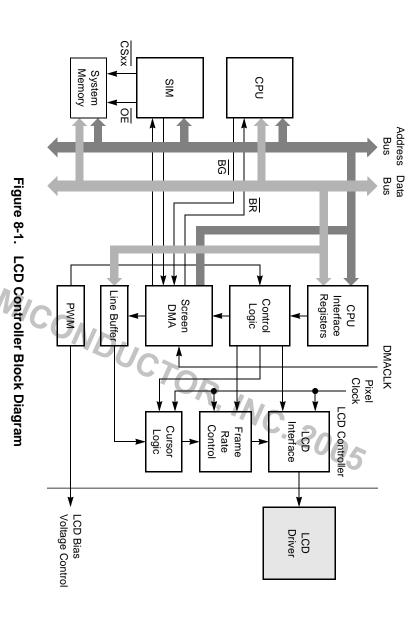
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- Fast fly-by-type, 16-bit-wide, burst DMA screen-refresh transfers from system memory
- Maximum display size of  $640 \times 512$  pixels
- Panel interface for 8-, 4-, 2-, and 1-bit-wide LCD data bus
- 16 simultaneous grayscale levels from a palette of 16 density levels
- Hardware blinking cursor that is programmable to a maximum of  $31 \times 31$  pixels
- Hardware panning (soft horizontal and vertical scrolling)
- 8-bit PWM for software contrast control
- New FRC algorithm that improves the flickering effect found in 4- and 16-grayscale LCD panels
- Support for self-refresh-type LCD panels ARCHIVEL



# LCD Controller Operation Freescale Semiconductor, Inc.



# .2 LCD Controller Operation

are organized. buffer, cursor logic, frame rate control, and an LCD panel interface. The LCD controller consists of CPU interface registers, control logic, a screen DMA controller, a line Figure 8-1 illustrates how these blocks

controller. The DMA generates a bus request (BR) signal to the core, and when the bus is granted, it the programmable number of clocks per transfer, which makes it easier to support a system with memory performs a few memory bursts to fill up the line buffer. The number of DMA clock cycles in each burst is The CPU interface registers provide control of different features of the LCD controller. Connected to the CPU bus, the control logic provides the internal control and counting signals for other blocks in the LCD with different speed grades.

blinking rate is adjustable when the BKEN bit in the LCD blink control (LBLKC) register is set number between 1 and 31 is used. The cursor may also be completely black or reversed video, and the logic block. The input is synchronized with the fast DMA clock, while the output is synchronized to the The line buffer collects display data from system memory during DMA cycles and outputs it to the cursor block-shaped cursor on the display screen. The height and width of the cursor can be changed, as long as a relatively slow LCD pixel clock. The cursor control logic, when enabled, is used to generate a

times that a pixel is turned on when the display is refreshing. Since crystal formulations and driving out of 16 density levels, as shown in Table 8-1 on page 8-7. The density level corresponds to the number of mapping register (LGPMR). Frame rate control is mainly used for grayscale displays and generates a maximum of 16 grayscale levels voltage may vary, the quality of the grayscale can be fine-tuned by programming the LCD gray palette

# Freescale Semiconductor, Inco Controller Operation

to suit different LCD panel requirements. panel's data bus. The polarity of the LFLM, LP, and LCLK signals and pixel data can all be programmed The LCD interface logic is used to pack the display data into the correct size and output it to the LCD

# Connecting the LCD Controller to an LCD Panel

The following signals are used to connect the LCD controller to an LCD panel:

- output pixel data can be negated through programming. See Section 8.3.10, "LCD Polarity Configuration Register," for more information. The LCD controller is initially configured to drive single-screen monochrome LCD panels. The data bus size for an LCD panel can be configured to Data is arranged differently on the bus, depending on which LCD panel mode is selected. The LD[7:0]—The LCD Data bus lines transfer pixel data to the LCD panel so that it can be displayed. 1, 2, 4, or 8 bits by programming the LPICF register.
- for more information. it deasserts and remains inactive until the next frame. The LFLM can be programmed to be an active high or active low signal in software. See Section 8.3.10, "LCD Polarity Configuration Register," active after the last line pulse of the frame and remains active until the next line pulse, at which point The LCD Frame Marker signal indicates the start of a new display frame. LFLM becomes
- Polarity Configuration Register," for more information. can be programmed to be an active high or active low signal in software. See Section 8.3.10, "LCD -The LCD Line Pulse signal is used to latch a line of shifted data onto an LCD panel. The LLP
- software. See Section 8.3.10, "LCD Polarity Configuration Register," for more information. is synchronized. The LCLK can be programmed to be an active high or active low signal in LCLK—The LCD Shift Clock signal is the clock output to which the output data to the LCD panel
- 0, which enables the LACD signal to toggle on every frame. See Section 8.3.11, "LACD Rate Control Register," for more information. number N is equal to the alternation code's 7-bit value plus one. The default value for LACDRC programmed so that the LACD will toggle once every 1 to N frames or LLP pulse. The targeted The LACD signal will toggle after a preprogrammed number of FLM or LP pulses. It can be polarization on the panel. This signal can be programmed to toggle for a period of 1 to 16 frames. —The LCD Alternate Crystal Direction output signal is toggled to alternate the crystal

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### 8.2.1.1 Panel Interface Timing

line, while the LFLM signal marks the first line of the displayed page. drivers' internal shift register. The LLP signal latches the shifted pixel data into a wide latch at the end of a is timed by the LCLK, LLP, and LFLM signals. The LCLK signal clocks the pixel data into the display The LCD controller continuously passes the pixel data into the LCD panel via the LCD data bus. The bus

the end of the current line of serial data. The LLP signal enclosed by the LFLM signal marks the end of the illustrates the LCD interface timing for 1-, 2-, and 4-bit LCD data bus operation. The LLP signal signifies first line of the current frame. The LCD controller is designed to support most monochrome LCD panels. Figure 8-2 on page 8-4

configuration (LPOLCF) register to 1. In addition to the interface timing pins, the LACD pin will toggle the polarity of these signals, set the FLMPOL, LPPOL, LCKPOL, and PIXPOL bits in the LCD polarity Some LCD panels can use an active low LFLM, LLP, or LCLK signal and reversed pixel data. To change after a preprogrammed number of LFLM pulses. The purpose of this pin is to prevent the crystal in the LCD panel from degrading.



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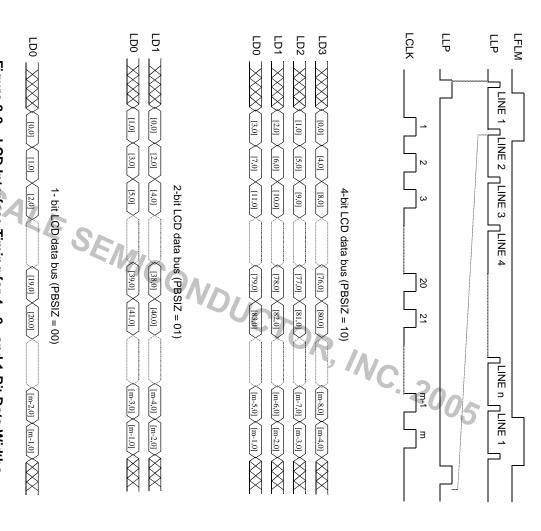


Figure 8-2. LCD Interface Timing for 4-, 2-, and 1-Bit Data Widths

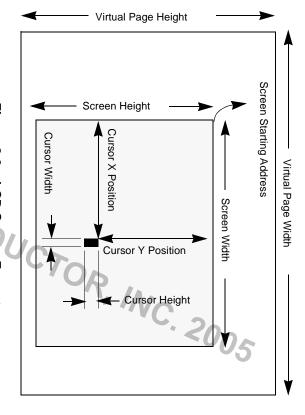
### **8.2.2** Controlling the Display

 $320 \times 240$  for gray level display may cause flickering due to a slow refresh rate. The best efficiency is achieved when the screen width is a multiple of the DMA controller's 16-bit bus width. pixels in black-and-white display and  $320 \times 240$  pixels in gray level display. A screen size larger than The LCD controller is designed to drive single-screen monochrome STN LCD panels with up to  $640 \times 512$ 

### 8.2.2.1 Format of the LCD Screen

illustrates the relationship between the portion of a large graphics file displayed on the screen and the actual page. The units in the figure are measured in pixel counts. The screen width and height of the LCD panel are programmable through software. Figure 8-3 on page 8-5





Freescale Semiconductor, InccD Controller Operation

Figure 8-3. Screen Format

displayed on the LCD panel. to by the LCD screen starting address (LSSA) register. Therefore, the shaded area in Figure 8-3 will be The LCD screen width (LXMAX) and LCD screen height (LYMAX) registers are where the size of the LCD panel is specified. The LCD controller will start scanning the display memory at the location pointed

the screen. The LVPH parameter shows the bottom of the page, but it is not used by the LCD controller. programmer, through software, to position the starting address so that the scanning logic's system memory horizontally scrolled (panned) anywhere inside the virtual page boundaries. However, it is up to the virtual page height parameters. By changing the LSSA register, a screen-sized window can be vertically or The maximum page width and page height are specified by the LCD virtual page width (LVPW) and LCD pointer does not stretch beyond the virtual page width or height. Otherwise, strange objects will appear on

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### Format of the Cursor

can be shown with different properties. These properties can be transparent (cursor is disabled), full (black setting the BKEN bit in the LBLKC cursor), reversed video, full (white cursor), or blinking. The hardware cursor blink can be made to blink by window specified by the cursor's reference position, cursor width, and cursor height, the original pixel bits pixel counter), specifies the screen position of the pixel data being processed. When the pixel falls within a to keep track of the current pixel's vertical position. YCNT, in conjunction with XCNT (the horizontal To define the position of the hardware cursor, the LCD controller maintains a vertical line counter (YCNT) periodically. The speed at which the cursor blinks may be controlled by selecting the BDx bit in the LBLKC register. The half-period may be as long as 2 seconds. ARCHIVE



# LCD Controller Operation Freescale Semiconductor, Inc.

### Mapping the Display Data

or fully off. The LCD controller supports 1 or 2 bits per pixel graphics mode. In the 1-bit mode, each bit in the display memory corresponds to a pixel in the LCD panel. The corresponding pixel on the screen is either fully on illustrates how the system memory data in both modes are mapped LCD panel, program the appropriate bit in the corresponding address of the display memory. Figure 8-4 In 2-bit mode, each pixel is represented by two bits of display memory. To map the data to the

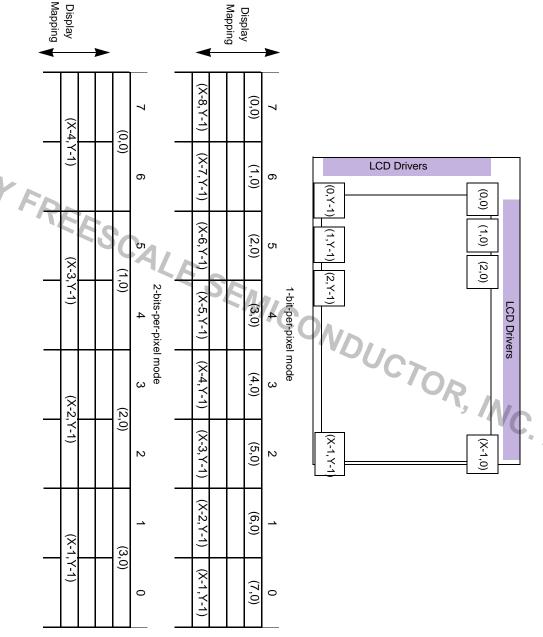


Figure 8-4. Mapping Memory Data on the Screen

## **Generating Grayscale Tones**

registers to program the grayscale level. between black and white can be selected using the information in Table 8-1 on page 8-7. Use the LGPMR can generate 16 simultaneous grayscale levels out of a palette consisting of 16 shades. The two levels LCD panel by adjusting the density of ones and zeroes that appear over the frames. The LCD controller In 2-bits-per-pixel mode, circuitry inside the LCD controller generates intermediate grayscale tones on the



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### Freescale Semiconductor, Inco Controller Operation

**Table 8-1. Grey Palette Density** 

1	1	a a
0.933	14/15	Э
0.875	7/8	D
0.8	4/5	О
0.75	3/4	В
0.666	2/3	А
0.6	3/5	6
0.555	5/9	8
0.5	1/2	7
0.444	4/9	9
0.4	2/5	5
0.333	1/3	4
0.25	1/4	3
0.2	1/5	2
0.125	1/8	1
05	0	0
Density (in Decimal)	Density	Gray Code (Hex)

eleven-sixteenths, and one. This flexible mapping scheme allows optimizing the visual effect for the specific panel or application during a four-level grayscale display mode. and one might be more visually pleasing than a linearly spaced scale like zero, five-sixteenths related to the frame rate. For certain types of graphics, a logarithmic scale like zero, one-fourth, one-half, Since crystal formulations and driving voltages vary, the visual grayscale effect may or may not be linearly The Controlling Frame Rate Modulation function available in previous NOTE:

ARCHIVED MC68VZ328. versions of the DragonBall integrated processor

### 8.2.3 Using Low-Power Mode

pin. The software can be programmed to achieve PANEL\_OFF by using parallel I/O in the following an MC68VZ328 system, this signal is not supported, but can be easily implemented using a parallel I/O Some panels may have a PANEL\_OFF signal, which is used to turn off the panel for low-power mode. In

- 1. Drive the LCD bias voltage to 0 V.
- Set the LCDON bit to 0 in the LCD clocking control (LCKCON) register, turning off the LCD controller.

To turn the LCD controller back on, follow the following steps:

- Set the LCDON bit to 1 in the LCKCON register, which turns on the LCD controller.
- 2. Pause for 1 or 2 ms.
- 3. Drive the LCD bias voltage to +15 V or -15 V.

refresh operations will then be halted in this mode. When the LCD controller is turned back on, DMA and by stopping its own pixel clock prior to the next line buffer fill DMA. Further screen DMA and display When setting the LCDON bit in the CLKCON register to 0, the LCD controller will enter low-power mode screen refresh activities will resume synchronously.

## 8.2.4 Using the DMA Controller

obstruction by using zero LCD access wait-states (one clock per access). chip-select logic inside the system integration module. It is possible to minimize bus bandwidth output enable and chip-select signals for the corresponding system memory chip are asserted by the memory. The read data is then internally passed to the internal pixel buffer. During the LCD access cycles buffer needs data, it asserts the BR signal to request the bus from the core. Once the core grants the bus transfer is required. Each cycle is evenly distributed across the time frame. Every time the internal line transferred to the corresponding pixels on the screen. To minimize bus obstruction, a burst type and fly-by to be continuously refreshed at a rate of 50 Hz to 70 Hz, the pixel bits in the memory will be read and The LCD DMA controller is a fly-by-type, 16-bit-wide, fast data transfer device. Since the LCD screen has (BG is asserted), the DMA controller gets control of the bus signal and issues a number of words read from

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# **8.2.4.1** Bus Bandwidth Calculation Example

issues involved in estimating bandwidth overhead to the data bus. Consider a typical scenario: Since LCD screen refresh occurs periodically, the load that the LCD controller puts on the host data bus becomes an important consideration to the high-performance handheld system designer. There are many

- Screen size:  $320 \times 240$  pixels
- Bits per pixel: 2 bits per pixel
- Screen refresh rate: 60 Hz
- System clock: 16.58 MHz
- Host bus size: 16 bit
- DMA access cycle: 2 cycles per 16-bit word

The following T<sub>1</sub> period is used by the LCD controller to update one line of the screen:



8-0

# Freescale Semiconductor, InccD Controller Operation

$$\Gamma_1 = \frac{1}{60 \text{ Hz}} \times \frac{1}{240 \text{ lines}}$$
$$= 69.4 \text{ } \mu\text{s}$$

cycle will hold up the bus: During the same period, the line buffer must be filled. The following  $T_{DMA}$  duration is how long the DMA

$$T_{DMA} = \frac{320 \text{ pixels} \times 2 \text{ bits per pixel} \times 2 \text{ clocks}}{16.67 \text{ MHz} \times 16 \text{-bit bus}}$$

$$= 4.8 \text{ } \mu\text{s}$$

Thus, the percentage of host bus time taken up by the LCD controller's DMA is  $P_{\mathrm{DMA}}$ :

$$P_{\text{DMA}} = \frac{4.8, \, \mu \text{s}}{69.4, \, \mu \text{s}}$$
  
= 6.92,%

### Self-Refresh Mode

pulse. mode, the LCD module will update the screen periodically from internal RAM using the LP and FRM The LCD driver from Epson was used as a reference for the design of the refresh mode. In self-refresh DUCTOR,

### 8.2.5.1 **Entering Self-Refresh Mode**

frame is reached. The LP and FRM pulse continue as in normal mode, but there are no pulses on either the Setting the self-refresh register bit 7 to 1 means that the LSCLK and LD will remain 0 when the end of the LSCLK or LD.

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### Canceling Self-Refresh Mode

is reached. On entering normal mode, data is sent out from the beginning of the page Setting the self-refresh register bit 7 to 0 means that the normal mode is entered when the end of the frame ARCHIVED BY FREE

### 8.3 Programming Model

sample programming examples. The remaining sections of this chapter provide detailed descriptions of the registers, their settings, and

### **LCD Screen Starting Address** Register

settings for the bits in the register are listed in Table 8-2 to be displayed. The bit assignments for the register are shown in the following register display. The The LCD screen starting address (LSSA) register is used to inform the LCD panel where to fetch the data

LSSA			_	CD	Scre	en S	tartir	LCD Screen Starting Address Register	ddres	ss Re	egist	er	_	)×(FF	" FF	)x(FF)FFFA00
	ВІТ 31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	BIT 16
	SSA 31	SS A30	SS A29	SS A28	SS A27	SS A26	SS A25	SS A24	SS A23	SS A22	SS A21	SS A20	SS A19	SS A18	SS A17	SSA 16
TYPE	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7 0 0								0x0000	000							
	2	3	3 3	i	:	3 3		9	-	}	}	}	}	1	-	(
	SSA 15	SS A14	SS A13	SS A12	SS A11	SS A10	SS A9	SS A8	SS A7	SS A6	SS A5	SS A4	SS A3	SS A2	SS A1	
TYPE	W	W	W	W	W	W	MJ	W	W	W	W	W	W	W	W	
RESET	0	0	0	0	0	0	S	0	0	0	0	0	0	0	0	0
- - -						_		0x0000	000							
							4									

Table 8-2. LCD Screen Starting Address Register Description

Name	Description	Setting
SSAx Bits 31–1	Screen Starting Address 31–1—This field is the screen starting address of the LCD panel. The LCD controller will start fetching pixel data from system memory at this address. This field must start at a location that will enable a complete picture to be stored in 1 Mbyte memory boundary (A[19:00]). In other words, A[31:20] has a fixed value for a picture's image.	See description.
Reserved Bit 0	Reserved	This bit is reserved and should be set to 0.



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**Programming Model** 

# **LCD Virtual Page Width Register**

assignments for the register are shown in the following register display. The settings for the bits in the register are listed in Table 8-3. The LCD virtual page width (LVPW) register contains the width of the displayed image. The bit

	RESET	TYPE			LVPW
	_	W	VP8	BIT 7	
	_	W	VP7	6	LCD
	_	W	VP6	5	Virtual
OXIT	1	W	VP5	4	Page Width
)/	<b>P</b> .	W	VP4	3	n Register
	_	W	VP3	2	<(
	_	rw	VP2	1	0x(FF)
	_	W	VP1	BIT 0	FFFA05

### Table 8-3. **LCD Virtual Page Width Register Description**

Name	Description	Setting
VPx Bits 7–0	WPx Virtual Page Width 8–1—These bits specify the virtual page width of the LCD panel Bits 7–0 in terms of word count. The virtual page width is the virtual width in pixels divided by 16 for a black-and-white display, by 8 for a 4-grayscale display, and by 4 for a 16-grayscale display.	See descrip- tion

## **LCD Screen Width Register**

register display. The settings for the bits in the register are listed in Table 8-4. This register must be a multiple of 16. The bit assignments for the register are shown in the following The LCD screen width register (LXMAX) is used to specify the width of the LCD panel's screen in pixels

LXMAX					LCD Screen Width Register	ocre	en ∨	Vidth	Regi	ster			0x	(FF	)FF	)x(FF)FFFA08
	BIT 15 14 13 12	14	13	12	11	10	9	œ	7	6	Οī	4	ω	2	_	ВІТ 0
					177		XM9	XM8	2MX	XM9	XM5	XM4				
TYPE					1/1		W	W	W	W	W	W				
о п о п	0	0	0	0	0	0	_	_	_	_	_	_	0	0	0	0
7 17 6 17				E.				0x03F0	FO							

### Table 8-4. LCD Screen Width Register Description

Name	Description	Setting
Reserved Bits 15–10	Reserved	These bits are reserved and should be set to 0.
XMx Bits 9–4	<b>Maximum Width 9–4</b> —These bits represent the width of the LCD panel in the number of pixels.	See description.
Reserved Bits 3–0	Reserved	These bits are reserved and should be set to 0.

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### Programming Model

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# 8.3.4 LCD Screen Height Register

the register are listed in Table 8-5 The bit assignments for the register are shown in the following register display. The settings for the bits in The LCD screen height register (LYMAX) is used to define the height of the LCD panel's screen in pixels.

### LYMAX 3 12 LCD Screen Height Register 8MX YM7 YM6 YM5 YM4 YM3 ω 0x(FF)FFFA0A YM2 YM1 MY M

## Table 8-5. LCD Screen Height Register Description

RESET

0

0

0

0

0

0 0

0x01FF

₹

W

₹

TYPE

Name	Description	Setting
Reserved Bits 15–9	Reserved	These bits are reserved and should be set to 0.
YMx Bits 8–0	Maximum Height 8-0—These bits represent the height of the LCD panel in the number of pixels, which is equal to YMAX + 1.	See description.

# 8.3.5 LCD Cursor X Position Register

on the LCD panel. The bit assignments for the register are shown in the following register display. The settings for the bits in the register are listed in Table 8-6. The LCD cursor X position (LCXP) register is used to determine the horizontal pixel position of the cursor

LCXP				LCD Cursor X Position Register	O D	sor >	^ Po	sitior	า Re	giste	Pr		0	)×(FI	F)FF	FFFA18
	BIT 15	14	13	12	41	10	9	8	7	6	5	4	3	2	1	BIT 0
	CC1	000			7		CX P9	CX P8	CX P7	96 CX	CX P5	CX P4	CX P3	CX P2	P1	CXP0
TYPE	W	W		9	,		W	W	W	W	ſW	W	W	W	W	rw
D D D D D D D D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7 10 01			) i .	~				0x0000	0							

# Table 8-6. LCD Cursor X Position Register Description

Name	Description	Setting
<b>CCx</b> Bits 15–14	Cursor Control 1 and 0—These bits are used to control the format of the cursor.	00 = Transparent, cursor is disabled. 01 = Full (black) cursor. 10 = Reversed video. 11 = Full (white) cursor.
Reserved Bits 13–10	Reserved	These bits are reserved and should be set to 0.

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Table 8-6. LCD Cursor X Position Register Description (Continued)

CXPx C Bits 9–0 h	Name
Cursor X Position 9–0—These bits represent the cursor's horizontal starting position, X, in terms of pixel count (from 0 to XMAX).	Description
See description.	Setting

### 8.3.6 **LCD Cursor Y Position Register**

settings for the bits in the register are listed in Table 8-7. the LCD panel. The bit assignments for the register are shown in the following register display. The The LCD cursor Y position (LCYP) register is used to determine the vertical pixel position of the cursor on

;	ZD	_			5
 	RESET	TYPE			LCYP
	0			BIT 15 14 13 12 11 10 9	
	0			14	
	0			13	
	0			12	_
	0 0 0 0 0			11	CD.
	0			10	C
	0			9	rsor
7 //	0	W	CYP 8	8	<b>∀</b> P
0x000	0	W	CYP CYP	7	LCD Cursor Y Position
Ō	0	۲W	CYP 6	6	n Re
	0	W	CYP 5	5	≷egisteı
	0	W	CYP 4	4	7
	0	W	CYP 3	ω	
	0	W	CYP 2	2	0x(F
	0	W	CYP 1	1	FF)FFFA1
	0	W	CYP0	BIT 0	FA1A
				-	

Table 8-7. LCD Cursor Y Position Register Description

	CYPx Bits 8–0	Reserved Bits 15–9	Name
ARCHIVED BY FREES	<b>Cursor Vertical Y Pixel 8–0</b> —These bits represent the cursor's vertical starting position, Y, in terms of pixel count (from 0 to YMAX).	Reserved	Description
	See description.	These bits are reserved and should be set to 0.	Setting

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# **LCD Cursor Width and Height Register**

cursor, in screen pixels. The bit assignments for the register are shown in the following register display. The settings for the bits in the register are listed in Table 8-8. The LCD cursor width and height (LCWCH) register is used to determine the width and height of the

BIT	LCWCH
4	
13	
12	LCD Cursor W
<del></del>	Curso
10	or Wid
9	Vidth and Height Register
∞	<u>T</u>
7	eigh
0	t R
6 5 2	egis
4	ster
ω	
2	0x(FF)
<u> </u>	:)FF
BH	)FFFA1C

7 0 0	0 0 1 1	TYPE		
	0			BIT 15
	0			14
	0			13
	0	V	CW4	12
	0	W	CW3	11
	0	W	CW2 CW1 CW0	10
0x0101	0	V	CW1	9
	_	V	CW0	8
0,	0 0 0	7 4	>	7 6 5
	0	V	CH4	4
	0	W	СН3 СН2	3
	0	₹	CH2	2
	0	₹	СН1 СН0	_
	_	W	СНО	BIT 0

Table 8-8. **LCD Cursor Width and Height Register Description** 

Name	Description	Setting
Reserved Bits 15–13	Reserved	These bits are reserved and should be set to 0.
CWx Bits 12–8	Cursor Width 4–0—These bits specify the width of the hardware cursor in pixel count (from 1 to 31).	See description.
Reserved Bits 7–5	Reserved	These bits are reserved and should be set to 0.
CHx Bits 4–0	Cursor Height 4–0—These bits specify the height of the hardware cursor in pixel count (from 1 to 31).	See description.
Note: The cursor is disa	<b>Note:</b> The cursor is disabled if the CWx or CHx bits are set to 0.	

## 3.3.8 LCD Blink Control Register

Table 8-9 on page 8-15. the register are shown in the following register display. The settings for the bits in the register are listed in The LCD blink control register (LBLKC) is used to control how the cursor blinks. The bit assignments for ARCHIVED BY FI



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LBLKC	ВІТ 7	LCD I		Blink Control Register	egister 3	N	0x(FF)	FFFA1F
	BIT 7	6	5	4	З	2	1	BIT 0
	BKEN	BD6	BD5	BD4	BD3	BD2	BD1	BD0
TYPE	W	W	W	W	W	W	W	W
RESET	0	_	_	_	_	0	_	_

Table 8-9. **LCD Blink Control Register Description** 

Name	Description	Setting
BKEN B	Blink Enable—This bit determines if the cursor will blink or remain steady.	1 = Blink is enabled 0 = Blink is disabled (default)
Bits 6-0 o	Blink Divisor 6–0—These bits determine if the cursor will toggle once per a specified number of internal frame pulses plus one. The half-period may be as long as 2 seconds.	See description

### LCD Panel Interface **Configuration Register**

register are shown in the following register display. The settings for the bits in the register are listed in The LCD panel interface configuration (LPICF) register is used to determine the data bus width of the LCD panel and to determine if it is a black-and-white or grayscale display. The bit assignments for the

LPICF	LCD	Panel I	LCD Panel Interface Configuration Register	Configura	ation Re	gister	0x(FF	)FFFA20
	BIT 7	6	Ŋ	4	ω	2	_	ВІТ 0
			1/		PBS	PBSIZ1-0	G	GS1-0
TYPE			X		W	W	W	rw
D II COIT	0	0	0	0	0	0	0	0
- -		Fo	-0	0x00	00			

Table 8-10. LCD Panel Interface Configuration Register Description

Name	Description	Setting
Reserved Bits 7–4	Reserved 2	These bits are reserved and should be set to 0.
<b>PBSIZ1-0</b> Bits 3-2	Panel Bus Width 1-0—These bits specify the bus width of the LCD panel.	00 = 1 bit. 01 = 2 bit. 10 = 4 bit. 11 = 8 bit.
<b>GS1-0</b> Bits 1-0	<b>Grayscale Mode Selection 1–0</b> —These bits determine the mode of operation of the grayscale display device.	00 = Black-and-white mode. 01 = Four-level grayscale mode. 10 = Sixteen-level grayscale mode. 11 = Reserved.

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### **Programming Model**

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# 8.3.10 LCD Polarity Configuration Register

settings for the bits in the register are listed in Table 8-11. the LCD panel. The bit assignments for the register are shown in the following register display. The The LCD polarity configuration (LPOLCF) register controls the polarity of the interface signal that goes to

### **LPOLCF** RESET TYPE BIT 7 0 LCD Polarity Configuration Register 0 0 0 0x00 LCKPOL 0 FLMPOL 0 0x(FF)FFFA21 LPPOL 0 PIXPOL 0

Table 8-11. LCD Polarity Configuration Register Description

Reserved Bits 7–4  LCKPOL Bit 3  Reserved  CCD Shift Clock Polarity—This bit controls the polarity of the active edge of the LCD shift clock.  FLMPOL Bit 2  Frame Marker Polarity—This bit controls the polarity of the frame marker.  LPPOL Bit 1  PIXPOL Bit 0  Pixel Polarity—This bit controls the polarity of the line pulse.	Name	Description	Setting
δ λ ο ο ο ο	Reserved Bits 7–4	Reserved	These bits are reserved and should be set to 0.
5 x o	LCKPOL Bit 3	<b>LCD Shift Clock Polarity</b> —This bit controls the polarity of the active edge of the LCD shift clock.	0 = Active negative edge of LCLK. 1 = Active positive edge of LCLK.
δΓ λ	FLMPOL Bit 2	<b>Frame Marker Polarity</b> —This bit controls the polarity of the frame marker.	0 = Frame marker is active high. 1 = Frame marker is active low.
<u>Б</u>	LPPOL Bit 1	<b>Line Pulse Polarity</b> —This bit controls the polarity of the line pulse.	0 = Line pulse is active high. 1 = Line pulse is active low.
	PIXPOL Bit 0	Pixel Polarity—This bit controls the polarity of the pixels.	0 = Pixel polarity is active high. 1 = Pixel polarity is active low.

# 3.3.11 LACD Rate Control Register

The settings for the bits in the register are listed in Table 8-12 on page 8-17 The LCD alternate crystal direction rate control (LACDRC) register is used to control the alternate rates of the liquid crystal direction. The bit assignments for the register are shown in the following register display



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LACDRC		LACE	Rate C	_ACD Rate Control Register	egister		0x(FF)	FFFA23
	BIT 7	6	Οī	4	ω	2	_	ВІТ 0
	ACDSLT	ACD6	ACD5	ACD4	ACD3	ACD2	ACD1	ACD0
TYPE	ſW	W	W	W	W	W	W	ſW
D D D D D D D D D D D D D D D D D D D	0	0	0	0	0		0	0
7 0 0				Q.	0x00	?(		

Table 8-12. LACD Rate Control Register Description

Name	Description	Setting
ACDSLT i	Clock Source Select—This bit selects the clock source for the internal counter that generates an LACD signal.	0 = Select frame pulse as input clock 1 = Select line pulse as input clock
ACDx Bits 6-0	Alternate Crystal Direction Control 6–0—These bits represent the ACD toggle rate control code. The LACD signal will toggle once every 1 to 128 FLM/LP cycles based on the value specified in this register. The actual number of FLM cycles is the value programmed plus one. Shorter cycles tend to give better results.	See description

# 8.3.12 LCD Pixel Clock Divider Register

clock. The bit assignments for the register are shown in the following register display. The settings for the bits in the register are listed in Table 8-13. The LCD pixel clock divider (LPXCD) register is used to program the divider, which generates the pixel

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LPXCD		LCD Pi)	kel Clock	( Divider	LCD Pixel Clock Divider Register	,	0x(FF)	FFFA25
	BIT 7	6	σ	4	ω	2	_	ВІТ 0
		2	PCD5	PCD4	PCD3	PCD2	PCD1	PCD0
TYPE			W	W	W	W	W	ľW
D III O III II	0	0	0	0	0	0	0	0
7 0 0		RE		Q	0x00			

Table 8-13. LCD Pixel Clock Divider Register Description

Name	Description	Setting
Reserved Bits 7–6	Reserved	These bits are reserved and should be set to 0.
PCDx Bits 5–0	<b>Pixel Clock Divider 5–0</b> —These bits represent the pixel clock divisor. The LCDCLK signal from the PLL is divided by N (PCD5–0 + 1) to yield the actual pixel clock. Values of 1–63 will yield N = 2 to N = 64. If these bits are set to 0 (N = 1), the PIX clock will be used directly, bypassing the divider circuit. Refer to Chapter 4, "Clock Generation Module and Power Control Module," for more information.	See description.

### Programming Model

## Freescale Semiconductor, Inc.

# 8.3.13 LCD Clocking Control Register

settings for the bits in the register are listed in Table 8-14. memory cycle. The bit assignments for the register are shown in the following register display. The The LCD clocking control (LCKCON) register is used to enable the LCD controller and control the LCD

LCKCON		LCD C	LCD Clocking Control F	Control	ol Register		0x(FF)	FFFA27
	BIT 7	6	5	4	3	2	1	BIT 0
	LCDON				Unused			
TYPE	۲W	ſW	W	W	W	W	W	rw
RESET	0	0	0	0	0,	0	0	0
7 [ 0 [				Ç	00%			

Table 8-14. LCD Clocking Control Register Description

Name	Description	Setting
LCDON Bit 7	<b>LCD Control</b> —This bit enables the LCD controller. Default is off.	0 = Disable the LCD controller 1 = Enable the LCD controller
Unused Bits 6–0	These bits are not used by the chip and may be used for temporary storage. At reset these bits are cleared.	See description

# 8.3.14 LCD Refresh Rate Adjustment Register

introducing an idle interval between alternate LCD DMA and display cycles. The bit assignments for the register are shown in the following register display. The settings for the bits in the register are listed in The LCD refresh rate adjustment (LRRA) register is used to fine-tune the display refresh rate by

LRRA			LCD	LCD Refresh Rate Adjustment Register	esh F	Rate /	√dju	stm	ent l	Regi	ister		0	×(F	(FF)FFFA2	FA28
	BIT 15	14	13	12	11	10	9	œ	7	6	Ŋ	4	ω	2	_	ВІТ 0
				M							RR	RRA[9:0]				
TYPE				7			۲W	W	W	W	ſW	W	W	rw rw rw rw rw rw rw rw	W	W
DE CET	0	0	0	0	0	0	0	0	_	_	_	_	_	_	_	_
7 0 1			2				0x0	0x00FF								

Table 8-15. LCD Refresh Rate Adjustment Register Description

Name	Description	Setting
Reserved	Reserved	These bits
Bits 15-10	7/	arereserved
		and should
	°C	be set to 0.
	V	

### Semiconductor, Inc. **Programming Model**

Table 8-15. LCD Refresh Rate Adjustment Register Description (Continued)

Name	Description
RRAx Bits 9-0	<b>Refresh Rate 9–0</b> —These bits contain the frame period, which can be calculated as follows:
	FRAME PERIOD = (12 + XMAX + RRA) x YMAX x (PXCD + 1) x LCDCLK_PERIOD where:
	Frame period = time for each screen update
	XMAX = screen width in number of pixels
	RRA = hexadecimal value stored in the LRRA register
	YMAX = screen height in number of pixels
	PXCD = hexadecimal value stored in the LPXCD register
	LCDCLK_PERIOD: refer to Section 4.4.1, "PLL Control Register," on page 4-8 for
	setting LCDCLK period

# 8.3.15 LCD Panning Offset Register

bits in the register are listed in Table 8-16. The LCD panning offset register (LPOSR) is used to control how many pixels the picture is shifted to the The bit assignments for the register are shown in the following register display. The settings for the

LPOSR		LCD Pani		ning Offset Ro	Register		0x(FF)	FFFA2D
	BIT 7	6	5	4	3	2	1	ВІТ 0
					POS3	POS2	POS1	POS0
TYPE			36		W	W	W	W
D III O III III III III III III III III	0	0	0	0	0	0	0	0
7 0 0 0			LE	0x00	90			
			1/					

Table 8-16. LCD Panning Offset Register Description

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Name	Description	Setting
Reserved Bits 7–4	Reserved	These bits are reserved and should be set to 0.
POSx Bits 3–0	<b>Pixel Offset Code</b> —These bits specify the number of pixels being shifted to the left of the display panel. This is independent of the black-and-white or gray mode.	0001 = Picture is shifted 1 pixel to the left. 0010 = Picture is shifted 2 pixels to the left
	niode.	1111 = Picture is shifted 15 pixels to the left.
Note: W	Note: When the LOPSR register is being modified, the software must adjust the cursor's reference position.	ust adjust the cursor's reference position.

#### LCD Frame Rate **Control Modulation Register**

MC68EZ328, but it is unused in the MC68VZ328. This register is removed and not available for the This register of address space 0x(FF)FFFA31 is used for frame rate modulation control in the temporary storage of data.



### Programming Model

## Freescale Semiconductor, Inc.

# **LCD Gray Palette Mapping Register**

the bits in the register are listed in Table 8-17. (LGPMR). The bit assignments for the register are shown in the following register display. The settings for two intermediate grayscale shading densities can be adjusted in the LCD gray palette mapping register For four-level grayscale displays, full black and full white are the two predefined display levels. The other

LGPMR		LCD Gray I	3ray Palette	~	lapping Register	<u>e</u> r	0x(FF	)FFFA33	
	BIT 7	<b>о</b>	σı	4	ω	2	<u> </u>	ВІТ 0	
	G23	G22	G21	G20	G13	G12	G11	G10	
TYPE	W	W	W	W	rw ,	ſW	W	W	
) ) ) 1	_	0	0	0	0	_	0	0	
, , , ,				0	0x84				

Table 8-17. LCD Gray Palette Mapping Register Description

Name	Description	Setting
<b>G23–G20</b> Bits 7–4	<b>Grayscale 23–20</b> —These bits represent one of the two grayscale shading densities.	See description
<b>G13–G10</b> Bits 3–0	<b>Grayscale 13–10</b> —These bits represent the other grayscale shading density.	See description

# 8.3.18 PWM Contrast Control Register

register display. The settings for the bits in the register are listed in Table 8-18 adjusts the contrast of the LCD panel. The bit assignments for the register are shown in the following The pulse-width modulator contrast control register (PWMR) is used to control the PWMO signal, which

PWMR BIT 15		13	14 13 12 <b>F</b>	PWI	M Contr	ontras	A Contrast Control Register  10 9 8 7 6 6  SRC1-0 CCPE PW PW PW  R PW PW	rol R	egis:	ter 5	4 W 4	з <b>О</b>	<b>X(TF</b> 2 PW 2	)FFFA3( 1 8IT 0 PW PW	<b>A36</b> BIT 0
ВІТ 15		13	12	11	ਰੇ	9	œ	7	o	Οī	4	ω	2	_	0 B <u>I</u> T
				A	SRC	1-0	CCPE N	4 Md	6 W		PW 4	PW 3	PW 2	1 PW	0 W
TYPE				F	W	W	W	W	W	W	W	W	W	W	W
BESET 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7			R	7			0x0	0x0000							

Table 8-18. PWM Contrast Control Register Description

Name	Description	Setting
Reserved Bits 15–11	Reserved	These bits are reserved and should be set to 0.
<b>SRC1–0</b> Bits 10–9	<b>Source 1–0</b> —These bits select the input clock source for the PWM counter. The PWM output frequency is equal to the frequency of the input clock divided by 256.	00 = Line pulse. 01 = Pixel clock. 10 = LCD clock. 11 = Reserved.

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Table 8-18. **PWM Contrast Control Register Description (Continued)** 

Name	Description	Setting
CCPEN Bit 8	Contrast Control Enable—This bit is used to enable or disable the contrast control function.	0 = Contrast control is off. 1 = Contrast control is on.
PWx Bits 7–0	Pulse Width 7-0—This bit controls the pulse-width of the built-in pulse-width modulator, which controls the contrast of the LCD screen. See Chapter 15, "Pulse-Width Modulator 1 and 2," for more information.	See description.

# Refresh Mode Control Register

reserved. The bit assignment for the register is shown in the following register display. The settings for the Only a single bit in this register is used to enable or disable LCD self-refresh mode. The remaining bits are

RMCR	Refr	esh Mo	Refresh Mode Control Register	ol Reg	ister		0x(FF)I	)x(FF)FFFA38
	BIT 7	6	5	4	3	2	1	BIT 0
	REF_ON							
TYPE	ľW		C					
RESET	0	0	0	0	0	0	0	0
7			EN	0x00				

Refresh Mode Control Register Description

	Note: On e	Reserved Bits 6-0	REF_ON Bit 7	Name
ARCHIVEDBYF	On entering self-refresh mode, the LSCLK and LD[7:0] signals stay low. FRM and LP work as normal.	Reserved	<b>Self-Refresh On</b> —Setting this bit enables the self-refresh mode of operation with the LCD panel.	Description
	ow. FRM and LP work as normal.	These bits are reserved and should be set to 0.	0 = Disable self-refresh mode. 1 = Enter self-refresh mode.	Setting



\_HI + F\_LO <= 8

πп

\_H <= 8

### **Programming Example**

# Freescale Semiconductor, Inc.

### 8.3.20 DMA Control Register

needs to be refilled, a new DMA transfer must be initiated. The DMA control register controls when the data is then passed to the LCD for display. When enough data has been removed from the buffer that it register are shown in the following register display. The settings for the bits are listed in Table 8-20. buffer should be refilled and the DMA burst length used when refilling. The bit assignments for the The LCD controller contains an  $8 \times 16$  pixel buffer, which stores DMA-in data from system memory. This

DMACR			DMA Control Register	ntrol Reg	ister C		0x(FF)	(FF)FFFA39	
	ВІТ 7	6	5	4	3	2	1	ВІТ 0	
		DMA	DMABL[3:0]		,		DMATM[2:0]		
TYPE	W	ſW	W	WI	R	W	W	W	ļ
RESET	0	_	_	0	Q	0	_	0	
- -				. 9	0x62				

**DMA Control Register Description** 

Name	Description	Setting
<b>DMABL[3:0]</b> Bits 7-4	<b>DMA Burst Length</b> —This field sets the number of words to be loaded to the pixel buffer in each DMA cycle.	See description and table footnote.
Reserved Bit 3	Reserved	This bit is reserved and should be set to 0.
<b>DMATM[2:0]</b> Bits 2–0	<b>DMA Trigger Mark</b> —This field sets the low-level mark in the pixel buffer to trigger a DMA request. The low-level mark equals to the number of words left in the pixel buffer.	See description and table footnote.
Note: Since the	<b>Note:</b> Since the FIFO size is 8 $\times$ 16. DMABL and DMATM must be programmed based on the following criteria:	ed on the following criteria:

## Programming Example

image is 320 pixels wide and panned by 3 pixels. with a resolution of 240  $\times$  160 pixels, 4 levels of grayscale, and a 4-bit LCD data interface. The following is an example of how to program the related registers to properly configure an LCD panel

#### Example 8-1. **Programming Example**

'SWITCH OH HODG, A WAIT SCALE FOI HEHOLY CYCLE	("OVE:D #302, #3555A2/	
in the property of the propert	かけて サイクシ サイカラ サンプ	
shift picture by 3 pixels	move.b #\$03,#\$FFFA2D	
refresh rate adjustment	move.b #10,#\$FFFA29	
pixel clock rate equal 1/4 of LCDCLK from PIL	move.b #3,#\$FFFA25	
;ICD panel data bus is 4 bits, 4 level gray	move.b #\$09, #\$FFFA20	
;4 level gray and 320 pixels wide image	move.b #40,#\$FFFA05	
;ICD vertical size is 160	move.w #159,#\$FFFA0A	
;ICD horizontal size is 240	move.w #240, #\$FFFA08	
display data address starts at \$A80000	NT move.1 #\$A80000, #\$FFFA00	LCDINT



### Freescale Semiconductor, Inc.

### Chapter 9 nterrupt Controller

controller of the MC68VZ328 supports all internal interrupts as well as external edge- and level-sensitive interrupts. There are seven interrupt levels. Level 7 has the highest priority and level 1 has the lowest. Interrupts can originate from the following sources: This chapter describes the interrupt controller and all of the signals associated with it. The interrupt /NC. 2005

- EMUIRQ or hardware breakpoint interrupt (level 7)
- IRQ6 external interrupt (level 6)
- Timer unit 1 (level 6)
- Timer unit 2 (configurable from level 1 to 6)
- Pulse-width modulator unit 1 (level 6)
- Pulse-width modulator unit 2 (configurable from level 1 to 6)
- external interrupt—pen (level 5)
- Serial peripheral interface unit 1 (configurable from level 1 to 6)
- Serial peripheral interface unit 2 (level 4)
- UART unit 1 (level 4)
- UART unit 2 (configurable from level 1 to 6)
- Software watchdog timer interrupt (level 4)
- Real-time clock (level 4)
- Real-time interrupt (level 4)
- Keyboard interrupt (level 4)
- General-purpose interrupt  $\overline{\text{INT}}[3:0]$  (level 4)—these pins can be used as keyboard interrupts
- external interrupt (level 3)
- IRQ2 external interrupt (level 2)
- IRQ1 external interrupt (level 1) ARCHIVEI



### Interrupt Processing

### Interrupt Processing

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each stage of the flow diagram are as follows: Interrupts on the MC68VZ328 are processed as illustrated in the flowchart shown in Figure 9-1. Details on

- higher interrupts pending; otherwise, the highest priority interrupt is served first. Next, it prioritizes them and presents the highest priority request to the CPU if there are no The interrupt controller collects interrupt events from both on- and off-chip peripherals
- 12 after the completion of the current instruction. The CPU responds to the interrupt request by executing an interrupt acknowledge bus cycle
- $\omega$ interrupt vector for that interrupt request onto the CPU bus. The interrupt controller recognizes the interrupt acknowledge (IACK) cycle and places the
- and begins execution at that address The CPU reads the vector and address of the interrupt handler in the exception vector table

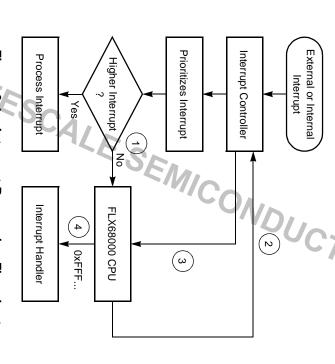


Figure 9-1. Interrupt Processing Flowchart

the responsibility of the interrupt controller Steps 2 and 4 are the responsibility of the CPU, whereas steps 1 and 3 are the responsibility of the interrupt controller. External devices must not respond to IACK cycles with a vector because the response is solely

interrupt acknowledge cycle is executed. interrupts globally to determine which priority levels can currently generate interrupts. Also in step 2, the described in the M68000 User's Manual. In step 2, the CPU's status register (SR) is available to mask On the MC68VZ328, steps 2 and 4 operate exactly as they would on other M68000 devices, which are

program address from that vector address, and then jumps to that 4-byte address. This 4-byte address is the In step 4, the CPU reads the vector number, multiplies it by four to get the vector address, fetches a 4-byte location of the first instruction in the interrupt handler.

one interrupt vector for each interrupt level. The most significant 5 bits of the interrupt vector are prioritized by the software during the execution of the interrupt service routine. The MC68VZ328 provides The interrupt priority is based on the interrupt level. The interrupts with the same interrupt level are



masked, you can find out its status in the interrupt pending register. maskable. Writing a 1 to a bit in the interrupt mask register disables that interrupt. If an interrupt is programmable, but the lower 3 bits reflect the interrupt level that is being serviced. All interrupts are

### 9.2 Exception Vectors

and the vector numbers for user interrupts are configurable. For additional information regarding exception processing, see the M68000 Family Programmer's Reference Manual. vector, as described in Table 9-1. User interrupts are part of the exception processing on the MC68VZ328. software routine that is used to handle an exception. Each exception has a vector number and an exception vector. An exception vector is the memory location from which the processor fetches the address of a A vector number is an 8-bit number that can be multiplied by four to obtain the address of an exception

10-17 Ш D  $\Box$ 0 Vector Number Decimal 16-23 24 5 4 13 12 10 0 Decimal 64-92 Address Number 52 48 44 40 0 4 040-05C 060 03C 02C 024 020 01C 018 014 010 000 800 004 Hex 030 028 000 038 034 Space SP SD Ş Level 1 interrupt autovector Uninitialized interrupt vector Unassigned, reserved<sup>3</sup> Unassigned, reserved<sup>3</sup> Unassigned, reserved<sup>3</sup> Unassigned, reserved<sup>3</sup> Spurious interrupt<sup>4</sup> Line 1010 emulator Line 1111 emulator TRAPV instruction Reset: initial SSP<sup>2</sup> Privilege violation Illegal instruction Reset: initial PC CHK instruction Divide-by-zero Address error **Assignment** 

ole 9-1. Exception Vector Assignment

## Freescale Semiconductor, Inc.

Table 9-1. Exception Vector Assignment (Continued)

Vector Number	Address	Address Number	655001	Assignment
Hex Decimal	Decimal	Hex	Opace	05
1A 26	104	068	SD	Level 2 interrupt autovector
1B 27	108	290	SD	Level 3 interrupt autovector
1C 28	112	070	SD	Level 4 interrupt autovector
1D 29	116	074	SD	Level 5 interrupt autovector
1E 30	120	078	SD	Level 6 interrupt autovector
1F 31	124	07C	SD	Level 7 interrupt autovector
20–2F 32–47	128–188	080-0BC	SD	TRAP instruction vectors <sup>5</sup>
30–3F 48–63	192–255	0C0-0FF	SD	Unassigned, reserved <sup>3</sup>
40–FF 64–255	256-1020	100-3FC	SD	User interrupt vectors
4 OD donotoo ouronio				

<sup>1.</sup>SP denotes supervisor program space and SD denotes supervisor data space.

#### NOTE:

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5.TRAP #n uses vector number 32 + n (decimal)

startup, the user interrupt vector must be programmed, thereby allowing the processor to handle interrupts properly. MC68VZ328 does not provide autovector interrupts. At system

#### .3 Reset

program counter. pointer), and the address in the next two words of the reset exception vector is fetched as the initial processor is forced into the supervisor state. The interrupt priority mask is set at level 7. The address in the reset is aborted and cannot be recovered. Neither the program counter nor the status register is saved. The initialization and to recover from a catastrophic failure. Any processing that is in progress at the time of the The reset exception corresponds to the highest exception level. A reset exception is processed for system first two words of the reset exception vector is fetched by the processor as the initial SSP (supervisor stack

initial SSP should point to a RAM space, and the initial PC should point to the startup code within the CSA0 signal should be used to decode an EPROM/ROM memory space. In this case, the first two long EPROM/ROM space so that the processor can execute the startup code to bring up the system. words of the EPROM/ROM memory space should be programmed to contain the initial SSP and PC. The At startup or reset, the default chip-select (CSA0) is asserted and all other chip-selects are negated. The



in the supervisor program space. 2.Reset vector 0 requires four words, unlike the other vectors which only require two words, and it is located

<sup>3.</sup> Vector numbers 12-14, 16-23, and 48-63 are reserved for future enhancements by Motorola. No peripheral

devices should be assigned to these numbers. The spurious interrupt vector is taken when there is a bus error indication during interrupt processing

# Freescale Semiconductor, MaGupt Controller Operation

#### NOTE:

because it is an input-only signal. CPU, and the RESET pin will not go low when this instruction is issued The MC68VZ328 supports the reset instruction. However, it only resets the

The MC68VZ328's  $\overline{RESET}$  signal should be held low for at least 1.2 s after  $V_{DD}$  is applied. See Section 4.3.2.1, "PLLCLK Initial Power-up Sequence," on page 4-5 for detailed information about appear as inputs with pull-up resistors turned on, unless otherwise specified. The multiplexed, parallel I/O D[7:0]/PA[7:0] function is controlled by the WDTH8 bit in the system control register. If the value of selecting the optimum RESET delay. After reset, all peripheral function signals and parallel I/O signals WDTH8 is 0, it is D[7:0]. If WIDTH8 is 1, it is PA[7:0].

# Operation Mode Selection During Reset

so special attention should be paid when using these signals. Refer to Chapter 2, "Signal Descriptions," The selection of the modes is controlled by the EMUIRQ, EMUBRK, and HIZ signals during system reset, more information. The MC68VZ328 supports three modes of operation: normal mode, emulation mode, and bootstrap mode

# Data Bus Width for Boot Device Operation

during the rising edge of the RESET signal, the 16-bit boot device will be configured. Otherwise, it will be The word size of the boot device (ROM/EPROM/FLASH) is determined by the BUSW signal. If it is high configured as an 8-bit boot device.

# Interrupt Controller Operation

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during the interrupt acknowledge cycle, and the CPU uses this vector number to generate a vector address When interrupts are received by the controller, they are prioritized, and the highest enabled, pending interrupt is posted to the CPU. Before the CPU responds to this interrupt, the status register is copied points to the interrupt service routine. The CPU then resumes instruction execution to execute the interrupt interrupt status register. The new program counter is updated to the content of the interrupt vector, which bus reflect the priority level of the current interrupt. The interrupt controller generates a vector number internally, and then the supervisor bit of the CPU status register is set, placing the processor into supervisor service routine. value (which points to the next instruction to be executed after the interrupt) and the saved copy of the Except for the reset exception, the CPU saves the current processor status, including the program counter mode. The CPU then responds with an interrupt acknowledge cycle in which the lower 3 bits of the address

# Interrupt Priority Processing

interrupt service routine and a higher priority interrupt is posted, the process described in Section 9.4, service routine should end with the rte instruction, which restores the processing state prior to the interrupt. Interrupts within the same level should be prioritized in software by the interrupt handler. The interrupt interrupt handler continues. The newer interrupt is postponed until its priority becomes the highest. newer interrupt is lower than or equal to the priority of the current interrupt, execution of the current "Interrupt Controller Operation," repeats, and the higher priority interrupt is serviced. If the priority of the Interrupt priority is based on the priority level of the interrupt. If the CPU is currently processing an



### 9.4.2 Interrupt Vectors

in the interrupt pending register (IPR). located anywhere within the 0x100 to 0x400 address range. The 5 most significant bits of the interrupt vectors form the user interrupt vector section of Table 9-1 on page 9-3. The user interrupt vectors can be The MC68VZ328 provides one interrupt vector for each of the seven user interrupt levels. These interrupt interrupts are maskable by the interrupt controller. If an interrupt is masked, its status can still be accessed vector number are programmable, but the lower 3 bits reflect the interrupt level being serviced. All

### Vector Generation

interrupt vector base is set to point to 0x100 (0x40<<2), which is the beginning of the user interrupt vectors interrupt vector register (IVR) to allow the interrupt vector number to point to any address in the exception shown in Table 9-1 on page 9-3. The coding for the vector numbers is provided in Table 9-2. configure the IVR to locate user interrupt vectors. For example, if you write a value of 0x40 to the IVR, the cannot be reused. This leaves only a small range of address space (0x100 to 0x400) to which you can vector table. However, many of the vector addresses are assigned to the core's internal exceptions and The interrupt controller provides a vector number to the core. You can program the upper 5 bits of the

**Table 9-2.** 

**Interrupt Vector Numbers** 

Interrupt Level 4 Level 5 Level 3 Level 6 Level 7 **Vector Number** xxxxx011 xxxxx100 xxxxx101 xxxxx110 xxxxx111

ARCHIVEDBY interrupt vector register. **Note:** xxxxx is replaced by the upper 5 bits of the

Level 2

xxxxx010

Level 1



## Freescale Semiconductor, Inc.

**Programming Model** 

### Programming Model

process interrupts, generate vector numbers, and post interrupts to the core. This section describes registers that you may need to configure so that the interrupt controller can properly

#### NOTE:

programmed as level-triggered interrupts, these interrupts are cleared at the corresponding status bit in the interrupt status register (ISR). When (INT[3:0], IRQ1, IRQ2, IRQ3, and IRQ6) can be cleared by writing a 1 to the requesting sources. level-triggered interrupts to the interrupt handler, and they are cleared at the requesting sources. All interrupts from internal peripheral devices are When programmed as edge-triggered interrupts, all external interrupts

## 9.6.1 Interrupt Vector Register

address. During system startup, this register should be configured so that the MC68VZ328's external and interrupt, which has the interrupt vector 0x3C. with the upper 5 bits to form an 8-bit vector number. The CPU uses the vector number to generate a vector During the interrupt acknowledge cycle, the lower 3 bits, encoded from the interrupt level, are combined The interrupt vector register (IVR) is used to program the upper 5 bits of the interrupt vector number. has been programmed, the interrupt vector number 0x0F is returned to the CPU as an uninitialized internal interrupts can be handled properly by their software handlers. If an interrupt occurs before the IVR

The register bit assignments are shown in the following register display, and their settings are described in

IVR			Interrupt	Vector I	Vector Register		0x(FF	FF)FFF300
	BIT 7	6	5	4	3	2	1	ВІТ 0
			VECTOR					
TYPE	W	ſW	WI	W	W			
DE CET	0	0	o	0	0	0	0	0
- -			RE	0	0x00			
			9					

Table 9-3. Interrupt Vector Register Description

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### Programming Model

## Freescale Semiconductor, Inc.

## 9.6.2 Interrupt Control Register

interrupt controller whether the interrupt signal is an edge-triggered or a level-sensitive interrupt, as well as whether it has positive or negative polarity. The bit assignments for this register are shown in the following register display, and the settings for the bit positions are listed in Table 9-4. The interrupt control register (ICR) controls the behavior of the external interrupt inputs. It informs the

ICR				Inter	rupt (	Contr	Interrupt Control Register	egiste	J.			_	×0	FF)	Ŧ	(FF)FFF30
	BIT 15	14	13	12	1	10	9	œ	4	6	Ŋ	6 5 4 3 2	ω	2		ВІТ (
	POL1	POL1 POL2 POL3 POL6 ET1 ET2 ET3 ET6 POL5	POL3	POL6	ET1	ET2	ET3	ЕТ6	POL5							
TYPE	W	W	W	W	W	۲W	W	W	W							
D D D D D D D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7 0 0							0x0000	0								

Table 9-4. Interrupt Control Register Description

Name	Description	Setting
<b>POL1</b> Bit 15	<b>Polarity Control 1</b> —This bit controls interrupt polarity for the IRQ1 signal. In level-sensitive mode, negative polarity produces an interrupt when the signal is at logic level low. Positive polarity produces an interrupt when the signal is at	0 = Negative polarity. 1 = Positive
	logic level high. In edge-triggered mode, negative polarity produces an interrupt when the signal goes from logic level high to logic level low. Positive polarity generates an interrupt when the signal goes from logic level low to logic level high.	polarity.
POL2 Bit 14	Polarity Control 2—This bit controls interrupt polarity for the IRQ2 signal. In level-sensitive mode, negative polarity produces an interrupt when the signal is at logic level low. Positive polarity produces an interrupt when the signal is at logic level high. In edge-triggered mode, negative polarity produces an interrupt when the signal goes from logic level high to logic level low. Positive polarity generates an interrupt when the signal goes from logic level low to logic level high.	0 = Negative polarity. 1 = Positive polarity.
POL3 Bit 13	Polarity Control 3—This bit controls interrupt polarity for the IRQ3 signal. In level-sensitive mode, negative polarity produces an interrupt when the signal is at logic level low. Positive polarity produces an interrupt when the signal is at logic level high. In edge-triggered mode, negative polarity produces an interrupt when the signal goes from logic level high to logic level low. Positive polarity generates an interrupt when the signal goes from logic level low to logic level high.	0 = Negative polarity. 1 = Positive polarity.
POL6 Bit 12	Polarity Control 6—This bit controls interrupt polarity for the IRQ6 signal. In level-sensitive mode, negative polarity produces an interrupt when the signal is at logic level low. Positive polarity produces an interrupt when the signal is at logic level high. In edge-triggered mode, negative polarity produces an interrupt when the signal goes from logic level high to logic level low. Positive polarity generates an interrupt when the signal goes from logic level low to logic level high.	0 = Negative polarity. 1 = Positive polarity.
ET1 Bit 11	<b>IRQ1</b> Edge Trigger Select—When this bit is set, the IRQ1 signal is an edge-triggered interrupt. In edge-triggered mode, a 1 must be written to the IRQ1 bit in the interrupt status register to clear this interrupt. When this bit is low, IRQ1 is a level-sensitive interrupt. In this case, the external source of the interrupt must be cleared.	0 = Level-sensitive interrupt. 1 = Edge-sensitive interrupt.

	Name	Description	Setting
T.	<b>ET2</b> Bit 10	<b>IRQ2</b> Edge Trigger Select—When this bit is set, the IRQ2 signal is an edge-triggered interrupt. In edge-triggered mode, a 1 must be written to the IRQ2 bit in the interrupt status register to clear this interrupt. When this bit is low, IRQ2 is a level-sensitive interrupt. In this case, the external source of the interrupt must be cleared.	0 = Level-sensitive interrupt. 1 = Edge-sensitive interrupt.
	ET3 Bit 9	IRQ3 Edge Trigger Select—When this bit is set, the IRQ3 signal is an edge-triggered interrupt. In edge-triggered mode, a 1 must be written to the IRQ3 bit in the interrupt status register to clear this interrupt. When this bit is low, IRQ3 is a level-sensitive interrupt. In this case, the external source of the interrupt must be cleared.	0 = Level-sensitive interrupt. 1 = Edge-sensitive interrupt.
<b>.</b>	ET6 Bit 8	IRQ6 Edge Trigger Select—When this bit is set, the IRQ6 signal is an edge-triggered interrupt. In edge-triggered mode, a 1 must be written to the IRQ6 bit in the interrupt status register to clear this interrupt. When this bit is low, IRQ6 is a level-sensitive interrupt. In this case, the external source of the interrupt must be cleared.	0 = Level-sensitive interrupt. 1 = Edge-sensitive interrupt.
	POL5 Bit 7	<b>Polarity Control 5</b> —This bit controls interrupt polarity for the IRQ5 signal. In level-sensitive mode, negative polarity produces an interrupt when the signal is at logic level low. Positive polarity produces an interrupt when the signal is at logic level high. In edge-triggered mode, negative polarity produces an interrupt when the signal goes from logic level high to logic level low. Positive polarity generates an interrupt when the signal goes from logic level low to logic level high.	<ul><li>0 = Negative polarity.</li><li>1 = Positive polarity.</li></ul>
	Reserved Bits 6–0	Reserved	These bits are reserved and should remain at their default value.

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**Note:** Clear interrupts after changing modes. When modes are changed from level to edge interrupts, an edge can be created, which causes an interrupt to be posted.

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### 9.6.3 Interrupt Mask Register

interrupt pending register. At reset, all the interrupts are masked and all the bits in this register are set to 1. controller will not generate an interrupt request to the CPU, but its status can still be observed in the interrupt is set. There is one control bit for each interrupt source. When an interrupt is masked, the interrupt The interrupt mask register (IMR) can mask out a particular interrupt if the corresponding bit for the

Í	R F S F T	TYPE			RESET		TYPE			IMR	
	0			BIT 15	c	>			31 31		
	0			4	c	>			30		
	_	W	2 WM	13	c	>			29		
	_	W	AR T2	12	c	>			28		
	_	W	a∏≦	<u> </u>	c	>			27	<del>-</del>	
	<u> </u>	W	2 N ≦	10	c	>			26	iterru	
7 .		W	¹N≅	ø	c	>			25	pt M	
0xFFFF	-	WI	o N≝	œ	0x0	>			24	lask	
Ä	_	۲W	MP WM	946	0x00FF	٠	W	ME	23	nterrupt Mask Register	
	<u> </u>	W	MK B	6		0	WI	H MR	22	ster	
	<u> </u>	W	MR 2	O	-	_	W	MS PI1	21		
	_	W	MR TC	4	-	_	W	MIR Q5	20		
	<u></u>	_	W	MW DT	ω	-	_	W	MIR Q6	19	0
		W	MU AR T1	Ν	-	_	W	MIR Q3	18	×(FF	
	_	W	MT MR 1	<u> </u>	-	_	W	MIR Q2	17	)x(FF)FFF304	
	_	W	MS PI2	о ВІТ	-	_	W	MIR Q1	BIT 16	<del>-</del> 304	

Table 9-5. Interrupt Mask Register Description

Name	Description	Settings
Reserved Bits 31–24	Reserved	These bits are reserved and should be set to 0.
MEMIQ Bit 23	Mask Emulator Interrupt—When set, this bit indicates that the EMUIRQ pin and in-circuit emulation breakpoint interrupt functions are masked. It is set to 1 after reset. These interrupts are level 7 interrupts to the CPU.	0 = Enable EMUIRQ interrupt 1 = Mask EMUIRQ interrupt
MRTI Bit 22	Timer for Real-Time Clock—When set, this bit indicates that the real-time interrupt timer is masked. It is set to 1 after reset.	<ul><li>0 = Enable real-time interrupt timer interrupt.</li><li>1 = Masked real-time interrupt timer interrupt.</li></ul>
MSPI1 Bit 21	Mask SPI1 Interrupt—When set, this bit indicates that the SPI1 interrupt is masked. It is set to 1 after reset.	0 = Enable SPI 1 interrupt. 1 = Mask SPI 1 interrupt.
MIRQ5 Bit 20	Mask IRQ5 Interrupt—When set, this bit indicates that IRQ5 is masked. It is set to 1 after reset.	$0 = \text{Enable}   \overline{\text{IRQ5}}   \text{interrupt.}$ $1 = \text{Mask}   \overline{\text{IRQ5}}   \text{interrupt.}$
MIRQ6 Bit 19	Mask IRQ6 Interrupt—When set, this bit indicates that IRQ6 is masked. It is set to 1 after reset.	$0 = \text{Enable} \frac{\overline{IRQ6}}{IRQ6}$ interrupt. 1 = Mask IRQ6 interrupt.
MIRQ3 Bit 18	Mask IRQ3 Interrupt—When set, this bit indicates that IRQ3 is masked. It is set to 1 after reset.	$0 = \text{Enable} \overline{\text{IRQ3}}$ interrupt. $1 = \text{Mask} \overline{\text{IRQ3}}$ interrupt.

Table 9-5. Interrupt Mask Register Description (Continued)

P	7	
Name	Description	Settings
MIRQ2 Bit 17	Mask IRQ2 Interrupt—When set, this bit indicates that IRQ2 is masked. It is set to 1 after reset.	$0 = \text{Enable} \frac{ RQ2 }{ RQ2 }$ interrupt. $1 = \text{Mask} \frac{ RQ2 }{ RQ2 }$ interrupt.
MIRQ1 Bit 16	Mask IRQ1 Interrupt—When set, this bit indicates that IRQ1 is masked. It is set to 1 after reset.	$0 = \text{Enable } \frac{ RQ1 }{ RQ1 }$ interrupt. 1 = Mask  RQ1  interrupt.
Reserved Bits 15–14	Reserved	These bits are reserved and should be set to 0.
MPWM2 Bit 13	Mask PWM 2 Interrupt—When set, this bit indicates that PWM 2 is masked. It is set to 1 after reset.	0 = Enable pulse-width modulator 2 interrupt. 1 = Mask pulse-width modulator 2 interrupt.
MUART2 Bit 12	Mask UART 2 Interrupt—When set, this bit indicates that UART 2 is masked. It is set to 1 after reset.	0 = Enable UART 2 interrupt. 1 = Mask UART 2 interrupt.
MINT3 Bit 11	Mask External INT3 Interrupt—Setting this bit masks the INT3 interrupt. It is set to 1 after reset.	$0 = \text{Enable } \overline{\text{INT3}}$ interrupt. $1 = \text{Mask } \overline{\text{INT3}}$ interrupt.
MINT2 Bit 10	Mask External INT2 Interrupt—Setting this bit masks the INT2 interrupt. It is set to 1 after reset.	0 = Enable INT2 interrupt. 1 = Mask INT2 interrupt.
MINT1 Bit 9	Mask External INT1 Interrupt—Setting this bit masks the INT1 interrupt. It is set to 1 after reset.	0 = Enable INT1 interrupt. 1 = Mask INT1 interrupt.
MINTO Bit 8	Mask External INTO Interrupt—Setting this bit masks the INTO interrupt. It is set to 1 after reset.	0 = Enable INTO interrupt. 1 = Mask INTO interrupt.
MPWM1 Bit 7	Mask PWM 1 Interrupt—Setting this bit masks the PWM 1 interrupt. It is set to 1 after reset.	0 = Enable pulse-width modulator 1 interrupt. 1 = Mask pulse-width modulator 1 interrupt.
MKB Bit 6	Mask Keyboard Interrupt—Setting this bit masks the keyboard interrupt. It is set to 1 after reset.	<ul><li>0 = Enable keyboard interrupt.</li><li>1 = Mask keyboard interrupt.</li></ul>
MTMR2 Bit 5	Mask Timer 2 Interrupt—Setting this bit masks the timer interrupt. It is set to 1 after reset.	0 = Enable timer 2 interrupt. 1 = Mask timer 2 interrupt.
MRTC Bit 4	Mask RTC Interrupt—Setting this bit masks the real-time clock (time of day) interrupt. It is set to 1 after reset.	0 = Enable real-time clock interrupt. 1 = Mask real-time clock interrupt.
MWDT Bit 3	Mask Watchdog Timer Interrupt—Setting this bit masks the watchdog timer interrupt. It is set to 1 after reset.	<ul><li>0 = Enable watchdog timer interrupt.</li><li>1 = Mask watchdog timer interrupt.</li></ul>
MUART1 Bit 2	Mask UART 1 Interrupt—When set, this bit indicates that UART 1 is masked. It is set to 1 after reset.	0 = Enable UART 1 interrupt. 1 = Mask UART 1 interrupt.
MTMR1 Bit 1	Mask Timer 1 Interrupt—Setting this bit masks the timer interrupt. It is set to 1 after reset.	0 = Enable timer 1 interrupt. 1 = Mask timer 1 interrupt.
MSPI2 Bit 0	Mask SPI 2 Interrupt—When set, this bit indicates that the SPI 2 interrupt is masked. It is set to 1 after reset.	0 = Enable SPI 2 interrupt. 1 = Mask SPI 2 interrupt.

## 9.6.4 Interrupt Status Register

interrupt is posted to the core. If there are multiple interrupt sources at the same level, the software handler may need to prioritize them, depending on the application. interrupt status register (ISR). When the bits in this register are set, they indicate that the corresponding During the interrupt service, the interrupt handler determines the source of interrupts by examining the

When programmed as edge-triggered interrupts, external interrupts INT[3:0], IRQ1, IRQ2, IRQ3, and  $IRQ\overline{6}$  can be cleared by writing a 1 to the corresponding status bit in the register. When programmed as Each interrupt status bit in this register reflects the interrupt request from its respective interrupt source. peripheral devices are level-triggered interrupts to the interrupt handler, and they are cleared at the level-triggered interrupts, these interrupts are cleared at the requesting sources. All interrupts from internal

	RESET		TYPE				RESET	TYPE			ISR
		0			ВІТ 15		0			8HT 31	
		0			14		0			30	
		0	W	PW M2	13		0			29	
		0	W	UA RT 2	12		0			28	
		0	W	INT 3	11		0			27	Inte
CX	1/	0	W	INT 2	10		0			26	errup
		0	W	INT 1	9		0			25	nterrupt Status Register
	0×00000000	0	W	0 INT	8	0x0000	0	<b>V</b>		24	tus F
	0000	0	W	PW M1	7	00000	0	W	Ω <u>≡</u> M	23	₹egis
		0	W	KB	6		0	W	RTI	22	ter
		0	W	TM R2	5		0	W	1 SPI	21	
		0	W	RT C	4		0	W	IRQ 5	20	
		0	W	T WD	3		0	W	Q 1R	19	
		0	W	UA RT 1	2		0	W	IRQ 3	18	0xFF
		0	W	TM R1	1		0	W	IRQ 2	17	)xFFFFF30C
		0	W	SPI 2	BIT 0		0	W	IRQ 1	16	30C

Table 9-6. Interrupt Status Register Description

Name	Description	Settings
Reserved Bits 31–24	Reserved	These bits are reserved and should be set to 0.
EMIQ Bit 23	Emulator Interrupt Status—When set, this bit indicates that the in-circuit emulation module or EMUIRQ pin is requesting an interrupt on level 7. This bit can be generated from three interrupt sources: two breakpoint interrupts from the in-circuit emulation module and an external interrupt from EMUIRQ, which is an active low, edge-sensitive interrupt. To clear this interrupt, you must read the ICEMSR register to identify the interrupt source and write a 1 to the corresponding bit of that register. See Section 16.2.4, "In-Circuit Emulation Module Status Register," on page 16-10 for more information.	<ul><li>0 = No emulator interrupt is pending.</li><li>1 = An emulator interrupt is pending.</li></ul>

Table 9-6. Interrupt Status Register Description (Continued)

Name	Description	Settings
<b>RTI</b> Bit 22	Real-Time Interrupt Status (Real-Time Clock)—When set, this bit indicates that the real-time timer has reached its predefined frequency count. The frequency can be selected inside the real-time clock module, which can function as an additional timer.	0 = Real-time timer has not reached predefined frequency count. 1 = Real-time timer has reached predefined frequency count.
<b>SPI1</b> Bit 21	SPI 1 Interrupt Status—When set, this bit indicates an interrupt event from SPI unit 1.	0 = No SPI 1 interrupt is pending. 1 = An SPI 1 interrupt is pending.
IRQ5 Bit 20	Interrupt Request Level 5—This bit, when set, indicates that an external device is requesting an interrupt on level 5. If the IRQ5 signal is set to be a level-sensitive interrupt, the source of the interrupt must first be cleared.	0 = No level 5 interrupt is pending. 1 = A level 5 interrupt is pending.
IRQ6 Bit 19	Interrupt Request Level 6—This bit, when set, indicates that an external device is requesting an interrupt on level 6. If the IRQ6 signal is set to be a level-sensitive interrupt, the source of the interrupt must first be cleared. If IRQ6 is set to be an edge-triggered interrupt, the interrupt must be cleared by writing a 1 to this bit. Writing a 0 to this bit has no effect.	<ul><li>0 = No level 6 interrupt is pending.</li><li>1 = A level 6 interrupt is pending.</li></ul>
IRQ3 Bit 18	Interrupt Request Level 3—This bit, when set, indicates that an external device is requesting an interrupt on level 3. If the IRQ3 signal is set to be a level-sensitive interrupt, the source of the interrupt must first be cleared. If IRQ3 is set to be an edge-triggered interrupt, the interrupt must be cleared by writing a 1 to this bit. Writing a 0 to this bit has no effect.	<ul><li>0 = No level 3 interrupt is pending.</li><li>1 = A level 3 interrupt is pending.</li></ul>
IRQ2 Bit 17	Interrupt Request Level 2—This bit, when set, indicates that an external device is requesting an interrupt on level 2. If the IRQ2 signal is set to be a level-sensitive interrupt, the source of the interrupt must first be cleared. If IRQ2 is set to be an edge-triggered interrupt, the interrupt must be cleared by writing a 1 to this bit. Writing a 0 to this bit has no effect.	<ul><li>0 = No level 2 interrupt is pending.</li><li>1 = A level 2 interrupt is pending.</li></ul>
IRQ1 Bit 16	Interrupt Request Level 1—This bit, when set, indicates that an external device is requesting an interrupt on level 1. If the IRQ1 signal is set to be a level-sensitive interrupt, the source of the interrupt must first be cleared. If IRQ1 is set to be an edge-triggered interrupt, the interrupt must be cleared by writing a 1 to this bit. Writing a 0 to this bit has no effect.	<ul><li>0 = No level 1 interrupt is pending.</li><li>1 = A level 1 interrupt is pending.</li></ul>
Reserved Bits 15–14	Reserved	These bits are reserved and should be set to 0.
PWM2 Bit 13	Pulse-Width Modulator 2 Interrupt—This bit indicates that an interrupt event from PWM unit 2 is pending. The interrupt level is configurable from level 1 to level 6. See Section 9.6.6, "Interrupt Level Register," for more details.	<ul><li>0 = No PWM 2 interrupt is pending.</li><li>1 = A PWM 2 interrupt is pending.</li></ul>

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Table 9-6. Interrupt Status Register Description (Continued)

UART 2 Interrupt Request—When set, this bit indicates that the UART 2 module needs service. The interrupt level is configurable from level 1 to level 6. See Section 9.6.6, "Interrupt Level Register," for more details.  External INT3 Interrupt—This bit, when set, indicates that a level 4 interrupt has occurred. It is usually for a keyboard interface. When it is programmed as edge-triggered, it can only be cleared by writing a 1 to the port D register. See Section 10.4.5, "Port D Registers," on page 10-16 for details.  External INT2 Interrupt—This bit, when set, indicates that a level 4 interrupt has occurred. It is usually for a keyboard interface. When it is programmed as edge-triggered, it can only be cleared by writing a 1 to the port D register. See Section 10.4.5, "Port D Registers," on page 10-16 for details.  External INT1 Interrupt—This bit, when set, indicates that a level 4	nis bit, when sually for a l lered, it can Section 10.4	WM 1) Interr	Keyboard Interrupt Request—This bit, there is a level 4 interrupt event from a k		Status—This bit indica a level 4 interrupt.	Timer 2 Interrupt Status—This bit indica occurred. This is a level 4 interrupt.  Real-Time Clock Interrupt Request—T that there is a level 4 interrupt event from pending.
External IN 1 Interrupt — This bit, when set, includes that a level 4		<b>External INTO Interrupt</b> —This bit, when set, indicates that a level 4 interrupt has occurred. It is usually for a keyboard interface. When it is programmed as edge-triggered, it can only be cleared by writing a 1 to the port D register. See Section 10.4.5, "Port D Registers," on pending.	<u> </u>	vel 4 len it ing a on on at	when set, indicates that a level 4 for a keyboard interface. When it t can only be cleared by writing a 1 10.4.5, "Port D Registers," on Interrupt—This bit, when set, rupt event from PWM unit 1 s bit, when set, indicates that m a keyboard pending.  indicates that a timer 2 event has 0 indicates that a timer 2 event has 0	when set, indicates that a level 4 for a keyboard interface. When it t can only be cleared by writing a 1 10.4.5, "Port D Registers," on Interrupt—This bit, when set, rupt event from PWM unit 1 s bit, when set, indicates that m a keyboard pending.  st—This bit, when set, indicates that is t from the real-time clock that is 1

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	Table 9-6. Interrupt Status Register Description (Continued)	nued)
Name	Description	Settings
UART1 Bit 2	UART 1 Interrupt Request—When set, this bit indicates that the UART 1 module needs service. This is a level 4 interrupt.	0 = No UART1 service request is pending. 1 = UART1 service is needed.
TMR1 Bit 1	<b>Timer 1 Interrupt Status</b> —This bit indicates that a timer 1 event has occurred. This is a level 6 interrupt.	0 = No timer 1 event occurred. 1 = A timer 1 event has occurred.
<b>SPI2</b> Bit 0	<b>SPI Unit 2 Interrupt Status</b> —When set, this bit indicates an interrupt event from SPI unit 2.	<ul><li>0 = No SPI 2 interrupt is pending.</li><li>1 = An SPI 2 interrupt is pending.</li></ul>

## 9.6.5 Interrupt Pending Register

source requests an interrupt, but that interrupt is masked by the interrupt mask register, then that interrupt the interrupt bit will be set in both registers. bit will be set in this register, but not in the interrupt status register. If the pending interrupt is not masked, The read-only interrupt pending register (IPR) indicates which interrupts are pending. If an interrupt

IPR					Inte	rrupt	Pen	ding	nterrupt Pending Register	ister	C, (		0	×(FF	x(FF)FFF310	<del>-</del> 310
	31 BT	30	29	28	27	26	25	24	23	22	21	20	19	18	17	BIT 16
									ω M∃	RTI	ldS	IRQ 5	IRQ 6	IRQ 3	IRQ 2	IRQ 1
TYPE									W	W	W	W	W	W	W	W
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BIT 15	<b>1</b>	13	12	<u> </u>	10	Ø	0x000000 8	000000	<b>o</b>	ΟΊ	4	ω	Ν	_	0 BIT
			PW M2	UA RT 2	3 N	2 2	ı N	οZ	MY M1	ΚB	TM R2	RT	T DW	UA RT 1	R1	SPI 2
TYPE			W	W	W	۲W	W	W	W	W	W	W	W	W	W	W
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
							En.	***************************************								

Table 9-7. Interrupt Pending Register Description

Name	Description	Settings
Reserved Bits 31–24	Reserved	These bits are reserved and should be set to 0.
EMIQ Bit 23	Emulator Interrupt Pending—When set, this bit indicates that the in-circuit emulation module or EMUIRQ pin is requesting an interrupt	0 = No emulator interrupt is pending.
	on level 7. This bit can be generated from three interrupt sources: two breakpoint interrupts from the in-circuit emulation module and an external interrupt from EMUIRQ, which is an active low, edge-sensitive interrupt. To clear this interrupt, you must read the ICEMSR register to identify the interrupt source and write a 1 to the corresponding bit of that register. See Section 16.2.4, "In-Circuit Emulation Module Status Register," on page 16-10 for more information.	1 = An emulator interrupt is pending.
<b>RTI</b> Bit 22	Real-Time Interrupt Pending (Real-Time Clock)—When set, this bit indicates that the real-time timer interrupt is pending. The frequency can be selected inside the real-time clock module, which can function as an additional timer.	<ul><li>0 = No real-time timer interrupt is pending.</li><li>1 = A real-time timer interrupt is pending.</li></ul>
<b>SPI1</b> Bit 21	SPI 1 Interrupt Pending—When set, this bit indicates an interrupt event from SPI unit 1.	0 = No SPI 1 interrupt is pending. 1 = An SPI 1 interrupt is pending.

Table 9-7. Interrupt Pending Register Description (Continued)

Name	Description	Settings
IRQ5 Bit 20	Interrupt Request Level 5—This bit, when set, indicates that an external device is requesting an interrupt on level 5. If the IRQ5 signal is set to be a level-sensitive interrupt, the source of the interrupt must first be cleared.	0 = No level 5 interrupt is pending. 1 = A level 5 interrupt is pending.
IRQ6 Bit 19	Interrupt Request Level 6—This bit, when set, indicates that an external device is requesting an interrupt on level 6. If the IRQ6 signal is set to be a level-sensitive interrupt, the source of the interrupt must first be cleared. If IRQ6 is set to be an edge-triggered interrupt, the interrupt must be cleared by writing a 1 to this bit. Writing a 0 to this bit has no effect.	<ul><li>0 = No level 6 interrupt is pending.</li><li>1 = A level 6 interrupt is pending.</li></ul>
IRQ3 Bit 18	Interrupt Request Level 3—This bit, when set, indicates that an external device is requesting an interrupt on level 3. If the IRQ3 signal is set to be a level-sensitive interrupt, the source of the interrupt must first be cleared. If IRQ3 is set to be an edge-triggered interrupt, the interrupt must be cleared by writing a 1 to this bit. Writing a 0 to this bit has no effect.	<ul><li>0 = No level 3 interrupt is pending.</li><li>1 = A level 3 interrupt is pending.</li></ul>
IRQ2 Bit 17	Interrupt Request Level 2—This bit, when set, indicates that an external device is requesting an interrupt on level 2. If the $\overline{IRQ2}$ signal is set to be a level-sensitive interrupt, the source of the interrupt must first be cleared. If $\overline{IRQ2}$ is set to be an edge-triggered interrupt, the interrupt must be cleared by writing a 1 to this bit. Writing a 0 to this bit has no effect.	<ul><li>0 = No level 2 interrupt is pending.</li><li>1 = A level 2 interrupt is pending.</li></ul>
IRQ1 Bit 16	Interrupt Request Level 1—This bit, when set, indicates that an external device is requesting an interrupt on level 1. If the IRQ1 signal is set to be a level-sensitive interrupt, the source of the interrupt must first be cleared. If IRQ1 is set to be an edge-triggered interrupt, the interrupt must be cleared by writing a 1 to this bit. Writing a 0 to this bit has no effect.	<ul><li>0 = No level 1 interrupt is pending.</li><li>1 = A level 1 interrupt is pending.</li></ul>
Reserved Bits 15–14	Reserved	These bits are reserved and should be set to 0.
<b>PWM2</b> Bit 13	Pulse-Width Modulator 2 Interrupt—This bit indicates an interrupt event from PWM unit 2 is pending. The interrupt level is configurable from level 1 to level 6. See Section 9.6.6, "Interrupt Level Register," for more details.	<ul><li>0 = No PWM 2 interrupt.</li><li>1 = A PWM 2 interrupt is pending.</li></ul>
UART2 Bit 12	<b>UART 2 Interrupt Request</b> —When this bit is set, it indicates that the UART 2 module needs service. The interrupt level is configurable from level 1 to level 6. See Section 9.6.6, "Interrupt Level Register," for more details.	<ul><li>0 = No UART 2 interrupt request is pending.</li><li>1 = UART 2 interrupt request is pending.</li></ul>
INT3 Bit 11	External INT3 Interrupt—This bit, when set, indicates that a level 4 interrupt has occurred. It is usually for a keyboard interface. When it is programmed as edge-triggered, it can only be cleared by writing a 1 to the port D register. See Section 10.4.5, "Port D Registers," on page 10-16 for details.	0 = No NT3 interrupt is pending. 1 = An NT3 interrupt is pending.



### Table 9-7. Interrupt Pending Register Description (Continued)

		•
Name	Description	Settings
INT2	<b>External INT2 Interrupt</b> —This bit, when set, indicates that a level 4 $0 = \text{No INT2}$ interrupt is	$0 = No \overline{INT2}$ interrupt is
Bit 10	interrupt has occurred. It is usually for a keyboard interface. When it	pending.
	is programmed as edge-triggered, it can only be cleared by writing a	1 = An INT2 interrupt is
	1 to the port D register. See Section 10.4.5, "Port D Registers," on	pending.
	page 10-16 for details.	
INT1	External INT1 Interrupt—This bit, when set, indicates that a level 4	$0 = No \overline{INT1}$ interrupt is
Bit 9	interrupt has occurred. It is usually for a keyboard interface. When it	pending.
	is programmed as edge-triggered, it can only be cleared by writing a	1 = An INT1 interrupt is
	1 to the port D register. See Section 10.4.5, "Port D Registers," on	pending.
	page 10-16 for details.	

Name	Description	Settings
INT2 Bit 10	External INT2 Interrupt—This bit, when set, indicates that a level 4 interrupt has occurred. It is usually for a keyboard interface. When it is programmed as edge-triggered, it can only be cleared by writing a 1 to the port D register. See Section 10.4.5, "Port D Registers," on page 10-16 for details.	0 = No INT2 interrupt is pending. 1 = An INT2 interrupt is pending.
INT1 Bit 9	External INT1 Interrupt—This bit, when set, indicates that a level 4 interrupt has occurred. It is usually for a keyboard interface. When it is programmed as edge-triggered, it can only be cleared by writing a 1 to the port D register. See Section 10.4.5, "Port D Registers," on page 10-16 for details.	0 = No NTT interrupt is pending. 1 = An NTT interrupt is pending.
INTO Bit 8	External INTO Interrupt—This bit, when set, indicates that a level 4 interrupt has occurred. It is usually for a keyboard interface. When it is programmed as edge-triggered, it can only be cleared by writing a 1 to the port D register. See Section 10.4.5, "Port D Registers," on page 10-16 for details.	0 = No INTO interrupt is pending. 1 = An INTO interrupt is pending.
PWM1 Bit 7	Pulse-Width Modulator (PWM 1) Interrupt—This bit, when set, indicates that there is a level 6 interrupt event from PWM unit 1 pending.	<ul><li>0 = No PWM 1 interrupt.</li><li>1 = A PWM 1 interrupt is pending.</li></ul>
<b>KB</b> Bit 6	Keyboard Interrupt Request—This bit, when set, indicates that there is a level 4 interrupt event from a keyboard pending.	<ul><li>0 = No keyboard interrupt is pending.</li><li>1 = A keyboard interrupt is pending.</li></ul>
TMR2 Bit 5	<b>Timer 2 Interrupt Pending</b> —This bit indicates that a timer 2 event has occurred. This is a level 4 interrupt.	0 = No timer 2 event occurred. 1 = A timer 2 event has occurred.
RTC Bit 4	Real-Time Clock Interrupt Request—This bit, when set, indicates that there is a level 4 interrupt event from the real-time clock that is pending.	<ul><li>0 = No real-time clock interrupt is pending.</li><li>1 = A real-time clock interrupt is pending.</li></ul>
WDT Bit 3	Watchdog Timer Interrupt Request—This bit indicates that a watchdog timer interrupt is pending. This is a level 4 interrupt.	<ul><li>0 =No watchdog timer interrupt is pending.</li><li>1 = A watchdog timer interrupt is pending.</li></ul>
UART1 Bit 2	<b>UART 1 Interrupt Request</b> —When this bit is set, it indicates that the UART 1 module needs service. This is a level 4 interrupt.	0 = No UART 1 service request is pending. 1 = UART 1 service is needed.
TMR1 Bit 1	Timer 1 Interrupt Pending—This bit indicates that a timer 1 event has occurred. This is a level 6 interrupt.	<ul><li>0 = No timer 1 event occurred.</li><li>1 = A timer 1 event has occurred.</li></ul>
<b>SPI2</b> Bit 0	<b>SPI Unit 2 Interrupt Pending</b> —When set, this bit indicates an interrupt event from SPI unit 2.	0 = No SPI 2 interrupt is pending. 1 = An SPI 2 interrupt is pending.

### INC. Programming Model

### 9.6.6 Interrupt Level Register

control register (ILCR) controls the interrupt level for these interrupts. version, MC68EZ328. Interrupts generated from these modules are level configurable. The interrupt level TIMER 2, UART 2, PWM 2, and SPI 1 are new modules to the MC68VZ328 compared to the previous

	<b>ILCR</b>
ВІТ	
7	
2	
3	
7	Int
5	errup
o	ot Le
o	vel R
7	Interrupt Level Register
n	ter
D	
וו	2
_	
သ	0
s	×(FF

F)FFF314

7 10 11	D II O II I	TYPE		
	0			15
	_	₹	SP	14
	_	₹	SPI1_LEVEL	13
	0	₹	/EL	12
	0			11
	_	¥	UAI	10
	0	₹	JART2_LEVEL	9
0x6	_	8	VEL	8
0x6533	0			7
	0	₹	PW	6
	_	₹	M2_LEVEL	OI
	_	₹	VEL	4
	0			ω
	0	₹	MT	2
	_	V	TMR2_LEVEL	_
	_	V	VEL	0

corresponding interrupt source to generate different interrupt levels. Programming register bits 14-12, 10-8, 6-4, and 2-0 with the values shown in Table 9-8 causes the

Table 9-8. Interrupt Level Register Field Values

Undefined level 000  Note: Values 000 and 111 are not allowed to be programmed into	Level 1	Level 3	Level 4	Level 5	Level 6	Undefined level	Interrupt Level
000	001	010	100	101	110	111	Value in Register Bits 14–12, 10–8, 6–4, and 2–0

After reset, each of these four interrupts is set to the default level indicated

- TIMER2IRQ (level 3)
- UART2IRQ (level 5)
- PWM2IRQ (level 3)
- SPI2IRQ (level 6)



### 9.7 Keyboard Interrupts

request. This event-driven approach significantly reduces power consumption. KB0 to KB7 (multiplexed with INT[3:0], IRQ1, IRQ2, IRQ3, and IRQ6) are input pins for the keyboard interface. They are internally sleep when no key is being pressed. Once a key is pressed, however, the core wakes up to service the Keyboard interrupt features provide a smart power-management capability. The CPU core can be put to ORed together and generate an interrupt that indicates to the core that a key has been pressed

### 9.8 Pen Interrupts

pen interrupt supports both pen-down and pen-up interrupts. The polarity of the pen interrupt can be set by interrupt can be implemented with the MC68VZ328 system. With the special design circuitry inside, this normally used as a pen interrupt. Connecting the  $\overline{IRQ5}$  to a transistor network with the A/D, a pen-down A/D starts collecting data. On the MC68VZ328, IRQ5 is a level 5 interrupt with pull-up properties that is the microprocessor. When the touch panel is touched, the CPU is activated through the interrupt and the achieve low power consumption and system performance, the A/D is usually connected to an interrupt of involves a touch panel connected to an analog-to-digital (A/D) converter and the microprocessor. To The MC68VZ328 is designed to support pen and touch panel inputs. In most of these systems, the setup programming the POL5 bit of the interrupt control register.



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#### **//O Ports** Chapter 10



and pull-up resistors (or pull-down resistors in some ports) can be enabled or disabled. When pins are noted in the programming information about the specific ports. programmed as dedicated I/O, a pin's direction cannot be controlled. A few exceptions to this rule are When pins are programmed as GPIO, the direction of individual pins (input or output) can be configured.

### **Port Configuration**

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Several ports have pins that can be configured for one of several dedicated I/O functions. Table 10-1 on page 10-2 shows the I/O functions available for each port. With the exception of Port A, every port is multiplexed with at least one other dedicated I/O function.

external interrupts. It has four dedicated interrupt control registers in addition to the previously referenced exceptions are Port A and Port D. Port A does not have a select register since it can only be used as a Ports are programmed by four dedicated 8-bit registers: direction, data, pull-up enable, and select. The four registers. functions is controlled by other registers in the MC68VZ328. Port D is unique in that it is used for handling dedicated I/O function. Some pins have multiple dedicated functions assigned to them. Selection of these GPIO. The remaining registers have select registers controlling whether the pin is assigned as a GPIO or a

current. After reset, it is recommended the user select 2 mA drive strength for those signals not requiring signals, including all of the ports. By default, all I/O pins on the MC68VZ328 default to a 4 mA driving high current to ensure maximum power savings The I/O drive control register (IOCR) in system control controls the drive strength (in mA) of all I/O ARCH



### Status of I/O Ports During **Fagescale** Semiconductor, Inc.

Table 10-1. Dedicated I/O Functions of Ports

			DRAM controller	3
	SPI	LCD controller	Bus control	$\boldsymbol{x}$
	00	SPI	UART	J
	Address bit 0	In-circuit emulation	Bus control	G
	70	Chip-select	LCD contrast	
Interrupt request 5	Address bits 23-20	CGM	DRAM controller	П
Bus control	UART	DRAM controller	SPI	Ш
	Vo		Interrupt controller	D
			LCD controller	С
PWM output	GP timers	DRAM controller	Chip-select	В
	03		Lower byte of data bus	Α
Dedicated I/O Module	Dedicated I/O Module	Dedicated I/O Module	Dedicated I/O Module	Port

### Status of I/O Ports During Reset

warm reset refers to any reset initiated while power to the processor remains uninterrupted. A power-up reset occurs the first time power is supplied to the MC68VZ328. Power-up resets are also called cold start Two types of resets affect the states of the MC68VZ328's I/O ports: warm reset and power-up reset. A

### **10.2.1** Warm Reset

the Reset Assertion Time Length. The previous states of Ports B and M before reset assertion are, for the Ports B and M maintain their previous programmed states on reset assertion and retain their states during the I/O port registers. Register reset values are found in Table 3-1 on page 3-2 and Table 3-2 on page 3-8 their default states on assertion of the reset signal and remain at their default states during the time period purposes of the figure, assumed. labeled Reset Assertion Time Length. The port default state is determined by the register reset values of Figure 10-1 on page 10-3 details timing during a warm reset. All I/O ports, except Ports B and M, reset to ARCHIVED



# Freescale Semiconductors almos I/O Ports During Reset

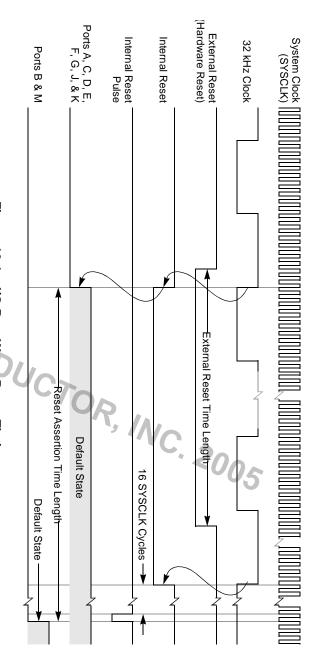


Figure 10-1. I/O Port Warm Reset Timing

internal reset pulse signal are as follows: the external reset has been asserted. The resets for Ports B and M are triggered by the negation of the reset signal. The internal reset signal is synchronized with the first falling edge of the 32 kHz clock after internal reset pulse signal. The sequence of events (as shown in Figure 10-1) leading to the assertion of the As shown in Figure 10-1, resets for Ports A, C-G, J, and K are triggered by the assertion of the internal

- The external reset signal is negated.
- 5 The first falling edge of 32 kHz occurs.
- generated. After 16 cycles of SYSCLK, the internal reset pulse, whose width is 1 SYSCLK cycle, is

details appear in Chapter 7, "DRAM Controller." states of Port B and Port M allows multiplexed DRAM control signals to remain active during the system DRAM during unpredictable reset time lengths, thereby preserving DRAM data after reset negation. More Reset Assertion Time Length. This feature allows the DRAM controller to maintain the refresh cycles for Port B and Port M are designed to maintain or hold their previous states during the Reset Assertion Time Length to support the "data retention during reset" feature of the DRAM controller. Holding the previous

### Power-up Reset

and Port M are unknown during the Reset Assertion Time Length. Because Port B and Port M do not reset until the negation of the internal reset pulse signal, they do not have a previous state on a power-up reset. The power-up reset sequence of events is the same as for a warm reset, except that the I/O states of Port B

internal resistors enabled, this cannot be guaranteed. For any external device that may be sensitive to the connected to other available ports whose state can be ascertained brief unknown states of Port B or Port M on power-up resets, it is recommended that the device be While preliminary testing indicates that, on power-up reset, Ports B and M are configured as inputs with

### 10.2.3 **Summary of Port Behavior During Reset**

(see Figure 10-1 on page 10-3) for power-up resets and warm resets. Table 10-2 summarizes the behavior of all MC68VZ328 I/O ports during the Reset Assertion Time Length

MC68VZ328 I/O Port Status During the Reset Assertion Time Length

I/O Ports	Warm Reset	Power-up Reset
A	Resets to default state	Resets to default state
В	Maintains previous state	Unknown state
С	Resets to default state	Resets to default state
D	Resets to default state	Resets to default state
E	Resets to default state	Resets to default state
F	Resets to default state	Resets to default state
G	Resets to default state	Resets to default state
ر	Resets to default state	Resets to default state
Х	Resets to default state	Resets to default state
Μ	Maintains previous state	Unknown state
<b>Note:</b> The default stat	<b>Note:</b> The default state is defined by the reset values of the corresponding I/O port's registers. Please refer to Table 3-1 on page 3-2 and Table 3-2 on page 3-8 for details.	onding I/O port's registers. Please refer to

lable 3-1 on page 3-2 and lable 3-2 on page 3-8 for details.

### **Port Operation**

The following subsections describe details of the I/O ports' operation.

# Data Flow from the I/O Module

The operation of a port connected to another module in the MC68VZ328 is illustrated in Figure 10-2 on ARCHIVEDBY



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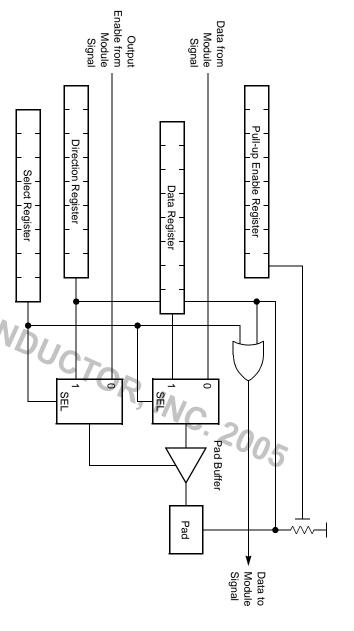


Figure 10-2. I/O Port Operation

For example, if Figure 10-2 represents the D0 bit of Port E, when the SEL0 in the select register is cleared, the "data from module" line is connected to the serial peripheral interface module's TXD signal always output. When the dedicated module controls the port, the direction register is ignored. There are a is the master SPMTXD signal. The SPI module controls the direction of data flow for the pin, which is select register is clear (the default is set at reset), the SPI module pin function is enabled. Bit D0 of Port E line, thus enabling the output and disabling the "data to module" line. As long as the SELx bit of the port's (SPITXD). Because SPITXD is output-only, the MC68VZ328 asserts the "output enable from module" few exceptions that are described in the individual port programming sections that follow.

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## 0.3.2 Data Flow to the I/O Module

signal is connected to the SPIRXD input of the SPI. module" line, and the "data from module" line is not disabled (see Figure 10-2). The "data to module" (SPIRXD) signal. In this case, SPIRXD is input-only; thus, the chip negates the "output enable from An example of data flow to the I/O module is the D1 bit of Port E. This signal's function is the SPI's RXD

## 10.3.3 Operating a Port as GPIO

written to the PxDATA register before entering the selected mode overdriven. To prevent data loss when changing from one mode to another, the intended data should be level is presented during write accesses. This may not be the same as the data that was written if the pin is and presented to the CPU when a read cycle is executed. While the DIRx bit is 0 (output), the actual pin presented to the pin. If the DIRx bit in the direction register is 0 (input), data present on the pin is sampled While the SELx bit is set (if the DIRx bit of the PxDIR is 1), data written to the port's data register is

10-5

# 10.3.4 Port Pull-up and Pull-down Resistors

pull-down enabled. Resistor assignments for individual ports is shown in Table 10-3. Meanwhile, Port G defaults to the dedicated function, except for the HIZ/P/D/PG3 pin, which defaults to the PG3 function. selected or not. After reset, Ports A-F, J, K, and M default to the I/O function with internal pull-up or The pull-up and pull-down resistors are enabled by setting the pull-up or pull-down enable register's bits to Pull-up and pull-down resistors can be selected individually regardless of whether the I/O port is

Port	Pull-up	Pull-down
A, B, D, E, G, and J	All bits	None
С	None	All bits
F	Bits 7, 2-0	Bits 6–3
K	Bits 3-0	Bits 7–4
M	Bit 5	Bits 4-0

Table 10-3. Pull-up and Pull-down Resistors by Port

# Programming Model er's remaining section

The chapter's remaining sections provide programming information about individual ports

### **Port A Registers**

The Port A registers are general-purpose 8-bit I/O registers. They consist of the following:

- Port A direction register (PADIR)
- Port A data register (PADATA)
- Port A pull-up enable register (PAPUEN)

used as PA[7:0] only when the MC68VZ328 is operating as an 8-bit system by setting the WDTH8 bit in the system control register (0xFFFFF000). If the MC68VZ328 is operating in either 16-bit or mixed 8- and Port A functions either as a GPIO (PA[7:0]) or the lower data byte of the data bus (D[7:0]). Port A can be 16-bit systems, the pins only function as D[7:0].

bus (D[7:0]) with internal pull-up resistors enabled. At reset the WDTH8 bit of the SCR is cleared, resulting in Port A becoming the lower data byte of the data

In sleep mode, all of the data bus pins (D[15:0]) are individually pulled up with 1 M $\Omega$  resistors ARCHIVE



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**Programming Model** 

### 10.4.1.1 Port A Direction Register

PADATA bit position. The settings for the bit positions are shown in Table 10-4 The Port A direction register controls the direction (input or output) of the line associated with the

PADIR		Po	Port A Dire	irection Re	Register	00	0x(FF	)FFF400
	BIT 7	6	5	4	3	2	1	BIT 0
	DIR7	DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0
TYPE	ľW	W	W	rw	W	W	W	w
RESET	0	0	0	0	2	0	0	0
7.00				0×	0x00			

Table 10-4. Port A Direction Register Description

Name	Description	Setting
DIRx I	<b>Direction</b> —These bits control the direction of the pins in an 8-bit system.	0 = Input 1 = Output

### 10.4.1.2 Port A Data Register

whether they are configured as input or output. The settings for the bit positions are shown in Table 10-5 configured as an output. The actual value on the pin is reported when these bits are read, regardless of inputs will accept the data, but the data written to each cannot be accessed until the respective pin is While the DIRx bits are high (output), the Dx bits control the pins. While the DIRx bits are low (input), the The eight PADATA bits control or report the data on the pins while the associated SELx bits are high. Dx bits report the signal driving the pins. The Dx bits can be written at any time. Bits that are configured as

PADATA		Por	t A Dat	Port A Data Register	.er		0x(FF	x(FF)FFF401	
	BIT 7	o	O1	4	ω	2	_	BIT 0	
	D7	D6	D5	D4	D3	D2	D1	D0	
TYPE	rw	W	W	W	W	WI	W	W	
	_	4	_	<u></u>	_	<u></u>	<u></u>	<u></u>	
RESET		*Actua	al bit value c	0x depends on e	0xFF* *Actual bit value depends on external circuits connected to pin.	s connected t	to pin.		

Table 10-5. Port A Data Register Description

Name	Description	Setting
Dx	Data—These bits reflect the	0 = Drives the output signal low when DIRx is set to 1 or the
Bits 7-0	status of the I/O signal in an	external signal is low when DIRx is set to 0
	8-bit system.	1 = Drives the output signal high when DIRx is set to 1 or the
	14	external signal is high when DIRx is set to 0

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# 10.4.1.3 Port A Pull-up Enable Register

settings for the bit positions are shown in Table 10-6. The Port A pull-up enable register (PAPUEN) controls the pull-up resistors for each line in Port A. The

7.00	RE SET	TYPE			PAPUEN
	_	W	PU7	BIT 7	
	<b>-</b>	W	PU6	6	Port A Pull-up
	_	W	PU5	5	Pull-up E
0xFF	_	W	PU4	4	Enable R
ji	<i>}</i> /	W	PU3	3	Register
	_	W	PU2	2	0
	_	W	PU1	1	0x(FF)
	_	W	PU0	BIT 0	)FFF402

Table 10-6. Port A Pull-up Enable Register Description

Name	Description	Setting
PUx Bits 7–0	<b>Pull-up</b> —These bits enable the pull-up resistors on the port.  0 = Pull-up resistors are disabled the port.	0 = Pull-up resistors are disabled 1 = Pull-up resistors are enabled

### 0.4.2 Port B Registers

Port B is made up of the following 8-bit general-purpose I/O registers:

- Port B direction register (PBDIR)
- Port B data register (PBDATA)
- Port B pull-up enable register (PBPUEN)
- Port B select register (PBSEL)

Each signal line connects to an external pin. Each bit on Port B is individually configured

### 10.4.2.1 Port B Direction Register

PBDATA bit position. When the data bit is assigned to a dedicated I/O function, the direction bits are ignored. The settings for the bit positions are shown in Table 10-7 on page 10-9 The Port B direction register controls the direction (input or output) of the line associated with the



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PBDIR		Po	Port B Direction		Register		0x(FF	)FFF408	
	ВІТ 7	6	5	4	3	2	1	ВІТ 0	
	DIR7	DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0	
TYPE	rw	W	W	۲W	W	WJ	W	ſW	
D II O II I	0	0	0	0	0		0	0	
7000				0x	0x00	3			

Table 10-7. Port B Direction Register Description

Name	Description	Setting
DIRx Bits 7–0	<b>Direction</b> —These bits control the direction of the pins. They reset to 0. With the exception of bit 6, if a bit is selected as a dedicated 1 = Output I/O in PBSEL, the DIR bit is ignored.	They reset 0 = Inputs dedicated 1 = Output

### 10.4.2.2 Port B Data Register

The settings for the PBDATA bit positions are shown in Table 10-8.

PBDATA		Pc	Port B Data Register	Regist	er		0x(FF	)FFF409
	BIT 7	<b>o</b>	σı	4	ω	2	_	ВІТ 0
	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	W	W	WI	۲W	W	W	W	ſW
	_	_	5/	_	_	_	_	_
RESET		*Actı	0xFF* *Actual bit value depends on external circuits connected to pin.	0xFF* pends on exterr	:F* ternal circuits	connected to	o pin.	

Table 10-8. Port B Data Register Description

Name	Description	Setting
Dx Da	Data—These bits reflect the	0 = Drives the output signal low when DIRx is set to 1 or the
Bits 7–0 sta	status of the I/O signal in an	external signal is low when DIRx is set to 0
<u>~</u>	8-hit system	
	51. 0) 0.0111.	1 = Drives the output signal high when DIRx is set to 1 or the

These pins can be programmed as GPIO when these other assignments are not used. Port B is multiplexed with chip-select, DRAM control, TIN/TOUT, and PWM dedicated I/O signals.

the signal driving the pins. The Dx bits can be written at any time. Bits that are configured as inputs will configured as input or output. an output. The actual value on the pin is reported when these bits are read, regardless of whether they are accept the data, but the data written to each cannot be accessed until the corresponding pin is configured as bits are high (output), the Dx bits control the pins. While the DIRx bits are low (input), the Dx bits report These bits control or report the data on the pins while the associated SELx bits are high. While the DIRx

### Port B **Dedicated I/O Functions**

dedicated I/O signals whose assignments are shown in Table 10-9. The eight PBDATA lines are multiplexed with the chip-select, DRAM control, TIN/TOUT, and PWM

Table 10-9. Port B Dedicated Function Assignments

7 D:	6 D:	5 D:	4 D:	3 D:	2 D:	1 D:	0 D:	Bit GPIC
Data bit 7	Data bit 6	Data bit 5	Data bit 4	Data bit 3	Data bit 2	Data bit 1	Data bit 0	GPIO Function
PWMO1	TIN/TOUT	CSD1/CAS1	CSD0/CAS0	CSC1/RAS1	CSC0/RAS0	CSB1/SDWE	CSB0	Dedicated I/O Functions

Bit 0 is used only as D0 or CSB0. No additional programming is required. the chip-select D (CSD) register, which is described in Section 6.3.3, "Chip-Select Registers," on page 6-8 Bits 1-5 operate as chip-select signals or DRAM signals. Signal selection is controlled by bit 9 (DRAM) in

for details about the operation and programming of the pin. though the pin is assigned to the GP timers. Refer to Section 12.1.4, "TOUT/TIN/PB6 Pin," on page 12-3 register pins, the TOUT/TIN/PB6 pin direction is still controlled by the DIR6 bit in the Port B register even PBDIR register. Clearing the bit makes the line TIN. Setting the bit to 1 makes it TOUT. Unlike other port The TIN/TOUT line can be specified as either timer-input or timer-output by programming bit 6 in the

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The PWMO1 signal is an output signal resulting from the logical operation (AND or OR) of both the PWM 1 and PWM 2 modules. Bits 3–2 (P[1:0]) of the peripheral control register (PCR) select the logic used for combining the modules. The PB7/PWMO1 pin defaults to a GPIO input pulled high. Refer to Chapter 15, "Pulse-Width Modulator 1 and 2," for additional information.

# Port B Pull-up Enable Register

settings for the bit positions are shown in Table 10-10 on page 10-11. The Port B pull-up enable register (PBPUEN) controls the pull-up resistors for each line in Port B. The



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7 10 11	DE SET	TYPE rw	PU7	ВІТ 7	PBPUEN
	_	>	J7	Г7	_
	_	W	PU6	6	Port B F
	_	W	PU5	5	ull-up E
0×	_	W	PU4	4	Port B Pull-up Enable Register
0xFF	_	W	PU3	3	Register
	0	W	PU2	2	
	_	W	PU1	1	0x(FF)
	<u></u>	W	PU0	ВІТ 0	FFF40A

Table 10-10. Port B Pull-up Enable Register Description

Name	Description	Setting
PUx Bits 7–0	<b>Pull-up</b> —These bits enable the pull-up resistors on the port.	0 = Pull-up resistors are disabled 1 = Pull-up resistors are enabled

#### Port B Select Register

as a general purpose I/O or to a dedicated I/O function. The settings for the bit positions are shown in The Port B select register (PBSEL) determines if a bit position in the data register (PBDATA) is assigned

PBSEL		Por		B Select Register	ter		0x(FF)	FFF40B
	BIT 7	6	5	4	3	2	1	BIT 0
	SEL7	SEL6	SEL5	SEL4	SEL3	SEL2	SEL1	SEL0
TYPE	W	W	W	W	W	ľW	W	ľW
7 7 7 1	_	_	1	_	_	_	_	_
7			LE	0xFF	Ŧ			

## Port B Select Register Description

SELxSelect —These bits select whether the internal chip0 = The dedicated function pins are connected.Bits 7-0function or I/O port signals are connected to the1 = The I/O port function pins are connected.	Name	Description	Setting
	SELx Bits 7-0	Select —These bits select whether the internal chip function or I/O port signals are connected to the	0 = The dedicated function pins are connected. 1 = The I/O port function pins are connected.

#### **Port C Registers**

Port C is composed of the following 8-bit general-purpose I/O registers:

- Port C direction register (PCDIR)
- Port C data register (PCDATA)
- Port C pull-down enable register (PCPDEN)
- Port C select register (PCSEL)

is individually configured Each signal in the PCDATA register connects to an external pin. As with the other ports, each bit on Port C

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## 10.4.3.1 Port C Direction Register

DIR bits are ignored. The settings for the bit positions are shown in Table 10-12 PCDATA bit position. When the data bit is assigned to a dedicated I/O function by the PCSEL register, the The Port C direction register controls the direction (input or output) of the line associated with the

	DIR7 DIR6 DIR5 DIR4	BIT 7 6 5 4	PCDIR Port C Direction Reg
WI	DIR3	3	Register
WI	DIR2	2	2
WI	DIR1	1	0x(FF)
W	DIRO	BIT 0	)FFF410

0

0

0

0

0

0x00

Table 10-12. Port C Direction Register Description

Name	Description	Setting
<b>DIRx</b> Bits 7–0	<b>Direction</b> —These bits control the direction of the pins in an 8-bit system. They reset to 0.	0 = Input 1 = Output

### 10.4.3.2 Port C Data Register

The settings for the PCDATA bit positions are shown in Table 10-13.

PCDATA			Port C Data Register	ta Regist	.er		0x(FF	=F)FFF411
	BIT 7	<b>o</b>	5	4	ω	2	_	ВІТ 0
	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	ſW	W	WI	WI	١w	W	W	rw
	0	0		0	0	0	0	0
RESET		* >	$0\text{x}00^*$ Actual bit value depends on external circuits connected to pin.	0x1 depends on ex	0x00* external circuits	connected to	o pin.	

Table 10-13. Port C Data Register Description

Name	Description	Setting
Dx Bits 7–0	Data—These bits reflect the status of the I/O signal.	0 = Drives the output signal low when DIRx is set to 1 or the external signal is low when DIRx is set to 0 1 = Drives the output signal high when DIRx is set to 1 or the external signal is high when DIRx is set to 0

Port C is primarily multiplexed with the LCD controller's signals. These pins can be programmed as GPIO Panel," on page 8-3 for more detailed information. when the LCD controller is not used. See Section 8.2.1, "Connecting the LCD Controller to an LCD

the signal driving the pins. The Dx bits can be written at any time. Bits that are configured as inputs will bits are high (output), the Dx bits control the pins. While the DIRx bits are low (input), the Dx bits report These bits control or report the data on the pins while the associated SELx bits are high. While the DIRx



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an output. The actual value on the pin is reported when these bits are read, regardless of whether they are configured as input or output. accept the data, but the data written to each cannot be accessed until the corresponding pin is configured as

## 10.4.3.3 Port C Dedicated I/O Functions

assignments are shown in Table 10-14. The eight PCDATA lines are multiplexed with the LCD controller dedicated I/O signals whose

Table 10-14. Port C Dedicated Function Assignments

	7 Data bit 7 LACD	6 Data bit 6 LCLK	5 Data bit 5 LLP	4 Data bit 4 LFLM	3 Data bit 3 LD3	2 Data bit 2 LD2	1 Data bit 1 LD1	0 Data bit 0 LD0	Bit GPIO Function Dedicated I/O Function	
--	-------------------	-------------------	------------------	-------------------	------------------	------------------	------------------	------------------	--	--

# 10.4.3.4 Port C Pull-down Enable Register

The Port C pull-down enable register (PCPDEN) controls the pull-down resistors for each line in Port C The settings for the bit positions are shown in Table 10-15.

PCPDEN		Port C Pull-dov	ull-down	Enable	Enable Register	7	0x(FF	)FFF412
	BIT 7	0	Сī	4	ω	2	_	BIT 0
	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
TYPE	W	WI	W	W	W	W	W	w
DE CET	_	1	_	_	_	_	_	_
7 6				0	0xFF			
		3						

# Table 10-15. Port C Pull-down Enable Register Description

Name	Description	Setting
PDx Pull- Bits 7–0 port.	<b>Pull-down</b> —These bits enable the pull-down resistors on the port.	0 = Pull-down resistors are disabled 1 = Pull-down resistors are enabled

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### 10.4.3.5 Port C Select Register

assigned as a GPIO or to a dedicated I/O function. The settings for the bit positions are shown in The Port C select register (PCSEL) determines if a bit position in the Port C data register (PCDATA) is

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P

#### ort C Select Register

#### 0x(FF)FFF413

	RESET	TYPE		
	<u> </u>	ſW	SEL7	BIT 7
	<b>-</b>	W	SEL6	6
	_	W	SEL5	5
0 <u>×</u>	_	W	SEL4	4
<b>)</b>	<u>-</u>	W	SEL3	3
	_	W	SEL2	2
	_	W	SEL1	1
	_	W	SEL0	BIT 0

Table 10-16. Port C Select Register Description

	SELx Bits 7–0	Name	
ARCHIVED BY FREESCALE SEMIC	Select—These bits select whether the internal chip function or I/O port signals are connected to the pins.  0 = The dedicated function pins are connected.  1 = The I/O port function pins are connected.	Description Setting	

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#### 10.4.4 Port D Operation

should be used as either a general-purpose, interrupt-generating port or as a keyboard input port Figure 10-3 illustrates how this type of port operates. Port D has the same functionality as other GPIO ports, except that it also has interrupt capabilities.

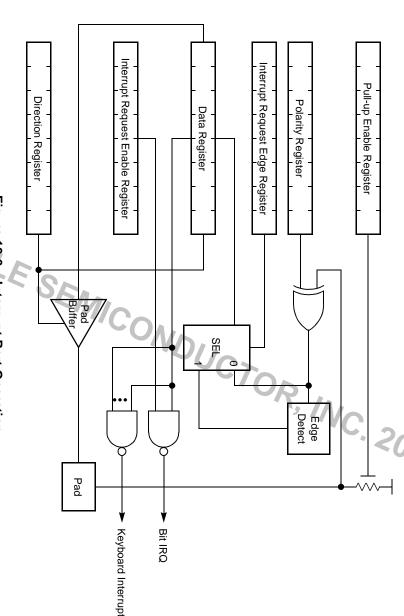


Figure 10-3. Interrupt Port Operation

Register," on page 9-12 for more details bit is the logical OR result of all eight bits, which is applied to the MC68VZ328 interrupt controller as a Port D generates nine interrupt signals. Eight of these interrupts are generated by the bits of each port. One level 4 keyboard interrupt (KB) in the interrupt status register. See Section 9.6.4, "Interrupt Status ARCHIVED BY FRI

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#### 10.4.5 Port D Registers

Unlike the other ports, Port D is unique in that it is comprised of eight 8-bit I/O registers. They consist of the following: /CTOR, /NC. 2005

- Port D direction register (PDDIR)
- Port D data register (PDDATA)
- Port D pull-up enable register (PDPUEN)
- Port D select register (PDSEL)
- Port D polarity register (PDPOL)
- Port D interrupt request enable register (PDIRQEN)
- Port D keyboard enable register (PDKBEN)
- Port D interrupt request edge register (PDIRQEG)

#### 10.4.5.1 **Port D Direction Register**

The Port D direction register controls the direction (input or output) of the line associated with the DIR bits are ignored. The settings for the PDDIR bit positions are shown in Table 10-17. PDDATA bit position. When the data bit is assigned to a dedicated I/O function by the PDSEL register, the

PDDIR		Port	rt D Direct	Figor T	Register		0x(FF	)FFF418
	BIT 7	6	5	4	3	2	1	BIT 0
	DIR7	DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0
TYPE	ľW	WI	W	ſW	W	W	W	۲W
D II O II I	0	0	0	0	0	0	0	0
7.00			14	O <sub>X</sub>	0x00			

## Table 10-17. Port D Direction Register Description

	DIRx Bits 7–0	Name
ARCHIVED BY F	<b>Direction</b> —These bits control the direction of the pins in an 8-bit system. They reset to 0.	Description
	0 = Input 1 = Output	Setting



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#### 10.4.5.2 Port D Data Register

The settings for the PDDATA bit positions are shown in Table 10-18

PDDATA		Pc	Port D Data Register	a Regist	er	0	0x(FF	)FFF419
	BIT 7	თ	σı	4	ω	2	_	BIT 0
	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	W	W	W	ſW	W	rw	WI	W
	_	_	_	_	Ż,	_	_	_
RESET		*Actı	0xFF* *Actual bit value depends on external circuits connected to pin.	0xF epends on ex	0xFF* external circuits	connected to	pin.	
					,			

Table 10-18. Port D Data Register Description

Name	Description	Setting
<b>Dx</b> Bits 7–0	Data—These bits reflect the status of the I/O signal.	0 = Drives the output signal low when DIRx is set to 1 or the external signal is low when DIRx is set to 0
		1 = Drives the output signal high when DIRx is set to 1 or the external signal is high when DIRx is set to 0

are shown in Table 10-19. Port D signals can be programmed as GPIO when not used for handling external The eight PDDATA lines are multiplexed with the INT and IRQ dedicated I/O signals whose assignments

an output. The actual value on the pin is reported when these bits are read, regardless of whether they are the signal driving the pins. The Dx bits can be written at any time. Bits that are configured as inputs will configured as input or output. accept the data, but the data written to each cannot be accessed until the corresponding pin is configured as bits are high (output), the Dx bits control the pins. While the DIRx bits are low (input), the Dx bits report These bits control or report the data on the pins while the associated SELx bits are high. While the DIRx

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Table 10-19. Port D Dedicated Function Assignments

Data bit 7	6 Data bit 6 IR	5 Data bit 5	4 Data bit 4 IR	3	2		0	Bit GPIO Function Dedicated I	S
IRQ6	IRQ3	IRQ2	IRQ1	INT3	INT2	INT1	NT0	Dedicated I/O Function	

### **Port D Interrupt Options**

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Interrupt bits 3–0 ( $\overline{\text{INT}}[3:0]$ ), interrupt request bits 3–1 ( $\overline{\text{IRQ}}[3:1]$ ), interrupt request bit 6 ( $\overline{\text{IRQ6}}$ ), or Port D bits 7-0 can be configured as edge- or level-triggered interrupt signals.

#### NOTE:

interrupt controller. When programmed as level-triggered interrupts, these programmed as edge-triggered interrupts, they can be cleared by writing a When external interrupts  $\overline{\text{INT}}[3:0]$ ,  $\overline{\text{IRQ1}}$ ,  $\overline{\text{IRQ2}}$ ,  $\overline{\text{IRQ3}}$ , and  $\overline{\text{IRQ6}}$  are interrupts are cleared at the requesting sources. 1 to the corresponding status bit in the interrupt status register in the

described in Chapter 9, "Interrupt Controller." To support keyboard applications, the I/O function can be used with interrupt capabilities, which are

the interrupt is determined by the POLx bits of the PDPOL register. KBENx bits of the PDKBEN register. Individual interrupts can be configured as either edge- or The individual interrupt bits can be masked on a bit-by-bit basis. level-sensitive by asserting or clearing the IQEGx bits of the PDIRQEG register. Likewise, the polarity of The KB is enabled or disabled by the

signals and OR (negative logic) can be selected to generate keyboard (KB) interrupts to the CPU. The KBx generate a CPU interrupt. configured as an input or output on a bit-by-bit basis. When they are configured as inputs, each pin can signal is an active low, level-sensitive interrupt of the selected pins. Like the other ports, each pin can be interrupt on INT[3:0]. Edge interrupts on INT[3:0] can only interrupt the CPU when the system is awake The INT[3:0] signals are all level 4 interrupts, but IRQx has its own level. Any combination of Port D All of the interrupt signals in the table can be used as system wake-up interrupts, except for the edge

## Port D Pull-up Enable Register

settings for the bit positions in PDPUEN are shown in Table 10-20 The Port D pull-up enable register (PDPUEN) controls the pull-up resistors for each line in Port D. The

PDPUEN		Port D F	ull-up E	Port D Pull-up Enable Register	Register		0x(FF)	FFF41A	
	BIT 7	6	σı	4	ω	2	_	BIT 0	
	PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0	
TYPE	ſW	WI	W	W	WI	ſW	W	W	
7 7 7 7	_	1	_	_	_	_	_	_	
7 6 6 6		Y /		<b>©</b>	0xFF				

#### Table 10-20. Port D Pull-up Enable Register Description

Name Description	on Setting
PUx  Pull-up—These bits enable the pull-up resistors on the port.  0 = Pull-up re 1 = Pull-up re	-up resistors on the port.  0 = Pull-up resistors are disabled  1 = Pull-up resistors are enabled



### 10.4.5.5 Port D Select Register

assigned as a GPIO or to a dedicated I/O function. The settings for the bit positions of PDSEL are shown in The Port D select register (PDSEL) determines if a bit position in the Port D data register (PDDATA) is

PDSEL		Po	Port D Select I	ct Regist	ster 2		0x(FF)	FFF41B
	ВІТ 7	<b>o</b>	Ŋ	4	3	2	_	BIT 0
	SEL7	SEL6	SEL5	SEL4	/(			
TYPE	ſW	W	W	W	//			
RESET	_	_	_	_	0	0	0	0
7000				0x				

Table 10-21. Port D Select Register Description

Name	Description	Setting
SELx	Select—These bits select whether the internal	0 = The dedicated function pins are connected.
Bits 7-4	chip function or I/O port signals are connected to the pins.	1 = The I/O port function pins are connected.
Reserved Bits 3–0	Reserved	These bits are reserved and should be set to 0.

### 10.4.5.6 Port D Polarity Register

These bits select the input signal polarity of INT[3:0]. The polarity of the rising or falling edge is selected by the POLx bits. Interrupts are active high (or rising edge) when these bits are low. Interrupts are active Table 10-22. low (or falling edge) while these bits are high. The settings for the bit positions of PDPOL are shown in

PDPOL		Port	ort D Polarity	rity Registeı	ster		0x(FF)	FFF41C
	BIT 7	6	5	4	3	2	1	BIT 0
		E			POL3	POL2	POL1	POL0
TYPE		K			WI	W	WI	W
D II O II I	0	60	0	0	0	0	0	0
7 0 0		5/-		0x	0x00			
		3						

Table 10-22. Port D Polarity Register Description

Name	Description	Setting
Reserved Bits 7–4	Reserved	These bits are reserved and should be set to 0.
POLx Bits 3–0	Polarity—These bits determine the input signal 0 = Data is unchanged. polarity of INT[3:0] interrupts. 1 = The input data is inverse by the presented to the holds.	<ul><li>0 = Data is unchanged.</li><li>1 = The input data is inverted before being presented to the holding register.</li></ul>

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# Port D Interrupt Request Enable Register

controller module. The settings for the bit positions of PDIRQEN are shown in Table 10-23. The interrupt enable bits (IQEN[3:0]) determine which  $\overline{\text{INT}}$ [3:0] will generate an interrupt to the interrupt

PDIRQEN	Port	D Interr	upt Req	uest Ena	Port D Interrupt Request Enable Register	ster	0x(FF)	FF)FFF41D
	BIT 7	თ	Οī	4	ω	2	_	ВІТ 0
					IQEN3	IQEN2	IQEN1	IQEN0
TYPE					W	W	W	W
RESET	0	0	0	0	P	0	0	0
- - -				9	0x00			

Table 10-23. Port D Interrupt Request Enable Register Description

Name	Description	Setting
Reserved Bits 7–4	Reserved	These bits are reserved and should be set to 0.
IQENx Bits 3-0	Interrupt Enable—These bits select the INT[3:0] pins that are presented to the interrupt controller.	0 = Interrupt disabled. 1 = Interrupt enabled.
	C	

#### 10.4.5.8 Port D Keyboard Enable Register

the bit positions of PDKBEN are shown in Table 10-24 to be configured as an input. The SELx, POLx, IQENx, and IQEGx bits have no effect on the functionality generate a keyboard interrupt to the interrupt controller. When a KBENx bit is selected, the DIRx bits need All the selected signals are active low in reference to the external pins, and those that are asserted will Deasserting the interrupt source is the only way to clear a keyboard interrupt. The settings for

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PDKBEN		Port D K	Keyboard	Enable I	Register	·	0x(FF)	FFF41E
	BIT 7	6	51	4	ω	2	_	BIT 0
	KBEN7	KBEN6	KBEN5	KBEN4	KBEN3	KBEN2	KBEN1	KBEN0
TYPE	ſW	W	W	WI	W	W	W	w
D 0 0 1 1	0	0	0	0	0	0	0	0
7	h	Y		0x	0x00			

Table 10-24. Port D Keyboard Enable Register Description

Name	Description	Setting
KBENx Bits 7–0	<b>Keyboard Enable</b> —These bits select the INT[3:0] pins that are presented to the interrupt controller.	0 = The keyboard interrupt is disabled. 1 = The keyboard interrupt is enabled.

# Port D Interrupt Request Edge Register

settings for the bit positions of PDIRQEG are shown in Table 10-25 on page 10-21 interrupt for INT[3:0] cannot be used for system wake up. The level-sensitive interrupt should be used. The The polarity of the rising or falling edge is selected by the POLx bits. It should be noted that the edge-level



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DIRQEG	Port I	t D Inter	D Interrupt Request	quest Ed	t Edge Register	ster	0x(FF)	FFF41F
	BIT 7	6	5	4	3	2	1	ВІТ 0
					IQEG3	IQEG2	IQEG1	IQEG0
TYPE					W	W	W	W
D III O III III III III III III III III	0	0	0	0	0	0	0	0
7 -				0	0x00	?(		

Table 10-25. Port D Interrupt Request Edge Register Description

Name	Description	Setting
Reserved Bits 7–4	Reserved	These bits are reserved and should be set to 0.
IQEGx Bits 3–0	<b>Edge Enable</b> —The polarity of the rising or falling edge is selected by the POLx bits. $0 = \underline{\text{Level-sensitive interrupts are selected}}$ $1 = \underline{\text{INT}[3:0]}$ edge-sensitive interrupts are selected	0 = Level-sensitive interrupts are selected. 1 = INT[3:0] edge-sensitive interrupts are selected.

#### Port E Registers

Port E is composed of the following 8-bit general-purpose I/O registers:

is individually configured. Port E is multiplexed with the serial peripheral interface (SPI) and UART Each signal in the PEDATA register connects to an external pin. As with the other ports, each bit on Port E Port E pull-up enable register (PEPUEN)

Port E select register (PESEL)

signal in the Drive

#### Port E **Direction Register**

DIR bits are ignored. The settings for the bit positions of the PEDIR register are shown in Table 10-26 PEDATA bit position. When the data bit is assigned to a dedicated I/O function by the PESEL register, the The Port E direction register controls the direction (input or output) of the line associated with the

PEDIR	YK	Port E Dire	)irection Reເ	Register		0x(FF)	)FFF420
	BIT 7 <b>(27)</b> 6	5	4	3	2	1	ВІТ 0
	DIR7 DIR6	6 DIR5	DIR4	DIR3	DIR2	DIR1	DIR0
TYPE	W. W.	ſW	۲W	W	W	ſW	W
D II O II I	0	0	0	0	0	0	0
7	//		0x00	00			
	4						

Table 10-26. Port E Direction Register Description

Name	Description	Setting
DIRx Bits 7–0	<b>Direction</b> —These bits control the direction of the pins in an 8-bit system. They reset to 0.	0 = Input 1 = Output

### 10.4.6.2 Port E Data Register

The settings for the bit positions of the PEDATA register are shown in Table 10-27.

PEDATA		Po	Port E Data	ta Register	ier	0	0x(FF	)FFF421
	BIT 7	თ	Оī	4	ω	2	_	BIT 0
	D7	D6	D5	D4	D3	▼ D2	D1	D0
TYPE	W	۲W	WI	W	WI	ſW	۲W	W
	_	_	_	_	Ż	_	_	_

\*Actual bit value depends on external circuits connected to pin.

Table 10-27. Port E Data Register Description

Dx  Data—These bits reflect the Bits 7–0  Status of the I/O signal in an 8-bit system.  Data—These bits reflect the external signal low when DIRx is set to 1 or the external signal is high when DIRx is set to 1 or the external signal is high when DIRx is set to 0	Name	Description	Setting
status of the I/O signal in an 8-bit system.	Dx	Data—These bits reflect the	0 = Drives the output signal low when DIRx is set to 1 or the
	Bits 7-0	status of the I/O signal in an	external signal is low when DIRx is set to 0
external signal is high when DIRx is set to 0		8-bit system.	1 = Drives the output signal high when DIRx is set to 1 or the
			external signal is high when DIRx is set to 0

detailed information. "Serial Peripheral Interface 1 and 2," and Section 2.6, "Bus Control Signals," on page 2-6 for more can be programmed as GPIO when the SPI, UART, and bus control features are not used. See Chapter 13. Port E is multiplexed with the serial peripheral interface (SPI), UART, and bus control signals. These pins

accept the data, but the data written to each cannot be accessed until the corresponding pin is configured as an output. The actual value on the pin is reported when these bits are read, regardless of whether they are the signal driving the pins. The Dx bits can be written at any time. Bits that are configured as inputs will bits are high (output), the Dx bits control the pins. While the DIRx bits are low (input), the Dx bits report These bits control or report the data on the pins while the associated SELx bits are high. While the DIRx

## .4.6.3 Port E Dedicated I/O Functions

assignments are shown in Table 10-28. The eight PEDATA lines are multiplexed with the SPI and UART dedicated I/O signals whose

Table 10-28. Port E Dedicated Function Assignments

	4 Data bit 4	Data bit 3	2 Data bit 2	Data bit 1	0 Data bit 0	Bit 49 GPIO Function	<b>)</b>
TXD1	RXD1	DWE/UCLK	SPICLK2	SPIRXD	SPITXD	Dedicated I/O Function	

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Table 10-28. Port E Dedicated Function Assignments (Continued)

CTS1	Data bit 7	7
RTS1	Data bit 6	6
Dedicated I/O Function	GPIO Function	Bit

## Port E Pull-up Enable Register

The Port E pull-up enable register (PEPUEN) controls the pull-up resistors for each line in Port E. The settings for the bit positions of the PEPUEN register are shown in Table 10-29.

	RESET	TYPE			PEPUEN
	_	W	PU7	BIT 7	
	<b>-</b>	W	PU6	6	Port E F
	_	W	PU5	5	⊃ull-up E
0xFF		W	PU4	4	Port E Pull-up Enable Register
Ťİ	_	W	PU3	3	egister
	_	W	PU2	2	
	_	W	PU1	1	0x(FF
	_	W	PU0	ВІТ 0	)FFF422

#### Table 10-29. Port E **Pull-up Enable Register Description**

PUx Pull-up—These bits enable the pull-up resis- Bits 7–0  Pull-up—These bits enable the pull-up resis- 1 = Pull-up resistors are disabled 1 = Pull-up resistors are enabled	Name	Description	Setting
	PUx Bits 7–0	<b>Pull-up</b> —These bits enable the pull-up resistors on the port	0 = Pull-up resistors are disabled 1 = Pull-up resistors are enabled

### Port E Select Register

are shown in Table 10-30. assigned as a GPIO or to a dedicated I/O function. The settings for the bit positions of the PEDIR register The Port E select register (PESEL) determines if a bit position in the Port E data register (PEDATA) is

PESEL		Po	rt E Sele	Select Register	ter		0x(FF)	FFF423	
	BIT 7	<b>o</b>	Οī	4	ω	2	_	BIT 0	
	SEL7	SEL6	SEL5	SEL4	SEL3	SEL2	SEL1	SEL0	
TYPE	W	W	W	۲W	W	W	W	W	
D III O III III III III III III III III	1 12	_	_	_	_	_	_	_	
7 0 -	<b>D</b>			0x	0xFF				

#### Table 10-30. Port E **Select Register Description**

Name	Description	Setting
SELx Bits 7–0	SELx Select—These bits select whether the internal chip Bits 7–0 Bits 7–0  Select—These bits select whether the internal chip function or I/O port signals are connected to the pins.  0 = The dedicated function pins are connected 1 = The I/O port function pins are connected	0 = The dedicated function pins are connected. 1 = The I/O port function pins are connected.

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#### Port F Registers

Port F is composed of the following 8-bit general-purpose I/O registers

Port F direction register (PFDIR)
Port F data register (PFDATA)
Port F pull-up enable register (PFPUEN)
Port F select register (PFSEL)
Each signal in the PFDATA register connects to an external pin. As on the other ports, each bit on Port F individually configured. individually configured.

### **Port F Direction Register**

PFDATA bit position. When the data bit is assigned to a dedicated I/O function by the PFSEL register, the The Port F direction register controls the direction (input or output) of the line associated with the The settings for the PFDIR bit positions are shown in Table 10-31

PFDIR		Po	Port F Direction	ction Re	Register		0x(FF	)FFF428	
	ВІТ 7	6	5	4	3	2	1	BIT 0	
	DIR7	DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0	
TYPE	W	W	WI	WJ	WI	WI	WI	W	
D D D D D D D T D	0	0	0	0	0	0	0	0	
7				Ç0	0x00				

	Table 10-31.	
	Port F	
	Direction	
	Register	
•	Description	

	DIRx Bits 7–0	Name
ARCHIVED BY FREES	<b>Direction</b> —These bits control the direction of the pins in an 8-bit system. They reset to 0.	Description
	0 = Input 1 = Output	Setting

**Programming Model** 

#### 10.4.7.2 Port F Data Register

The settings for the bit positions of the PFDATA register are shown in Table 10-32

PFDATA		Pc	Port F Data Register	a Regist	er	05	0x(FF	)FFF429
	BIT 7	o	σı	4	ω	2	_	ВІТ 0
	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	W	ſW	W	ΓW	WI	rw	WI	rw
	_	_	_	_	V,	<u> </u>	_	<b>_</b>
RESET		*Actı	0xFF* *Actual bit value depends on external circuits connected to pin.	0xFF* epends on exterr	:F* ternal circuits	connected to	pin.	
				-	<b>)</b>		7	

Table 10-32. Port F Data Register Description

Name	Description	Setting
Dx	Data—These bits reflect the	0 = Drives the output signal low when DIRx is set to 1 or the external
Bits 7–0 s	status of the I/O signal in an	signal is low when DIRx is set to 0
<u> </u>	8-bit system.	1 = Drives the output signal high when DIRx is set to 1 or the external
		signal is high when DIRx is set to 0

programmed as GPIO when the address bus and the dedicated I/O signals are not in use. Port F is multiplexed with address lines A[23:20] and several dedicated functions. These pins can be

an output. The actual value on the pin is reported when these bits are read, regardless of whether they are accept the data, but the data written to each cannot be accessed until the corresponding pin is configured as bits are high (output), the Dx bits control the pins. While the DIRx bits are low (input), the Dx bits report These bits control or report the data on the pins while the associated SELx bits are high. While the DIRx ARCHIVED BY FREESCA!

## Port F Dedicated I/O Functions

The eight PFDATA lines are multiplexed with the dedicated I/O signals whose assignments are shown in

Table 10-33. Port F Dedicated I/O Function Assignments

	,(	
CSA1	Data bit 7	7
A23	Data bit 6	6
A22	Data bit 5	5
A21	Data bit 4	4
A20	Data bit 3	3
CLKO	Data bit 2	2
ĪRQ5	Data bit 1	1
LCONTRAST	Data bit 0	0
Dedicated I/O Function	GPIO Function	Bit

interrupt. adjust the supply voltage to the LCD panel. Bit 1 can be programmed as IRQ5, an external level 5 The LCONTRAST function controls the pulse-width modulator (PWM) inside the LCD controller to

and electromagnetic emission. This signal defaults to a PF2 input signal. See Section 4.2, "CGM Bit 7 is used for the chip-select signal CSA1. See Section 6.2, "Chip-Select Operation," on page 6-2 for Operational Overview," on page 4-3 for more information about this signal. This signal is provided for external reference. The CLKO output clock signal is internally connected to the SYSCLK clock output of the internal CGM The output can be disabled to reduce power consumption

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# Port F Pull-up/Pull-down Enable Register

F. The settings for the PFPUEN bit positions are shown in Table 10-34. The Port F pull-up/pull-down enable register (PFPUEN) controls the pull-up resistors for each line in Port

PFPUEN	Port	Port F Pull-up/Pull-dow	ıp/Pull-d	ے	Enable Register	ster	0x(FF)	FFF42A
	BIT 7	6	Οī	4	ω	2	_	BIT 0
	PU7	PD6	PD5	PD4	PD3	PU2	PU1	PU0
TYPE	W	۲W	W	W	W	١w	W	ſW
RESET	_	_	_	_	<i> </i>	_	_	_
7 0 1				0x	0xFF			

Table 10-34. Port F Pull-up/Pull-down Enable Register Description

Name	Description	Setting
<b>PU7</b> Bit 7	<b>Pull-up</b> —This bit enables the pull-up resistor on the port.	0 = Pull-up resistor is disabled 1 = Pull-up resistor is enabled
PDx Bits 6–3	<b>Pull-down</b> —These bits enable the pull-down resistors on the port.	0 = Pull-down resistors are disabled 1 = Pull-down resistors are enabled
PUx Bits 2-0	<b>Pull-up</b> —These bits enable the pull-up 0 = Pull-up resistors are disabled resistors on the port.	0 = Pull-up resistors are disabled 1 = Pull-up resistors are enabled

### 10.4.7.5 Port F Select Register

The Port F select register (PFSEL) determines if a bit position in the data register (PFDATA) is assigned as a GPIO or to a dedicated I/O function. The settings for the PFSEL bit positions are shown in Table 10-35.

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PFSEL		Por	↑F Sele	ort F Select Register	ster		0x(FF)	FFF42B	
	ВІТ 7	S	бī	4	ω	2	_	ВІТ 0	
	SEL7	SEL6	SEL5	SEL4	SEL3	SEL2	SEL1	SEL0	
TYPE	rw	M	W	W	۲W	W	W	W	,
D   0   1   1   1   1   1   1   1   1   1	_	0	0	0	0	_	_	_	
- -		F		0	0x87				

### Table 10-35. Port F Select Register Description

Name	Description	Setting
SELx Bits 7–0	SELx Select—These bits select whether the internal chip function or I/O port signals are connected to the pins.	<ul><li>0 = The dedicated function pins are connected.</li><li>1 = The I/O port function pins are connected.</li></ul>

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#### 10.4.8 Port G Registers

Port G is comprised of the following 8-bit general-purpose I/O registers

- Port G direction register (PGDIR)
- Port G data register (PGDATA)
- Port G pull-up enable register (PGPUEN
- Port G select register (PGSEL)

not connected to external pins. Port G provides a total of six pins, and each bit is individually configured Each signal in the PGDATA register connects to an external pin. It should be noted that pins 6 and 7 are

## 10.4.8.1 Port G Direction Register

DIR bits are ignored. The settings for the PGDIR bit positions are shown in Table 10-36. PGDATA bit position. The Port G direction register controls the direction (input or output) of the line associated with the When the data bit is assigned to a dedicated I/O function by the PGSEL register, the

PGDIR	) 	Po	Port G Direction F	ection Re	Register	)	0x(FF)	Ŧ
	ВІТ 7	6	5	4	3	2	1	BIT 0
			DIR5	DIR4	DIR3	DIR2	DIR1	DIR0
TYPE			W	WJ	W	W	rw	W
D D D D D D T	0	0	0	0	0	0	0	0
7000			Se.	Q)	0x00			

Table 10-36.	
Port G	
Direction	(
Register	
Description	

Name	Description	Setting
Reserved Bits 7–6	Reserved	These bits are reserved and should be set to 0.
DIRx Bits 5–0	<b>Direction</b> —These bits control the direction of the pins in an 8-bit system. They reset to 0.	0 = Input 1 = Output

### 10.4.8.2 Port G Data Register

The settings for the bit positions of the PGDATA register are shown in Table 10-37 on page 10-29



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RESET TYPE BIT 7 0 0 Port G Data Register ₹ D5 \_ ₹ Ω D3 ₹ 22 0x(FF)FFF431 ₹ \_ BIT 0 DO ₹

Table 10-37. Port G Data Register Description

\*Actual bit value depends on external circuits connected to pin.

Name	Description	Setting
Reserved Bits 7–6	Reserved	These bits are reserved and should be set to 0.
<b>D</b> x Bits 5–0	Data—These bits reflect the status of the I/O signal in an 8-bit system.	0 = Drives the output signal low when DIRx is set to 1 or the external signal is low when DIRx is set to 0 1 = Drives the output signal high when DIRx is set to 1 or the external signal is high when DIRx is set to 0

programmed as GPIO when the address bus and the dedicated I/O signals are not in use. Port G is multiplexed with address line A0 and several dedicated I/O functions. These pins can be

setting the bits in the PGDIR register. whether they are configured as input or output. See Table 10-36 on page 10-28 for information about configured as an output. The actual value on the pin is reported when these bits are read, regardless of will accept the data, but the data written to each cannot be accessed until the corresponding pin is report the signal driving the pins. The Dx bits can be written at any time. Bits that are configured as inputs DIRx bits are high (output), the Dx bits control the pins. While the DIRx bits are low (input), the Dx bits All of the bits control or report the data on the pins while the associated SELx bits are high. While the

## .4.8.3 Port G Dedicated I/O Functions six PGDATA lines are multiplexed with the dedicated I/

The six PGDATA lines are multiplexed with the dedicated I/O signals whose assignments are shown in Table 10-38.

Table 10-38. Port G Dedicated I/O Function Assignments

BUSW/DTACK A0 EMUIRQ HIZ/P/D EMUCS EMUBRK
---

T

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acknowledge signal. The MC68VZ328 microprocessor will latch the BUSW signal at the rising edge of the reset, this signal defaults to A0. BUSW is the default bus width for the CSA0 signal. The DTACK signal is the external input data Reset signal. Its mode will determine the default bus width for CSA0. Bit 1 is Address 0. After system

or in data space during emulation mode. The remaining bits are dedicated in-circuit emulation controls. used in conjunction with in-circuit emulation that shows whether the current bus cycle is in program space pin defaults to a GPIO input pulled high, but can be programmed as the  $P/\overline{D}$  function.  $P/\overline{D}$  is a status signal release. For normal operation, this pin must be pulled high during system reset or left unconnected. This will put the MC68VZ328 into Hi-Z mode, in which all MC68VZ328 pins are three-stated after reset Bit 3 is HIZ/P/D (High Impedance or Program/Data). During system reset, a logic low of this input signal See Chapter 16, "In-Circuit Emulation," for detailed information on their operation.

# **Port G Operational Considerations**

dedicated function, except bit 3, which has an I/O function. To ensure normal operation, the EMUIRQ and emulation mode. EMUBRK pins must stay high or not be connected during system reset. Otherwise, the chip will enter Port G can be used as a GPIO as long as caution is exercised. After reset, the Port G pins default to the

I/O when the system is 16-bit and there is no pull-up after reset for this pin. When bits 2–5 are used as I/O, the emulation mode cannot be used during development and debugging. Once development is complete, bits 2–5 can be used as I/O in the final system. Bit 1 (A0) can be used as

## Port G Pull-up Enable Register

Table 10-39 for the bit settings of the PGPUEN register. The pull-up enable register (PGPUEN) controls the pull-up resistors for each line in Port G. See

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GPUEN		Port G	Port G Pull-up Enable	Enable F	Register		0x(FF)	)FFF432
	BIT 7	6	5	4	ω	2	_	ВІТ 0
			PU5	PU4	PU3	PU2	PU1	PU0
TYPE		5	ľW	W	W	WI	W	ſW
DE OE	0	0	_	_	_	<u> </u>	0	<u> </u>
; ; ;		RE		0×	0x3D			

#### Table 10-39. Port G Pull-up Enable Register Description

Name	Description	Setting
Reserved Bits 7–6	Reserved	These bits are reserved and should be set to 0.
PUx Bits 5–0	<b>Pull-up</b> —These bits enable the pull-up resistors on the port.	0 = Pull-up resistors are disabled 1 = Pull-up resistors are enabled

#### 10.4.8.6 Port G Select Register

in the PGSEL register. The select register (PGSEL) determines if a bit position in the data register (PGDATA) is assigned as a GPIO or to a dedicated I/O function. See Table 10-40 on page 10-31 for information about setting the bits



**Programming Model** 

RESET 0 0	TYPE		BIT 7 6	<b>GSEL</b> Port
0	W	SEL5	5	Port G Select I
0	W	SEL4	4	ct Register
_	W	SEL3	3	ster
0	W	SEL2	2	
0	W	SEL1	_	0x(FF)
0	W	SEL0	BIT 0	)FFF433

Table 10-40. Port G Select Register Description

<ul><li>0 = The dedicated function pins are connected.</li><li>1 = The I/O port function pins are connected.</li></ul>	Select—These bits select whether the internal chip function or I/O port signals are connected to the pins. 0 = The dedicated function pins are connected.	SELx Bits 5-0
These bits are reserved and should be set to 0.	Reserved	Reserved Reserved Bits 7–6
Setting	Description	Name

#### 10.4.9 Port J Registers

Port J is composed of the following four general-purpose I/O registers:

Each signal in the PJDATA register connects to an external pin. As on the other ports, each bit on Port J is Port J pull-up enable register (PJPUEN)

Port J select register (PJSEL)

signal in the pro-

### **Port J Direction Register**

position. When the data bit is assigned to a dedicated I/O function by the PJSEL register, the DIR bits are The direction register controls the direction (input or output) of the line associated with the PJDATA bit ignored. The settings for the bit positions are shown in Table 10-41

PJDIR	FPO	Port J Direction I		Register		0x(FF)	)FFF438
	BIT 7 6	5	4	3	2	1	ВІТ 0
	DIR7 DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0
TYPE	rw	W	W	W	W	W	rw
В П О П Т	0	0	0	0	0	0	0
7.00	VE		0 X	0x00			

Port J Direction Register Description

Name	Description	Setting
DIRx Bits 7–0	<b>Direction</b> —These bits control the direction of the pins in an 8-bit system. They reset to 0.	0 = Input 1 = Output

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### 10.4.9.2 Port J Data Register

PJDATA	The bit settings for the PJDATA
Port J Data Register	The bit settings for the PJDATA register are shown in Table 10-42.
05	7

\*Actual bit value depends on external circuits connected to pin.

RESET

TYPE

D7

₩ D6

₩ D5

₽ 5

₹D3

₹ 2

₹ 2

0x(FF)FFF439

DO BIT 0

Table 10-42. Port J Data Register Description

Dx  Data—These bits reflect the Bits 7–0  Status of the I/O signal in an 8-bit system.  Data—These bits reflect the external signal low when DIRx is set to 1 or the external signal is high when DIRx is set to 1 or the external signal is high when DIRx is set to 0	Name	Description	Setting
status of the I/O signal in an 8-bit system.	Dx	Data—These bits reflect the	0 = Drives the output signal low when DIRx is set to 1 or the
	Bits 7-0	status of the I/O signal in an	external signal is low when DIRx is set to 0
external signal is high when DIRx is set to 0		8-bit system.	1 = Drives the output signal high when DIRx is set to 1 or the
			external signal is high when DIRx is set to 0

be programmed as GPIO when the dedicated I/O signals are not in use. Port J is multiplexed with the configurable SPI (with internal FIFO) and UART 2 signals. These pins can

configured as input or output. an output. The actual value on the pin is reported when these bits are read, regardless of whether they are accept the data, but the data written to each cannot be accessed until the corresponding pin is configured as the signal driving the pins. The Dx bits can be written at any time. Bits that are configured as inputs will bits are high (output), the Dx bits control the pins. While the DIRx bits are low (input), the Dx bits report These bits control or report the data on the pins while the associated SELx bits are high. While the DIRx

## 0.4.9.3 Port J Dedicated I/O Functions

The eight PJDATA lines are multiplexed with the dedicated I/O signals whose assignments are shown in

Table 10-43. Port J Dedicated I/O Function Assignments

Bit	GPIO Function	Dedicated I/O Function
0 8	Data bit 0	MOSI
Q'ı	Data bit 1	OSIM
2	Data bit 2	SPICLK1
3	Data bit 3	SS
C <sub>4</sub>	Data bit 4	RXD2
<b>P</b> 5	Data bit 5	TXD2
6	Data bit 6	RTS2

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Table 10-43. Port J Dedicated I/O Function Assignments (Continued)

7 Data bit 7 CTS2

Signals," on page 13-3. The remaining 4 bits are control signals for UART 2; more information appears in Section 14.2.3, "Serial Interface Signals," on page 14-3. Bits 0–3 are control signals connected to SPI 1. Their operation is detailed in Section 13.2.4, "SPI 1

## 10.4.9.4 Port J Pull-up Enable Register

for the PJPUEN register are shown in Table 10-44. The pull-up enable register (PJPUEN) controls the pull-up resistors for each line in Port J. The bit settings

PJPUEN	BIT 7	Port J	Pull-up I	Port J Pull-up Enable Register	egister	S	0x(FF)	FFF43A
	BIT 7	6	5	4	3	2	1	BIT 0
	PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0
TYPE	W	W	W	WI	W	W	W	W
RE SET	_	_	_	Q	_	_	_	_
7 0 -				C <sub>(</sub>	0xFF			

## Table 10-44. Port J Pull-up Enable Register Description

Pull-up—These bits enable the pull-up resis-	Name	Description	Setting
	PUx Bits 7–0	Pull-up—These bits enable the pull-up resistors on the port	0 = Pull-up resistors are disabled

### 10.4.9.5 Port J Select Register

The select register (PJSEL) determines if a bit position in the data register (PJDATA) is assigned as a GPIO or to a dedicated I/O function. The bit settings for the PJSEL register are shown in Table 10-45

PJSEL	Q <sup>2</sup>	Port J Select I	elect Register	ster		0x(FF)	FFF43B
	BIT 7	5	4	3	2	1	ВІТ 0
	SEL7 SEL6	:L6 SEL5	SEL4	SEL3	SEL2	SEL1	SEL0
TYPE	rw / rw	w	W	W	W	W	W
D II O II T	j	_	0	_	_	_	<u> </u>
; ; ;	VE			0xEF			

### Table 10-45. Port J Select Register Description

Name	Description	Setting
SELx Bits 7–0	Select—These bits select whether the internal chip function or I/O port signals are connected to the pins.  0 = The dedicated function pins are connected to the pins.	0 = The dedicated function pins are connected. 1 = The I/O port function pins are connected.

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<del>1</del>0

#### 10.4.10 Port K Registers

Port K is composed of the following 8-bit general-purpose I/O registers

Port K direction register (PKDIR)
Port K data register (PKDATA)
Port K pull-up/-down enable register (PKPUEN)
Port K select register (PKSEL)
Each signal in the PKDATA register connects to an external pin. As on the other ports, each bit on Port K is individually configured

## **Port K Direction Register**

ignored. The settings for the PKDIR register bit positions are shown in Table 10-46. position. When the data bit is assigned to a dedicated I/O function by the PKSEL register, the DIR bits are The direction register controls the direction (input or output) of the line associated with the PKDATA bit

PKDIR		Port k	Û	irection Re	Register		0x(FF	)FFF440
	ВІТ 7	o	ΟΊ	4	ω	2	_	ВІТ 0
	DIR7	DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0
TYPE	ſW	WI	W	WJ	۲W	W	W	ľW
D D D D D D H	0	0	0	0	0	0	0	0
7 0 0				O <sub>X</sub>	0x00			

Table 10-46. Port K Direction Register Description

Name	Description	Setting
DIRx	Direction—These bits control the direction of	0 = The pins are inputs.
Bits 7-0	the pins in an 8-bit system. They reset to 0.	1 = The pins are outputs.

### Port K Data Register

The settings for the PKDATA register bit positions are shown in Table 10-47 on page 10-35





**Programming Model** 

#### BIT 7 D7 В Port K Data Register D5 Ω D3 22 0x(FF)FFF441 BIT 0 DO

\*Actual bit value depends on external circuits connected to pin.

RESET

TYPE

₹

0 ₹

₹

₹

₹

**→** §

₹

0

0

Table 10-47. Port K Data Register Description

Name	Description	Setting
Dx	Data—These bits reflect the status of	0 = Drives the output signal low when DIRx is set to 1 or the
Bits 7-0	Bits 7–0 the I/O signal in an 8-bit system.	external signal is low when DIRx is set to 0
		1 = Drives the output signal high when DIRx is set to 1 or the
		external signal is high when DIRx is set to 0

GPIO when the dedicated I/O signals are not in use. Port K is multiplexed with the IrDA, SPI, and LCD controller signals. These pins can be programmed as

configured as input or output. an output. The actual value on the pin is reported when these bits are read, regardless of whether they are accept the data, but the data written to each cannot be accessed until the corresponding pin is configured as the signal driving the pins. The Dx bits can be written at any time. bits are high (output), the Dx bits control the pins. While the DIRx bits are low (input), the Dx bits report These bits control or report the data on the pins while the associated SELx bits are high. While the DIRx Bits that are configured as inputs will

## 0.4.10.3 Port K Dedicated I/O Functions

The eight PKDATA lines are multiplexed with the dedicated I/O signals whose assignments are shown in

Table 10-48. Port K Dedicated I/O Function Assignments

4/	RC	4	/1							_
	7	6	ΟΊ	4	3	2	1	0	Bit	
	Data bit 7	Data bit 6	Data bit 5	Data bit 4	Data bit 3	Data bit 2	Data bit 1	Data bit 0	GPIO Function	3
	LD7	LD6	LD5	LD4	UDS	LDS	R₩	DATA_READY/PWM2	Dedicated I/O Function	

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selected. This pin defaults to Port K data bit 0, GPIO input, pulled high. data. PWMO2 is an output signal from the PWM 2 module. If this pin is configured as this dedicated function and PKDIR0 is set to 1, the PWMO2 signal is selected. If PKDIR0 is 0, DATA\_READY is When bit 0 is set as DATA\_READY, it can be used in master mode to signal the SPI master to clock out

bit 1, GPIO input, pulled high. When selected bit 1 ( $R\overline{W}$ ) is connected to the 68000 CPU Read/Write signal, this pin defaults to Port K

more detailed information. The remaining bits are involved with bus control. See Section 2.6, "Bus Control Signals," on page 2-6 for

#### Port K Pull-up/Pull-down **Enable** Register

line in Port K. The settings for the PKPUEN register bit positions are shown in Table 10-49 The pull-up/pull-down enable register (PKPUEN) controls the pull-up and the pull-down resistors for each

PKPUEN	Port	Port K Pull-up/Pull-dow	ıp/Pull-c	down Enable I	$\mathbf{T}$	Register	0x(FF	)FFF442	
	BIT 7	6	Б	4	ω	2	_	BIT 0	
	PD7	PD6	PD5	PD4	PU3	PU2	PU1	PU0	
TYPE	ľW	WI	W	TW	W	W	W	ſW	
RESET	_	_	_	Q	_	_	_	_	
7.00				C OXFF	Ή				

#### Table 10-49. Port K Pull-up/Pull-down Enable Register Description

<b>PUx Pull-up/Pull-down Enable</b> —These bits enable  O = Pull-up and pull-down resistors are disabled  the pull-up and pull-down resistors on the port.  1 = Pull-up and pull-down resistors are enabled	Name	Description	Setting
the pull-up and pull-down resistors on the port.	PUx	Pull-up/Pull-down Enable—These bits enable	0 = Pull-up and pull-down resistors are disabled
		the pull-up and pull-down resistors on the port.	1 = Pull-up and pull-down resistors are enabled

### Port K Select Register

The select register (PKSEL) determines if a bit position in the data register (PKDATA) is assigned as a Table 10-50. GPIO or to a dedicated I/O function. The settings for the PKSEL register bit positions are shown in

PKSEL		Po	Port K Select	ct Registe	ter		0x(FF)	)FFF443
	ВІТ 7	o o	Ŋ	4	ω	Ν	<u> </u>	BIT 0
	SEL7	SEL6	SEL5	SEL4	SEL3	SEL2	SEL1	SEL0
TYPE	rw	LM.	۲W	W	W	W	W	rw
7 7 7		_	_	_	_	_	_	_
7 7 7 8	V			0x	0xFF			

#### Table 10-50. Port K Select Register Description

Name	Description	Setting
SELx Bits 7–0	SELxSelect—These bits select whether the internal chip0 = The dedicated function pins are connectedBits 7-0function or I/O port signals are connected to the pins.1 = The I/O port function pins are connected	0 = The dedicated function pins are connected. 1 = The I/O port function pins are connected.

**Programming Model** 

#### **Port M Registers**

Port M is composed of the following four general-purpose I/O registers

Port M direction register (PMDIR)
Port M data register (PMDATA)
Port M pull-up enable register (PMPUEN)
Port M select register (PMSEL)
Each signal in the PMDATA register connects to an external pin. It should be noted that pins 6 and 7 are not connected to external pins.

## **Port M Direction Register**

ignored. The settings for the PMDIR register bit positions are shown in Table 10-51. position. When the data bit is assigned to a dedicated I/O function by the PMSEL register, the DIR bits are The direction register controls the direction (input or output) of the line associated with the PMDATA bit

<b>PMDIR</b>		Port M	rt M Dire	1 Direction Re	Register		0x(FF	(FF)FFF448
	BIT 7	6	5	4	3	2	1	ВІТ 0
			DIR5	DIR4	DIR3	DIR2	DIR1	DIR0
TYPE			W	ΓW	W	W	rw	rw
R R R R R R R R R R R R R	0	0	0	0	0	0	0	0
- - -				O <sub>X</sub>	0x00			

Table 10-51.	
Port M	
Direction	
Register	
Description	

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	DIRx Bits 5–0	Reserved Bits 7–6	Name
ARCHIVED BY FR	<b>Direction</b> —These bits control the direction of the pins in an 8-bit system. They reset to 0.	Reserved	Description
	0 = The pins are inputs. 1 = The pins are outputs.	These bits are reserved and should be set to 0.	Setting

### Port M Data Register

n in Table 10-52

PMDATA	The settings for the PMDATA register bit positions are shown
	registe
ס	r bit
<u> </u>	od 1
ort M Data Regi	sitio
<u> </u>	ns a
ת	are
D	sho
⊇.	WI

\*Actual bit value depends on external circuits connected to pin.

RESET

0

0

₹ D5

₹ Ω

D3 ₹ 9

D2 ₹ 0

0 ₹  $\overline{\Delta}$  0x(FF)FFF449

BIT 0  $D_0$ ₹ 0

TYPE

BIT 7

0

Table 10-52. Port M Data Register Description

Name	Description	Setting
Reserved Bits 7–6	Reserved	These bits are reserved and should be set to 0.
<b>Dx</b> Bits 5–0	Data—These bits reflect the status of the I/O signal in an 8-bit system.	0 = Drives the output signal low when DIRx is set to 1 or the external signal is low when DIRx is set to 0 1 = Drives the output signal high when DIRx is set to 1 or the external signal is high when DIRx is set to 0

the SDRAM I/O signals are not in use. Port M is multiplexed with the SDRAM controller signals. These pins can be programmed as GPIO when

configured as input or output. an output. The actual value on the pin is reported when these bits are read, regardless of whether they are accept the data, but the data written to each cannot be accessed until the corresponding pin is configured as the signal driving the pins. The Dx bits can be written at any time. bits are high (output), the Dx bits control the pins. While the DIRx bits are low (input), the Dx bits report These bits control or report the data on the pins while the associated SELx bits are high. While the DIRx ARCHIVED BY FREES Bits that are configured as inputs will



**Programming Model** 

## 0.4.11.3 Port M Dedicated I/O Functions

The six PMDATA lines are multiplexed with the dedicated I/O signals whose assignments are shown in

Table 10-53. Port M Dedicated I/O Function Assignments

7	6	5	4	3	2	1	0	Bit
DA	(D)	Data bit 5	Data bit 4	Data bit 3	Data bit 2	Data bit 1	Data bit 0	GPIO Function
		DMOE	SDA10	DQML	DQMH	SDCE	SDCLK	Dedicated I/O Function

"DRAM Controller," for more details. All of the dedicated I/O functions are involved in the operation of the DRAM controller. See Chapter 7,

#### Port M Pull-up/Pull-down **Enable** Register

line in Port M. The settings for the PMPUEN register bit positions are shown in Table 10-54 The pull-up/pull-down enable register (PMPUEN) controls the pull-up and pull-down resistors for each

PMPUEN	Port N	M Pull-up/Pull-dow	p/Pull-d	_	n Enable Register	ister	0x(FF)	FFF44A
	BIT 7	6	5	4	3	2	1	ВІТ 0
		117	PU5	PD4	PD3	PD2	PD1	PD0
TYPE			W1	W	W	ſW	W	ľW
D D D D D D D D D D D D D D D D D D D	0	0	_	_	<u></u>	_	_	<b>-</b>
7 0 1		FA		Q	0x3F			

# Table 10-54. Port M Pull-up/Pull-down Enable Register Description

Name	Description	Setting
Reserved Bits 7–6	Reserved	These bits are reserved and should be set to 0.
PUx Bits 5–0	Pull-up/Pull-down Enable—These bits enable 0 = Pull-up and pull-down resistors are disabled the pull-up and pull-down resistors are enabled	0 = Pull-up and pull-down resistors are disabled 1 = Pull-up and pull-down resistors are enabled

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### Port M Select Register

GF The select register (PMSEL) determines if a bit position in the data register (PMDATA) is assigned as ted I/O function. The settings for the PMSEL register bit positions are shown in

ble 10-55.	O or to a	
	a dedicat	0

**PMSEL** 

RESET

İ	
	Ţ
	N NO
	≤
	Se
	1 Select
	Register
	1SI
	9

•		70	FOIL IN Select Register	Ct Kegis	<u>נו</u>		OX(FF)	X(FF)FFFF44D
	BIT 7	6	Οī	4	3	2	_	ВІТ 0
			SEL5	SEL4	SEL3	SEL2	SEL1	SEL0
PE			W	ſW	W	ſW	W	W
2	0	0	_	_	<b>,</b> - ,	_	_	_

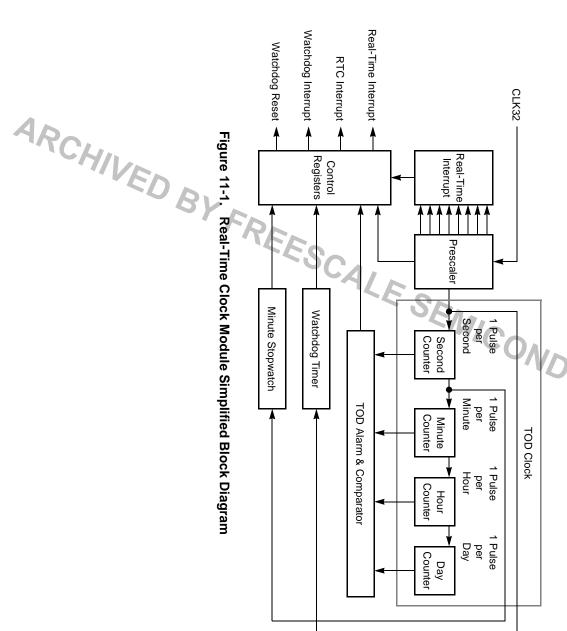
Table 10-55. Port M Select Register Description

	SELx Bits 5–0	Reserved Bits 7–6	Name
ARCHIVED BY FREESCALE SEMI	<b>Select</b> —These bits select whether the internal chip function or I/O port signals are connected to the pins.	Reserved	Description
	0 = The dedicated function pins are connected. 1 = The I/O port function pins are connected.	These bits are reserved and should be set to 0.	Setting

### Chapter 11 Real-Time Clock

<sup>INC.</sup> 2005

This chapter describes the real-time clock (RTC) module, which is composed of six blocks as shown in Figure 11-1: the prescaler, time-of-day (TOD) clock, TOD alarm, programmable real-time interrupt, a watchdog system reset. The following sections describe how each block operates and interacts with other module can generate three different level 4 interrupts to the interrupt controller. The RTC can also generate watchdog timer, and minute stopwatch, as well as control registers and bus interface hardware. The RTC modules in both the RTC and the MC68VZ328.



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#### **RTC Overview**

that generates real-time interrupts to the interrupt controller. In addition, the RTC contains a 2-second clock is composed of second, minute, hour, and day counters. If enabled, the TOD alarm generates an RTC in Figure 11-1 on page 11-2. The 1 Hz signal is used to increment the counters in the TOD clock. The TOD watchdog timer and a minute stopwatch. interrupt timer is designed to support application software by providing a fully programmable event times interrupt when programmed alarm settings coincide with the TOD counters. The programmable real-time The prescaler uses the CLK32 clock to create a 1 Hz clock used by all of the blocks in the RTC, as shown

controller: a watchdog interrupt, a real-time interrupt, and an RTC interrupt. Each interrupt produced by enable register. The mapping of the RTC internal interrupts to the interrupt controller is shown in the RTC, both internally and externally, can be individually enabled or disabled in the real-time interrupt The RTC can generate 15 event-related interrupts producing three level 4 interrupts to the interrupt

Internal Name	Interrupt Controller	Resolution
Real-time interrupt	Real-time interrupt	Eight different rates
Stopwatch	Real-time clock	Minutes
1HZ	Real-time clock	Seconds
MIN	Real-time clock	Minutes
HR	Real-time clock	Hours
DAY	Real-time clock	Days
ALM	Real-time clock	Seconds
Watchdog	Watchdog	Minutes

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Table 11-1. RTC Interrupt Mapping

assumed that the real-time clock enable (RTCEN) bit in the real-time control register is set (default). The watchdog timer and the entire RTC can also be enabled and disabled. In the following descriptions it is

#### 11.1.1 Prescaler

information on the power modes of the MC68VZ328. The actual frequency of the CLK32 is determined by power mode. See Section 4.3.1, "CLK32 Clock Signal," on page 4-4 for more information about the The prescaler divides the CLK32 reference clock down to 1 pulse per second, resulting in a signal labeled 38.4 kHz frequency crystal. the external crystal used as the crystal oscillator. The MC68VZ328 supports either a 32.768 kHz or a CLK32; see Section 4.5, "Introduction to the Power Control Module," on page 4-10 for detailed 1HZ. After an initial power up, the CLK32 signal is always available, even when the unit is in a reduced

#### NOTE

If a 38.4 kHz crystal is used as the crystal oscillator, the REFREQ bit in the make the RTC timing incorrect. real-time control register (RTCCTL) must be set. Failure to set this bit will



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available, as well as an interrupt at the midnight rollover of the hours counter. The prescaler stages are tapped to support real-time interrupt features. A periodic interrupt at 1 Hz is

### Time-of-Day Counter

6 bits) and the hours counter (5 bits) are maintained in the RTC timer register (RTCTIME). The day time-of-day counter, most designs use the counters in this fashion. The four counters (seconds, minutes, increments in day counts. be read at any time. The seconds, minutes, and hours data is maintained in 24-hour time format, which counter (9 bits) can count up to 512 days and is located in its own register (DAYR). The four counters can hours, and days) are toggled by the 1 Hz clock from the prescaler. The seconds and minutes counters (each Although the four counters that constitute the time-of-day counter are not restricted to operation as

#### NOTE:

example, if 26 is written to the hours counter, the counter will remain 26 range validity of data in the TOD clock. counter will return to zero. It is the responsibility of the user to ensure the until incremented by the minutes counters. When incremented, the hours MC68VZ328 does not check for range validity. If an out-of-range value is TOD clock can accept values that exceed their valid range. The entered, the counter will reset to zero the next time it is incremented. For To allow maximum flexibility in design, each of the four counters in the

reaching a count of 23, produces an interrupt (DAY) with the next increment from the minutes counter. The counter resets to 00 and increments the day counter. incremented. Both counters reset to 00 and increment the next counter. Likewise, the hours counter, after seconds and minutes counters each produce an MIN or HR interrupt (if enabled) the next time they are Each of the four counters may be enabled to produce an interrupt when it rolls over. Upon reaching 59, the

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#### Alarm

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minutes, and hours counters are in the RTC alarm register (RTCALRM). The day alarm register (DAYALRM) contains the 9-bit DAYSAL field. The alarm is composed of four registers that mirror those found in the time-of-day counter. The seconds,

service routine should change the values in the alarm registers or disable the ALM bit. minutes, and seconds for the time that the alarm is to generate an interrupt. The alarm is enabled when the If the alarm is not disabled, it will recur every 24 hours. If a single event alarm is desired, then the interrupt matches the time in the TOD alarm, the ALM bit in the real-time interrupt status register (RTCISR) is set. AL bit in the real-time interrupt enable register (RTCIENR) is set. When the time in the TOD counter An alarm is set by accessing the RTCALRM and DAYALRM register and loading the days, hours ARCHIVEL



application software is running, it is responsible for keeping the 2-second watchdog timer from timing out. intended sequence. At this time the watchdog timer generates either an interrupt or a reset signal to the If the watchdog timer times out, it is an indication that the software is no longer being executed in the The watchdog timer is an added check that a program is running and sequencing properly. When the

Programming the watchdog timer (WATCHDOG) register determines if the 2-second rollover produces a value of 10. The timer can be reset by writing any value into it. Otherwise, either a software reset or watchdog interrupt will be generated when the timer reaches a binary It is recommended that the watchdog timer be periodically cleared by software once it is enabled. The watchdog timer is clocked by the 1 Hz clock from the prescaler and therefore has 1-second resolution. watchdog interrupt or a system reset. At reset, the watchdog timer is enabled and generates a system reset.

## 11.1.5 Real-Time Interrupt Timer

debouncing, or communication polling. selected rates. Applications for the real-time interrupt can include digitizer sampling, keyboard There is a real-time interrupt available to the user. This interrupt will occur at one of eight different

interrupts are shown in Table 11-9 on page 11-12. Bits RTE0-RTE7 in the RTC interrupt enable register (RTCIENR) enable each of the eight different predefined rates. When the real-time interrupt occurs, it interrupt timer to operate. If the RTC and watchdog timer are disabled, the real-time interrupt stops. applies a level 4 interrupt to the MC68VZ328 interrupt controller. The real-time clock (RTCEN bit in the Each of the eight real-time interrupts operates at a fixed frequency. The frequencies of the real-time RTCCTL) or the watchdog timer (EN bit in the watchdog register) must be enabled for the real-time

#### 11.1.6 Minute Stopwatch

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stopwatch counts down and remains at decimal -1 until it is reprogrammed. The minute stopwatch can be register is enabled with -1 (decimal) in the STPWCH register, an interrupt will be posted on the next used to generate an interrupt after a certain number of minutes have elapsed. If the SW bit in the RTCIENR minute tick. When enabled, the minute stopwatch performs a countdown that has a 1-minute resolution. The minute

#### 11.1.6.1 **Minute Stopwatch Application Example**

unknown number of seconds from the time the stopwatch is set until the first minute (SW bit) in the RTCISR occurs after 5 minutes. In addition to the 5 minutes of the stopwatch, there is an value is decremented. An SW interrupt is generated when the counter counts to -1. The stopwatch interrupt interrupt (SW bit) in the RTCIENR is enabled. At consecutive minute increments, the minute stopwatch accomplish this, the minute stopwatch is programmed with a value of 5 minutes, and then the stopwatch The minute stopwatch can be used to turn off the LCD controller after 5 minutes of inactivity. To ARCHI



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**Programming Model** 

### 11.2 Programming Model

Section 11.2.1, "RTC Time Register," through Section 11.2.9, "Stopwatch Minutes Register," provide programming information on the real-time clock.

### 11.2.1 RTC Time Register

RTCTIME register are described in Table 11-2. values. This register cannot be reset since the real-time clock is always enabled at reset. The settings for the minutes, and seconds. It can be read or written at any time. After a write, the current time assumes the new The real-time clock hours, minutes, and seconds (RTCTIME) register is used to program the hours,

RTCTIME	Ш		RT(	동	urs,	Minu	ıtes,	and	Sec	RTC Hours, Minutes, and Seconds Register	Reg	ister	0	×(FF	FF)FFFB00	:B00
	31 31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	ВІТ 16
						HOURS	0,						MINU	MINUTES		
TYPE				W	W	W	W	W			W	W	۲W	W	W	۲W
D II O II O	0	0	0	×	×	×	×	×	0	0	×	×	×	×	×	×
- -								O <sub>X</sub>	×							
	15 15	14	3	12	1	10	9	œ	7	0	ΟΊ	4	ω	2	<u> </u>	0 BIT
							, n	· V					SECONDS	SDNC		
TYPE							M				W	W	W	W	W	rw
B E D E D E D E D E D E D E D E D E D E	0	0	0	0	0	0	0	0	0	0	×	×	×	×	×	×
- -						_	C	0x0	0x00XX							

RTC Hours, Minutes, and Seconds Register Description

Name	Description	Setting
Reserved Bits 31–29	Reserved	These bits are reserved and should be set to 0.
<b>HOURS</b> Bits 28–24	Hours—These bits indicate the current hour.	The bits can be set to any value between 0 and 23.
Reserved Bits 23–22	Reserved 1	These bits are reserved and should be set to 0.
MINUTES Bits 21–16	Minutes—These bits indicate the current minute.	The bits can be set to any value between 0 and 59.
Reserved Bits 15–6	Reserved	These bits are reserved and should be set to 0.
SECONDS Bit 5-0	Seconds—These bits indicate the current second.	The bits can be set to any value between 0 and 59.

## 11.2.2 RTC Day Count Register

current day assumes the new value. This register cannot be reset since it is used to keep the time. The to 00 and increments the day counter. This register can be read or written at any time. After a write, the value of DAYR is 512. When the hours counter in RTCTIME reaches 23, the next time increment resets it The real-time clock day count register (DAYR) contains the data from the day counter. The maximum

TYPE  TYPE  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	DAYR					RTO	RTC Day Counter Register	/ Cou	unter	Rec	jister	C			0x(ff)	Ť	f)FFFB1A
DAYS    O 0 0 0 0 0 0 7 7 7 7 7 7 7 7 7 7 7 7 7		BIT 15	14	13	12	1	10	9	œ	7	6	O	4	ω	2	_	0 BIT
0 0 0 0 0 0 0 ? ? ? ? ? ? ? ? ?											2,		DAYS				
PESET 0 0 0 0 0 0 0 ? ? ? ? ? ? ? ? ? ?	TYPE								W	W	W	W	W	W	W	W	rw
	D D D D D D T D T	0	0	0	0	0	0	0	٠,>	?	.2	٠,	.>	٠,	.>	٠,	٠,
0x0XXX	7								0x0	\( \times \)							

Table 11-3. **RTC Day Counter Register Description** 

	DAYS Bits 8–0	Reserved Bits 15–9	Name
ARCHIVED BY FREESCALES	<b>Days</b> —This field indicates the current setting of the day.	Reserved	Description
	The bits can be set to any value between 0 and 511.	These bits are reserved and should be set to 0.	Setting

**Programming Model** 

## 11.2.3 RTC Alarm Register

seconds can be read or written at any time. After a write, the current time assumes the new values. The settings for the RTCTIME register are described in Table 11-4. The real-time clock alarm (RTCALRM) register is used to configure the alarm. The hours, minutes, and

RTCALRM	R M				_	RTC Alarm Register	Alarr	n Re	giste	Ä	21			0x(ff	)FFF	FFFB04
	8IT 31	30	29	28	27	26	25	24	23	22	2	20	19	18	17	ВІТ 16
						HOURS	0,			<b>/</b>			MINC	MINUTES		
TYPE				W	W	W	W	W			W	W	W	W	W	rw
7 7 7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7								0x00C	00000	O,						
	15	14	13	12	1	10	9	00	7	6	Ŋ	4	ω	2	_	0
									1	Ì			SECONDS	SDNC		
TYPE									1		W	W	W	W	W	rw
RESET	0	0	0	0	0	0	0	0x00c	00000	0	0	0	0	0	0	0

able 11-4. RTC Alarm Register Description

Name	Description	Setting
Reserved Bits 31–29	Reserved	These bits are reserved and should be set to 0.
<b>HOURS</b> Bits 28–24	<b>Hours</b> —These bits indicate the value of the hours field in the current alarm setting.	This field can be set to any value between 0 and 23. Default is value 0.
Reserved Bits 23–22	Reserved	These bits are reserved and should be set to 0.
MINUTES Bits 21–16	Minutes—These bits indicate the value of the minutes field in the current alarm setting.	This field can be set to any value between 0 and 59. Default is value 0.
Reserved Bits 15–6	Reserved	These bits are reserved and should be set to 0.
SECONDS Bit 5-0	<b>Seconds</b> —These bits indicate the value of the seconds field in the current alarm setting.	This field can be set to any value between 0 and 59. Default is value 0.

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# 11.2.4 RTC Day Alarm Register

generates the alarm. It can be read or written at any time. After a write, the current time assumes the new values. The settings for the DAYALRM register are described in Table 11-5. The real-time clock day alarm (DAYALRM) register contains the numerical value of the day that

7	BESET	TYPE			DAY,
-	0			BIT 15	DAYALRM
	0			14	
	0			13	
	0			13 12 11 10	
	0			11	RT
	0			10	C Da
	0			9	RTC Day Alarm Register
0x0C	0 0	₹		8	arm F
0x0000	0	8		7	₹egi
O <sub>i</sub>	0	₹	<b>/</b>	6	ster
	0	₹	_	5	21
	0	₹	DAYSAL	4	
	0	W	'	ω	_
	0	₹		2	0x(ff)
	0	₹		4	)FFF
	0	8		BIT 0	FFFB1C

Table 11-5. **RTC Day Alarm Register Description** 

16	DAYSAL Bits 8–0	Reserved Bits 15–9	Name	
ARCHIVED BY FREESCALE SEN	<b>Days Alarm</b> —This field indicates the numerical setting of the day that will enable the alarm.	Reserved	Description	
	The bits can be set to any value between 0 and 511.	These bits are reserved and should be set to 0.	Setting	

**Programming Model** 

# Watchdog Timer Register

bits to enable the watchdog timer and to determine if the result of a time out is an interrupt or a system reset. The settings for the WATCHDOG register are described in Table 11-6. The watchdog timer (WATCHDOG) register provides all of the control of the watchdog timer. It provides

TYPE  RESET  O  O  O	
0   14	) : ;
	)
0 13	
0 12	
0 1 1	:
Watchd	•
OG III	ł
oxc oxc	
Vatchdog I imer Register  10 9 8 7 6  CNTR INTF   0 0 0 0 0 0 0x0001	J
Og	
0 5	
4 0	
ο ω	
2	
TW TW	
1 RES	

Watchdog Timer Register Description

Name	Description	Setting
Reserved Bits 15–10	Reserved	These bits are reserved and should be set to 0.
CNTR Bits 9–8	Counter—These bits represent the value of the watchdog counter, which counts up in 1-second increments. When the watchdog counter counts to 10, it generates a watchdog interrupt.  Note: Because the watchdog counter is incremented by a 1 Hz signal from the real-time clock, the average tolerance of the counter is 0.5 seconds. Greater accuracy is obtained by polling the 1 Hz flag of the RTCISR.	Writing any value to these bits will reset the counter to 00 (default).
INTF Bit 7	Interrupt Flag—When this bit is set, a watchdog interrupt has occurred. This bit can be cleared by writing a 1 to it.	0 = No watchdog interrupt occurred. 1 = A watchdog interrupt occurred.
Reserved Bits 6–2	Reserved	These bits are reserved and should be set to 0.
ISEL Bit 1	Interrupt Selection—This bit selects the watchdog reset. It is cleared at reset.	0 = Selects the watchdog reset (default). 1 = Select the watchdog interrupt.
<b>EN</b> Bit 0	Watchdog Timer Enable—This bit enables the watchdog timer. It is set at reset.	<ul><li>0 = Disable the watchdog timer.</li><li>1 = Enable the watchdog timer (default).</li></ul>
16	ARCHIVE	

## 11.2.6 RTC Control Register

frequency information to the prescaler. The settings for the RTCCTL register are described in Table 11-7. The real-time clock control (RTCCTL) register is used to enable the real-time clock and provide reference

| RTCCTL   RTCCOntrol Register   RTCCTL   RTCCOntrol Register   RTCEN   RTCEN   REET   RTCEN   RTCEN   REET   RTCEN          |
|---|--------|
| 9 8 7 6  9 8 7 6  RTCEN  0 0 1 0  0x0080  |        |
| 9 8 7 6  9 8 7 6  RTCEN  0 0 1 0  0x0080  |        |
| 9 8 7 6  9 8 7 6  RTCEN  0 0 1 0  0x0080  |        |
| 9 8 7 6  9 8 7 6  RTCEN  0 0 1 0  0x0080  |        |
| 9 8 7 6  9 8 7 6  RTCEN  0 0 1 0  0x0080  |        |
| 9 8 7 6  9 8 7 6  RTCEN  0 0 1 0  0x0080  |        |
| RTCEN 0 0x0080  |        |
| 7. 7.   |        |
| 7. 7.   | 0x0080 |
| 温   | DA     |
| REFREQ<br>W   | 11,    |
| 4 0   |        |
| °   ° g   |        |
|   |        |
| 1 BIT 0   |        |
| BIT   |        |

Table 11-7. RTC Control Register Description

Name	Description	Setting
Reserved Bits 15–8	Reserved	These bits are reserved and should be set to 0.
RTCEN Bit 7	Real-Time Clock Enable—This bit, when set, enables the real-time clock.	0 = Disable the real-time clock 1 = Enable the real-time clock (default)
Reserved Bit 6	Reserved	This bit is reserved and should be set to 0.
REFREQ Bit 5	Reference Frequency—This bit is set to the frequency of the crystal oscillator.	0 = Reference frequency is 32.768 kHz (default). 1 = Reference frequency is 38.4 kHz.
Reserved Bits 4–0	Reserved	These bits are reserved and should be set to 0.

# 1.2.7 RTC Interrupt Status Register

interrupts. Each bit is set when the corresponding event occurs. You must clear these bits by writing ones information about the frequency of the RTC interrupts, refer to Table 11-9 on page 11-12 mode. The settings for the RTCISR register are described in Table 11-8 on page 11-11. For more which also clears the interrupt. This register can post interrupts while the system clock is idle or in sleep The real-time clock interrupt status register (RTCISR) indicates the status of the various real-time clock



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еŗ	

0x(ff)FFFB0E

; (	RESET	TYPE		
	0	V	RIS7	BIT 15
	0	W	RIS6	14
	0	W	RIS5	13
	0	W	RIS4 RIS3	12
	0	W	RIS3	11
	0	W	RIS2	10
0x(	0	V	RIS1 RIS0	9
0x0000	0	₹	RIS0	8
	0			7
	0			6
	0	¥	HR	5
	0	W	1HZ	4
	0	₹	DAY	з
	0	W	/ ALM N	2
	0	W	MIN	1
	0	W	WS	BIT 0

**RTC Interrupt Status Register Description** 

ALM Alarm Flag—If Bit 2 flag is set on a real-time clock.  Note: The ala For a single ala	DAY  Bit 3  24-hour clock in day counter in t is posted.	1HZ 1 Hz Flag—If e Bit 4 increment of the clock.	HR Hour Flag—Th Bit 5 of the hour cour	Reserved Reserved Bits 7–6	RISO Real-Time Inte	RIS1 Real-Time Inte	RIS2 Real-Time Inte	RIS3 Real-Time Inte Bit 11 shows the statu	RIS4 Real-Time Inte Bit 12 shows the statu	RIS5 Real-Time Inte Bit 13 shows the statu	RIS6 Real-Time Inte Bit 14 shows the statu	RIS7 Real-Time Inte	Name
Alarm Flag—If this bit is enabled, an alarm flag is set on a compare match between the real-time clock and the alarm register's value.  Note: The alarm will recur every 24 hours. For a single alarm, clear the interrupt enable in	Day Flag—If enabled, this bit is set for every 24-hour clock increment (at midnight) of the day counter in the TOD clock, and an interrupt is posted.	1 Hz Flag—If enabled, this bit is set on every increment of the second counter in the TOD clock.	<b>Hour Flag</b> —This bit is set on every increment of the hour counter in the TOD clock.	EES	Real-Time Interrupt Status Bit 0—This bit shows the status of real-time interrupt 0.	Real-Time Interrupt Status Bit 1—This bit shows the status of real-time interrupt 1.	Real-Time Interrupt Status Bit 2—This bit shows the status of real-time interrupt 2.	Real-Time Interrupt Status Bit 3—This bit shows the status of real-time interrupt 3.	Real-Time Interrupt Status Bit 4—This bit shows the status of real-time interrupt 4.	Real-Time Interrupt Status Bit 5—This bit shows the status of real-time interrupt 5.	Real-Time Interrupt Status Bit 6—This bit shows the status of real-time interrupt 6.	Real-Time Interrupt Status Bit 7—This bit shows the status of real-time interrupt 7.	Description
<ul><li>0 = No alarm interrupt occurred.</li><li>1 = An alarm interrupt occurred.</li></ul>	0 = No 24-hour rollover interrupt occurred. 1 = A 24-hour rollover interrupt occurred.	0 = No 1 Hz interrupt occurred. 1 = A 1 Hz interrupt occurred.	0 = No 1-hour interrupt occurred. 1 = A 1-hour interrupt occurred.	These bits are reserved and should be set to 0.	0 = No RIS0 interrupt occurred. 1 = RIS0 interrupt occurred.	0 = No RIS1 interrupt occurred. 1 = RIS1 interrupt occurred.	0 = No RIS2 interrupt occurred. 1 = RIS2 interrupt occurred.	0 = No RIS3 interrupt occurred. 1 = RIS3 interrupt occurred.	0 = No RIS4 interrupt occurred. 1 = RIS4 interrupt occurred.	0 = No RIS5 interrupt occurred. 1 = RIS5 interrupt occurred.	0 = No RIS6 interrupt occurred. 1 = RIS6 interrupt occurred.	0 = No RIS7 interrupt occurred. 1 = RIS7 interrupt occurred.	Setting

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Table 11-8. RTC Interrupt Status Register Description (Continued)

Table 11-9. Real-Time Interrupt Frequency Settings

Real-Time Interrupt Frequency	32.7/ Referer	32.768 kHz Reference Clock	38.4 kHz Reference Clock	· kHz ce Clock
RFE7	512 Hz	1.9531 ms	600 Hz	1.6666 ms
RFE6	256 Hz	3.9062 ms	300 Hz	3.3333 ms
RFE5	128 Hz	7.8125 ms	150 Hz	6.6666 ms
RFE4	64 Hz	15.625 ms	75 Hz	13.3333 ms
RFE3	32 Hz	31.25 ms	37.5 Hz	26.6666 ms
RFE2	16 Hz	62.5 ms	18.75 Hz	53.3333 ms
RFE1	8 Hz	125 ms	9.375 Hz	106.6666 ms
RFE0	4 Hz	250 ms	4.6875 Hz	213.3333 ms
		1/		

# 11.2.8 RTC Interrupt Enable Register

corresponding bit is set. The settings for the RTCIENR register are described in Table 11-10 on page 11-13. For information about the frequency of the real-time interrupts, refer to Table 11-9 The RTC interrupt enable register (RTCIENR) is used to enable the interrupts in the RTCSIR if the ARCHIVED BY FI



Interrint Enable Degister	
Dogistor	
0	
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	:								Ċ					(1.1/1.)	'	
	BIT 15	14	13	12	<u> </u>	10	9	œ	7	6	Οī	4	ω	2	_	
,	RIE7	RIE6	RIE5	RIE4	RIE3	RIE4 RIE3 RIE2 RIE1	RIE1	RIE0			HR	1HZ	DAY	NIM WIN AWD ZHI	NIN	ws r
TYPE	ſW	۲W	W	rw	rw	rw	۲W	W			W	W	W	W	W	
о п о п	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
7 10 11							0	0x0000			4					

able 11-10. RTC Interrupt Enable Register Description

Name	Description	Setting
<b>RIE7</b> Bit 15	Real-Time Interrupt Enable Bit 7—This bit enables the real-time interrupt 7. The frequency of this interrupt is shown in Table 11-9 on page 11-12.	0 = RIE7 interrupt is disabled. 1 = RFE7 interrupt is enabled.
RIE6 Bit 14	Real-Time Interrupt Enable Bit 6—This bit enables the real-time interrupt 6. The frequency of this interrupt is shown in Table 11-9 on page 11-12.	0 = RIE6 interrupt is disabled. 1 = RIE6 interrupt is enabled.
RIE5 Bit 13	Real-Time Interrupt Enable Bit 5—This bit enables the real-time interrupt 5. The frequency of this interrupt is shown in Table 11-9 on page 11-12.	0 = RIE5 interrupt is disabled. 1 = RIE5 interrupt is enabled.
<b>RIE4</b> Bit 12	Real-Time Interrupt Enable Bit 4—This bit enables the real-time interrupt 4. The frequency of this interrupt is shown in Table 11-9 on page 11-12.	0 = RIE4 interrupt is disabled. 1 = RIE4 interrupt is enabled.
RIE3 Bit 11	Real-Time Interrupt Enable Bit 3—This bit enables the real-time interrupt 3. The frequency of this interrupt is shown in Table 11-9 on page 11-12.	0 = RIE3 interrupt is disabled. 1 = RIE3 interrupt is enabled.
RIE2 Bit 10	Real-Time Interrupt Enable Bit 2—This bit enables the real-time interrupt 2. The frequency of this interrupt is shown in Table 11-9 on page 11-12.	0 = RIE2 interrupt is disabled. 1 = RIE2 interrupt is enabled.
RIE1 Bit 9	Real-Time Interrupt Enable Bit 1—This bit enables the real-time interrupt 1. The frequency of this interrupt is shown in Table 11-9 on page 11-12.	0 = RIE1 interrupt is disabled. 1 = RIE1 interrupt is enabled.
RIEO Bit 8	Real-Time Interrupt Enable Bit 0—This bit enables the real-time interrupt 0. The frequency of this interrupt is shown in Table 11-9 on page 11-12.	0 = RIE0 interrupt is disabled. 1 = RIE0 interrupt is enabled.
Reserved Bits 7–6	Reserved 10	These bits are reserved and should be set to 0.
HR Bit 5	<b>Hour Flag</b> —This bit enables interrupts occurring at a one-per-hour rate.	0 = 1-hour interrupt disabled. 1 = 1-hour interrupt enabled.
<b>1HZ</b> Bit 4	1 Hz Flag—This bit enables interrupts occurring at a 1 Hz rate.	0 = 1 Hz interrupt disabled. 1 = 1 Hz interrupt enabled.
DAY Bit 3	Day Interrupt Enable—This bit enables the day interrupt occurring at a midnight rollover (0000 hours) of the day counter.	<ul><li>0 = 24-hour rollover interrupt is disabled.</li><li>1 = 24-hour rollover interrupt is enabled.</li></ul>

#### Programming Mode

## Freescale Semiconductor, Inc

Table 11-10. RTC Interrupt Enable Register Description (Continued)

Name	Description	Setting
ALM Bit 2	<b>Alarm Interrupt Enable</b> —This bit enables the alarm interrupt.	0 = Alarm interrupt is disabled. 1 = Alarm interrupt is enabled.
MIN Bit 1	Minute Interrupt Enable—This bit enables the MIN interrupt at the rate of one interrupt per minute.	0 = 1-minute interrupt is disabled. 1 = 1-minute interrupt is enabled.
SW Bit 0	Stopwatch Interrupt Enable—This bit enables the stopwatch interrupt.  Note: The stopwatch counts down and remains at decimal -1 until it is reprogrammed. If this bit is enabled with -1 (decimal) in the STPWCH register, an interrupt will be posted on the next minute tick.	<ul><li>0 = 1-minute interrupt is disabled.</li><li>1 = 1-minute interrupt is enabled.</li></ul>

# 11.2.9 Stopwatch Minutes Register

stopwatch counter is decremented by the minute (MIN) output from the TOD clock. The average tolerance of the count is 0.5 minutes. The settings for the STPWCH register are described in Table 11-11. The stopwatch minutes (STPWCH) register contains the current stopwatch countdown value. The

#### NOTE:

RTCISR register or by polling the minute interrupt service routine For improved accuracy, enable the stopwatch by polling the MIN bit of the

STPWCH	SH				Stop	Stopwatch Mi	ch M	nute	s Re	linutes Register	_		0	X(FF	)FFF	0x(FF)FFFB12
	ВІТ 15	14	13	13 12	11	10	9	8	7	6	5	4	3	2	1	BIT 0
						4							CNT	1L		
TYPE						C					W	W	WI WI WI WI WI	W	W	ſW
D II O II O	0	0	0	0	0	0	0	0	0	0	_	_	_	_	_	_
7 6 7					Se			0x0	0x003F							

Table 11-11. Stopwatch Minutes Register Description

Reserved Bits 15–6  CNT Stopwatch Count—This field contains Bits 5–0  Stopwatch Count—This field contains the stopwatch countdown value.  The highest possible value is 62 minutes. The countdown will not be activated again until a non-zero value, which is less than 63 minutes, is written to this register.	Name	Description	Setting
Stopwatch Count—This field contains the stopwatch countdown value.	Reserved Bits 15–6	Reserved 20	These bits are reserved and should be set to 0.
	CNT Bits 5–0	Stopwatch Count—This field contains the stopwatch countdown value.	The highest possible value is 62 minutes. The countdown will not be activated again until a nonzero value, which is less than 63 minutes, is written to this register.



#### **General-Purpose** Chapter **Timers**

<sup>INC.</sup> 2005

operate as a single 32-bit timer. programmable clock frequency derived from SYSCLK. The two timers may also be cascaded together to interrupt when the timer reaches a programmed value. Each timer has an 8-bit prescaler providing a a capture event on either the leading or trailing edges of an input pulse. The timer can also generate an registers. Each timer counter value can be captured using an external event and can be configured to trigger This chapter describes in detail the operation of the general-purpose timer modules of the MC68VZ328 The GP timers consist of two general-purpose 16-bit timers, a prescaler, and compare and capture

## 12.1 GP Timer Overview

operation of the GP timers in detail Figure 12-1 illustrates the general-purpose timer block diagram. The following sections describe the The two 16-bit timers (Timer 1 and Timer 2) that make up the general-purpose timers are identical.

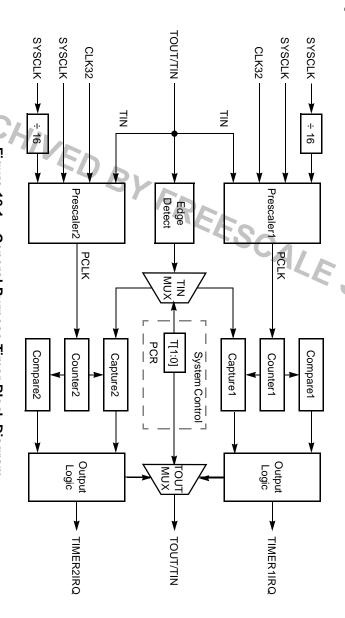


Figure 12-1. General-Purpose Timer Block Diagram

# .1.1 Clock Source and Prescaler

output of each prescaler drives its respective counter. fed to a prescaler that acts as a divider with a programmable division ratio ranging from 1 to 256. The The clock source for each timer is individually selectable through software. The selected clock source

oscillator or 436 seconds using a 38.4 kHz oscillator. programmable prescaler allows a maximum period of 512 seconds when using a 32.768 kHz crystal (PCLK) that drives the counter. The prescaler divides the input clock by a value between 1 and 256. The PRESCALER field of the timer prescaler register (TPRERx) selects the divide ratio of the input clock The clock input source is selected by the CLKSOURCE field of the timer control registers (TCTLx). The The clock sources are SYSCLK, SYSCLK/16, CLK32, and an external clock from the timer I/O pin (TIO).

Section 4.5.2, "CGM Operation During Sleep Mode," on page 4-12 for more information on CLK32 Of the four clock sources, only CLK32 continues to operate while the MC68VZ328 is in sleep mode. See operation during sleep mode.

#### NOTE:

register before changing either the clock source or prescaler setting Ensure that the timer is disabled by clearing the TEN bit in the TCTLx

# Timer Events and Modes of Operation

occur when the value in the counter matches the contents of the compare register. Capture events occur when a defined transition of the TOUT/TIN pin is detected. There are two types of events that produce interrupts: compare events and capture events. Compare events

occurs. It does not affect counter operation following capture events. A description of each mode follows free-running/restart bit in the TCTLx register only controls how the counter operates after a compare event The counter can be programmed to run in one of two modes: restart or free-running. The

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### **12.1.2.1** Restart Mode

In restart mode, the following actions occur when the compare value in the timer compare register (TCMPx) matches the value in the timer counter register (TCNx):

- 1. The counter resets to 0x0000.
- 2 The compare event (COMP) bit of the timer status register (TSTATx) is set.
- $\omega$ The TIMERx interrupt is issued to the interrupt controller if the IRQEN bit of the TCTLx register is set.
- 4. The timer counter resumes counting

signals, audio tones. This mode is useful when you need to generate periodic events or, when it is used with the timer output

### 12.1.2.2 Free-Running Mode

counter continues counting without resetting to 0x0000. When 0xFFFF is reached, the counter rolls over to 0x0000 and continues counting. Free-running mode is similar in operation to restart mode, except that when a compare event occurs, the





#### **GP Timer Overview**

## **Timer Capture Register**

transitions of the TIN that can trigger a capture event: transition of the signal applied to the TIN pin is detected by the capture edge detector. There are three Each timer has a 16-bit capture register that takes a "snapshot" of the timer counter when a defined

- Capture on rising edge
- Capture on falling edge
- Capture on rising or falling edge

that produce the capture edge can be as short as 20 ns. The minimum time between pulses is two PCLK The type of transition that triggers the capture is selected by the CAP field of the TCTLx register. Pulses

sent to the MC68VZ328 interrupt controller if the capture function is enabled and the IRQEN bit of the TCTLx register is set. The timer is disabled at reset. When a capture event occurs, the CAPT status bit is set in the TSTATx register. A TIMERx interrupt is

### **TOUT/TIN/PB6 Pin**

direction of the pin is also controlled in the Port B registers. "Port B Dedicated I/O Functions," on page 10-10. Because the TOUT/TIN/PB6 is a bidirectional pin, the pin is assigned to the GP timers or to pin 6 of Port B (the default setting), as described in Section 10.4.2.3 The TOUT/TIN pins are multiplexed with bit 6 of the Port B registers. The Port B registers determine if the

#### NOTE:

controlled by the DIR6 bit in the Port B direction register even though the pin is assigned to the GP timers. Unlike other port register pins, the TOUT/TIN/PB6 pin direction is still

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(PCR) switches the TIN input between capture register 1 and capture register 2. When T = 0x00 the TIN is trigger to the edge-detect circuit for the capture registers. The T[1:0] field in the peripheral control register connected to Timer 1, and when T = 0x01 the TIN is connected to Timer 2 When the in direction is selected, the pin (TIN) is available as a clock input to the timer or as the input

compare event occurs When the out direction is enabled, the pin (TOUT) is used to toggle or output a pulse when a timer ARCHIVED BY FRI



### 12.1.5 Cascaded Timers

the T[1:0] field of the PCR. See Section 5.2.2, "Peripheral Control Register," on page 5-4 for more details. Both timers can be cascaded together to create a 32-bit counter. The cascade configuration is controlled by

pin is in (DIR6 = 0), the TIN signal is applied to Timer 2. If the direction is out (DIR6 = 1), the TOUT is connected to Timer 1. Timer 2 are cascaded together. Timer 1 becomes the MSW, and Timer 2 is the LSW. If the direction of the Table 12-1 shows the two possible configurations of cascaded timers. When T[1:0] = 0x10, Timer 1 and

(DIR6 = 0), the TIN signal is applied to Timer 1. If the direction is out (DIR6 = 1), the TOUT is connected When T[1:0] = 0x11, Timer 2 becomes the MSW and Timer 1 is the LSW. If the direction of the pin is in

Table 12-1. Cascade Timer Settings

Timer 2	Timer 1	Timer 1	Timer 2	<u> </u>
Timer 1	Timer 2	Timer 2	Timer 1	10
TOUT From	TINTO	LSW	MSW	T[1:0] PCR

# Compare and Capture Using Cascaded Timers

also be accomplished using the CAPT status bit instead of the COMP status bit. When the timers are cascaded, the associated compare and capture registers are not. The flow diagram in 12-2 on page 12-5 suggests one method for 32-bit compares using a cascaded timer. Captures can

When the MSW status bit sets, check the status bit of the LSW. If it is not set, loop until it does set After the compare to Timers 1 and 2 is written, the COMP or CAPT status bit of the MSW is checked ARCHIVED BY FREESCALE



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ARCHIVED BY FREESCALE compare 32-bit 22-bit mpare

2. Compare Routine for 32-Bit Cascaded Timers Yes MSW status bit set? LSW status bit set? Set flag /VC-82005

## Programming Model

describing the register settings apply to both registers GP timers module. Because the two timers are identical, the register description and the associated table The following sections provide programming information about the settings of the two 16-bit timers in the

### **Timer Control Registers** and 2

Each timer control (TCTLx) register controls the overall operation of its corresponding GP timer. The settings for the registers are described in Table 12-2. The TCTL registers control the following:

- Selecting the free-running or restart mode after a compare event
- Selecting the capture trigger event
- Controlling the output compare mode
- Enabling the compare event interrupt
- Selecting the prescaler clock source
- Enabling and disabling the GP Timer

	RESET	TYPE			TCTL2		RESET	TYPE			TCTL1	•	S	•	• 0	•	
	0			ВІТ 15			0			ВІТ 15		Enabling and disabling the GP Timer	Selecting the prescaler clock source	Enabling the compare event interrupt	Controlling the output compare mode	Selecting the capture trigger event	
	0			14			0			14		g and o	g the p	g the c	ing the	g the c	C
	0			13			0			13		lisabli	rescal	ompar	e outpu	apture	
F	0			12			0			12		ng the	er cloc	e even	ıt com	trigge	C
	0	7	111	11	Time		0			11	Time	GP Ti	k sour	t interi	pare m	r even	
	0		Ì	10	Timer Control Register 2	LE	0			10	Timer Control Register 1	mer	ce	upt	ode	t	
	0			9	ntrol		0		1	9	ontrol						
0x0000	0	W	FRR	8	Reg	0x0000	0	W	FRR	8	Reg	V/	)/	,			
ō	0	W	CAP	7	jister	ō	0	W	CAP	7	jister		)(	C	77		1
	0	W		6	8		0	W		6	<u> </u>						1
	0	W	МО	5			0	W	МО	5							
	0	W	IRQEN	4			0	۲W	IRQEN	4							
	0	W	CLK	з	0×		0	W	CLK	з	0×						
	0	W	CLKSOURCE	2	(FF)		0	W	CLKSOURCE	2	(FF)						
	0	W	CE	_	Ť		0	W	CE	_	ĘĘ						
	0	W	TEN	BIT 0	0x(FF)FFF610		0	W	TEN	BIT 0	0x(FF)FFF600						

Table 12-2.

Timer Control Register Description

Reserved Free-Running/Restart—This bit controls the Description These bits are reserved and should be set to 0. Restart mode (default) Setting

FRR Bit 8

event occurs. In free-running mode, the counter mode of operation after a compare

Free-running mode

counter continues after the compare. In restart

Reserved Bits 15-9

Name

	TEN Bit 0	CLKSOURCE Bit 3–1	IRQEN Bit 4	OM Bit 5	CAP Bits 7–6	Name
ARCHIVED BY FREESCALES	<b>Timer Enable</b> —This bit enables or disables the associated timer.	Clock Source—This field controls the clock source to the prescaler. The stop count freezes the counter at its current value.  Note: To use TIN/TOUT as a TIN input, ensure that the SEL6 bit in the Port B select register (PBSEL) is cleared. Also ensure that DIR6 = 0.	Interrupt Request Enable—This bit enables an interrupt on a compare event.	Output Mode—This bit selects the output mode of the timer after a compare event occurs. The output appears for one SYSCLK period.	Capture Edge—This field selects the type of transition on the TIN input that triggers a capture event.  Note: To use TIN/TOUT as a TIN input, ensure that the SEL6 bit in the Port B select register (PBSEL) is cleared.	Description
	0 = Timer is disabled (default). 1 = Timer is enabled.	000 = Stop counter (default). 001 = SYSCLK to prescaler. 010 = SYSCLK/16 to prescaler. 011 = TIN to prescaler. 1xx = CLK32 to prescaler.	00 = Disable the compare interrupt (default). 01 = Enable the compare interrupt.	0 = Active-low pulse (default). 1 = Toggle output.	00 = Disable capture function (default). 01 = Capture on rising edge. 10 = Capture on falling edge. 11 = Capture on rising or falling edges.	Setting



# Timer Prescaler Registers 1 and 2

for the registers are described in Table 12-3. Each timer prescaler register (TPRERx) controls the divide ratio of the associated prescaler. The settings

	RESET	TYPE			TPRER
	0	W		BIT 15 14 13 12	_
	0	W		14	
	0	V		13	
	0	W	Not Used	12	-
	0	W	sed	11	Timer Prescaler Register
	0	V		10	Pres
	0	V		9	cale
0x0000	0	₹		8	Rec
<b>D</b>	0	V		7	jiste
۲,	0	N.		6	
	0	rw rw	) (	5	201
	0	V	Pre	4	
	0	¥	Prescaler	3	0
	0	rw rw rw		2	×(F
	0	₹		_	F)F
	0	W		BIT 0	0x(FF)FFF602

TPRER	2			_	Timer Prescaler	Pres	cale	r Register 2	iste	2			0	×(F	F)FI	FF612
	BIT 15	14	13 1	12	11	10	9	8	7	6	5	4	3	2	1	ВІТ 0
				Not Used	sed			1				Pres	Prescaler			
TYPE	۲W	W	W	W	/ rw	rw rw pw	W	W	ਔ	rw rw rw	W	W	W	rw rw rw	W	rw
D F F F F	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
700								0x0000								

**Timer Prescaler Register Description** 

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# Timer Compare Registers 1 and 2

event is generated when the counter matches the value in this register. This register is set to 0xFFFF at system reset. The settings for the registers are described in Table 12-4. Each timer compare (TCMPx) register contains the value that is compared with the counter. A compare

COMPARE	Name		, () ()	D II II II II	TYPE			TCMP2		RESET		TYPE			TCMP1		
	,			_	W		BIT 15			-	_	W		BIT 15			
Compare Value—Write this field's value to				_	8		14			-	_	W		14			
e Value		Table		_	₹		13			-	_	W		13			
Write	Descr	Table 12-4. Timer Compare Register Description		_	V		12	Tin		-	_	W		12	Tin		
this fi	Description	Time		_	¥			11	ner C		•	_	W		1	ner C	
eld's v		er Cor		_	V		10	Timer Compare Register 2		•	_	W		10	Timer Compare Register 1		
alle to		npare	Cę		₹	COI	9	are	9	Ə	_	W	CO	9	are		
		Regi	0xFFFF	4	W	COMPARE	8	Regi		0xFFFF	_	W	COMPARE	8	Regi		
This field has a valid range 0x0000 to 0xEEEE		ster [		_	₹		7	ster	O	4	_	W		7	ster		
eld ha		)escr		_	₩		6	Ν		3	<u> </u>	W	V	6	7		
s a va		iptior		_	₹		5				_	W		Ol	<		
	Setting			_	₹		4			•	_	W		4			
co en	ing			_	₹		ω	9			_	W		ω	9		
0000				_	₹		2	(F)		•	_	W		2	(F		
† 0 0 0				_	₹		_	Ţ		•	_	W		_	ijĘ,		
FFFF				_	V		BIT 0	0x(FF)FFF614		-	_	W		BIT 0	0x(FF)FFF604		

	COMPARE Bits 15-0	Name
ARCHIVED BY FREESCA	Compare Value—Write this field's value to generate a compare event when the counter matches this value.	Description
	This field has a valid range 0x0000 to 0xFFFF.	Setting

# 1 and 2

Each timer capture register (TCRx) stores the counter value when a capture event occurs. The settings for

								0x0000								7 0 0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D F F F F F F F F F F F F F F F F F F F
W	₹	₹	V	₹	₹	₹	V	PW	V	8	W	V	₹	8	W	TYPE
							Ш	CAPTURE								
BIT 0	1	2	3	4	5	6	3	8	9	10	11	12	13	14	BIT 15	
(FF)FFF616	F)FF	)×(F	C			2	ster	Fimer Capture Register 2	ture	Cap	imer	_				TCR2
						۲,	5	0x0000								
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RESET
W	₹	W	₹	₹	V	W.	8	W	W	₹	₹	₹	V	₹	W	TYPE
					) (			CAPTURE								
BIT 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	BIT 15	
(FF)FFF606	F)FF	)×(F	6		201	_	ster	Timer Capture Register	ture	Cap	imer	_				TCR1

Гable 12-5.
Timer
Capture
Register
Description

	CAPTURE Bits 15-0	Name	
ARCHIVED BY FREESCAL	Capture Value—This field stores the counter value that existed at the time of the capture event.	Description	
	This field has a valid range 0x0000 to 0xFFFF.	Setting	

### Freescale Semiconductor, Inc. **Programming Model**

# 12.2.5 Timer Counter Registers 1 and 2

time without affecting the current count. The settings for the registers are described in Table 12-6 Each read-only timer counter (TCNx) register contains the current count. The TCNx can be read at any

Table 12-6. Timer Counter Register Description	RESET 0 0 0 0 0 0 0 0 0	TYPE ' ' ' ' ' ' '	COUNT	BIT 15 14 13 12 11 10 9 8	TCN2 Timer Counter Register 2		0x0000	RESET 0 0 0 0 0 0 0 0	TYPE ' ' ' ' ' ' ' '	COUNT	BIT 15 14 13 12 11 10 9 8	TCN1 Timer Counter Register
12-6.	0	¬		12	<u></u> ≓			0	¬		12	≓
Time	0	¬		11	ner (			0	¬		<u> </u>	ner (
er Cou	0	¬		10	Sount			0	¬		10	ount
nter	0	¬	0	9	er F		0	0	¬	0	9	er F
Regis	0	7	TNUO	8	₹egis		x0000	0	¬	TNUO	<b>∞</b>	₹egis
ster I	0	-		7	ter	) (		0	¬		7	ter
Desc	0	¬		6	2		9	0	V		6	_
ription	0	-		5				0	7	) (	σı	30
_	0	¬		4				0	¬		4	
	0	¬		з	0			0	¬		ω	0
	0	¬		2	× E			0	¬		2	Ě
	0	¬		_	Ŧ)FF			0	¬		_	Ŧ,
	0	¬		BIT 0	)x(FF)FFF618			0	¬		BIT 0	(FF)FFF608

	COUNT Bits 15-0	Name
ARCHIVED BY FREESCALE	<b>Timer Counter Value</b> —This 16-bit field contains the current count value.	Description
	This field has a valid range 0x00000 to 0xFFFF.	Setting

# 12.2.6 Timer Status Registers 1 and 2

occurs, it is indicated by setting the CAPT bit. When a compare event occurs, the COMP bit is set. Both bits are cleared by writing 0x0. To be cleared, these bits must first be examined, and the bit must have a value of 0x1. This ensures that an interrupt will not be missed if it occurs between the status read and when Each timer status (TSTATx) register indicates the corresponding timer's status. When a capture event

TSTAT1					Time	Timer Status Register	atus	Re	gist	er 1	C			0	x(FF)F	)x(FF)FFF60A
	BIT 15	14	13	12	1	10	9	<b>∞</b>	7	6	ΟI	4	ω	2	<b>-</b>	ВІТ 0
						Not	Not Used			S	7				CAPT	COMP
TYPE	W	W	W	W	W	W	W	۲W	W	W.J	W	W	W	W	ſW	W
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TSTAT2					Time	Timer Status Register 2	atus	R <sub>e</sub>	Regist	er 2				0	x(FF)F	(FF)FFF61A
	BIT 15	14	13	12	1	10	9	ω /	7	<b>o</b>	Οī	4	ω	2	<u> </u>	BIT 0
						Not	Not Used								CAPT	COMP
TYPE	W	W	W	W	W	W	M	W	W	W	W	W	W	W	ſW	W
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
								0x0	0x0000							

	Table 12-7.
	Timer
	Status
(	Register
	Description

		•
Name	Description	Setting
Not used Bits 15–2	These bits are not used.	I
CAPT Bit 1	Capture Event—This status bit, when set, indicates that a capture event occurred.	<ul><li>0 = No capture event occurred.</li><li>1 = A capture event has occurred.</li></ul>
<b>COMP</b> Bit 0	Compare Event—This status bit, when set, indicates when a compare event occurs.	<ul><li>0 = No compare event occurred.</li><li>1 = A compare event has occurred.</li></ul>



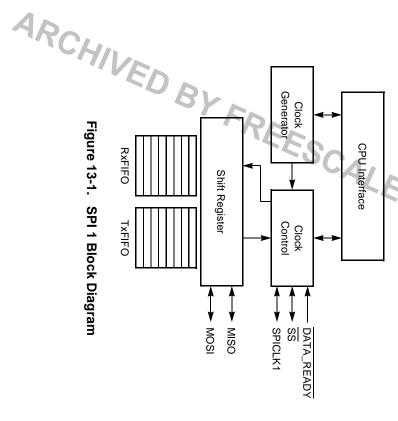
#### Serial Peripheral hapter 13 Interface 7 and 2

describes the operation and programming of both SPI modules, The MC68VZ328 contains two serial peripheral interface (SPI) modules, SPI 1 and SPI 2. This chapter

interface module, allowing the MC68VZ328 to interface with either an external SPI master or an SPI slave SPI 2 design. Equipped with a data FIFO, SPI 1 may operate as a master- or slave-configurable SPI While SPI 2 operates as a master-mode-only SPI module, SPI 1 represents an enhanced version of the

### 13.1 SPI 1 Overview

configurable serial peripheral interface block diagram. signals enables faster data communication with fewer software interrupts. Figure 13-1 illustrates the This section discusses how SPI 1 may be used to communicate with external devices. SPI 1 contains  $8 \times 16$  data-in FIFO and an  $8 \times 16$  data-out FIFO. Incorporating the DATA\_READY and SS control



(A) MOTOROI

#### SP \_ Operation

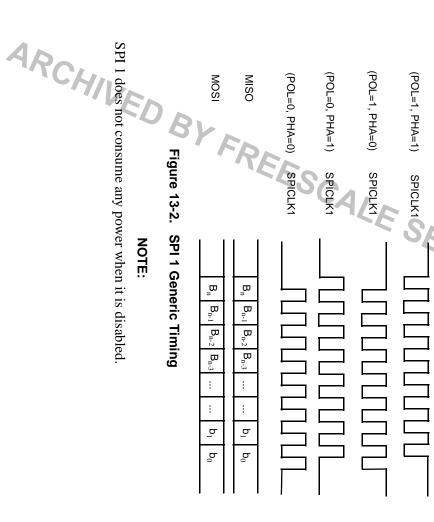
0 to these bits in the PKSEL and PJSEL registers, respectively. See Section 10.4.9.5, "Port J Select (MOSI, MISO, and SPICLK1) of the Port J register. Therefore, before SPI 1 is used, it is necessary to write The SPI 1 signal pins are multiplexed with bit 0 (DATA\_READY) of the Port K register and bits 3-0 Register," on page 10-33 and Section 10.4.10.5, "Port K Select Register," on page 10-36 for detailed

#### **Using SPI 1** as Master

signals, SS and DATA\_READY, are used for data transfer rate control. The user may also program the devices. If the external device is a transmit-only device, the SPI master's output port can be ignored and sample period control register to a fixed data transfer rate. used for other purposes. In order to utilize the internal TxD and RxD data FIFOs, two auxiliary output If SPI 1 is configured as master, it uses a serial link to transfer data between the MC68VZ328 and a peripheral device. A chip-enable signal and a clock signal are used to transfer data between the two

#### Using SPI 1 as Slave

If SPI 1 is configured as slave, the SPI 1 control register can be configured to match the external SPI master's timing. SS becomes an input signal and can be used for data latching from and loading to the internal data shift registers, as well as to increment the data FIFO. Figure 13-2 shows the generic SPI





#### SPI 1 Operation

### 13.2.3 **SPI 1 Phase and Polarity Configurations**

changes on the rising edges of the clock and is shifted in on falling edges. The most significant bit is output on the first rising SPICLK1 edge. The polarity of SPICLK1 may be configured (to invert the SPICLK1 most significant bit is output when the CPU loads the transmitted data. In phase 1 operation, output data operation, output data changes on the falling clock edges, and input data is shifted in on rising edges. The allows it to operate with most serial peripheral devices available in the marketplace. signal), but it does not change the edge-triggered events that are internal to the SPI 1. This flexibility Data is clocked using any one of four programmable clock phase and polarity variations. During phase 0 When SPI 1 is used as master, the SPICLK1 signal is used to transfer data in and out of the shift register.

### 13.2.4 SPI 1 Signals

The following signals are used to control SPI 1:

- shift register. signal from the data shift register when in master mode. In slave mode it is the RxD input to the data MOSI—Master Out/Slave In bidirectional signal, which is multiplexed with PJO, is the TxD output
- signal to the data shift register in master mode. In slave mode it is the TxD output from the data shift MISO—Master In/Slave Out bidirectional signal, which is multiplexed with PJ1, is the RxD input
- in master mode. In slave mode it is the input SPI clock signal. SPICLK1—SPI Clock bidirectional signal, which is multiplexed with PJ2, is the SPI clock output
- input in slave mode. -Slave Select bidirectional signal, which is multiplexed with PJ3, is output in master mode and
- PK0 and will edge- or level-trigger an SPI burst if used ARCHIVED BY FREESCAL -SPI 1 Data Ready input signal is used only in master mode. It is multiplexed with



#### SPI 1 **Programming Model**

This section provides information for programming SPI 1.

# **SPI 1 Receive Data Register**

device during data transaction. The bit position assignments for this register are shown in the following register display. The settings for this register are described in Table 13-1. This read-only register holds the top of the  $8 \times 16$  RxFIFO, which receives data from an external SPI

<b>DATA</b> Bits 7–0	Name			RESET		TYPE			SPIRXD	
Data—Top of SPI 1's RxFIFO (8 x 16)		Table			0	7		BIT 7		
SPI 1's RxI	Description	9 13-1. SI			0	¬		6	SPI 1	
=IFO (8 × 16	n	ป 1 Receiv			0	7		5	SPI 1 Receive Data Register	
	C	e Data	V/~		0	¬		4	Data	
່he data in t າ the interru		Register		0x0000	0	7	DATA	3	a Regist	
The data in this register has no meaning if the RR bit in the interrupt control/status register is cleared.	Setting	Table 13-1. SPI 1 Receive Data Register Description			0	7		2	er	4
o meaning it egister is cl	J				0	¬		1	0x(FF	
the RR bit eared.					0	7		BIT 0	0x(FF)FFF700	

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# Freescale Semiconductor, Ingal 1 Programming Model

# 13.3.2 SPI 1 Transmit Data Register

are discarded and may be written with any value. For example, to transfer 10-bit data, a 16-bit word is written to the SPITXD register, and the 6 MSBs are treated as "don't care" and will not be shifted out. In described in Table 13-2 assignments for this register are shown in the following register display. The settings for this register are this register are ignored while the SPIEN bit in the SPI 1 control/status register is clear. The bit position slave mode, if no data is loaded to the TxFIFO, zeros are shifted out serially as the TxD signal. Writes to FIFO element is determined by the bit count setting in the SPI 1 status/control register. The unused MSBs written to this register can be of either 8-bit or 16-bit size. The number of bits to be shifted out of a 16-bit data exchange process. In either master or slave mode, a maximum of 8 data words are loaded. Data TxFIFO is not full, even if the XCH bit is set. For example, a user may write to TxFIFO during the SPI This write-only data register is the top of the  $8 \times 16$  TxFIFO. Writing to TxFIFO is permitted as long as

TYPE W W W W W W W W W RESET 0 0 0 0 0 0 0 0 0 0	SPITXD		SPI 1	SPI 1 Transmit Data		Register		0x(FF	)FFF702
DATA  w w w w w w w w 0 0 0 0 0 0 0		ВІТ 7	6	Οī	4 <b>C</b>	ω	2	_	ВІТ 0
					DATA				
. 0 0	TYPE	W	W	W	W	٧	W	W	W
	7 7 7 7	0	0	0	0	0	0	0	0
	7				O <sub>×00</sub>				

Table 13-2. SPI 1 Transmit Data Register Description

	DATA Bits 7–0	Name
ARCHIVED BY FREESCAL	Data—Top SPI data to be loaded to the 8 x 16 TxFIFO	Description
	See description	Setting

# SPI 1 Programming Model Freescale Semiconductor, Inc.

# 13.3.3 SPI 1 Control/Status Register

this register are shown in the following register display. The settings for this register are described in This register controls the configuration and operation of the SPI 1 module. The bit position assignments for Table 13-3.

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
MODE SPIEN XCH SS SS PHA POL	XCH SS SS CTL ON TWO TWO TWO TWO TWO TWO TWO TWO TWO TWO
PHA POL	
BIT COUNT	BIT COUNT  rw rw rw  0 0 0 0

Table 13-3. SPI 1 Control/Status Register Description

Name	Description	Setting
DATA RATE Bits 15–13	Data Rate—This field selects the bit rate of the SCLK based on the division of the system clock. The master clock for SPI 1 in master mode is SYSCLK.	000 = Divide SYSCLK by 4 001 = Divide SYSCLK by 8 010 = Divide SYSCLK by 16 011 = Divide SYSCLK by 32 100 = Divide SYSCLK by 64 101 = Divide SYSCLK by 128 110 = Divide SYSCLK by 256 111 = Divide SYSCLK by 512
DRCTL Bits 12–11	DATA_READY Control—In master mode, these 2 bits select the waveform of the DATA_READY input signal. In slave mode, they have no effect.	00 = Don't care DATA_READY 01 = Falling edge trigger input 10 = Active low level trigger input 11 = RSV
MODE Bit 10	SPI 1 Mode Select—This bit selects the mode of SPI 1.	0 = SPI 1 is slave mode 1 = SPI 1 is master mode
SPIEN Bit 9	<b>SPI 1 Enable</b> —This bit enables SPI 1. This bit must be asserted before initiating an exchange. Writing a 0 to this bit flushes the Rx and Tx FIFOs.	0 = Serial peripheral interface is disabled 1 = Serial peripheral interface is enabled
XCH Bit 8	Exchange—In master mode, writing a 1 to this bit triggers a data exchange. This bit remains set while either the exchange is in progress or SPI 1 is waiting for active DATA_READY input while DATA_READY is enabled. This bit is cleared automatically when all data in the TxFIFO and shift registers are shifted out. In slave mode, this bit must be clear.	1 = Initiates exchange (write) or busy (read) 0 = Idle
SSPOL Bit 7	SS Polarity Select—In both master and slave modes, this bit selects the polarity of SS signal.	0 = Active low 1 = Active high

		BIT COUNT Bits 3-0	POL Bit 4	PHA Bit 5	SSCTL Bit 6	Name
ARCHIVED BY FREESCALE	In master mode, a 16-bit data word is loaded from TxFIFO to the shift register, and only the least significant n bits (n = BIT COUNT) are shifted out. The next 16-bit word is then loaded to the shift register.  In slave mode, when the SSCTL bit is 0, this field controls the number of bits received as a data word loaded to RxFIFO. When the SSCTL bit is 1, this field is ignored.	<b>Bit Count</b> —This field selects the length of the transfer. A maximum of 16 bits can be transferred.	<b>Polarity</b> —This bit controls the polarity of the SCLK signal.	<b>Phase</b> —This bit controls the clock/data phase relationship.	<b>SS Waveform Select</b> —In master mode, this bit selects the output wave form for the SS signal. In slave mode, this bit controls RxFIFO advancement.	Description
	1110 = 15-bit transfer 1111 = 16-bit transfer	0000 = 1-bit transfer 0001 = 2-bit transfer	0 = Active high polarity (0 = idle) 1 = Active low polarity (1 = idle)	0 = Phase 0 operation 1 = Phase 1 operation	Master Mode:  0 = SS stays low between SPI 1 bursts  1 = Insert pulse between SPI 1 bursts  Slave Mode:  0 = RxFIFO advanced by Bit Count  1 = RxFIFO advanced by SS rising ed	Setting



# SPI 1 Programming Model Freescale Semiconductor, Inc.

# SPI 1 Interrupt Control/Status Register

assignments for this register are shown in the following register display. The settings for this register are described in Table 13-4. This register is used to provide interrupt control and status of various operations in SPI 1. The bit position

#### **SPIINTCS** RESET 15 15 0 4 0 ₹ z R ₹ 0 SPI 1 Interrupt Control/Status Register ᅩᇛ 0 ${\sf Z}^{\sf RRE}_{\sf E}$ ₹ 0 고퓨 ₹ 0 ᅩᅤ ₹ 0x0000 $^{\rm Z} \, \underline{\underline{\mathbb{H}}}$ ₹ ő ₹ 0 0 Oπ 0 ₹ S 0 $\pi \pi$ 0 ₹ エ双 4 ₹ 0 ᄁᄁ 0 ₹ 0 ₹ I о <u>В</u>Т 0

Table 13-4. SPI 1 Interrupt Control/Status Register Description

Name	Description	Setting
BOEN Bit 15	Bit Count Overflow Interrupt Enable—This bit, when set, allows an interrupt to be generated when an overflow bit count condition exists. See the description of the BO (bit 7) for details.	0 = Disable bit count overflow interrupt. 1 = Enable bit count overflow interrupt.
ROEN Bit 14	RxFIFO Overflow Interrupt Enable—This bit, when set, allows an interrupt to be generated when an overflow occurs in the RxFIFO. See the description of the RO (bit 6) for details.	0 = Disable RxFIFO overflow interrupt. 1 = Enable RxFIFO overflow interrupt.
RFEN Bit 13	RxFIFO Full Interrupt Enable—This bit, when set, allows an interrupt to be generated when there are 8 data words in the RxFIFO. See the description of the RF (bit 5) for details.	0 = Disable RxFIFO full interrupt enable. 1 = Enable RxFIFO full interrupt enable.
RHEN Bit 12	RxFIFO Half Interrupt Enable—This bit, when set, allows an interrupt to be generated when the contents of the RxFIFO is more than or equal to 4 data words. See the description of the RH (bit 4) for details.	<ul><li>0 = Disable half interrupt enable.</li><li>1 = Enable half interrupt enable.</li></ul>
RREN Bit 11	RxFIFO Data Ready Interrupt Enable—This bit, when set, allows an interrupt to be generated when at least 1 data word is ready in the RxFIFO. See the description of the RR (bit 3) for details.	0 = Disable data ready interrupt enable. 1 = Enabled data ready interrupt enable.
TFEN Bit 10	TxFIFO Full Interrupt Enable—This bit, when set, causes an interrupt to be generated when the TxFIFO buffer is full and the RFEN bit is set.	0 = Disable TxFIFO full interrupt. 1 = Enable TxFIFO full interrupt.
THEN Bit 9	TxFIFO Half Interrupt Enable—This bit, when set, causes an interrupt to be generated when the TxFIFO buffer is half empty and the THEN bit is set.	0 = Disable TxFIFO half interrupt. 1 = Enable TxFIFO half interrupt.

Table 13-4. SPI 1 Interrupt Control/Status Register Description (Continued)

AR	CHIVE	TE TxFIFO Empty Status—This bit, when set, Bit 0 causes an interrupt to be generated when the TxFIFO buffer is empty and the TEEN bit is set. Note: When the FIFO is empty, data shifting may still be ongoing. To ensure no data transaction is ongoing, read the XCH bit in control register.	TH  TxFIFO Half Status—This bit, when set, indi- Bit 1  cates that the contents of the TxFIFO is more than or equal to 4 data words.	TF TxFIFO Full Status—This bit, when set, indi- Bit 2 cates there are 8 data words in the TxFIFO.	RxFIFO Data Ready Status—This bit, when Bit 3 set, indicates that at least 1 data word is ready in the Rx FIFO.	RH RxFIFO Half Status—This bit, when set, indi- cates the contents of the RxFIFO is more than or equal to 4 data words.	RxFIFO Full Status—This bit, when set, indi- Bit 5 cates that there are 8 data words in RxFIFO.	RXFIFO Overflow—This bit indicates that the Bit 6 RxFIFO has overflowed and at least 1 data word is has been overwritten. The RO flag is automatically cleared after a data read.	Bit Count Overflow—This bit is set when the SPI is in "slave SPI FIFO advanced by SS rising edge" mode and the slave is receiving more than 16 bits in one burst. This bit is cleared after a data read from the SPIRXD register.  Note: There is nothing to indicate which data word has overflowed; hence, the bad data word may still be in the FIFO if it is not empty.	Bit 8 when set, causes an interrupt to be generated when the TxFIFO buffer is empty and the TE bit is set.
		0 = At least 1 data word is in Tx FIFO. 1 = TxFIFO is empty.	<ul><li>Less than four empty slots in TxFIFO.</li><li>More than or equal to four empty slots in TxFIFO.</li></ul>	= Less than 8 data words in TxFIFO. = 8 data words in TxFIFO.	0 = RxFIFO is empty. 1 = At least 1 data word is ready in the RxFIFO.	<ul><li>0 = Contents of RxFIFO is less than 4 data words.</li><li>1 = Contents of RxFIFO is greater than or equal to 4 data words.</li></ul>	0 = Less than 8 data words in RxFIFO. 1 = 8 data words in RxFIFO.	0 = RxFIFO has not overflowed. 1 = RxFIFO has overflowed. At least 1 data word in the RxFIFO is overwritten.	= No bit count overflow. = At least 1 data word in RxFIFO has bit count overflow error.	1 = Enable TxFIFO empty interrupt.



# SPI 1 Programming Model Freescale Semiconductor, Inc.

### 13.3.5 SPI 1 Test Register

shown in the following register display. The settings for this register are described in Table 13-5 number of words currently in the TxFIFO and RxFIFO. The bit position assignments for this register are The configurable SPI test (SPITEST) register indicates the state machine status of SPI 1 as well as the

	RESET	TYPE			SPITEST
	0			BIT 15	TS
	0			14	
	0			13	
	0			12	
	0	₹		11	
	0	₹	SST/	10	SPI
	0	₩	SSTATUS	9	1 Te
0x0	0	₩		8	st Re
000	0	₹		7	SPI 1 Test Register
O	0	₹	RXCN	6	4
	0	₹	CNT	5	2
	0	₹		4	
	0	8		3	_
	0	₹	TXC	2	)×(FF
	0	₹	TXCNT	1	=)FFF7
	0	₹		BIT 0	F708

Table 13-5. SPI 1 Test Register Description

Name	Description	Setting
Reserved Bits 15–12	Reserved	These bits are reserved and should be set to 0.
SSTATUS Bits 11–8	State Machine Status—This field indicates the state machine status. These bits are used for test purposes only.	See description.
RXCNT Bits 7–4	<b>RxFIFO Counter</b> —This field indicates the number of data words in the RxFIFO.	0000 = RXFIFO is empty. 0001 = 1 data word in RXFIFO. 0010 = 2 data words in RXFIFO. 0011 = 3 data words in RXFIFO.
	CALE	0100 = 4 data words in RXFIFO. 0101 = 5 data words in RXFIFO. 0110 = 6 data words in RXFIFO. 0111 = 7 data words in RXFIFO. 1000 = 8 data words in RXFIFO.
TXCNT Bits 3–0	<b>TxFIFO Counter</b> —This field indicates the number of data words in the TxFIFO.	0000 = TxFIFO is empty. 0001 = 1 data word in TxFIFO. 0010 = 2 data words in TxFIFO.
	FRE	0011 = 3 data words in TxFIFO. 0100 = 4 data words in TxFIFO. 0101 = 5 data words in TxFIFO.
	By	0111 = 7 data words in TxFIFO. 1000 = 8 data words in TxFIFO.

### 13.3.6 **SPI 1 Sample Period Control Register**

described in Table 13-6 on page 13-11. assignments for this register are shown in the following register display. The settings for this register are CLK32 signal. Unless a different crystal is used, the CLK32 signal is 32.768 kHz. The bit position between samples can be from 0 to about 1 second at the resolution of the data rate clock (SPICLK1) or the This register controls the time inserted between data transactions in master mode. The time inserted



SPI

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ISP	C		(0	SPI 1	Sar	nple	Peri	od C	SPI 1 Sample Period Control Register	ol Re	gist	еr		0x(F	F)FF	F70A	
	BIT 15	4	13	14 13 12	1	10	9	œ	7	6	O1	4	ω	2	_	BIT 0	
	CSRC								WAIT	·							
PΕ	W	₹	rw rw	V	₹	₹	₹	₹	₹	₹	₹	₹	₹	V	₹	V	
ρ Π Η	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
-								0×0000	000		)						

Table 13-6. SPI 1 Sample Period Control Register Description

Name	Description	Setting
CSRC Bit 15	Counter Clock Source—This bit selects the clock source for the sample period counter.	0 = SPICLK1 clock 1 = CLK32 (32.68 kHz normal crystal used)
WAIT Bits 14–0	Wait—Number of clock periods inserted between data transactions in master mode	0000 = 0 clocks 0001 = 1 clock
	<i>D</i> 11	0002 = 2 clocks
	D <sub>M</sub>	7FFF = 32767 clocks (approximately 1 second)

### SPI 2 Overview

on whether you are using unidirectional or bidirectional communication mode. It provides the clock for analog-to-digital converters, and other peripherals. The SPI 2 module is a 3- or 4-wire system, depending data transfer and can only function as a master device. It is fully compatible with the serial peripheral This section discusses how SPI 2 can be used to communicate with external devices, such as EEPROMs, interface on Motorola's 68HC05 and 68HC11 microprocessors. Figure 13-3 shows the SPI 2 block

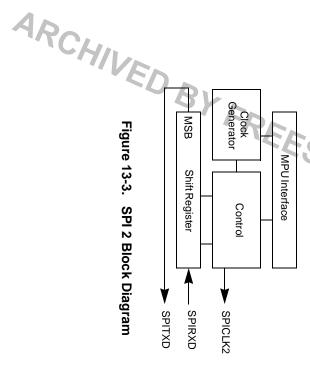


Figure 13-3. SPI 2 Block Diagram

### 13.5 SPI 2 Operation

is freed to be used for other purposes. See Figure 13-4. transfer data between the two devices. If the external device is a transmit-only device, SPI 2's output port data between the MC68VZ328 and a peripheral device. A chip-enable signal and a clock signal are used to The serial peripheral interface 2 operates as a master-mode-only SPI module using a serial link to transfer

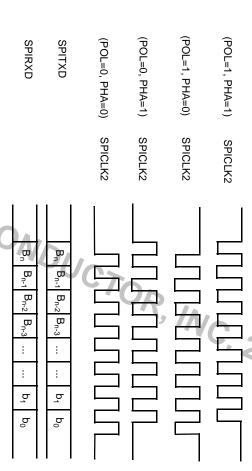


Figure 13-4. SPI 2 Generic Timing

000 to these bits in the PESEL register. See Section 10.4.6, "Port E Registers," on page 10-21 for more The SPI 2 pins are multiplexed with bits 2–0 of the Port E registers, so when you use SPI 2, you must write

#### NOTE:

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The SPI 2 module does not consume any power when it is disabled.

and you can clear this bit by writing a 0 to it. written while the SPI 2 module is disabled or busy. Once the data is loaded, the XCH bit is set in the more information. You can discover the status of the interrupt in the IRQ bit of the SPICONT2 register, posted when the exchange is complete. See Section 9.6.3, "Interrupt Mask Register," on page 9-10 for you clear the MSPI bit in the interrupt mask register before you trigger an exchange, an interrupt will be SPICONT2 register, which triggers an exchange. The XCH bit remains set until the transfer is complete. If control bits. The SPI 2 module is then ready to accept data into the SPIDATA2 register, which cannot be perform a serial data transfer, set the ENABLE bit; then, in a separate write cycle, set the appropriate You must enable the ENABLE bit in the SPICONT2 register before you can change any other bits. To

exchanges. The enable signal required by some SPI slave devices should be provided by an I/O port pin. For systems that need more than 16 clocks to transfer data, the ENABLE bit can remain asserted between ARCHIVEL



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# Freescale Semiconductor, Inc.

**SPI 2 Phase and Polarity Configurations** 

## Onductor, inc. SPI 2 Operation

changes on the falling clock edges and input data is shifted in on rising edges. The most significant bit is edges of the clock and is shifted in on falling edges. The most significant bit is output on the first rising output when the CPU loads the transmitted data. In phase 1 operation, output data changes on the rising using any one of four programmable clock phase and polarity variations. In phase 0 operation, output data to the SPI 2 module. This flexibility allows it to operate with most serial peripheral devices on the market SPICLK2 edge. Polarity inverts SPICLK2, but does not change the edge-triggered events that are internal The SPI 2 module uses the SPICLK2 signal to transfer data in and out of the shift register. Data is clocked

### 13.5.2 SPI 2 Signals

The following signals are used to control the SPI 2 module:

- SPITXD—The Transmit Data pin, which is multiplexed with PEO, is the output of the shift register A new data bit is presented, but it depends on whether you have selected phase or polarity
- A new bit is shifted in, but it depends on whether you have selected phase or polarity The Receive Data pin, which is multiplexed with PE1, is the input to the shift register
- the SPI 2 module is idle, and it is high in polarity 1 mode triggered, the selected number of clock pulses are issued. In polarity 0 mode, this signal is low while -The SPI 2 master Clock output pin is multiplexed with PE2. When the SPI 2 module is

#### NOTE:

may be assigned to this function. A chip-select signal may be required by the external device. A GPIO pir



SPI 2 Programming Model Freescale Semiconductor, Inc.

# 13.6 SPI 2 Programming Model

This section provides information for programming SPI 2

## 13.6.1 SPI 2 Data Register

assignments for this register are shown in the following register display. The settings for this register are described in Table 13-7 The SPI 2 data (SPIDATA2) register exchanges data with external slave devices. The bit position

דוסוד
PE rw rw rw rw rw rw rw rw rw rw rw rw rw

Table 13-7. SPI 2 Data Register Description

Name	Description	Setting
DATA Bits 15–0	Data—Top of SPI 2's RxFIFO (8 × 16)	The data in this register has no meaning if the RR bit in the interrupt control/status register is clear.

# 13.6.2 SPI 2 Data Register Timing

SPICONT2 register is set. In phase 0, data is presented on the SPITXD pin when this register is written. In presented to the external device will be bit 9, followed by the remaining bits. outgoing data is automatically MSB justified. For example, if the exchange length is 10 bits, the first bit phase 1, the first data bit is presented on the first SPICLK2 edge. At the end of the exchange, data from the The data bits are exchanged with the external device. The data must be loaded before the XCH bit in the peripheral is present in this register and bit 0 is the least significant bit. As data is shifted MSB first,

#### OTE:

bit is set. XCH bit is set. This field contains unknown data if it is read while the XCH Writes to this field are ignored while the ENABLE bit is clear or while the



# Freescale Semiconductor, Ingal 2 Programming Model

# 13.6.3 SPI 2 Control/Status Register

status. The bit position assignments for this register are shown in the following register display. The settings for this register are described in Table 13-8. The SPI 2 control/status (SPICONT2) register controls how the SPI 2 module operates and reports its

	RESET	TYPE			SPICONT
	0	₹	DA-	BIT 15	)NT2
	0	w w	DATA RATI	14	
	0	₹	JΕ	13 12 11 10	
	0			12	
	0			11	m
	0			10	<del>P</del>
	0	۲W	ENABLE	9	SPI 2 Control/Status Register
0×0000	0	ſW	XCH	8	ol/Statu
00	0	₹	IRQ	7	s Re
O <sub>i</sub>	0,	V	IRQEN	6	gister
	0	₩	PHA	5	2
	0	W	POL	4	
	0	₹		3	0x(
	0	rw rw rw	BIT COUN	2	FF)
	0	₹	TNNO	1	FFF80
	0	₹	, i	BIT 0	802

able 13-8. SPI 2 Control/Status Register Description

Name	Description	Setting
DATA RATE Bits 15–13	Data Rate—This field selects the bit rate of the SPICLK2 signal based on the division of the	000 = Divide SYSCLK by 4. 001 = Divide SYSCLK by 8.
	system clock. The master clock for the SPI 2 module is SYSCLK.	010 = Divide SYSCLK by 16. 011 = Divide SYSCLK by 32.
	111	100 = Divide SYSCLK by 64. 101 = Divide SYSCLK by 128.
	7/	110 = Divide SYSCLK by 256.
	SE	111 = Divide SYSCLK by 512.
Reserved Bits 12–10	Reserved	These bits are reserved and should be set to 0.
ENABLE Bit 0	<b>Enable</b> —This bit enables the SPI 2 module.	0 = The SPI 2 module is disabled.
Ü	exchange is complete.	I – THE OFFE ENDOUGHERS TO ENDOUGH.
XCH Bit 8	<b>Exchange</b> —This bit triggers a data exchange and remains set while the exchange is in	<ul><li>0 = Idle.</li><li>1 = Initiate an exchange (write) or busy (read).</li></ul>
	progress. During the busy period, the SPIDATA2 register cannot be written.	
IRQ B÷ 7	Interrupt Request—This bit is set when an	0 = An exchange is in progress or idle.
סונ /	interrupt is generated. The MSPI bit of the	= The exchange is complete.
	interrupt mask register must be cleared for the interrupt to be posted to the core. See	
	Section 9.6.3, "Interrupt Mask Register," on	
	page 9-10 for more information. This bit	
	0. You can write a 1 to this bit to generate an	
	interrupt request for system debugging.	

Name	Description	Setting
IRQEN Bit 6	Interrupt Request Enable—This bit enables an interrupt to be generated when an SPI 2 module exchange is finished. This bit does not affect the operation of the IRQ bit; it only affects the interrupt signal to the interrupt controller.	<ul><li>0 = Disable interrupt generation.</li><li>1 = Allow interrupt generation.</li></ul>
PHA Bit 5	<b>Phase</b> —This bit controls the clock and data phase relationship.	0 = Phase 0 operation. 1 = Phase 1 operation.
POL Bit 4	<b>Polarity</b> —This bit controls the polarity of the SCLK signal.	0 = Active high polarity (0 = idle). 1 = Active low polarity (1 = idle).
Bits 3-0	Bit Count—This field selects the length of the transfer. A maximum of 16 bits can be transferred.  In master mode, a 16-bit data word is loaded from the TxFIFO to the shift register, and only the least significant n bits (n = BIT COUNT) are shifted out. The next 16-bit word is then loaded to the shift register.  In slave mode (when the SSCTL bit is 0), this field controls the number of bits received as a data word loaded to the RxFIFO. When the	0000 = 1-bit transfer. 0001 = 2-bit transfer. 

Table 13-8.

SPI 2 Control/Status Register Description (Continued)



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# Universal Asynchronous & Receiver/Transmitter 1 This chapter describes to the MCFOTT

the MC68VZ328 may be used to communicate with external serial devices. UART 1 in the DragonBall VZ unless the divider and prescaler are adjusted accordingly to compensate for the increased clock speed 33.16 MHz system clock, software written for the MC68EZ328 version of the chip is not compatible frequency, which is 33.16 MHz, doubling the 16.58 MHz frequency of the MC68EZ328. For the to reduce the number of software interrupts. An improvement to both UARTs is the system clock input version of UART 1. One of the enhancements in the UART 2 design is an enlarged RxFIFO and TxFIFO processor is identical to the UART in the DragonBall EZ processor, while UART 2 represents an enhanced This chapter describes both UARTs in the DragonBall VZ integrated processor. The two UART ports in

Because the two UART modules are nearly identical, the signal nomenclature throughout this chapter uses an x suffix to represent either 1 or 2. For example, TXDx represents either TXD1 or TXD2 depending on which UART is being used.

# Introduction to the UARTs

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also discusses how to configure and program the UART modules, which have the following features: This section describes how data is transported in character blocks using the standard "start-stop" format. It

- Full-duplex operation
- Flexible 5-wire serial interface
- Direct "glueless" support of IrDA physical layer protocol
- Robust receiver data sampling with noise filtering
- 12-byte FIFO for receive, 8-byte FIFO for transmit (UART 1)
- "Old data" timer on receive FIFO
- 7- and 8-bit operation with optional parity
- Break generation and detection
- Baud rate generator
- Flexible clocking options
- Standard baud rates of 600 bps to 230.4 kbps with 16x sample clock
- External 1x clock for high-speed synchronous communication
- Eight maskable interrupts
- Low-power idle model



following modifications in the UART 2 module: The UART 2 module is an enhanced version of the UART 1. The features listed above are enhanced by the

- The size of the RxFIFO and TxFIFO is increased to 64 bytes each.
- Both the RxFIFO and TxFIFO half mark levels are user selectable.
- the RxFIFO level marker, rather than the RxFIFO half-full bit as is UART 1. The RTS signal can be triggered by either a near RxFIFO full condition or at the level defined by

providing a data-bit clock. Figure 14-1 illustrates a high-level block diagram of both UART modules internal baud rate generator. For those applications that need other bit rates, a 1x clock mode is available asynchronous communication. Serial data is transmitted and received at standard bit rates using the Both the UART 1 and UART 2 modules perform all of the normal operations associated with start-stop

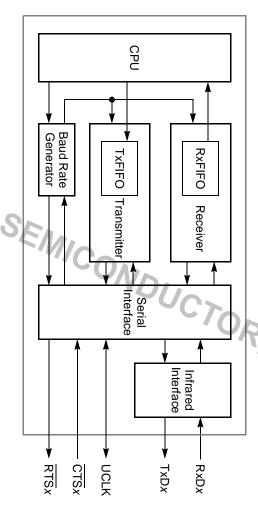


Figure 14-1. **UART** Simplified Block Diagram

### Serial Operation

The UART modules have two modes of operation—NRZ and IrDA. Section 14.2.1, "NRZ Mode," and Section 14.2.2, "IrDA Mode," describe these two modes of operation.

### **NRZ Mode**

is transmitted after the most significant bit. Figure 14-2 on page 14-3 illustrates a character in NRZ mode significant bit first, and each bit occupies a period of time equal to 1 full bit. If parity is used, the parity bit frame delimited by a start bit at the beginning and a stop bit at the end. Data bits are transmitted least The nonreturn to zero (NRZ) mode is primarily associated with RS-232. Each character is transmitted as a ARCHIV



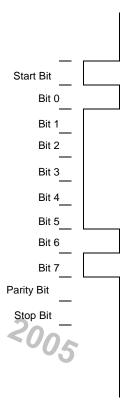


Figure 14-2. NRZ ASCII "A" Character with Odd Parity

### 14.2.2 IrDA Mode

illustrates a character in IrDA mode. connection can be made to external IrDA transceiver modules that uses active low pulses. Figure 14-3 a full bit-time period, zeros are transmitted as three-sixteenth (or less) bit-time pulses, and ones remain Infrared (IrDA) mode uses character frames as NRZ mode does, but, instead of driving ones and zeros for low. The polarity of transmitted pulses and expected receive pulses can be inverted so that a direct

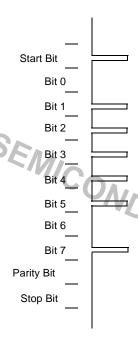


Figure 14-3. IrDA ASCII "A" Character with Odd Parity

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### Serial Interface Signals

in the following descriptions: The pins of both UART modules operate identically. Exceptions in pin and register nomenclature are noted The UART module has five signals that are used to communicate with external UART-compatible devices.

- configurable narrow pulse, is output for each zero bit that is transmitted transmitted as logic high and "spaces" transmitted as logic low. In IrDA mode, this pin, which is a infrared transceiver modules. in UART 2), is the RS-232 transmitter serial output. This pin connects to standard RS-232 or The RS-232 Transmit Data signal, which is multiplexed with PE5 in UART 1 (PJ5-While the UART is in NRZ mode, normal data is output with "marks"
- corresponding UART transmitter (UTX) register signal is asserted again. The current value of this pin can be read in the CTSx STAT bit of the (low) before it starts transmitting a character. If this signal is negated while a character is being active low input used for transmitter flow control. The transmitter waits until this signal is asserted transmitted, the character will be completed, but no additional characters are transmitted until this The Clear to Send signal, which is multiplexed with PE7 (PJ7 in UART 2), is an

### NOTE:

can be programmed to post an interrupt on rising and falling edges if the character whenever a character is ready to be transmitted. The CTSx pin If the NOCTSx bit of the UTX register is set, the transmitter sends a CTSD bit is set in the corresponding UART control (USTCNT) register.



(UMISC) register. This pin interfaces to standard RS-232 and infrared transceiver modules. required pulse polarity is controlled by the RXPOL bit of the corresponding UART miscellaneous expected. In IrDA mode, a pulse of at least 1.63 µs is expected for each zero bit received. The RXD1/RXD2—The Receive Data signal, which is multiplexed with PE4 (PJ4 in UART 2), is the receiver serial input. As for the TXDx pin, while the UART is in NRZ mode, standard NRZ data is

**UART Operation** 

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- of the corresponding UMISC register. this pin can be used as a general-purpose output controlled by the RTS1 bit (RTS2 bit in UART 2) indicates a pending FIFO overrun, this pin is negated (high). When not being used for flow control, transmitter's CTS pin. When the receiver FIFO is nearly full (four slots are remaining), which is ready to receive data by asserting this pin (low). This pin is then connected to the far-end two purposes. Normally, this signal is used for flow control, in which the receiver indicates that it RTS1/RTS2 -The Request to Send signal, which is multiplexed with PE6 (PJ6 in UART 2), serves
- Section 5.2.2, "Peripheral Control Register," on page 5-4 for more details. UART 2. For UCLK output, only one UART at a time is selected to drive this signal. Please refer to synchronous operation. The external UCLK pin connects to the UCLK of both UART 1 and clock to the baud rate generator, or it can output the bit clock at the selected baud rate for The UART Clock input/output signal serves two purposes. It can serve as the source of the

Both UART modules consist of three sub-blocks:

Transmitter

Receiver

Baud rate generator
Section 14.3.1, "Transmitter Open discuss these sub-blocks: Section 14.3.1, "Transmitter Operation," through Section 14.3.3, "Baud Rate Generator Operation,"

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### **Transmitter Operation**

empty, the transmitter outputs a continuous idle (which is 1 bit in NRZ mode and selectable polarity in added to the character, and it is serially shifted (LSB first) at the selected bit rate. The transmitter presents a new bit on each falling edge of the bit clock. IrDA mode). When a character is available for transmission, the start, stop, and parity (if enabled) bits are The transmitter accepts a character (byte) from the CPU bus and transmits it serially. While the FIFO is

### **TxFIFO Buffer Operation**

maskable interrupts. To take maximum advantage of the 8-byte FIFO (64-byte FIFO in UART 2), the TX AVAIL bit in the UTX register is clear or until there is no more data to transmit. The transmitter does FIFO EMPTY interrupt should be enabled. The interrupt service routine should load data until the The transmitter posts a maskable interrupt when it needs parallel data (TX AVAIL). There are three not generate another interrupt until the FIFO has completely emptied.



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**UART Operation** 

empty slots that is less than or equal to the number specified by the TxFIFO level marker of the FIFO level If the driver software has excessive interrupt service latency time, use the FIFO HALF interrupt. With marker interrupt register. UART 2 has a larger FIFO buffer, the transmitter generates an interrupt when the FIFO has a number of UART 1, the transmitter generates an interrupt when the FIFO has fewer than 4 bytes remaining. Because

If the FIFO buffer is not needed, only the TX AVAIL interrupt is required. This interrupt is generated bit is clear is ignored. when at least one space is available in the FIFO. Any data that is written to the FIFO while the TX AVAIL

### **CTS Signal Operation**

applications that do not need hardware flow control, such as IrDA, the NOCTSx bit of the UTX register  $\overline{\text{CTSx}}$  is used for hardware flow control. If  $\overline{\text{CTSx}}$  is negated (high), the transmitter finishes sending the character in progress (if any) and then waits for  $\overline{\text{CTSx}}$  to become asserted (low) again before starting the errors can be generated for debugging purposes by setting the FORCE PERR bit in the corresponding changes state. The CTSx DELTA bit of the UTX register goes high when the CTSx pin toggles. For reading the CTSx STAT bit of the UTX register. An interrupt can be generated when the CTSx pin UMISC register. should be set. While this bit is set, characters will be sent as soon as they are available in the FIFO. Parity next character. The current state of the CTSx pin is sampled by the bit clock and can be monitored by

(continuous zeros). Use the following procedure to send the minimum number of valid Break characters The SEND BREAK bit of the corresponding UTX register is used to generate a Break character

- Make sure the BUSY bit in the UTX register is set.
- Wait until the BUSY bit goes low.
- $\omega$ Clear the TXEN bit in the USTCNT register, which flushes the FIFO
- Wait until the BUSY bit goes low.
- 5 Set the TXEN bit.

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- 6 Set the SEND BREAK bit in the UTX register.
- Load a dummy character into the FIFO.
- Wait until the BUSY bit goes low.
- Clear the SEND BREAK bit.

the next character. After the procedure finishes, the FIFO should be empty and the transmitter should be idle and waiting for

monitor the BUSY bit to determine when the transmitter has actually completed sending the final If the TXEN bit of the USTCNT register is negated while a character is being transmitted, the character be used to determine when to disable the transmitter and turn the link around to receive IrDA applications UEN bit of the corresponding USTCNT register after the BUSY bit becomes clear. The BUSY bit can also character. Remember that there may be a long time delay, depending on the baud rate. It is safe to clear the the TXEN bit is cleared. When the message has been completely sent and the UART is to be disabled, will be completed before the transmitter returns to IDLE. The transmit FIFO is immediately flushed when

of bit time for each zero bit sent. Ones are sent as "no pulse." When the TXPOL bit of the UMISC register is low, pulses are active high. When the TXPOL bit is high, pulses are active low and idle is high. When IrDA mode is enabled, the transmitter produces a pulse that is less than or equal to three-sixteenths



and noise immunity are provided by sampling 16 times per bit and using a voting circuit to enhance sampling. IrDA operation must use asynchronous mode. In synchronous mode, RXDx is sampled on each bit is identified, the remaining bits are shifted in and loaded into the FIFO. rising edge of the bit clock, which is generated by the UART module or supplied externally. When a start start bit, qualifies it, and then samples the succeeding data bits at the perceived bit center. Jitter tolerance receiver operates in two modes—asynchronous and synchronous. In asynchronous mode, it searches for a The receiver block of the UART accepts a serial data stream, converting it into parallel characters. The

errors, breaks, and overruns are checked and reported. The 4 character status bits in the high byte (bits If parity is enabled, the parity bit is checked and its status is reported in the URX register. Similarly, frame 11-8) of the URX register are valid only when read as a 16-bit word with the received character byte.

## 14.3.2.1 Rx FIFO Buffer Operation

interrupt should be used. This interrupt is generated when one or more characters are present in the FIFO. available when this interrupt is generated. If the DATA READY bit in the URX register indicates that has been idle for more than 30 bit times. This is useful in determining the end of a block of characters The OLD DATA bit in the URX register indicates that there is data in the FIFO and that the receive line when no more than 4 empty bytes remain in the FIFO. If the FIFO is not needed, the DATA READY longer latency time, the FIFO HALF interrupt of the URX register can be used. This interrupt is generated more data is remaining in the FIFO, the FIFO can then be emptied byte by byte. If the software has a time, the FIFO FULL interrupt in the URX register can be enabled. The FIFO has no remaining space As with the transmitter, the receiver FIFO is flexible. If the software being used has short interrupt latency

connected directly to an external IrDA transceiver. transforms the infrared signal into an electrical signal. Polarity is programmable so that RXDx can be received. Otherwise, normal NRZ is expected. An infrared transceiver directly connected to the RXDx pin When IrDA mode is enabled, the receiver expects narrow (1.63 µs at a minimum) pulses for each zero bit

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# 14.3.3 Baud Rate Generator Operation

page 14-7 illustrates a block diagram of the baud rate generator. prescalers, an integer prescaler, and a second non-integer prescaler, as well as a 2<sup>n</sup> divider. Figure 14-4 on The baud generator provides the bit clocks to the transmitter and receiver blocks. It consists of two





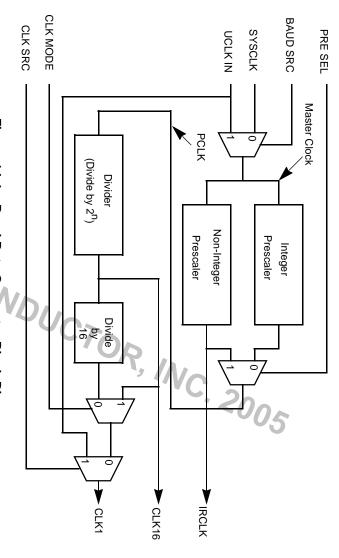


Figure 14-4. **Baud Rate Generator Block Diagram** 

the UCLK pin (input mode). By setting the BAUD SRC bit of the corresponding UART baud control applications, the UCLK signal can be configured as an input or output for the 1x bit clock. (UBAUD) register to 1, an external clock can directly drive the baud rate generator. For synchronous The baud rate generator's master clock source can be the system clock (SYSCLK), or it can be provided by

### Divider

sourced by the CLK16 signal. The divider is a 2<sup>n</sup> binary divider with eight taps-16x clock (CLK16) for the receiver. This clock is further divided by 16 to provide a 50-percent duty-cycle 1x clock (CLK1) to the transmitter. While the CLKM bit of the USTCNT register is high, CLK1 is directly -1, 2, 4, 8, 16, 32, 64, and 128. The selected tap is the

### Non-Integer Prescaler

enabled, zeros are transmitted as three-sixteenth bit-time pulses The non-integer prescaler is used to generate special, nonstandard baud frequencies. When IrDA mode is NOTE

used for controlling the pulse width, but it must be less than or equal to determined by the integer prescaler. The non-integer prescaler will then be If the integer prescaler is used in IrDA operation, the baud rate will be three-sixteenths of bit time.

For example, in IrDA mode, the non-integer prescaler provides a clock at 1.843200 MHz (115.200 kHz  $\times$  16). This clock is used to generate transmit pulses, which are three-sixteenths of a 115.200 kHz bit time.

Table 14-1 on page 14-8 contains the values to use for IrDA operation.

Non-Integer Prescaler Values

Select (Binary)	Minimum Divisor	Maximum Divisor	Step Size
000	2	3 127/128	821/1
001	4	7 63/64	1/64
010	8	15 31/32	1/32
011	16	31 15/16	1/16
100	32	63 7/8	1/8
101	64	127 3/4	1/4
110	128	255 1/2	1/2
111	ı	ζς,	I

Example 14-1 provides a sample divisor calculation.

### Example 14-1. Sample Divisor Calculation

33.16 MHz sysclk / 1.8432 MHz for IrDA bit time = 18.0
18.0 = 16 + (\$20 × 1/16)

Where:
16 = minimum divisor
\$20 = step value
1/16 = step size

Table 14-2 contains the values to program into the non-integer prescaler register for IrDA operation.

### Table 14-2. Non-Integer Prescaler Settings

ARCHI		
ARCHIVEDBY	IrDA	Mode
	011	Select (Binary)
	0x20	Step Value (Hex)



### 4.3.3.3 Integer Prescaler

contains the values that should be used in the UBAUD register for a default 33.16 MHz system clock The baud rate generator can provide standard baud rates from many system clock frequencies. Table 14-3

able 14-3. Selected Baud Rate Settings

ARCHIVE													
ARCHIVED BY FREESCAL	600	1200	2400	4800	9600	19200	38400	14400	28800	57600	115200	230400	Baud Rate
	7	S <sub>6</sub>	5	<b>/</b> /	3	2	1	4	3	2	1	0	Divider
	0x26	0x26	0x26	0x26	0x26	0x26	0x26	0x38	0x38	0x38	0x38	0x38	Prescaler (Hex)



Iniversal Asynchronous Receiver/Transmitter 1 and 2

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### **Programming Model**

## Freescale Semiconductor, Inc.

## 14.4 Programming Model

Interrupt Register," describe the UART registers and detailed information about their settings. The Section 14.4.1, "UART 1 Status/Control Register," through Section 14.4.14, "FIFO Level Marker UART 1 registers are described first.

# 14.4.1 UART 1 Status/Control Register

this register are described in Table 14-4. The bit position assignments for this register are shown in the following register display. The settings for The UART 1 status/control register (USTCNT1) controls the overall operation of the UART 1 module.

	RESET	TYPE			USTCNT
	0	₩	UEN	ВІТ 15	7
	0	₹	⊞ R	14	
	0	₹	ΕX	13	
	0	₹	ĕ6	12	Ç
	0	8	zR	11 10	R
	0	8	O ST OP	10	1 St
	0	V	ST	9	atus,
OXOOO	9	W	8/7	8	UART 1 Status/Control Register
000	0	¥	<b>₽8</b>	7	rol R
	0	₹	SD	6	egist
	0	W	RX FE	5	ë
	0	₹	HR X	4	
	0	8	R R	з	0
	0	8	E X	2	)x(FF)FFF90
	0	8	퓨ᅻ	1	)FFI
	0	8	AE TX	BIT 0	-900

Table 14-4. UART 1 Status/Control Register Description

Name	Description	Setting
UEN Bit 15	<b>UART 1 Enable</b> —This bit enables the UART 1 module. This bit resets to 0.	0 = UART 1 module is disabled 1 = UART 1 module is enabled
	<b>Note:</b> When the UART 1 module is first enabled after a hard reset and before the interrupts are enabled, set the UEN and RXEN bits and perform a word read operation on the URX register to initialize the FIFO and character status bits.	
RXEN Bit 14	<b>Receiver Enable</b> —This bit enables the receiver block. This bit resets to 0.	0 = Receiver is disabled and the receive FIFO is flushed 1 = Receiver is enabled
TXEN Bit 13	<b>Transmitter Enable</b> —This bit enables the transmitter block. This bit resets to 0.	<ul><li>0 = Transmitter is disabled and the transmit FIFO is flushed</li><li>1 = Transmitter is enabled</li></ul>
CLKM Bit 12	Clock Mode Selection—This bit selects the receiver's operating mode. When this bit is low, the receiver is in 16x mode, in which it synchronizes to the incoming datastream and samples at the perceived center of each bit period. When this bit is high, the receiver is in 1x mode, in which it samples the datastream on each rising edge of the bit clock. In 1x mode, the bit clock is driven by CLK16. This bit resets to 0.	<ul><li>0 = 16x clock mode (asynchronous mode)</li><li>1 = 1x clock mode (synchronous mode)</li></ul>
PEN Bit 11	<b>Parity Enable</b> —This bit controls the parity generator in the transmitter and the parity checker in the receiver.	0 = Parity is disabled 1 = Parity is enabled
ODD Bit 10	<b>Odd Parity</b> —This bit controls the sense of the parity generator and checker. This bit has no function if the PEN bit is low.	0 = Even parity 1 = Odd parity

Name	Description	Setting
STOP Bit 9	<b>Stop Bit Transmission</b> —This bit controls the number of stop bits transmitted after a character. This bit has no effect on the receiver, which expects one or more stop bits.	0 = One stop bit is transmitted 1 = Two stop bits are transmitted
<b>8/7</b> Bit 8	<b>8- or 7-Bit</b> —This bit controls the character length. When this bit is set to 7-bit operation, the transmitter ignores data bit 7 and, when receiving, the receiver forces data bit 7 to 0.	0 = 7-bit transmit-and-receive character length 1 = 8-bit transmit-and-receive character length
ODEN Bit 7	<b>Old Data Enable</b> —This bit enables an interrupt when the OLD DATA bit in the URX register is set.	0 = OLD DATA interrupt is disabled 1 = OLD DATA interrupt is enabled
CTSD Bit 6	CTS1 Delta Enable—When this bit is high, it enables an interrupt when the CTS1 pin changes state. When it is low, this interrupt is disabled. The current status of the CTS1 pin is read in the UTX register.	0 = CTS1 interrupt is disabled 1 = CTS1 interrupt is enabled
RXFE Bit 5	Receiver Full Enable—When this bit is high, it enables an interrupt when the receiver FIFO is full. This bit resets to 0.	0 = RX FULL interrupt is disabled 1 = RX FULL interrupt is enabled
RXHE Bit 4	Receiver Half Enable—When this bit is high, it enables an interrupt when the receiver FIFO is more than half full. This bit resets to 0.	0 = RX HALF interrupt is disabled 1 = RX HALF interrupt is enabled
RXRE Bit 3	Receiver Ready Enable—When this bit is high, it enables an interrupt when the receiver has at least 1 data byte in the FIFO. When it is low, this interrupt is disabled.	0 = RX interrupt is disabled 1 = RX interrupt is enabled
TXEE Bit 2	<b>Transmitter Empty Enable</b> —When this bit is high, it enables an interrupt when the transmitter FIFO is empty and needs data. When it is low, this interrupt is disabled.	0 = TX EMPTY interrupt is disabled 1 = TX EMPTY interrupt is enabled
TXHE Bit 1	<b>Transmitter Half Empty Enable</b> —When this bit is high, it enables an interrupt when the transmit FIFO is less than half full. When it is low, the TX HALF interrupt is disabled. This bit resets to 0.	0 = TX HALF interrupt is disabled 1 = TX HALF interrupt is enabled
TXAE Bit 0	<b>Transmitter Available for New Data</b> —When this bit is high, it enables an interrupt if the transmitter has a slot available in the FIFO. When it is low, this interrupt is disabled. This bit resets to 0.	0 = TX AVAIL interrupt is disabled 1 = TX AVAIL interrupt is enabled





# 14.4.2 UART 1 Baud Control Register

following register display. The settings for this register are described in Table integer prescaler, and the UCLK signal. The bit position assignments for this register are shown in the The UART 1 band control (UBAUD1) register controls the operation of the band rate generator, the

### **UBAUD1** RESET 0 0 요절한 ₹ 0 UART 1 Baud Control Register 12 0 BAU D SRC ₹ 0 6 0 ₹ DIVIDE 9 ₹ 0x003F ω σ \_ **PRESCALER** 0x(FF)FFF902 BIT 0

Table 14-5. UART 1 Baud Control Register Description

Name	Description	Setting
Reserved Bits 15–14	Reserved	These bits are reserved and should be set to 0.
UCLKDIR Bit 13	<b>UCLK Direction</b> —This bit controls the direction of the UCLK signal. When this bit is low, the signal is an input, and when it is high, it is an output. However, the SELx bit in the Port E registers must be 0. See Section 10.4.6, "Port E Registers," on page 10-21 for more information.	0 = UCLK is an input. 1 = UCLK is an output.
Reserved Bit 12	Reserved	This bit is reserved and should be set to 0.
BAUD SRC Bit 11	Baud Source—This bit controls the clock source to the baud rate generator.	<ul><li>0 = Baud rate generator source is from system clock.</li><li>1 = Baud rate generator source is from UCLK pin (UCLKDIR must be set to 0).</li></ul>
DIVIDE Bits 10–8	Divide—These bits control the clock frequency produced by the baud rate generator.	000 = Divide by 1. 001 = Divide by 2. 010 = Divide by 4. 011 = Divide by 8. 100 = Divide by 16. 101 = Divide by 32. 110 = Divide by 64. 111 = Divide by 128.
Reserved Bits 7–6	Reserved	These bits are reserved and should be set to 0.
PRESCALER Bits 5–0	Prescaler—These bits control the division value of the baud generator prescaler. The division value is determined by the following formula:  Prescaler division value =  65 (decimal) – PRESCALER	See description.

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## 14.4.3 UART 1 Receiver Register

enabled. However, the character status bits are only valid when read with the character bits in a 16-bit read access. The bit position assignments for this register are shown in the following register display. The Reading the UART 1 receiver register initializes the FIFO status bits. The receiver interrupts can then be Before enabling the receiver interrupts, the UEN and RXEN bits in the USTCNT register should be set. FIFO status bits reflect the current status of the FIFO. At initial power up, these bits contain random data. The UART 1 receiver (URX1) register indicates the status of the receiver FIFO and character data. The

	RESET	TYPE	77.77	I	URX1
	0	¬	FIFO FULL	ВІТ 15	
	0	¬	FIFO HALF	14	
	0	¬	DATA READY	13	
	0	7	OLD DATA	12	UAR1
	0	¬	N S S	11	「1R
000000	0	¬	FRAME ERROR	10	eceiver
Š	0	4	BREAK	9	UART 1 Receiver Regist
	0	7	PARITY ERROR	8	7/
	0	¬		7	
	0	_		6	
	0	¬		6 5 4 3 2	0
	0	7	RXI	4	×
	0	7	RX DAT/	ω	<u>H</u>
	0 0 0 0 0 0		♪	2	Ţ
	0	,		1 BIT	FF)FFF904
					_

able 14-6. UART 1 Receiver Register Description

Name	Description	Setting
FIFO FULL Bit 15	FIFO Full (FIFO Status)—This read-only bit indicates that the receiver FIFO is full and may generate an overrun. This bit generates a maskable interrupt.	0 = Receiver FIFO is not full 1 = Receiver FIFO is full
FIFO HALF Bit 14	FIFO Half (FIFO Status)—This read-only bit indicates that the receiver FIFO has four or fewer slots remaining in the FIFO. This bit generates a maskable interrupt.	0 = Receiver FIFO has more than four slots remaining 1 = Receiver FIFO has four or fewer slots remaining
DATA READY Bit 13	Data Ready (FIFO Status)—This read-only bit indicates that at least 1 byte is present in the receive FIFO. The character bits are valid only while this bit is set. This bit generates a maskable interrupt.	0 = No data in the receiver FIFO 1 = Data in the receiver FIFO
OLD DATA Bit 12	Old Data (FIFO Status)—This read-only bit indicates that data in the FIFO is older than 30 bit times. It is useful in situations where the FIFO FULL or FIFO HALF interrupts are used. If there is data in the FIFO, but the amount is below the FIFO HALF interrupt threshold, a maskable interrupt can be generated to alert the software that unread data is present. This bit clears when the character bits are read.	0 = FIFO is empty or the data in the FIFO is < 30 bit times old 1 = Data in the FIFO is > 30 bit times old
OVRUN Bit 11	FIFO Overrun (Character Status)—This read-only bit indicates that the receiver overwrote data in the FIFO. The character with this bit set is valid, but at least one previous character was lost. In normal circumstances, this bit should never be set. It indicates the software is not keeping up with the incoming data rate. This bit is updated and valid for each received character.	0 = No FIFO overrun occurred 1 = A FIFO overrun was detected

Table 14-6. UART 1 Receiver Register Description (Continued)

Name	Description	Setting
FRAME ERROR Bit 10	Frame Error (Character Status)—This read-only bit indicates that the current character had a framing error (missing stop bit), which indicates that there may be corrupted data. This bit is updated for each character read from the FIFO.	0 = Character has no framing error 1 = Character has a framing error
BREAK Bit 9	Break (Character Status)—This read-only bit indicates that the current character was detected as a BREAK. The data bits character are all 0 and the stop bit is also 0. The FRAME ERROR bit will 1 = Character is a break character always be set when this bit is set, and if odd parity is selected,  DARITY ERROR will also be set. This bit is undeted and valid.	0 = Character is not a break character 1 = Character is a break character
PARITY ERROR Bit 8	Parity Error (Character Status)—This read-only bit indicates that the current character was detected with a parity error, which indicates that there may be corrupted data. This bit is updated and valid with each character read from the FIFO. While parity is disabled, this bit always reads 0.	See description
RX DATA Bits 7–0	Rx Data (Character Data)—This read-only field is the top receive character in the FIFO. The bits have no meaning if the DATA READY bit is 0. In 7-bit mode, the most significant bit is forced to 0, and in 8-bit mode, all bits are active.	See description

## **14.4.4** UART 1 Transmitter Register

assignments for this register are shown in the following register display. The settings for this register are The UART 1 transmitter (UTX1) register controls how the transmitter operates. The bit position

UTX1			_	JART 1	Trans	1 Transmitter Register	Regis	ter			_	0×	Ŧ	Ϋ́	핅	(FF)FFF906	
	BIT 15	14	13	r) N	1	10	9	œ	7	6	Οī	4	ω	6 5 4 3 2	_	0 B <u>T</u>	
	FIFO	HALF	L WAN XL	SEND BREAK	NO CTS1	BUSY	CTS1 STAT	CTS1 CTS1 STAT DELTA				×	TX DATA	≻			
TYPE	Г	r	17.1	WI	W	W	۲W	W	\$	\$	<	\$	€	W W W W W	\$	8	
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0 0 0 0 0 0	0	0	
7 0 0			8)			0x0000	0										

able 14-7. UART 1 Transmitter Register Description

Name	Description	Setting
FIFO		0 = Transmitter FIFO is not empty
EMPTY Bit 15	the transmitter FIFO is empty. This bit generates a maskable interrupt.	1 = Transmitter FIFO is empty

Table 14-7. **UART 1 Transmitter Register Description (Continued)** 

	TX DATA Bits 7–0	CTS1 DELTA Bit 8	CTS1 STAT Bit 9	BUSY Bit 10	NOCTS1 Bit 11	SEND BREAK Bit 12	TX AVAIL Bit 13	FIFO HALF Bit 14	Name
ARCHIVEDBI	<b>Tx Data (Character) (Write-Only)</b> —This write-only field is the parallel transmit-data input. In 7-bit mode, bit 7 is ignored, and in 8-bit mode, all of the bits are used. Data is transmitted with the least significant bit first. A new character is transmitted when this field is written and has passed through the FIFO.	CTS1 Delta (CTS1 Bit)—When this bit is high, it indicates that the CTS1 signal changed state and generates a maskable interrupt. The current state of the CTS1 signal is available on the CTS1 STAT bit. An immediate interrupt may be generated by setting this bit high. The CTS1 interrupt is cleared by writing 0 to this bit.	CTS1 Status (CTS1 Bit)—This bit indicates the current status of the CTS1 signal. A "snapshot" of the pin is taken immediately before this bit is presented to the data bus. While the NOCTS1 bit is high, this bit can serve as a general-purpose input.	<b>Busy (Tx Status)</b> —When this bit is high, it indicates that the transmitter is busy sending a character. This bit is asserted while the transmitter state machine is not idle or the FIFO has data in it.	Ignore CTS1 (Tx Control)—When this bit is high, it forces the CTS1 signal that is presented to the transmitter to always be asserted, which effectively ignores the external pin.	Send Break (Tx Control)—This bit forces the transmitter to immediately send continuous zeros, which creates a break character. See Section 14.3.1.2, "CTS Signal Operation," for a description of how to generate a break.	<b>Transmit FIFO Available (FIFO Status)</b> —This read-only bit indicates that the transmitter FIFO has at least one slot available for data. This bit generates a maskable interrupt.	FIFO Half (FIFO Status)—This read-only bit indicates that the transmitter FIFO is less than half full. This bit generates a maskable interrupt.	Description
	See description	0 = CTS1 signal did not change state since it was last cleared 1 = CTS1 signal has changed state	0 = <u>CTS1</u> signal is low 1 = <u>CTS1</u> signal is high	0 = Transmitter is not sending a character 1 = Transmitter is sending a character	0 = Transmit only while the CTS1 signal is asserted 1 = Ignore the CTS1 signal	0 = Normal transmission 1 = Send break (continuous zeros)	0 = Transmitter does not need data 1 = Transmitter needs data	0 = Transmitter FIFO is more than half full 1 = Transmitter FIFO is less than half full	Setting



### Programming Model

14.4.5 UART 1 Miscellaneous Register

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register are described in Table 14-8. position assignments for this register are shown in the following register display. The settings for this The UART 1 miscellaneous (UMISC1) register contains miscellaneous bits to control test features of the UART 1 module. Some bits, however, are only used for factory testing and should not be used. The bit

### **UMISC1** TES BA 0 SRC 0 FORCE PERR 3 ₹ 0 **UART 1 Miscellaneous Register** 유등 12 0 BAUD RESET 0 ₹ T ES F 10 0 0x0000 ω NCS1 SY 꼭 0 ₹ 6 AEN R ₹ 유 등 공 공 0x(FF)FFF908 $\nabla \times \nabla$ 우고국 0 0 0

Table 14-8. UART 1 Miscellaneous Register Description

Name	Description	Setting
BAUD TEST Bit 15	Baud Rate Generator Testing—This bit puts the baud rate generator in test mode. The integer and non-integer prescalers, as well as the divider, are broken into 4-bit nibbles for testing. This bit should remain 0 for normal operation.	0 = Normal mode. 1 = Test mode.
CLKSRC	Clock Source—This bit selects the source of the 1x bit clock	0 = Bit clock is generated by the
Bit 14	for transmission and reception. When this bit is high, the bit clock is derived directly from the UCLK pin (it must be configured as an input). When it is low (normal), the bit clock is supplied by the baud rate generator. This bit allows high-speed synchronous applications, in which a clock is provided by the	baud rate generator.  1 = Bit clock is supplied by the  UCLK pin.
	5	
PERR Bit 13	mitter to generate parity errors, if parity is enabled. This bit is for system debugging.	<ul><li>0 = Generate normal parity.</li><li>1 = Generate inverted parity (error).</li></ul>
LOOP Bit 12	<b>Loopback</b> —This bit controls loopback for system testing purposes. When this bit is high, the receiver input is internally connected to the transmitter and ignores the RXD1 pin. The TXD1 pin is unaffected by this bit.	<ul><li>0 = Normal receiver operation.</li><li>1 = Internally connects the transmitter output to the receiver input.</li></ul>
BAUD RESET	<b>Baud Rate Generator Reset</b> —This bit resets the baud rate generator counters.	0 = Normal operation. 1 = Reset baud counters.
Bit 11		
IRTEST Bit 10	Infrared Testing—This bit connects the output of the IrDA circuitry to the TXD1 pin. This provides test visibility to the IrDA	0 = Normal operation. 1 = lrDA test mode.
Reserved	Reserved	These bits are reserved and should
Bits 9-8	9/	be set to 0.

	Reserved Bits 1–0	<b>TXPOL</b> Bit 2	RXPOL Bit 3	IRDA LOOP Bit 4	IRDAEN Bit 5	RTS1 Bit 6	RTS1 CONT Bit 7	Name
ARCHIVED BY FREESCALE SE	Reserved	<b>Transmit Polarity</b> —This bit controls the polarity of the transmitted data.	Receive Polarity—This bit controls the polarity of the received data.	<b>Loop Infrared</b> —This bit controls the loopback from the transmitter to the receiver in the IrDA interface. This bit is used for system testing purposes.	Infrared Enable—This bit enables the IrDA interface.	Request to Send Pin—This bit controls the RTS1 pin when the RTS1 CONT bit is 0.	RTS1 Control—This bit selects the function of the RTS1 pin.	Description
	These bits are reserved and should be set to 0.	0 = Normal polarity (1 = idle). 1 = Inverted polarity (0 = idle).	0 = Normal polarity (1 = idle). 1 = Inverted polarity (0 = idle).	<ul><li>0 = No infrared loop.</li><li>1 = Connect the infrared transmitter to an infrared receiver.</li></ul>	0 = Normal NRZ operation. 1 = IrDA operation.	$0 = \frac{\overline{RTS1}}{RTS1} \text{ pin is } 1.$ $1 = \overline{RTS1} \text{ pin is } 0.$	0 = RTS1 pin is controlled by the RTS1 bit.  1 = RTS1 pin is controlled by the receiver FIFO. When no more than four slots are available, RTS1 is negated.	Setting

# 14.4.6 UART 1 Non-Integer Prescaler Register

this register are described in Table 14-9. The bit position assignments for this register are shown in the following register display. The settings for The UART 1 non-integer prescaler register (NIPR1) contains the control bits for the non-integer prescaler.

NIPR1			UA	RT 1	Nor	1-Inte	<b>UART 1 Non-Integer Prescaler Register</b>	Pres	cale	r Re	giste	Ÿ	0	×(FF	(FF)FFF90	F90A
	BIT 15 14 13 12 11 10 9	14	13	12	11	10	9	8	8 7	6	O	4	3	2	1	ВІТ 0
	PRE SEL						SELECT	Γ		<b>W</b>		STEP	STEP VALUE	111		
TYPE	۲W					W	W	W	rw rw rw rw rw rw rw	W	W	W	W	۲W	W	rw
RESET	0	0	0	0	0	0	0	0	0 0 0 0	0	0	0	0	0	0	0

Table 14-9. UART 1 Non-Integer Prescaler Register Description

Name	Description	Setting
PRESEL Bit 15	Prescaler Selection—This bit selects the input to the baud rate generator	<ul><li>0 = Divider source is from the integer prescaler.</li><li>1 = Divider source is from the non-integer prescaler.</li></ul>
	divider. Refer to Figure 14-4 on page 14-7 for information about selecting the prescaler.	"CC
Reserved Bits 14–11	Reserved	These bits are reserved and should be set to 0.
SELECT Bits 10–8	Tap Selection—This field selects a tap from the non-integer divider.	000 = Divide range is 2 to 3 127/128 in 1/128 steps. 001 = Divide range is 4 to 7 63/64 in 1/64 steps. 010 = Divide range is 8 to 15 31/32 in 1/32 steps. 011 = Divide range is 16 to 31 15/16 in 1/16 steps. 100 = Divide range is 32 to 63 7/8 in 1/8 steps. 101 = Divide range is 64 to 127 3/4 in 1/4 steps. 110 = Divide range is 128 to 255 1/2 in 1/2 steps. 111 = Disable the non-integer prescaler.
STEP VALUE Bits 7-0	Step Value—This field selects the non-integer prescaler's step value.	0000 0000. Step = 0. 0000 0001. Step = 1.



Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently

are not available from Freescale for import or sale in the United States prior to September 2010; MC68VZ328 Product Family

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# Non-Integer Prescaler Programming Example

The following steps show how to generate a 3.072 MHz clock frequency from a 16.580608 MHz clock

Calculate the divisor:

divisor =  $16.580608 \text{ MHz} \div 3.072000 \text{ MHz} = 5.397333$ 

- 1 Find the value for the SELECT field in the NIPR. The divisor is between four and eight, so Table 14-1 on page 14-8 indicates that the SELECT field is 001. The divisor step size for the selected range is one sixty-fourth.
- $\omega$ should be rounded to the nearest integer value and converted to the hex equivalent: step size, which is one sixty-fourth or 0.015625 ( $1.397333 \div 0.015625 = 89.42$ ). The result Find the number of steps to program into the STEP VALUE field by subtracting the minimum divisor from the divisor (5.397333 - 4 = 1.397333) and dividing this value by the

89 (decimal) = 59 (hex)

The actual divisor will be 5.390625, which will produce a frequency of 3.075823 MHz (0.12 percent above the preferred frequency). ARCHIVED BY FREESCALE SEMICOND



### **Programming Model**

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# 14.4.8 UART 2 Status/Control Register

this register are described in Table 14-10. The bit position assignments for this register are shown in the following register display. The settings for The UART 2 status/control register (USTCNT2) controls the overall operation of the UART 2 module.

į	RESET	TYPE			USTCNT:
	0	₩	UEN	BIT 15	NT2
	0	W	E R N	14	
	0	V	TX EN	13	
	0	₹	CL KM	12	$\subseteq$
	0	V	PE N	11 10	Ŕ
	0	8	OD D	10	2 St
	0	₹	ST OP	9	atus
0×	0	V	8/7	8	/Cor
0000	0	V	EN OD	7	ntrol
1	0	W	CT SD	6	UART 2 Status/Control Register
	0	rw rw	RX FE	5	ster
	0	₹	RX HE	4	-(
	0	₽	R X	з	
	0	₹	TX EE	2	)×(FI
	0	W	₩,	٦	F)FFF91
	0	V	TX AE	ВІТ 0	F910

# Table 14-10. UART 2 Status/Control Register Description

Name	Description	Setting
UEN Bit 15	<b>UART 2 Enable</b> —This bit enables the UART 2 module. This bit resets to 0.	0 = UART 2 module is disabled 1 = UART 2 module is enabled
	<b>Note:</b> When the UART 2 module is first enabled after a hard reset and before the interrupts are enabled, set the UEN and RXEN bits and perform a word read operation on the URX register to initialize the FIFO and character status bits.	
RXEN Bit 14	Receiver Enable—This bit enables the receiver block. This bit resets to 0.	0 = Receiver is disabled and the receive FIFO is flushed 1 = Receiver is enabled
TXEN Bit 13	<b>Transmitter Enable—</b> This bit enables the transmitter block. This bit resets to 0.	0 = Transmitter is disabled and the transmit FIFO is flushed 1 = Transmitter is enabled
CLKM Bit 12	Clock Mode Selection—This bit selects the receiver's operating mode. When this bit is low, the receiver is in 16x mode, in which it synchronizes to the incoming datastream and samples at the perceived center of each bit period. When this bit is high, the receiver is in 1x mode, in which it samples the datastream on each rising edge of the bit clock. In 1x mode, the bit clock is driven by CLK16. This bit resets to 0.	0 = 16x clock mode (asynchronous mode) 1 = 1x clock mode (synchronous mode)
PEN Bit 11	Parity Enable—This bit controls the parity generator in the transmitter and the parity checker in the receiver.	0 = Parity is disabled 1 = Parity is enabled
ODD Bit 10	Odd Parity—This bit controls the sense of the parity generator and checker. This bit has no function if the PEN bit is low.	0 = Even parity 1 = Odd parity
STOP Bit 9	<b>Stop Bit Transmission</b> —This bit controls the number of stop bits transmitted after a character. This bit has no effect on the receiver, which expects one or more stop bits.	0 = One stop bit is transmitted 1 = Two stop bits are transmitted
<b>8/7</b> Bit 8	8- or 7-Bit—This bit controls the character length. When this bit is set to 7-bit operation, the transmitter ignores data bit 7 and, when receiving, the receiver forces data bit 7 to 0.	0 = 7-bit transmit-and-receive character length 1 = 8-bit transmit-and-receive character length

Гable 14-10.
<b>UART 2</b>
UART 2 Status/Control Re
Register
Register Description (Continue
(Continued)

	TXAE Bit 0	TXHE Bit 1	TXEE Bit 2	RXRE Bit 3	RXHE Bit 4	RXFE Bit 5	CTSD Bit 6	ODEN Bit 7	Name
ARCHIVED BY FREESC	Transmitter Available for New Data—When this bit is high, it enables an interrupt if the transmitter has a slot available in the FIFO. When it is low, this interrupt is disabled. This bit resets to 0.	Transmitter Half Empty Enable—When this bit is high, it enables an interrupt when the transmit FIFO is less than half full. When it is low, the TX HALF interrupt is disabled. This bit resets to 0.	<b>Transmitter Empty Enable</b> —When this bit is high, it enables an interrupt when the transmitter FIFO is empty and needs data. When it is low, this interrupt is disabled.	Receiver Ready Enable—When this bit is high, it enables an interrupt when the receiver has at least 1 data byte in the FIFO. When it is low, this interrupt is disabled.	Receiver Half Enable—When this bit is high, it enables an interrupt when the receiver FIFO is more than half full. This bit resets to 0.	Receiver Full Enable—When this bit is high, it enables an interrupt when the receiver FIFO is full. This bit resets to 0.	CTS2 Delta Enable—When this bit is high, it enables an interrupt when the CTS2 pin changes state. When it is low, this interrupt is disabled. The current status of the CTS2 pin is read in the UTX register.	Old Data Enable—This bit enables an interrupt when the OLD DATA bit in the URX register is set.	Description
	0 = TX AVAIL interrupt is disabled 1 = TX AVAIL interrupt is enabled	0 = TX HALF interrupt is disabled 1 = TX HALF interrupt is enabled	0 = TX EMPTY interrupt is disabled 1 = TX EMPTY interrupt is enabled	0 = RX interrupt is disabled 1 = RX interrupt is enabled	0 = RX HALF interrupt is disabled 1 = RX HALF interrupt is enabled	0 = RX FULL interrupt is disabled 1 = RX FULL interrupt is enabled	0 = <u>CTS2</u> interrupt is disabled 1 = <u>CTS2</u> interrupt is enabled	0 = OLD DATA interrupt is disabled 1 = OLD DATA interrupt is enabled	Setting



### Programming Model

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# 14.4.9 UART 2 Baud Control Register

following register display. The settings for this register are described in Table integer prescaler, and the UCLK signal. The bit position assignments for this register are shown in the The UART 2 band control (UBAUD2) register controls the operation of the band rate generator, the

### **UBAUD2** RESET 0 PR CCLX ₹ 0 UART 2 Baud Control Register 0 BAUD SRC 6 0 DIVIDE 0x003F ₹ 9 0 ₹ 0 ω ₹ ₹ PRESCALER ₹ BIT 0

# Table 14-11. UART 2 Baud Control Register Description

Name	Description	Setting
Reserved Bits 15–14	Reserved	These bits are reserved and should be set to 0.
UCLKDIR Bit 13	UCLK Direction—This bit controls the direction of the UCLK signal. When this bit is low, the signal is an input, and when it is high, it is an output. However, the SELx bit in the Port E registers must be 0. See Section 10.4.6, "Port E Registers," on page 10-21 for more information.	0 = UCLK is an input. 1 = UCLK is an output.
Reserved Bit 12	Reserved	This bit is reserved and should be set to 0.
BAUD SRC Bit 11	Baud Source—This bit controls the clock source to the baud rate generator.	<ul><li>0 = Baud rate generator source is from system clock.</li><li>1 = Baud rate generator source is from UCLK pin (UCLKDIR must be set to 0).</li></ul>
DIVIDE Bits 10-8	<b>Divide</b> —These bits control the clock frequency produced by the baud rate generator.	000 = Divide by 1. 001 = Divide by 2. 010 = Divide by 4. 011 = Divide by 8. 100 = Divide by 16. 101 = Divide by 32.
Reserved Bits 7–6	Reserved	These bits are reserved and should be set to 0.
PRESCALER Bits 5–0	Prescaler—These bits control the division value of the baud generator prescaler. The division value is determined by the following formula:  Prescaler division value = 65 (decimal) – PRESCALER	See description.

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## 14.4.10 UART 2 Receiver Register

access. The bit position assignments for this register are shown in the following register display. The enabled. However, the character status bits are only valid when read with the character bits in a 16-bit read Reading the UART 2 receiver register initializes the FIFO status bits. The receiver interrupts can then be Before the receiver interrupts are enabled, the UEN and RXEN bits in the USTCNT register should be set. FIFO status bits reflect the current status of the FIFO. At initial power up, these bits contain random data. The UART 2 receiver (URX2) register indicates the status of the receiver FIFO and character data. The

	RESET	TYPE			URX2
	0	¬	두끈ㅇ끆	BIT 15	
	0	7	FIFO	14	
	0	7	DATA READY	13	
	0	¬	OLD DATA	12	UAF
	0	¬	OVR N	11	₹T 2 I
0x0000	0	7	FRAME ERROR	10	UART 2 Receiver Regist
S	0	4	BREAK	9	r Regis
	0	7	PARIT Y ERRO R	8	ter
	0	¬		7	
	0	¬		6	
	0	¬		Q	
	0 0 0 0 0	¬	RX DATA	6 5 4 3 2	0 <u>×</u>
	0	¬	DATA	ω	Ŧ
	0			2	)Ę
	0	_		1 BIT	)FFF9
	0	7		0 3 7	14

Table 14-12. UART 2 Receiver Register Description

Name	Description	Setting
FIFO FULL	FIFO Full (FIFO Status)—This read-only bit indicates that the receiver FIFO is full and may generate an overrun. This bit generates a maskable interrunt	0 = Receiver FIFO is not full 1 = Receiver FIFO is full
FIFO	FIFO Half (FIFO Status)—This read-only hit indicates that the	0 = Receiver FIFO has more than
HALF	receiver FIFO has four or fewer slots remaining in the FIFO.	four slots remaining
Bit 14	This bit generates a maskable interrupt.	1 = Receiver FIFO has four or fewer slots remaining
DATA READY	<b>Data Ready (FIFO Status)</b> —This read-only bit indicates that at least 1 byte is present in the receive FIFO. The character bits	0 = No data in the receiver FIFO 1 = Data in the receiver FIFO
Bit 13	are valid only while this bit is set. This bit generates a maskable interrupt.	
OLD	Old Data (FIFO Status)—This read-only bit indicates that data in the FIFO is older than 30 bit times. It is useful in situations	0 = FIFO is empty or the data in the
Bit 12	where the FIFO FIFO HALF interrupts are used. If	1 = Data in the FIFO is > 30 bit times
	HALF interrupt threshold, a maskable interrupt can be gener-	Cic
	ated to alert the software that unread data is present. This bit clears when the character bits are read.	
OVRUN	FIFO Overrun (Character Status)—This read-only bit indi-	0 = No FIFO overrun occurred
Bit 11	cates that the receiver overwrote data in the FIFO. The character ter with this bit set is valid, but at least one previous character	1 = A FIFO overrun was detected
	was lost. In normal circumstances, this bit should never be set.	
	It indicates the software is not keeping up with the incoming	
	adia rate. Tilis bit is abadied alla valla foi edol Fecelved crial:	

Table 14-12. UART 2 Receiver Register Description (Continued)

Name	Description	Setting
FRAME ERROR Bit 10	Frame Error (Character Status)—This read-only bit indicates that the current character had a framing error (missing stop bit), which indicates that there may be corrupted data. This bit is updated for each character read from the FIFO.	0 = Character has no framing error 1 = Character has a framing error
BREAK Bit 9	Break (Character Status)—This read-only bit indicates that the current character was detected as a BREAK. The data bits are all 0 and the stop bit is also 0. The FRAME ERROR bit will always be set when this bit is set, and if odd parity is selected, PARITY ERROR will also be set. This bit is updated and valid with each character read from the FIFO.	0 = Character is not a break character 1 = Character is a break character
PARITY ERROR Bit 8	Parity Error (Character Status)—This read-only bit indicates that the current character was detected with a parity error, which indicates that there may be corrupted data. This bit is updated and valid with each character read from the FIFO. While parity is disabled, this bit always reads 0.	See description
RX DATA Bits 7–0	Rx Data (Character Data)—This read-only field is the top receive character in the FIFO. The bits have no meaning if the DATA READY bit is 0. In 7-bit mode, the most significant bit is forced to 0, and in 8-bit mode, all bits are active.	See description

# 4.4.11 UART 2 Transmitter Register

assignments for this register are shown in the following register display. The settings for this register are The UART 2 transmitter (UTX2) register controls how the transmitter operates. The bit position

UTX2			_	UART 2 Transmitter Register	Trans	imi <del>t</del> t	er Re	gister				0	×	$\Xi$	Ĥ	(FF)FFF916
	BIT 15	14	13	12	11	10	9	8	7	6	5	4	ω	2	1	7 6 5 4 3 2 1 BITO
	FIFO	FIFO	XT	SEND	ON	∪В	CTS2					ΥT	, ,	ΓΛ		
	EMPTY	HALF	AVAIL	BREAK	CTS2	S Y	STAT	DELTA				->	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	7		
TYPE	٦	r	17.1	W	W	W	W	W	8	\$	W W W W W	8	\$	\$	8	٧
0	0	0	0	0	0	0	0	0	0	0	0 0 0 0 0 0	0	0	0	0	0
7 0 1			8)			0x0	0x0000									

able 14-13. UART 2 Transmitter Register Description

Name	Description	Setting
FIFO	FIFO Empty (FIFO Status)—This read-only bit indicates that 0 = Transmitter FIFO is not empty	0 = Transmitter FIFO is not empty
EMPTY	the transmitter FIFO is empty. This bit generates a maskable	1 = Transmitter FIFO is empty
Bit 15	interrupt.	

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Table 14-13. **UART 2 Transmitter Register Description (Continued)** 

	TX DATA Bits 7–0	CTS2 DELTA Bit 8	CTS2 STAT Bit 9	BUSY Bit 10	NOCTS2 Bit 11	SEND BREAK Bit 12	TX AVAIL Bit 13	FIFO HALF Bit 14	Name
ARCHIVEDE	Tx Data (Character) (Write-Only)—This write-only field is the parallel transmit-data input. In 7-bit mode, bit 7 is ignored, and in 8-bit mode, all of the bits are used. Data is transmitted with the least significant bit first. A new character is transmitted when this field is written and has passed through the FIFO.	the CTS2 signal changed state and generates a maskable interrupt. The current state of the CTS2 signal is available on the CTS2 STAT bit. An immediate interrupt may be generated by setting this bit high. The CTS2 interrupt is cleared by writing 0 to this bit.	CTS2 Status (CTS2 Bit)—This bit indicates the current status of the CTS2 signal. A "snapshot" of the pin is taken immediately before this bit is presented to the data bus. While the NOCTS2 bit is high, this bit can serve as a general-purpose input.	<b>Busy (Tx Status)</b> —When this bit is high, it indicates that the transmitter is busy sending a character. This bit is asserted while the transmitter state machine is not idle or the FIFO has data in it.	Ignore CTS2 (Tx Control)—When this bit is high, it forces the CTS2 signal that is presented to the transmitter to always be asserted, which effectively ignores the external pin.	Send Break (Tx Control)—This bit forces the transmitter to immediately send continuous zeros, which creates a break character. See Section 14.3.1.2, "CTS Signal Operation," for a description of how to generate a break.	Transmit FIFO Has a Slot Available (FIFO Status)—This read-only bit indicates that the transmitter FIFO has at least one slot available for data. This bit generates a maskable interrupt.	FIFO Half (FIFO Status)—This read-only bit indicates that the transmitter FIFO is less than half full. This bit generates a maskable interrupt.	Description
	See description	0 = CTS2 signal did not change state since it was last cleared 1 = CTS2 signal has changed state	0 = CTS2 signal is low 1 = CTS2 signal is high	0 = Transmitter is not sending a character 1 = Transmitter is sending a character	0 = Transmit only while the CTS2 signal is asserted 1 = Ignore the CTS2 signal	0 = Normal transmission 1 = Send break (continuous zeros)	0 = Transmitter does not need data 1 = Transmitter needs data	0 = Transmitter FIFO is more than half full 1 = Transmitter FIFO is less than half full	Setting



### Programming Model

## Freescale Semiconductor, Inc.

### 14.4.12 **UART** 2 Miscellaneous Register

register are described in Table 14-14. position assignments for this register are shown in the following register display. The settings for this UART 2 module. Some bits, however, are only used for factory testing and should not be used. The bit The UART 2 miscellaneous (UMISC2) register contains miscellaneous bits to control test features of the

7 6	D II C II T	TYPE			UMISC2
	0	W	BA UD TES	BIT 15	8
	0	V	CLK SR C	14	
	0	W	FOR CE PER R	13	
	0	W	OP CP	12	UAR
	0	W	BAU D RES ET	11	JART 2 Miscellaneous Regist
	0	W	TES	10	/liscel
_	0			9	lane
000xC	0			8	noe
1	0	W	RTS 2 CO NT	7	s Rec
	0	₹	RT S2	6	jister
	0	₹	E D R	ъ	*
	0	V	RB P C	4	
	0	₹	RX PO L	ω	9
	0	8	TX PO L	2	(FF
	0			_	)FF
	0			BIT 0	FF)FFF918

Table 14-14. UART 2 Miscellaneous Register Description

		•
Name	Description	Setting
BAUD TEST Bit 15	Baud Rate Generator Testing—This bit puts the baud rate generator in test mode. The integer and non-integer prescalers, as well as the divider, are broken into 4-bit nibbles for testing. This bit should remain 0 for normal operation.	0 = Normal mode. 1 = Test mode.
CLKSRC Bit 14	Clock Source—This bit selects the source of the 1x bit clock for transmission and reception. When this bit is high, the bit clock is derived directly from the UCLK pin (it must be configured as an input). When it is low (normal), the bit clock is supplied by the baud rate generator. This bit allows high-speed	<ul><li>0 = Bit clock is generated by the baud rate generator.</li><li>1 = Bit clock is supplied by the UCLK pin.</li></ul>
	plied by the baud rate generator. This bit allows high-speed synchronous applications, in which a clock is provided by the external system.	
FORCE PERR Bit 13	Force Parity Error—When this bit is high, it forces the transmitter to generate parity errors, if parity is enabled. This bit is for system debugging.	0 = Generate normal parity. 1 = Generate inverted parity (error).
LOOP Bit 12	<b>Loopback</b> —This bit controls loopback for system testing purposes. When this bit is high, the receiver input is internally connected to the transmitter and ignores the RXD2 pin. The TXD2 pin is unaffected by this bit.	<ul><li>0 = Normal receiver operation.</li><li>1 = Internally connects the transmitter output to the receiver input.</li></ul>
BAUD RESET Bit 11	Baud Rate Generator Reset—This bit resets the baud rate generator counters.	0 = Normal operation. 1 = Reset baud counters.
IRTEST Bit 10	Infrared Testing—This bit connects the output of the IrDA circuitry to the TXD2 pin. This provides test visibility to the IrDA module.	0 = Normal operation. 1 = IrDA test mode.
Reserved Bits 9–8	Reserved	These bits are reserved and should be set to 0.

**UART 2 Miscellaneous Register Description (Continued)** 

	Reserved Bits 1–0	<b>TXPOL</b> Bit 2	RXPOL Bit 3	IRDA LOOP Bit 4	IRDAEN Bit 5	RTS2 Bit 6	RTS2 CONT Bit 7	Name
ARCHIVED BY FREESCALE SE	Reserved	<b>Transmit Polarity</b> —This bit controls the polarity of the transmitted data.	Receive Polarity—This bit controls the polarity of the received data.	<b>Loop Infrared</b> —This bit controls the loopback from the transmitter to the receiver in the IrDA interface. This bit is used for system testing purposes.	Infrared Enable—This bit enables the IrDA interface.	Request to Send Pin—This bit controls the RTS2 pin when the RTS2 CONT bit is 0.	RTS2 Control—This bit selects the function of the RTS2 pin.	Description
	These bits are reserved and should be set to 0.	0 = Normal polarity (1 = idle). 1 = Inverted polarity (0 = idle).	0 = Normal polarity (1 = idle). 1 = Inverted polarity (0 = idle).	<ul><li>0 = No infrared loop.</li><li>1 = Connect the infrared transmitter to an infrared receiver.</li></ul>	0 = Normal NRZ operation. 1 = IrDA operation.	$0 = \frac{\overline{RTS2}}{RTS2} \text{ pin is } 1.$ $1 = \overline{RTS2} \text{ pin is } 0.$	0 = RTS2 pin is controlled by the RTS2 bit.  1 = RTS2 pin is controlled by the receiver FIFO. When no more than four slots are available, RTS2 is negated.	Setting

### 14.4.13 **UART** 2 Non-Integer Prescaler Register

this register are described in Table 14-15. The UART 2 non-integer prescaler register (NIPR2) contains the control bits for the non-integer prescaler. The bit position assignments for this register are shown in the following register display. The settings for

### NIPR2 **BIT 15** SEL PRE 4 3 UART 2 Non-Integer Prescaler Register 12 10 SELECT 9 ω Ġι ω 0x(FF)FFF91A BIT 0

Table 14-15.
<b>UART 2</b>
Non-Integer
Prescale
r Register
Description

RESET

₹

0

0

0

0

0

0

6

0

0

0

0 ₹

₹

₹

0 ₹

0 ₹

0x0000

		STEP VALUE Bits 7-0	SELECT Bits 10–8	Reserved Bits 14–11	PRESEL Bit 15	Name
ARCHIVEDE	BYFR	Step Value—This field selects the non-integer prescaler's step value.	<b>Tap Selection</b> —This field selects a tap from the non-integer divider.	Reserved	Prescaler Selection—This bit selects the input to the baud rate generator divider. Refer to Figure 14-4 on page 14-7 for information about selecting the prescaler.	Description
	1111 1110. Step = 254. 1111 1111. Step = 255.	0000 0000. Step = 0. 0000 0001. Step = 1.	000 = Divide range is 2 to 3 127/128 in 1/128 steps. 001 = Divide range is 4 to 7 63/64 in 1/64 steps. 010 = Divide range is 8 to 15 31/32 in 1/32 steps. 011 = Divide range is 16 to 31 15/16 in 1/16 steps. 100 = Divide range is 32 to 63 7/8 in 1/8 steps. 101 = Divide range is 64 to 127 3/4 in 1/4 steps. 110 = Divide range is 128 to 255 1/2 in 1/2 steps. 111 = Disable the non-integer prescaler.	These bits are reserved and should be set to 0.	0 = Divider source is from the integer prescaler. 1 = Divider source is from the non-integer prescaler.	Setting

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### Freescale Semiconductor, Inc. **Programming Model**

# FIFO Level Marker Interrupt Register

reports a half-full condition. The bit position assignments for this register are shown in the following register display. The settings for this register are described in Table 14-16. The UART FIFO level marker register configures the level at which either the RxFIFO or the TxFIFO

-	C	Ó	Ó	d		Op	02 .	0x0102	C	Ć	Ć	Ć	ć	C	RESET
_	0	0	0	5	0	0	_	0	0	0	5	0	5	0	
w w	rw rw	8			//		₹	V	V	₹					TYPE
/EL MARKEI	RXFIFO LEVEL N	RXFI			V		(ER	. MARI	TXFIFO LEVEL MARKER	TXFIF					
1 BI	2	3	4	5	6	7	8	9	10	11	12	13	14	BIT 15	
FF)FFF91	×(FF	0		ल्	gist	t Re	rrup	Inte	arker	vel M	FIFO Level Marker Interrupt Register	끆		<b>X</b>	HMAR

# Table 14-16. FIFO Level Marker Interrupt Register Description

	RXFIFO LEVEL MARKER Bits 3-0	Reserved Bits 7–4	TXFIFO LEVEL MARKER Bits 11-8	Reserved Bits 15–12	Name
ARCHIVED BY FREES	<b>RxFIFO Level Marker</b> —This field defines the level at which the RxFIFO marker is set. When the RxFIFO status matches the level marker selected here, the RxFIFO half status bit is set and the RXFIFO HALF interrupt is generated if it is enabled.	Reserved	<b>TxFIFO Level Marker</b> —This field defines the level at which the TxFIFO marker is set. When the TxFIFO status matches the level marker selected here, the TxFIFO half status bit is set and the TXFIFO HALF interrupt is generated if it is enabled.	Reserved	Description
	See Table 14-17 on page 14-30 for settings.	These bits are reserved and should be set to 0.	See Table 14-17 on page 14-30 for settings.	These bits are reserved and should be set to 0.	Setting

FIFO Level Marker Settings

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1111	1110	1101	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001	0000	Tx FIFO Level Marker
>= 60	>= 56	>= 52	>= 48	>= 44	>= 40	>= 36	>= 32	>= 28	>= 24	>= 20	>= 16	>= 12	>= 8	>= 4	Disable	Number of Slots Empty
			2.E	M	//C	O,	Vi									

								- 11 /11								
1111	1110	1101	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001	0000	Rx FIFO Level Marker
>= 60	>= 56	>= 52	>= 48	>= 44	>= 40	>= 36	>= 32	>= 28	>= 24	>= 20	>= 16	>= 12	>= 8	>= 4	Disable	Number of Bytes Received

## Freescale Semiconductor, Inc.

### Pulse-Width Modulator 1 and 2 Chapter 15

convert digital data into analog waveforms. these modes, the PWM can be used to play back high-quality digital sounds, produce simple tones, or modulators has three modes of operation-This chapter describes the DragonBall VZ's two pulse-width modulators (PWMs). Each of the pulse-width -playback, tone, and digital-to-analog (D/A) conversion. Using

# Introduction to PWM Operation

external pin. The PWMO2 output is generated solely by PWM 2 and is brought to the PWMO2 external is generated by logically combining the output of both PWMs. The output is available at the PWMO1 pin. See Figure 15-1. PWM 1 uses 8-bit resolution, which is compatible with the MC68EZ328 (DragonBall EZ). PWM 2 uses 16-bit resolution, which is compatible with the MC68328 (the original DragonBall). The output PWMO1

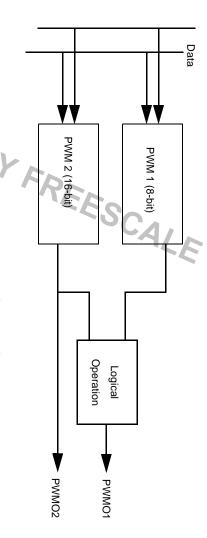


Figure 15-1. PWM 1 and PWM 2 System Configuration Diagram

programming the P[1:0] bits in the peripheral control register. See Section 5.2.2, "Peripheral Control The operation of the logical block combining the output of PWM 1 and PWM 2 is controlled by Register," on page 5-4 for details about the settings of these bits. ARCHI



## Freescale Semiconductor, Inc.

### 15.1.1 **PWM Clock Signals**

used by the pulse width modulator is made by the clock source (CLKSRC) bit in the PWM 1 control signal from one of two clock signals-Figure 15-2 shows a simplified block diagram of PWM 1. The prescaler and divider generate the PCLK -SYSCLK (the default) or CLK32. Selection of the source clock

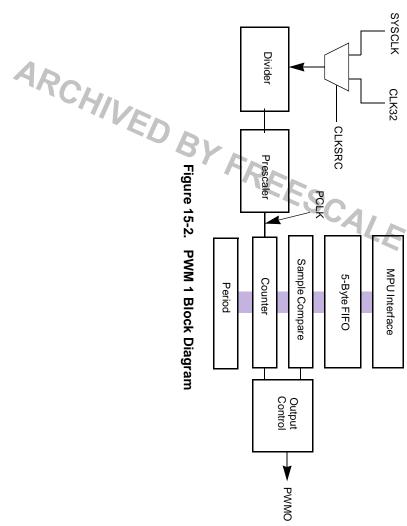
chain. The incoming clock source is divided by a binary value between 2 and 16. The CLKSEL (clock selection) field in the PWMC1 selects the frequency of the output of the divider

CLKSEL is equal to %11, divide by 16. In both cases, the following assumptions apply: For 16 kHz audio applications, CLKSEL is equal to %01, divide by 4. For DC-level applications

- SYSCLK = 16.58 MHz
- Prescaler = 0
- Period = default value

source by a factor from 1 to 128, respectively. the PWM 1 control register with any number between 0 and 127, which scales down the incoming clock 7-bit prescaler may be adjusted to achieve lower sampling rates by programming the prescaler field in

PWM 1 is an 8-bit PWM module that is optimized to generate high-quality sound from stored sample audio files. It can also generate simple or complex tones. It uses 8-bit resolution and a 5-byte FIFO to generate sound. Figure 15-2 illustrates the block diagram of the pulse-width modulator unit 1



**PWM 1 Block Diagram** 



### **PWM Operation**

The pulse-width modulator has three modes of operation—playback, tone, and D/A.

### 15.3.1 Playback Mode

sound for the best quality reproduction. through an external speaker. Although the PWM can reproduce the contents of a sound file, it is necessary to use a sampling frequency that is equal to or an even multiple of the one used to originally record the In playback mode, the pulse-width modulator uses the data from a sound file to output the resulting audio

counter continues counting, and when it overflows from 0xFF to 0x00, another sample period cycle begins is set to 1 and the counter begins counting up from 0x00. The sample value is compared on each count of the analog voltage of a particular audio sample. At the beginning of a sample period cycle, the PWMO pin PWM 1 produces variable-width pulses at a constant frequency. The width of the pulse is proportional to human-voice-quality sound, the sampling frequency is either 8 kHz or 16 kHz. The prescaler clock (PCLK) runs 256 times faster than the sampling rate when the PERIOD field of the the prescaler clock. When the sample and count values match, the PWMO signal is cleared to 0. The PWMP register is at its maximum value; for 16 kHz sampling, PCLK is 4.096 MHz. For

Figure 15-3 illustrates how variable-width pulses affect an audio waveform.



Figure 15-3. **Audio Waveform Generation** 

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently

are not available from Freescale for import or sale in the United States prior to September 2010; MC68VZ328 Product Family

Freescale Semiconductor, Inc.

used to play back 8 kHz sampled data while writing 4 bytes at each interrupt, interrupts occur every interrupt is generated when there are 1 or 0 bytes in the FIFO, in which case the software can write either four 1-byte samples or two 2-sample words into the FIFO. When a 16 kHz sampling frequency is being (big endian format) or as individual 8-bit bytes. A 5-byte FIFO minimizes interrupt overhead. A maskable Digital sample values can be loaded into the pulse-width modulator either as packed 2-sample 16-bit words

### **Tone Mode**

registers are programmed. The lowest frequency that can be generated is 0.25 Hz. In tone mode, the pulse-width modulator generates a continuous tone at a single frequency when the PWM

### D/A Mode

at the PWMO signal. It can be used to produce a different DC level when programmed using the sample fields in the PWMS1 register. When used in this manner, it becomes a D/A converter. The pulse-width modulator can output a frequency with a different pulse width if a low-pass filter is added

## 15.4 Programming Model

This section contains programming information about both PWM 1 and PWM 2

## 15.4.1 PWM 1 Control Register

settings are described in Table 15-1. PWM 1 FIFO. The register bit assignments are shown in the following register display. The register This register controls the operation of the pulse-width modulator, and it also contains the status of the

7 0 0	D II O II I	TYPE			PWMC
	0	۲W	CLKSRC	BIT 15	
	0	W			
	0	8		13	
	0	rw rw rw rw rw rw rw	PRE	14 13 12 11 1	
	0	₹	PRESCALER	11	P
	0	W	_ER	10	$\leq$
	0	₹		9	1 C
	0	8		8	ontr
0x002	0	8	IRQ	7	o R
Ö	0	W	IRQEN	6	PWM 1 Control Register
	_	V	FIFOAV EN	5	79
	0	V	EN	4	
	0	\$	REPEA	3	0
	0	\$	EAT	2	×(F
	0	W	CL	1	)FF
	0	W	.KSEL	BIT 0	FFF500

## able 15-1. PWM 1 Control Register Description

Name	Description	Setting
CLKSRC Bit 15	Clock Source—This bit is used to select the clock source to the pulse-width modulator.	0 = SYSCLK source is selected (default). 1 = CLK32 is selected.
	SE	<b>Note:</b> 32.768 kHz clock source is selected when using a 32.768 kHz crystal. If a 38.4 kHz
	4	crystal is used, 38.4 kHz is selected.
PRESCALER	Prescaler—This field is used to scale down	Any value between 0 and 127.
Bits 14-8	the incoming clock to divide by the	
	prescaler + 1. The prescaler is normally used to generate a low single-tone PWMO signal.	
	For voice modulation, these bits are set to 0	
	(divide by 1). The default value is 0.	
IRQ	Interrupt Request—This bit indicates that the	0 = The FIFO is not empty.
Bit 7	FIFO has one or no bytes remaining, which can be a signal of the need to fill the FIFO by	1 = The FIFO has one or no sample bytes remaining
	writing no more than two 16-bit words into the	,
	PWMS register. This bit automatically clears	
	an extra write cycle in the interrupt service rou-	
	tine. If the IRQEN bit is 0, this bit can be polled	
	This hit can be set to immediately nost a BWM.	
	interrupt for debugging purposes.	
IRQEN	Interrupt Request Enable—This bit controls	0 = The PWM interrupt is disabled (default).
Bit 6	the pulse-width modulator interrupt. While this bit is low, the interrupt is disabled.	1 = The PWM interrupt is enabled.

Table 15-1. **PWM 1 Control Register Description (Continued)** 

11 = Divide by 16. Provides an approximate 4 kHz sampling rate.
of the divider chain. The approximate sampling rates are calculated using a 16.58 MHz clock source (PRESCALER = 0 and PERIOD = default).
Clock Selection—This field selects the output
struct samples at 16 kHz by using the sample twice. This method shifts the carrier from an audible 8 kHz to a less sensitive 16 kHz frequency range, thus providing better sound-quality output.
during playback. To filter this carrier, a high-quality low-pass filter is required. For a higher playback rate, it is possible to recon-
and the data is played back at 8 kHz again, an 8 kHz humming noise (carrier) is generated
the use of a lower cost low-pass filter. For example, if the audio data is sampled at 8 kHz
head, thus reducing CPU loading when audio data is played back at a higher rate, and allows
The repeat feature reduces the interrupt over-
Sample Repeats—These write-only bits select
<b>Enable</b> —This bit enables or disables the pulse-width modulator. If this bit is not enabled, writing to other pulse-width modulator registers is ignored.
as long as this bit is set. If the FIFO is loaded while this bit is cleared, the write will be ignored.
FIFO Available—This bit indicates that the

\*When the pulse-width modulator is disabled, it is in low-power mode, the output pin is forced to 0, and the following

\*\*When the pulse-width modulator is enabled, it begins a new period, and the following events occur:

- The prescaler and counter are released and begin counting. The IRQ bit is set, thus indicating that the FIFO is empty.



running at the duty-cycle setting that was set last until the FIFO is reloaded or the pulse-width modulator is display. The register settings are described in Table 15-2. disabled. If the value in this register is higher than the PERIOD + 1, the output will never be reset, which they must be written to the low byte (SAMPLE1) only. The pulse-width modulator will revert to free register, they are automatically loaded into the FIFO in big-endian format. If 16-bit words are loaded, high byte is first placed into the 8-bit FIFO, and then low byte. When individual sample bytes are being written, This register serves as the input to the FIFO. When successive audio sample values are written to this

PWMS	BIT 15	₩ 14	₩ 13	PW 12 SAMPLEO	PWM 1 Sample Registe  11 10 9 8 7  IPLE0	√ Sar	mple 9	Reg 8	ister	₹	₹ 5	SAMPLE1	PLE1 3		)FFF5	**BIT 0
	BIT 15	14	13	12	=======================================	10	9	8	Q	6	51	4	ω	2	_	0 BIT
				SAMPI	LE0							SAM	PLE1			
TYPE	W	W	₹	V	V	W	₹	¥	W	₹	₹	₹	₹	₹	₹	V
D   C   C   C   C   C   C   C   C   C	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×
7 0 0							0xX	0xXXXX								

	SAMPLE1 Bits 7–0	SAMPLE0 Bits 15–8	Name
ARCHIVED BY FREESCA	<b>Sample 1</b> —This field represents the low byte of a two-sample word. This byte will be presented to the pulse-width modulator after the SAMPLE0 field. When used with single 8-bit samples, data must be written to this byte.	<b>Sample 0</b> —This field represents the high byte of a two-sample word. This byte is presented to the pulse-width modulator before the SAMPLE1 field.	Description
	None	None	Setting

Table 15-2.

**PWM 1 Sample Register Description** 

## Freescale Semiconductor, Inc.

**Programming Model** 

### 15.4.3 PWM 1 Period Register

counter is reset to start another period. Therefore, the following equation applies: This register controls the pulse-width modulator period. When the counter value matches PERIOD + 1, the

PWMO 
$$(Hz) = PCLK (Hz) / (PERIOD + 2)$$

Ean. 15-7

Writing 0xFF to this register achieves the same result as writing 0xFE.

in Table 15-3 The register bit assignments are shown in the following register display. The register settings are described

RESET			ВІТ 7	PWMP1
-	1 W		6	PWI
-	<b>-</b> ₹		5	M 1 Peri
0xFE	. W	PERIOD	4	PWM 1 Period Register
-	<b>-</b> ₹	U	ω	ē
_	1 W		2	
-	<u>,</u> ∧		_	0x(FF
c	> ₹		BIT 0	F)FFF504

Table 15-3. PWM 1 Period Register Description

Name	Description	Setting
PERIOD Bits 7–0	<b>Period</b> —This field represents the pulse-width modulator's period control value. None	None

## 15.4.4 PWM 1 Counter Register

The register bit assignments are shown in the following register display. The register settings are described This register contains the current count value and can be read at any time without disturbing the counter.

PWMCNT1		PWI	M 1 Cou	1 1 Counter Register	jister		0x(FF)	)FFF505
	BIT 7	0	σı	4	ω	2	_	BIT 0
		9		CC	COUNT			
TYPE	ſ	1/1	Г	r	ľ	r	r	r
D D D D D D D	0	0	0	0	0	0	0	0
7		By		Q	0x00			

Table 15-4. PWM 1 Counter Register Description

Name	Description	Setting
COUNT Bits 7-0	Count—This field represents the value of the current count.	None

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#### 15.5 PWM 2

PWM 2

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the pulse-width modulator unit 2. MC68328. Besides the difference in the PWM code size (8-bit versus 16-bit), the major difference between PWM 2 is a 16-bit PWM module that is compatible with the one used in the original DragonBall processor, PWM 2 and PWM 1 is that PWM 2 does not have a data FIFO. Figure 15-4 illustrates the block diagram of

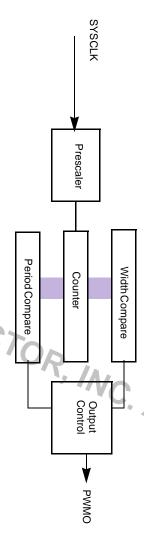


Figure 15-4. PWM 2 Block Diagram

## 15.5.1 PWM 2 Control Register

settings are described in Table 15-5. in this register. The register bit assignments are shown in the following register display. The register This register controls how the overall pulse-width modulator operates. Output pin status is also maintained

PWM(	32			_	M	126	or	VM 2 Control Register	egis	ster			0x	Ŧ	FF)FFF51	510
	BIT 15	14	3	12	<u> </u>	13 12 11 10 9	9	œ	7	6	Οī	4	ω	N	_	0 BIT
	PWMIRQ IRQEN	IRQEN				4		LOAD PIN	PIN		POL	PWMEN			CLKSEL	Г
TYPE	W	W				4		W	W		W	W		W	rw rw rw	W
D II O II O	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
, (					S			0x000C	8							

Table 15-5. PWM 2 Control Register Description

Name	Description	Setting
PWMIRQ	PWM Interrupt — This bit indicates that a period compare posted	0 = No PWM period rollover.
Bit 15	an interrupt. This bit may also be set to immediately post a PWM interrupt for debugging purposes. This bit is cleared after it is read while set. If the IRQEN bit is 0, this bit can be polled for the period comparator status.	1 = PWM period rolled over.
IRQEN Bit 14	Interrupt Enable—This bit enables the PWM interrupt.	0 = Disable PWM interrupt. 1 = Enable PWM interrupt.
Reserved Bits 13–9	Reserved	These bits are reserved and should be set to 0.
<b>LOAD</b> Bit 8	<b>Load New Setting</b> —This bit forces a new period value and width data to the registers. It automatically clears itself after the loading operation has been performed.	See description.

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Table 15-5. PWM 2 Control Register Description (Continued)

Name	Description	Setting
PIN Bit 7	<b>Pin Status Indicator</b> —This bit indicates the current status of the PWM.	0 = PWM output is high. 1 = PWM output is low.
Reserved Bit 6	Reserved	This bit is reserved and should be set to 0.
<b>POL</b> Bit 5	Output Polarity—This bit controls the PWM output polarity.	<ul><li>0 = Normal polarity.</li><li>1 = Inverted polarity.</li></ul>
PWMEN Bit 4	<b>PWM Enable</b> —This bit enables PWM 2.	0 = PWM 2 disabled. 1 = PWM 2 enabled.
Reserved Bit 3	Reserved	This bit is reserved and should be set to 0.
CLKSEL Bits 2-0	<b>Clock Selection</b> —These bits select the output of the divider chain.	000 = Divide by 4. 001 = Divide by 8.
	No	010 = Divide by 16. 011 = Divide by 32. 100 = Divide by 64.
		101 = Divide by 128.
	<sup>7</sup> /C	111 = Divide by 512.

### 15.5.2 PWM 2 Period Register

generated and the counter is reset to start another period. The register bit assignments are shown in the following register display. The register settings are described in Table 15-6. This register controls the period of PWM 2. When the counter value matches the value, an interrupt is

PWMP	Ŋ			_TJ	MM	M 2 Period Register	iod F	₹egi	ster				0 0	(FF	FF)FFF51	<del>-</del> 512
	ВІТ 15	14	13	12	11	10	9	8	7	6	5	4	з	2	1	ВІТ 0
							PERIOD	RIOD								
TYPE	W	W	W	MJ	W	W	WI WI WI WI WI WI WI WI WI	W	W	W	W	W	W	W	W	W
D II C II T	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
- -				3/			0x0000	000								
				3												

### Table 15-6. PWM 2 Period Register Description

Name	Description	Setting
PERIOD Bits 15–0	<b>Period</b> —This field represents the pulse-width modulator's period control value.	None

#### NOTE:

never go high. The pulse signal duty cycle will be 0 percent. There is an special case: when the register is set to \$00, the output will

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#### 15.5.3 **PWM 2 Pulse Width Register**

register display. The register settings are described in Table 15-7. This register controls the pulse width of PWM 2. The register bit assignments are shown in the following

7 0 1	DE CET	TYPE			Š
					Ž N
	0	V		BIT 15	2
	0	rw rw		14	
	0	₹		13	P
	0	₩		12	MM 2
	0	₩		13 12 11 10	PWM 2 Pulse Width Control Registe
	0	₩		10	e Widt
0x0	0	$\mathbb{Z}$	W	9	C H
0x0000	0	¥	WIDTH	8	ontr
DA	0	V		7	o R
	0	¥	/(	6	egis
	0	₹		5	<u>o</u>
	0	rw rw rw rw rw rw rw rw		4	
	0	V		3	<b>0</b>
	0	V		2	(FF
	0	V		1	)FFF
	0	V		BIT 0	((FF)FFF514

Table 15-7. **PWM 2 Pulse Width Control Register Description** 

Name	Description	Setting
WIDTH Bits 15-0	<b>Width</b> —When the counter matches the value in this register, the output is reset.	None

#### NOTE

never be reset. The resulting duty cycle is 100 percent. If PWMW2 is greater than the period register PWMP2, the output will

#### PWM 2 Counter Register

following register display. The register settings are described in Table 15-8. This register indicates the current counter value for PWM 2. The register bit assignments are shown in the

PWMCNT2	NT2			Pγ	$\leq$	12 C	nno;	ter F	M 2 Counter Register	ster				0x(F	<del>;</del> F	)x(FF)FFF516
	BIT 15 14 13 12	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT 0
								COUNT	JNT							
TYPE	W	W	W	WI WI WI WI WI WI WI WI WI WI WI	∀ `	W	W	W	W	W	W	W	W	W	W	W
D   C   C   C   C   C   C   C   C   C	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7 7 6				Y				0x0000	000							

Table 15-8. **PWM 2 Counter Register Description** 

	Name	Description	Setting
шО	COUNT Bits 15-0	Count—Indicates the current counter value.	None

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#### Chapter 16 In-Circuit Emulation

<sup>INC.</sup> 2005

designs using the MC68VZ328 microprocessor. Using four interface signals that are extended to external information about its operation and registers. The ICE module is designed to support low-cost emulator This chapter describes the in-circuit emulation (ICE) module of the MC68VZ328 and provides detailed in-circuit emulation module are as follows: pins, the ICE module has access to the 68000 CPU resources, with minimal restrictions. The features of the

- Dedicated chip-select for emulator debug monitor (using the EMUCS signal)
- Dedicated level 7 interrupt for in-circuit emulation
- or multiple hardware execution and bus breakpoints One address signal comparator and one control signal comparator with masking to support single
- One breakpoint instruction insertion unit

Figure 16-1 illustrates the block diagram of the in-circuit emulation module

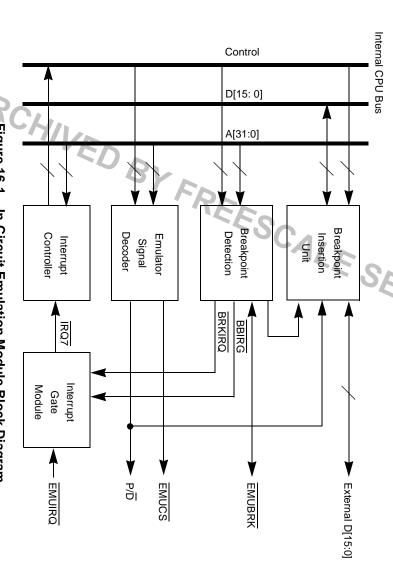


Figure 16-1. In-Circuit Emulation Module Block Diagram

The in-circuit emulation module's operation consists of the following tasks:

- Entering emulation mode
- Detecting breakpoints
- Using the signal decoder
- Using the interrupt gate module
- Using the A-line insertion unit

## **Entering Emulation Mode**

during system reset. After system reset, <u>EMUIRQ</u> becomes a falling edge trigger signal, which generates a level 7 interrupt when active. For emulation mode, the <u>CSAO</u> signal is not asserted for reset fetch, since it signal. To put the MC68VZ328 in emulation mode, the EMUIRQ signal must be driven low (externally) processor on reset vector fetch cycles. is in normal operation mode. The in-circuit emulation module internally generates a reset vector to the The in-circuit emulation module latches the state of the EMUIRO signal on the rising edge of the RESET IR, INC. 200,

monitor or boot code must start at 0xFFFC0020. The EMUCS signal is designed to cover system memory space from 0xFFFC0000 to 0xFFFCFFFF, and it is an 8-bit data bus width chip-select signal. If EMUIRQ another operation mode. is logic high during system reset, the in-circuit emulation module is disabled and the MC68VZ328 begins This hard-coded reset vector is PC = 0xFFFC0020 and SSP = 0xFFFCFFFC, which means that the

### **Detecting Breakpoints**

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masking, compares the hidden address signals. The EMUBRK signal, together with the internal compare is in multiple breakpoint mode, EMUBRK is an input that is asserted by the external address comparator result, generates the match signal to the breakpoint insertion unit. The external address comparator will compare the lower address while the internal comparator, with active time for this signal will vary, depending on the setting and width (wait state) of the bus cycle. The EMUBRK is an output, the generation of the EMUBRK signal is internally qualified by the AS signal. The When the in-circuit emulation module is configured to operate in single breakpoint mode, in which The execution breakpoint detector has one 32-bit address comparator and one control signal comparator. EMUBRK signal is asserted throughout the address matched cycle. When the in-circuit emulation module

reached, an exception vector fetch for an A-line exception will occur. At this point, EMUBRK is asserted execution breakpoint, the in-circuit emulation module inserts the 0xA0000 opcode at the location where a external to the core and will use the A-line instruction and level 7 interrupt. To accurately catch the Since the processor does not have built-in emulation support, the execution breakpoint is implemented to stop the process and switch control to the emulation monitor (selected by the EMUCS signal). the A-Line Insertion Unit." When the 0xA000 opcode is being executed, which means the breakpoint is breakpoint is set. For more information regarding the insertion mechanism, refer to Section 16.1.5, "Using

in emulation mode. However, normal memory reads to these two words will not cause an IRQ7 assertion. 0x28 and 0x2A. The A-line exception vector fetch will cause an IRQ7 assertion if a breakpoint is activated An exception vector fetch for an A-line exception consists of two consecutive word reads at addresses



# **Execution Breakpoints vs. Bus Breakpoints**

or read at a defined address location. To enter single bus breakpoint mode, bits, and then clear the PBEN and HMDIS bits. For multiple bus breakpoint mode, clear the SB bit. bus breakpoint is a breakpoint at which the current program execution stops when there is a memory write or read at a defined address location. To enter single bus breakpoint mode, set the SB, BBIEN, and CEN BBIEN and HMDIS bits in the same register. For multiple execution breakpoint mode, clear the SB bit. A PBEN, and CEN bits in the in-circuit emulation module control register (ICEMCR); and then clear the the monitor. To set up a single execution breakpoint, initialize the compare and mask registers; set the SB, An execution breakpoint is a breakpoint at which the current program execution stops and gives control to

## 16.1.3 Using the Signal Decoder

memory map is reserved for the emulator, and memory should not be assigned to this area. The port size of to the user. This monitor resides in the dedicated memory space 0xFFFC0000-0xFFFCFFFF (64K), which this monitor is 8-bit and the data bus is D[15:8]. is selected by the EMUCS signal with internal DTACK generation. In emulation mode, the respected The emulator requires a local resident debug monitor to be mapped at a specific location that is transparent

disassemble assembly code during trace (FC[2:0] = x01), and a 1 indicates a program access (FC[2:0] = x10). The emulator uses this signal to The  $P/\overline{D}$  signal indicates the characteristics of the current cycle. A 0 indicates a data access cycle

# 16.1.4 Using the Interrupt Gate Module

is generated, if it is enabled, when a program or bus breakpoint is hit. An external level 7 interrupt is directly connected to the EMUIRQ pin, which is a falling edge trigger signal. The level 7 interrupt vector is hard coded to 0xFFFC0010 if the HMDIS bit in the ICEMCR register is clear. If HMDIS is set, refer to Chapter 9, "Interrupt Controller," for information about generating a level 7 interrupt vector number. There are three level 7 interrupt sources: two are internal and one is external. An internal level 7 interrupt

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register (ICEMSR) to determine the source of the interrupt. Each of these interrupts can be cleared by the only source for level 7 interrupts. writing a 1 to the associated status bit. If the in-circuit emulation module is disabled, the EMUIRQ pin is When there is a level 7 interrupt, the software needs to check the in-circuit emulation module status

## 16.1.5 Using the A-Line Insertion Unit

level 7 interrupt is generated to the signal that a program breakpoint hits the in-circuit emulation module will wait for an A-line exception to occur. If an A-line exception occurs, a cycle when the address of this bus cycle matches the breakpoint address. When an A-line insertion occurs, The A-line insertion unit will physically replace the data bus contents with 0xA000 in an instruction fetch ARCHIVEL



### Programming Model

This section contains information about the ICE registers and programming information about their

#### In-Circuit Emulation Module Address **Mask Registers** Compare and

shown in the following register displays, and the settings of the bit assignments for both registers are compare the address bus value together with the control bus value to generate the EMUBRK signal. A described in Table 16-1 on page 16-5 comparator can take action if extra hardware breakpoints are needed. The register bit assignments are range can be set by using the address mask bits to break in a range of memory so that the external address corresponding address bit in the ICEMACR. The in-circuit emulation module's address comparator will breakpoint, and the in-circuit emulation module address mask register (ICEMAMR) is used to mask the The in-circuit emulation module address compare register (ICEMACR) is used to store the address of the



RESET

TYPE

0 ₹

0 ₹

0 4

0 ₹

0 ₹

0 ₹

0 ₹

0 ₹

0 ₹

0 4

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	BIT 30	CEMAMR	-	0 0	TYPE rw rw	AC1 AC 5 14	BIT 14 15		RESET 0 0	TYPE rw rw	AC3 AC 1 30	BIT 30	CEMACR
	29			0	W	AC1	13		0	W	AC2	29	ਨ
AM2	28	ICE N		0	ſW	AC1	12		0	W	AC2	28	CE Module Address Compare Register
AM2	27	CE Module Address Mask Register		0	ſW	AC1	11		0	W	AC2 7	27	dule /
AM2	26	e Add		0	W	AC1	10		0	W	AC2	26	∖ddre
<b>M</b> ≥	25	ress		0	W	AC 9	9		0	W	AC 25	25	ss C
M <sub>2</sub>	24	Ma	0x0	0	W	AC 8	8	OXO	0	W	AC 24	24	) mp
M <sub>2</sub> >	23	sk R	<u> </u>	0	W	AC 7	7		0	W	AC 23	23	oare
M <sub>2</sub> A	22	egis		0	W	AC 6	6		0	W	AC 22	22	Rec
M <sub>2</sub>	21	ter		0	W	AC 5	5		0	WJ	AC 21	21	jiste
M <sub>2</sub>	20			0	W	AC 4	4		0	W	AC 20	20	
5 ₹ ⊳	19	0×(F		0	W	AC 3	3		0	W	AC 19	19	0x(F
2 ≥	18	<del>ï</del>		0	۲W	AC 2	2		0	۲W	AC 18	18	÷)F
₁ <u>₹</u> ≽	17	뀪		0	W	AC 1	1		0	W	AC 17	17	Ŧ
AM1	ВІТ 16	0x(FF)FFFFFD04		0	ſW	AC0	віт о		0	W	AC16	BIT 16	0x(FF)FFFFFD00

Table 16-1. ICE Module Address Compare and Mask Registers Description

RESET

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0 ₹

0

0

0 AM 1

	<i>x</i>	
Name	Description	Setting
<b>ACx</b> Bits 31–0	Address Compare 31–0—These bits represent the value of the execution/bus breakpoint address. A match of address bits 31–0 with qualification of AS will generate a match signal.	See description.
<b>AMx</b> Bits 31–0	Address Wask 31–0—These bits mask the corresponding bits in the ACx field. With this masking scheme, a break can be made when the core is accessing a certain range of addresses.	<ul> <li>0 = The address is compared to the current address cycle.</li> <li>1 = Forces a true comparison ("don't care") on the corresponding bit.</li> </ul>

MOTOR

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<u>1</u>6-

BIT 0

#### **Programming Model**

### Freescale Semiconductor, Inc.

#### In-Circuit Emulation Module Control Compare and Mask Register

and will AND with the result from the address comparator and control comparator to generate the internal match signal. For program break mode, these two registers are "don't care." The register bit assignments EMUBRK signal in single breakpoint mode. In multiple breakpoint mode, EMUBRK is an input signal will compare the predefined control signals with the address compare match signal to generate the the corresponding control bit in the ICEMCMR. In bus breakpoint mode, the control signal comparator specific bus cycle, and the in-circuit emulation module control mask register (ICEMCMR) is used to mask bits are described in Table 16-2 and Table 16-3. The in-circuit emulation module control compare (ICEMCCR) register is used to set the breakpoint at a for both the compare and mask registers are shown in the following register displays. The settings for the

ICEMCCR	CR		$\overline{\square}$	ICE Module Control Compare Register	dule (	Contr	O C	omp	are	Rec	jiste	_	0×	(FF)	0x(FF)FFFFFD08	FD08
	BIT 15 14	14		13 12 11 10	11	10	9	9 8	7	6	5	5 4 3 2	3	2	1	BIT 0
								7							RW	PD
TYPE								)/							W	W
RESET	0	0	0	0	0	0	0	0 00000	0 0 0	0	0	0	0	0	0	0
							0	x0000								

Table 16-2. ICE Module Control Compare Register Description

Name	Description	Setting
Reserved Bits 15–2	Reserved	These bits are reserved and should be set to 0.
RW	Read or Write Cycle Selection—This bit is used to select the	0 = Write cycle breakpoint.
Bit 1	break at a read cycle or write cycle. When a break at a read cycle is selected, a breakpoint at the ROM location is possible.	1 = Read cycle breakpoint.
PD	Program or Data Cycle Selection—This bit is used to select the	0 = Data bus cycle.
Bit 0	break at a program cycle or data cycle.	1 = Instruction bus cycle.

ICEMCMR	ĬR			ō	CE Control Mask Register	ntrol	Mas	X Z	egis	ter			0×	(FF	)x(FF)FFFFFD0	FD0A
	BIT 15	14	13	12	1	10	9	9 8 7 6 5	7	6	5	4	4 3 2	2	_	BIT 0
															RWM	PDM
TYPE				<b>/</b>											W	W
D I C I T	0	0	0	0	0	0	0	0 0 0	0	0 0 0 0 0	0	0	0	0	0	0
7 0 1			D				0	0x0000								

Table 16-3. ICE Control Mask Register Description

Name	Description	Setting
Reserved Bits 15–2	Reserved	These bits are reserved and should be set to 0.

Table 16-3.

ICE Control Mask Register Description (Continued)

Description

-This

II II

Enable the comparator to compare itself against the RW bit. Force a true comparison ("don't care") on the corresponding

Setting

RWM Bit 1

#### PDM Bit 0 ARCHIVED BY FREESCALE SEMICONDUCTOR, IN Read or Write Cycle Mask bit masks the RW bit of the ICEMCCR. of the ICEMCCR Program or Data Cycle Mask—This bit masks the PD bit \_ 0 Enable the comparator to compare itself against the PD bit. Force a true comparison ("don't care") on the corresponding

#### **Programming Model**

## Freescale Semiconductor, Inc.

16.2.3 In-Circuit Emulation Module Control Register

module. The bit assignments for the ICE module control register are shown in the following register The in-circuit emulation module control register (ICEMCR) is used to control the in-circuit emulation

# display. The settings for the bits are described in Table 16-4.

7 7 0 1	BESET	TYPE			ICEMCR
	0			BIT 15 14 13 12 11 10 9 8	Ä
	0			14	
	0			13	
	0			12	
	0 0 0 0			11	CE
	0			10	Mo
	0			9	dul
	0			8	e C
_	0			7	òn
0x0000	0	W	SWEN	6	ICE Module Control Register
DA	0			5	gis
	0	rw	BBIEN	4	<b>20</b>
	0	W	HMDIS	3	0x
	0	₹	SB	2	Ê
	0	W	PBEN	1	)FFFFFD0(
	0	W	CEN	BIT 0	FD0C

#### Table 16-4. **ICE Module Control Register Description**

Name	Description	Setting
Reserved Bits 15-7	Reserved	These bits are reserved and should be set to 0.
SWEN Bit 6	<b>Software Enable EMU Module</b> —In normal mode, writing to this bit enables the breakpoint function.	<ul><li>0 = Disable breakpoint function.</li><li>1 = Enable breakpoint function.</li></ul>
Reserved Bit 5	Reserved	This bit is reserved and should be set to 0.
<b>BBIEN</b> Bit 4	Bus Break Interrupt Enable—When set, this bit enables the generation of a level 7 interrupt on a bus breakpoint.	<ul><li>0 = Disable level 7 interrupt generation on a bus breakpoint.</li><li>1 = Enable level 7 interrupt generation on a bus breakpoint.</li></ul>
HMDIS Bit 3	Hard-Map Disable—In emulation mode, this bit activates the internal hard-map operation. When this bit is clear, some memory locations are hard-coded to the specific values shown in Table 16-5 on page 16-9. If this bit is set or in normal mode, memory reads to these locations refer to the external memory.  Note: It is important to note that when writing to these locations, all writes are occurring to external memory. When the HMDIS bit is disabled, reads to these addresses are in word or long-word sizes.	See Table 16-5 on page 16-9.
SB Bit 2	Single BreakPoint—This bit controls the direction of the EMUBRK signal. In multiple breakpoint mode, the external address comparator will compare the lower address bits and the internal comparator will compare the higher address bits to generate a breakpoint matched signal.	0 = Configure the EMUBRK signal as an input (multiple breakpoint mode with external address compare for the lower addresses).  1 = Configure the EMUBRK signal as an output (single breakpoint based on the internal address compare register).
PBEN Bit 1	<b>Program Break Enable</b> —This bit is used to select a program or bus break.	0 = Select a bus break. 1 = Select a program break.

	lilided)
Description	Setting
Compare Enable—This bit is used to activate the comparison logic. It is recommended that the address compare and mask registers be programmed before setting this bit to valid.  O = Disable the breakpoint to valid.  1 = Enable the breakpoint comparison logic.	e the breakpoint parison logic. the breakpoint parison logic.

CEN Bit 0

Table 16-5. **Emulation Mode Hard Coded Memory Locations** 

ARCHIVED BY FREESCALE SE	(IRQ7 vector lower w	(IRQ7 vector upper w	0x2A	0x28	0x6	0x4	0x2	0x0	Address	
SE	ord) 0x0010	ord) 0xFFFC	0x0010	0xFFFC	0x0020	C	0xFFFC	OXFFFC	Hard Code	

# Typical Design Programm**ஈழ உடிக்கு ale Semiconductor, Inc.**

# 16.2.4 In-Circuit Emulation Module Status Register

settings for the bits are described in Table 16-6. The bit assignments for the ICE module status register are shown in the following register display. The The in-circuit emulation module status register (ICEMSR) is used to determine the source of an interrupt.

#### **ICEMSR** RESET **BIT 15** 0 4 0 0 0 ICE Module Status Register 0 6 0 9 0 ω 0 0 0x0000 0 0 0 EMUEN 0 BBIRQ 0 0x(FF)FFFFFD0E BRKIRQ 0 **EMIRQ** 0

## Table 16-6. ICE Module Status Register Description

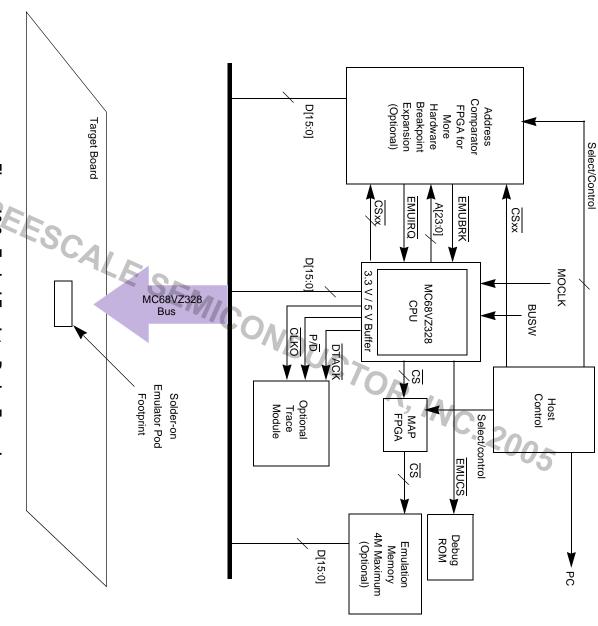
Name	Description	Setting
Reserved Bits 15–4	Reserved	These bits are reserved and should be set to 0.
EMUEN Bit 3	<b>Emulation Enable</b> —This bit, when set, enables ICE mode.	0 = Normal mode. 1 = ICE mode.
<b>BBIRQ</b> Bit 2	<b>Bus Break Interrupt Detected</b> —This bit is set when a bus breakpoint is hit. Writing a 1 to this bit clears it.	0 = Bus breakpoint has not occurred. 1 = Bus breakpoint has occurred.
BRKIRQ Bit 1	<b>Line Vector Fetch Detected</b> —This bit is set when a program breakpoint is hit. Writing a 1 to this bit clears it.	0 = Program breakpoint has not occurred. 1 = Program breakpoint has occurred.
EMIRQ Bit 0	EMUIRQ Falling Edge Detected—This bit is set when the EMUIRQ pin is going from high to low. Writing a 1 to this bit clears it.	See description.

#### Typical Design Programming Example

solder-on emulator pod. The entire MC68VZ328 bus should be buffered using level-shifting buffers when control to the PC or workstation via an RS-232 or a dedicated parallel interface, an optional address the emulator is designed in 5 V and the processor is running at 3.3 V bus MUX for hardware breakpoint insertion, and a MC68VZ328 pin-out extension to connect to the comparator for extra breakpoint expansion, optional map FPGA for emulation memory remapping, a data design that uses the MC68VZ328 as the processor to be emulated. Other functional units include the host Figure 16-2 on page 16-11 illustrates an example of a typical emulator design. It is a simple and low-cost ARCHI



# Freescale Semiconduçțe∦,⊳ba§n Programming Example



### Figure 16-2. Typical Emulator Design Example

#### 16.3.1 Host Interface

parallel I/O. The interface runs on the PC, and it will translate its requests to low-level commands and send activities between the emulation processor and the PC host. The interface can be an RS-232 or printer The host interface can be a processor-based or state-machine-based circuit that is used to coordinate the them to the emulator's controller if there is one.

# **Dedicated Debug Monitor Memory**

0xFFFC0000-0xFFFCFFFFF and is enabled or disabled by the  $\overline{EMUCS}$  signal. translated before it is passed to the interface on the PC. The monitor program is located in ROM at internal registers, in the system. This information is then transmitted to the host control processor to be When a breakpoint is matched, the CPU must report its status and grab the necessary contents, such as

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# Plug-in Emulator Design 底部內象Scale Semiconductor, Inc.

#### **Emulation Memory Mapping FPGA and Emulation** Memory

chip-select signals to map them to the emulation memory, instead of going directly to the target board downloaded to a shadowed RAM area for debugging purposes. The map FPGA will work with those memory that replaces the target memory for debugging at the initial stage. In some cases, ROM codes are Since the memory on the target board may not be fully built or debugged, it is necessary to have some

# 16.3.4 Optional Extra Hardware Breakpoint

upper hidden address line, and then a EMUIRQ signal is generated to tell the in-circuit emulation module external FPGA address comparator compares the lower address, the internal comparator compares the emulator. As discussed in Section 16.1.2, "Detecting Breakpoints," in multiple breakpoint mode the The FPGA address comparator can be added to enhance the number of hardware breakpoints in the to generate a breakpoint.

### 16.3.5 Optional Trace Module

signal to decide whether the trace capture is a program or data fetch. of all of the cycles, so that when a stop is encountered, the interface software can report all the cycle traces A trace module may also be added to enhance the function of the emulator. Trace captures the bus signals back for that breakpoint. This action is based on the timebase of the CLKO signal, P/D signal, and DTACK

#### Plug-in **Emulator Design** Example

Figure 16-3 on page 16-13 displays an example of a plug-in emulator design. The design is simple and low-cost, and it creates a very basic debugging environment. ARCHIVED BY FREES!



Figure 16-3. Plug-in Emulator Design Example

communicate with the PC without causing any problems. both RAM and ROM. The emulation module is buffered with 3.3 V to 5.0 V buffers so that it can generate chip-select signals to the UART (68HC681) or ADI interface and the debug RAM or ROM or Although there is only one hardware breakpoint in this design, all other software breakpoints can be generated by replacing the memory content of the A0 instruction. The EMUCS is decoded by a PAL to

system board for production testing, as well as diagnostic and failure analysis. built to ship with the software debugger package. These pins can remain on the production version of the The entire emulation module only uses 29 pins, including a ground signal. A very low-cost cable can be ARCHIVED BY FREE!



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# Application Development Fishescale Semiconductor, Inc.

#### **Application** Development Design Example

start-up designs and software development that occurs after the target hardware system is completed. Figure 16-4 displays an example of an application development system design. This example is for initial

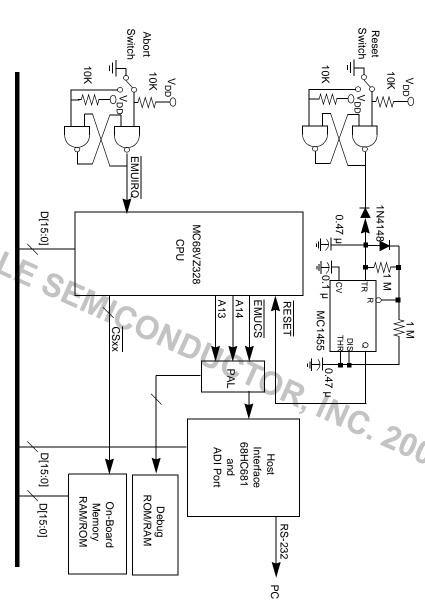


Figure 16-4. Application Development System Design Example

SRAM and ROM plug-in sockets for expansion. EMUIRQ signal. The RESET signal is EMUIRQ signal. The RESET signal is generated by the MC1455 monostable timer. The host interface port is selected by the PAL decoding the EMUCS, A13, and A14 signals. The board also provides optional There is one reset switch and one abort switch. The abort switch is debounced and connected to the ARCHIVED BY FI



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#### **Bootstrap Mode** Chapter 17

<sup>1</sup>NC. 2005

executed, providing a simple debugging environment for failure analysis and a channel to update programs stored in flash memory. The features of bootstrap mode are as follows: and programming the UART controllers. Once a program is downloaded to the MC68VZ328, it can be to download programs or data to the target system RAM using either the UART 1 or UART 2 controller. See Chapter 14, "Universal Asynchronous Receiver/Transmitter 1 and 2," for information on operating MC68VZ328. The bootstrap mode is designed to allow the initialization of a target system and the ability This chapter describes the operation and programming information of the bootstrap mode of the

- using UART 1 or UART 2 Allows system initialization and the ability to download both programs and data to system memory
- Accepts execution commands to run programs stored in system memory
- Provides a 32-byte instruction buffer for 68000 instruction storage and execution

## **Bootstrap Mode Operation**

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site (http://www.Motorola.com/DragonBall) to convert an S-record file to a bootstrap format file. or program requires the user convert the code to a bootstrap format file, which is a text file that contains bootstrap records. A DOS-executable program, STOB.EXE, can be downloaded from the DragonBall Web character can be any value and is not part of the program or data being downloaded. Downloading the data 38.4 kHz crystal, as well as to determine which UART port is being used for bootstrapping. The first character received is used to instruct the MC68VZ328 whether the PLL input clock is 32.768 kHz or parity, 8-bit character, and 1 stop bit, and then they are ready to accept bootstrap data download. The first In bootstrap mode, the MC68VZ328's UART 1 and UART 2 controllers are initialized to 19,200 baud, no

initialize the target system. Since internal registers are treated as a type of memory, each of them can be initialized by issuing a bootstrap record. Before a program is downloaded to system memory, the MC68VZ328's internal registers should be set to

0xFFFFC0. Whether initializing internal registers, downloading a program to system RAM, or issuing a disabled or the MC68VZ328 is operating in a CPU standalone system. The instruction buffer starts at core instruction, bootstrap mode will only accept bootstrap record transfers that are made using the UART downloaded. This feature enables the 68000 instructions to execute even if the memory systems are The record type determines what occurs. The bootstrap design provides a 32-byte instruction buffer to which 68000 instructions may be



# Bootstrap Mode Operation Freescale Semiconductor, Inc.

## 17.1.1 Entering Bootstrap Mode

of the CPU, and then the built-in bootstrap program runs and accepts data transfers. vector fetch timing. These two-long-word reset vectors are loaded to the stack pointer and program counter vectors are internally generated for reset vector fetch cycles. Figure 17-1 illustrates bootstrap mode reset MC68VZ328. Of the three modes, bootstrap has the highest priority. To enter bootstrap mode, the EMUBRK signal must be driven low and a system reset must be performed. After reset, bootstrap reset Bootstrap mode is one of the three operation modes (normal, emulation, and bootstrap) of the

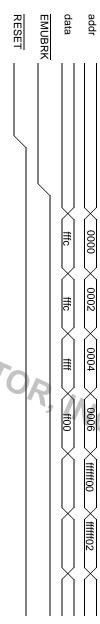


Figure 17-1. Bootstrap Mode Reset Timing

## 17.1.2 Bootstrap Record Format

Table 17-1. The two major attributes of b-records are that they are in uppercase and end with a carriage Bootstrap mode data transfers will only accept bootstrap records (b-records) whose format is shown in

Table 17-1. Bootstrap Record Format

4-Byte

#### 17.1.2.1 Data B-Record Format

be transferred. The data field contains the data to be transferred. transferred. The 4-byte address field indicates where the data will be stored, and this address could be any MC68VZ328 internal register location. The count field of the record contains the number of data bytes to There are two types of b-records that use the same format. The data b-record contains data to be

## 17.1.2.2 Execution B-Record Format

address field of the b-record. The count field for an execution b-record always contains 0x00, and no data is in the data field. The execution b-record tells the bootloader to run a program starting at the location specified by the

An execution b-record is used in two situations:

- execution. In this case, the address field of the b-record will be the start address of the program. After a program is downloaded to system RAM, issuing an execution b-record initiates program
- will be the start address of IBUFF. buffer space with nop--\$4e71, issuing an execution b-record executes the 68000 instruction that is stored in IBUFF and returns to bootloader mode. In this case, the address field of the b-record When loading a 68000 instruction into the instruction buffer and filling the remainder of the unused



# Freescale Semiconductor, Incotstrap Mode Operation

## 7.1.3 Setting Up the RS-232 Terminal

to ensure that each transferred ASCII character is echoed. To set up communication between your target system and the PC, set the communication specifications to 19,200 bps, no parity, 8-bit, and 1 stop bit. It is permissible to pause after each line (b-record) is transferred

character to the target system will initiate the link. The bootloader automatically determines which UART selected. Next, the bootloader adjusts the baud rate to match the 32.768 kHz or 38.400 kHz crystal by port is being used for bootstrap by sensing the receive FIFO in each UART. The first UART to have data is that the target system initially transmitted. as an acknowledgement. In addition, the bootloader echoes to the target system the same ASCII character reading the first received character. If the link is successful, the bootloader returns a unique character (@) After the hardware is set up, the system is powered up, and bootstrap mode is entered, sending any ASCII

#### NOTE:

character is echoed before bit 5 (TXD2) of the Port J select register is cleared. To re-enable the TXD2 pin in bootstrap mode, download the following b-record: "FFFFF43B01CF." The TXD2 pin of UART 2 is not enabled by default. Therefore, no

# **Changing the Speed of Communication**

uses a 32.768 kHz external crystal, the baud control register is initialized to 0x0126 after 19,200 bps is set 0x0126 to 0x0026 will switch the baud rate from 19,200 bps to 38,400 bps by issuing a b-record. After the up, assuming that the system clock is 16.58 MHz (the default). Changing the baud control register from described in Section 14.4.2, "UART 1 Baud Control Register," on page 14-12. For example, if the system terminal. Simply issue a b-record to reinitialize the band control register of the UART controller, which is last character of this b-record is sent (0), the echo of this last character will be in the new speed The communication baud rate may be changed after 19,200 bps is initially used to set up the RS-232 (38,400 bps). At this time, the host speed must immediately be adjusted to 38,400 bps.

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change the speed from 19,200 bps to 115,200 bps, follow these steps: Therefore, changing both bytes of the baud control register requires two steps, and each byte change must be issued at the standard communication speed for the host to set up new communication. For example, to The baud control register is a 2-byte register, and bootstrap mode data transfers are byte-sized write cycles.

- Issue the b-record "FFFFF9020100" to change the baud control register from 0x0126 to to synchronize with the target system. 0x0026, and the new speed changes to 38,400 bps. Next, change the host speed to 38,400 bps
- 5 final 115,200 bps speed, and readjust the host speed to 115,200 bps Issue another b-record to change the baud control register from 0x0026 to 0x0038 of the



# Bootstrap Mode Operation Freescale Semiconductor, Inc.

#### **System Initialization Programming** Example

internal registers. An init file can be built using a text editor. Example 17-1 is an initialization file for the MC68VZ328ADS board. Before downloading a program to system memory, the target system may need to be initialized using the

## Example 17-1. System Initialization Programming Example

```
FFFFFF102020000
FFFFFC00028F00
FFFFFC02029667
FFFFF106020200
FFFFFF11602029D
                      FFFFF112020091
                                                                       FFFFF000011C
                                                                                                               ********
                                                                                                  init.b
date: (
                                                                                                   04/20/98
                                                  disable
                                                       enable
                                                            enable
                                                                  Disable WD
                                                                       SCR init
                            CSB 0
                                       CSA
enable DRAM cs
            DRAM
                 DRAM
      CSD init
                                                                                                         ADS
           Control
                 Config
                                            level
                                                       chip
                                                             clko
                                                                                                         Ç
                                                  hardmap
                            256K
                                                                                                         default
                                                       select
      RAS0
                                            interrupt
      4M-6M,
                                                                                                         monitor
    RAS1 6M-8M
                                                                                                        config
      NDUCTOR, INC.
```

#### NOTE:

ARCHIVED BY FREESC, digit is received. Therefore, comments can be made in the b-record file as long as it contains no more than eight consecutive hexadecimal digits The bootloader starts receiving a new b-record when a nonhexadecimal



#### 17.1.6 **Application Programming Example**

Freescale Semiconductor, Incootstrap Mode Operation

assembly code is assembled and downloaded to system RAM. The code shown in Example 17-2 can be used to calculate a CRC value. The example demonstrates how

Example 17-2. **Application Programming Example** 

```
START:
                                                                                                     nextwd move.w
                                                                                                                   clr.
                      clr.l
add.l
       cmp.1 A0, 1 bpl.b lp2
                                           blt
clr.w
cmp.1
blt
                                                                                                                   പ്പ
dou
                            DO
                                                                               add.w
                                                                                       add.l
                                                                                             move.w
                                                                                                            clr.w
                     (A0)+,D0
                                                                       cmpi.w
                                                                                                                                  section
                                                                                                     (a0,d2),d6
               A0,A1
                                                                              d6,(a1)+
#2,d1
#2,d2
                                                nextwd
d2
d0,d1
                                                                                                                                  code
                                           nextwd
                                                                       #16,d2
                                                                                                                    ;d1
                                                                                                                    g
L
                                                                               Count;
                                                                                                             ;d2
                                                  Сору
                                                                                                                   used to
                                                                                                             ը.
ը.
                                                   the next word (nextwd)
                                                                                                            used
                                                                               the
                                                                 the whole
                                                                                                                   count the number of words copied
                                          whole
                                                                               number
                                                                                     number of
                                                                                                             Ç
                                                                                                            count
                                           sect
                                                                section
                                                                               of words
                                                                                       words
                                                                                                            the number
                                                                 has
                                           has
                                                                              copied
                                                                                      copied
                                           been
                                                                been copied
                                            copied
                                                                                                            words
                                                                                                            copied
```

After assembling and linking the program in Example 17-2, generate the following s-record file

```
$0030000FC
$1134000428142423C30200032C6548154420C4228
$113401000106DF04242B2806DEA4280D098B3C87D
$10940206AFA4E714E75B0
$9030000FC
```

Run the DOS program STOB.EXE to convert the preceding s-records to bootstrap format

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```
0000400010428142423C30200032C6548154420C42
000040101000106DF04242B2806DEA4280D098B3C8
00004020066AFA4E714E75
```

this b-record file will be loaded into system RAM, initialize the system by downloading an init b-record Download the preceding b-record file to the target system using the UART port in bootstrap mode. Since

where 00004000 is the start address of the program and the last two zeros identify the record as an execution b-record and not a data record To run the preceding program after it is downloaded to RAM, issue an execution b-record "0000400000"; To resume bootstrap mode operation after running a program, make the last instruction in the application

program a jmp \$FFFFFF5A to start receiving a new b-record

not implemented, the b-record can be terminated at any time by pressing the ENTER key. As long as Any b-record may be entered in a RS-232 terminal environment, but when a key is pressed, the character program execution b-record is not issued, the MC68VZ328 will remain in bootstrap mode produced by the keystroke is sent to the bootloader to be assembled. Although the backspace capability is



# Example of Instruction Buffer Usage

Example 17-3 demonstrates how to run a 68000 instruction using the instruction buffer.

Example
17-3.
Using I
Instruction
Butters

qon				ORG.L
end	nop	qon	move.w #\$55,D0	\$FFFFFC0
<sup>1</sup> NC		; fill the rest of IBUFF	<pre>; 4-byte long instruction(303C0055)</pre>	; instruction buffer location

FFFFFFC0 is the IBUFF address location): After the data is assembled and converted to b-record format, it appears as in the following lines (where

FFFFFFC00C303C00554E714E714E714E71 FFFFFFC000

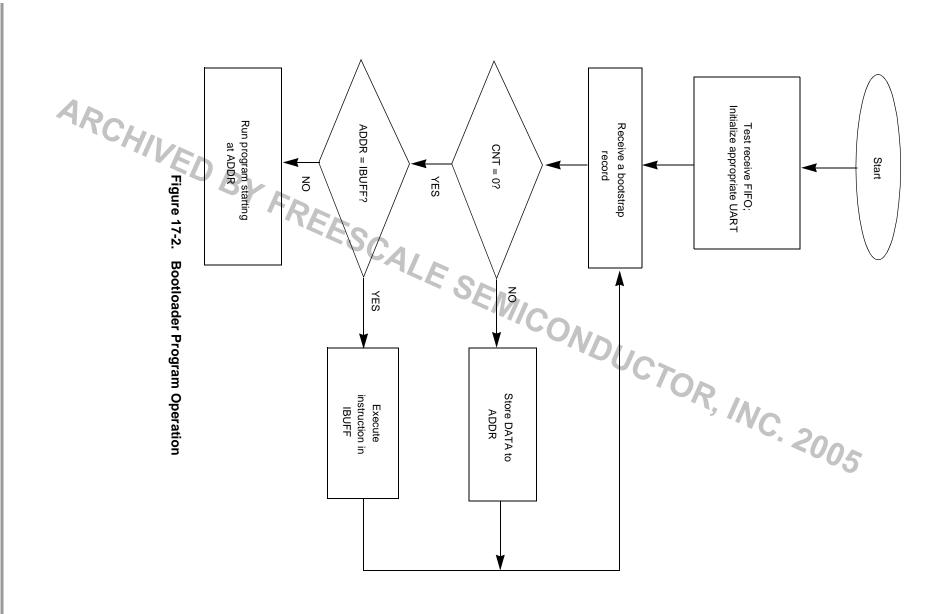
instruction in the instruction buffer. When the execution is complete, it accepts new b-record transfers. The the bootloader program. CPU registers D0–D6 and A0 are used by the bootloader program. Writing to these registers may corrupt The first b-record loads the instruction buffer. The second b-record tells the bootloader to run the

## Bootloader Flowchart

bootloader starts when the MC68VZ328 enters bootstrap mode The following flowchart illustrates how the bootloader program operates inside the MC68VZ328. The







#### Special Notes

The following information may be useful when the MC68VZ328 is in bootstrap mode

- A b-record is a string of uppercase hex characters with optional comments that follow.
- nine characters. However, the following characters can be used in a string of any length (all of these Comments in a b-record or b-record file must not contain any word or symbol that is longer than have an ASCII code value that is less than 0x30): SEMICONDUCTOR, INC.

  - ! (exclamation point)
  - (quotation mark)
  - # (number sign)
  - \$ (dollar sign)
  - % (percentage symbol)
  - & (ampersand)
  - (opening parenthesis)
  - (closing parenthesis)
  - \* (asterisk)
  - + (plus sign)
  - (minus sign)
  - (period)
  - / (forward slash)

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- a b-record (ASCII code value < 0x30) will force the bootloader to start a new b-record value greater than or equal to 0x30 are kept for b-record assembling. Sending a character that is not The bootloader program echoes all characters being received, but only those having an ASCII code
- corrupt the bootloader program. The D[6:0] and A0 registers are used by the bootloader program. Writing to these registers may
- Visit the DragonBall Web site at http://www.Motorola.com/DragonBall for bootstrap utility ARCHIVED BY FREI



## Freescale Semiconductor, Inc.

#### Application Guide Chapter 18

<sup>1</sup>NC. 2005

existing designs. It includes a design checklist and instructions for using the MC68VZ328 Application Development System (ADS) board to get the design process started as quickly as possible. This chapter contains helpful information that will assist with integrating the MC68VZ328 into new or

#### Design Checklist

during debugging or in the process of operating actual designs. used as guides during the design process. These guidelines are the result of issues that frequently occurred When the MC68VZ328 microprocessor is being integrated into an application, the following items can be

# **Determining the Chip ID and Version**

is necessary for obtaining the correct errata information for that version of the chip, ensuring more efficient example, with the number 0F98S, 0 is the revision number and F98S is the mask number. This information number for that particular chip. The mask number and the revision number are combined into one. For numbers. If Web access is not available, contact the local Motorola sales office product design. Once the mask and revision numbers are known, go to the DragonBall Web site (http://www.Motorola.com/DragonBall) and look for any MC68VZ328 chip errata pertaining to those Each chip has different sets of numbers etched onto it, and one of these sets is the mask and revision

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### 8-Bit Bus Width Issues

chip-select A control register. See Section 6.3.3, "Chip-Select Registers," on page 6-8 for more details. chip-select group A, which carries the boot chip select signal CSA0 and is normally connected to boot the PLLCR register is cleared). programmed to the PG0 function before the system clock is configured to divide by one (the PRESC bit in bus cycle and provides ample access time to memories. Therefore, BUSW/DTACK/PG0 should be is divided by two (the PRESC bit in the PLLCR register is set) after reset, which doubles the length of each cycles to a zero wait state until this pin is reconfigured to the PG0 function. Fortunately, the system clock to the DTACK function. This signal should be permanently driven low for an 8-bit system to force all bus Also, after reset, the BUSW/DTACK/PG0 pin can be selected as a DTACK or PG0 function, but it defaults by the rising edge of the RESET signal, and the latched BUSW status is indicated by the BSW bit of the boot ROM system, BUSW must be externally driven low during system reset. The BUSW status is latched for the  $\overline{\text{CSA0}}$  and  $\overline{\text{CSA1}}$  signals is only controlled by the BUSW/DTACK/PG0 signal. For a system with ROM, all the chip select signals are programmable to 8-bit or 16-bit mode after reset. The data bus width To ensure maximum flexibility, the MC68VZ328 supports both 8- and 16-bit data bus modes. Except the 16-bit data boot ROM, BUSW is pulled high or left unconnected during system reset. For an 8-bit data



# 18.1.3 Clock and Layout Considerations

during the initial power up. This section covers layout considerations affecting DragonBall timing issues during operation and also

- close to the chip as possible. Place the crystal within 0.5 inches of the MC68VZ328. The crystal and the capacitors must be as
- 250 ms power-up reset pulse is required. can be used. Since the internal module takes time to complete the reset operation, a minimum MC68VZ328. The RESET pin is a Schmitt trigger input signal. A simple power-up RC reset circuit If an RC reset circuit is being used, place the resistor and capacitor within 0.5 inches of the
- the power stability and enhance the noise immunity of the system. Use multiple power and ground planes. It is strongly recommended to use at least one ground plane, one 3.3 V  $V_{DD}$  plane, and one 5 V  $V_{SS}$  plane (if 5 V parts exist in the system). This helps improve

## 18.1.4 Bus and I/O Considerations

Several of the items that are warned against in this section appear to be good design practice. However, experience has demonstrated that not heeding the following suggestions can lead to problems.

- floating. Unused inputs can be tied directly to  $V_{SS}$  or  $V_{DD}$  or through pull-ups or pull-downs to  $V_{SS}$ Do not leave unused input pins floating. Unused inputs should be tied high or low, but not left
- pull-up enabled or as an output with pull-up disabled to reduce power consumption. Use the port pins efficiently. When port pins are not used, they should be configured as inputs with
- internal pull-up resistor can be used to pull up the RXD input signal. function. For instance, when using the RXD/PE4 signal and the RXD function, the associated The internal pull-up or pull-down resistors apply to both the dedicated function and the general I/O Apply internal pull-ups to dedicated function pins. Many pins are mixed with a dedicated function.

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- 1 megaohm, but their deviation is large. Do not rely solely on the value of internal pull-up resistors. The internal resistors are nominally
- design for system debugging and flash memory updating and TXD signals of the UART port, so it is recommended that a UART port be included in the and perform simple hardware debugging functions. However, bootstrap mode only uses the RXD and a bootstrap utility program that can be used to download programs and data to a target system Always provide a development interface port on your design. The MC68VZ328 has bootstrap mode





## Freescale Semiconductor, Inc.

Electrical Characteristics

This chapter documents electrical characteristics and providetailed information about host Section 19.3. "A C T Section 19.3. "A This chapter documents electrical characteristics and provides timing information necessary to design systems using the MC68VZ328 microprocessor. Section 19.2, "DC Electrical Characteristics," provides signal skew times. It also contains timing information for working with RAM, DRAM, and other Section 19.3, "AC Electrical Characteristics," consists of output delays, input setup and hold times, and detailed information about both maximum and minimum DC characteristics of the MC68VZ328. memory-related modules and peripherals.

Table 19-1. Maximum Ratings

ARCHIVED BY FR	Storage temperature	Maximum operating temperature range	Input voltage	Supply voltage	Rating	19.1 Maximum Ratings  Table 19-1 provides information on maximum ratings.  Table 19-1. Maximum Ratings
	Test	T <sub>A</sub>	V <sub>IN</sub>	V <sub>DD</sub>	Symbol	atings maximum ratings. Table 19-1. Maximum Ratings
	-55 to 150	$T_L$ to $T_H$ 0 to 70	-0.3 to 7.0	-0.3 to 7.0	Value	Ratings
	°C	°C	<b>~</b>	<	Unit	

# AC Electrical Characteristiffeescale Semiconductor, Inc.

# **Electrical Characteristics**

Table 19-2 contains both maximum and minimum DC characteristics of the MC68VZ328

Table 19-2. **Maximum and Minimum DC Characteristics** 

<del>1</del> 5	İ	I	Output leakage current $(V_{out} = V_{DD}, output is three-stated)$	loz
-4.0	I	I	Output low current $(V_{OL} = 0.4V, V_{DD} = 2.9 V)$	lor
I	I	4.0	Output high current (V <sub>OH</sub> = 0.8 V <sub>DD</sub> , V <sub>DD</sub> = 2.9 V)	lон
<u> </u>	I	I	Input high leakage current (V <sub>IN</sub> = V <sub>DD</sub> , no pull-up or pull-down)	Ī
<u>+</u>	I	ı	Input low leakage current (V <sub>IN</sub> = GND, no pull-up or pull-down)	Ē
0.4		<b>V</b> O –	Output low voltage (I <sub>OL</sub> = -2.5 mA)	V <sub>OL</sub>
I		$0.7V_{DD}$	Output high voltage (I <sub>OH</sub> = 2.0 mA)	V <sub>OH</sub>
0.4			Input low voltage	۷۱۲
I	l	0.7 V <sub>DD</sub>	Input high voltage	۲II
60	35		Standby current <sup>1</sup>	2
40	20	    /\	Full running operating current at 33 MHz	1
Maximum	Typical	Minimum		Symbol
	(3.0 ± 0.3) V		Characteristic	Number or

<sup>1.</sup>Standby current is measured only when the real-time clock is running

#### 9.3 **Electrical Characteristics**

at an operating frequency from 0 MHz to 33 MHz with an operating supply voltage from  $V_{DD\,max}$  under an operating temperature from  $T_L$  to  $T_H$ . All timing is measured at 95 pF loading. signals are specified relative to an appropriate edge of other signals. All timing specifications are specified The AC characteristics consist of output delays, input setup and hold times, and signal skew times. All

#### 19.3.1 CLKO Reference to Chip-Select Signals Timing

signals, see Chapter 6, "Chip-Select Logic." measure for this figure are found in Table 19-3 on page 19-3. For detailed information about the individual Figure 19-1 on page 19-3 compares the chip-select signal time referenced with the CLKO signal. Note that WS is the number of wait states in the current memory access cycle. The signal values and units of



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# Freescale Semiconductor,概要ectrical Characteristics

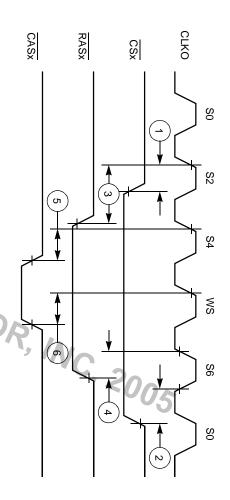


Figure 19-1. **CLKO Reference to Chip-Select Signals Timing Diagram** 

Table 19-3.

**CLKO Reference to Chip-Select Signals Timing Parameters** 

Number 0 Ŋ ω N CLKO high to CASx negated CLKO high to CASx asserted CLKO high to RASx negated CLKO high to RASx asserted CLKO low to CSx negated CLKO high to CSx asserted Characteristic Minimum  $(3.0 \pm 0.3) V$ Maximum 12 12 10 12 10 10 Unit S su sn sn sn SU

## 19.3.2 Chip-Select Read Cycle Timing

signals, see Chapter 6, "Chip-Select Logic." measure for this figure are found in Table 19-4 on page 19-4. For detailed information about the individual Figure 19-2 on page 19-4 shows the read cycle timing used by chip-select. The signal values and units of



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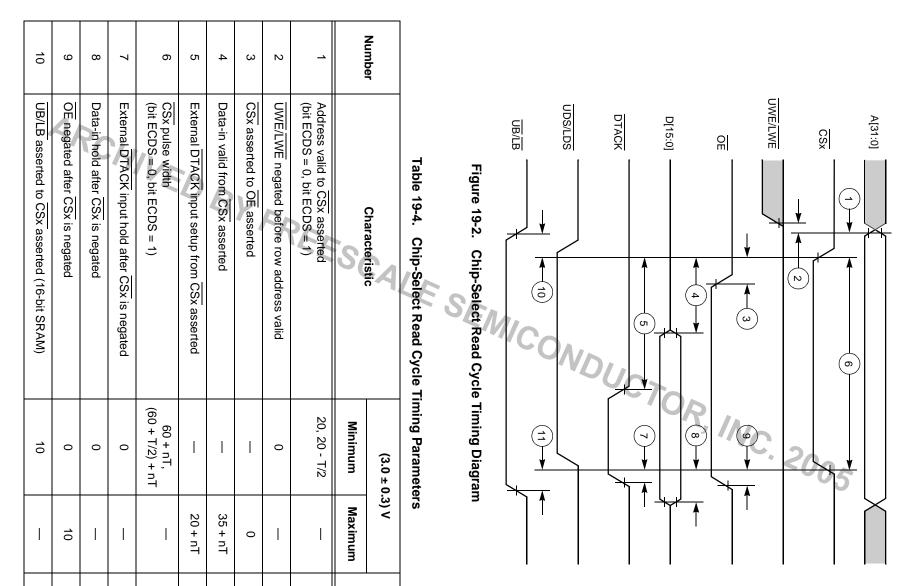
S

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Unit

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Table 19-4. Chip-Select Read Cycle Timing Parameters (Continued)

Nimbor	Characteristic	(3.0 ± 0.3) V	3) V	- - -
	Characteristic	Minimum	Maximum	Ç
11	CSx negated to UB/LB negated (16-bit SRAM)	70	I	ns
Note:	Note:			

n is the system clock period.

Tis the system clock period.

The external DTACK input requirement is eliminated when CSx is programmed to use internal DTACK.

CSx stands for CSA0, CSA1, CSB0, CSB1, CSC0, CSC1, CSD0, or CSD1.

A value in parentheses is used when early cycle detection is turned on.

#### 19.3.3 Chip-Select Write Cycle Timing

this figure are found in Table 19-5 on page 19-6. For detailed information about the individual signals, see Figure 19-3 shows the write cycle timing used by chip-select. The signal values and units of measure for "Chip-Select Logic."

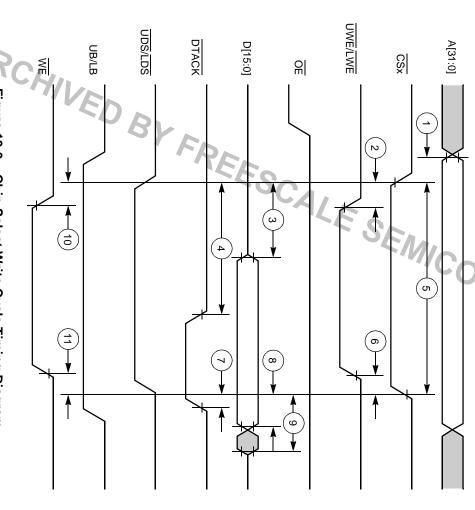


Figure 19-3. **Chip-Select Write Cycle Timing Diagram** 

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Table 19-5. **Chip-Select Write Cycle Timing Parameters** 

Nimber	Characteristic	$(3.0 \pm 0.3)  \text{V}$	.3) V	= =
Mailiba	Cital actalistic	Minimum	Maximum	Ç
_	Address valid to CSx asserted (bit ECDS = 0, bit ECDS = 1)	20, 20 <b>-</b> T/2	I	ns
2	CSx asserted to UWE/LWE asserted	6	4	ns
3	CSx asserted to data-out valid	<b>/</b> /	30	ns
4	External DTACK input setup from CSx asserted	<b>P</b> , –	20 + nT	su
σ	CSx pulse width (bit ECDS = 0, bit ECDS = 1)	60 + nT, (60 + T/2) + nT	I	ns
6	UWE/LWE negated before CSx is negated	10	20	ns
7	External DTACK input hold after CSx is negated	0	I	ns
8	Data-out hold after CSx is negated	8	1	ns
9	CSx negated to data-out in Hi-Z	I	18	su
10	CSx asserted to WE asserted (16-bit SRAM)	0	4	ns
11	WE negated before CSx is negated (16-bit SRAM)	10	20	ns
Note: n is the num	<b>Note</b> :  n is the number of wait-states in the current memory access cycle.			

T is the system clock period.

The external DTACK input requirement is eliminated when CSx is process stands for CSA0, CSA1, CSB0, CSB1, CSC0, CSC1, CSD0, or programmed to use the internal DTACK or CSD1.

A value in parentheses is used when early detection is turned on.

# 19.3.4 Chip-Select Flash Write Cycle Timing

individual signals, see Chapter 6, "Chip-Select Logic." units of measure for this figure are found in Table 19-6 on page 19-7. For detailed information about the Figure 19-4 on page 19-7 shows the flash write cycle timing used by chip-select. The signal values and



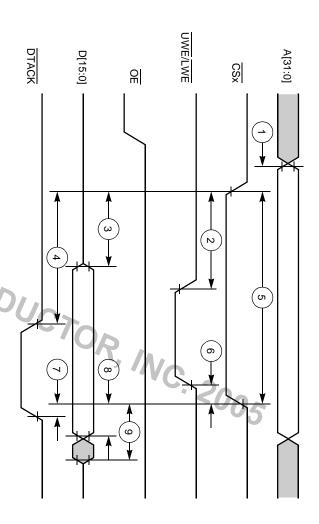


Figure 19-4. Chip-Select Flash Write Cycle Timing Diagram

Table 19-6. Chip-Select Flash Write Cycle Timing Parameters

Characteristic	(3.0 ± 0	.3) V	= 5 <del>*</del>
Silal acteriance	Minimum	Maximum	Ş
Address valid to $\overline{CSx}$ asserted (bit ECDS = 0, bit ECDS = 1)	20, 20 - T/2	I	ns
CSx asserted to UWE/LWE asserted	20	40	ns
CSx asserted to data-out valid	I	30	ns
External DTACK input setup from CSx asserted	1	20 + nT	ns
$\overline{\text{CSx}}$ pulse width (bit ECDS = 0, bit ECDS = 1)	60 + nT, (60 + T/2) + nT	I	ns
UWE/LWE negated before CSx is negated	10	20	ns
External DTACK input hold after CSx is negated	0	I	ns
Data-out hold after CSx is negated	8	1	ns
CSx negated to data-out in Hi-Z	I	18	ns
ber of wait states in the current memory access cycle.  em clock period.  I DTACK input requirement is eliminated when CSx is profor CSA0, CSA1, CSB0, CSB1, CSC0, CSC1, CSD0, or C	grammed to use th	ne internal DTAC	SK.
	Number  Characteristic  Address valid to CSx asserted (bit ECDS = 0, bit ECDS = 1)  CSx asserted to UWE/LWE asserted  External DTACK input setup from CSx asserted  External DTACK input setup from CSx asserted  WWE/LWE negated before CSx is negated  External DTACK input hold after CSx is negated  Rote:  Bata-out hold after CSx is negated  Bata-out hold after CSx is negated  Bata-out hold after CSx is negated  Rote:  Note:  Is the system clock period.  The external DTACK input requirement is eliminated when CSx is process to control CSA0, CSB1, CSB1, CSB1, CSD1, CSC1, CSD0, or CSX stands for CSA0, CSA1, CSB0, CSB1, CSC1, CSD0, or CSX is processed to the control co	Number         Characteristic         Minimum           1         Address valid to CSx asserted (bit ECDS = 0, bit ECDS = 1)         20, 20 - 1/2 (bit ECDS = 0, bit ECDS = 1)           2         CSx asserted to UWE/LWE asserted         20, 20 - 1/2 (bit ECDS = 1)           3         CSx pulse width (bit ECDS = 0, bit ECDS = 1)         —           4         External DTACK input setup from CSx asserted         —           5         CSx pulse width (bit ECDS = 1)         (60 + nT, (60 + T/2) + nT (60 + T/2) + nT (60 + T/2) + nT           6         UWE/LWE negated before CSx is negated         10           7         External DTACK input hold after CSx is negated         0           8         Data-out hold after CSx is negated         0           9         CSx negated to data-out in Hi-Z         —           10         8           9         CSx negated to data-out in Hi-Z         —           10         8           9         CSx negated to data-out in Hi-Z         —           10         8           9         CSx negated to data-out in Hi-Z         —           10         —           10         —           10         —           10         —           10         — <tr< td=""><td>(3.0 ± 0.3)    Minimum   20, 20 - T/2   20, 20 - T/2     60 + nT, (60 + T/2) + nT   10   0   8   8   Frogrammed to use the or CSD1.</td></tr<>	(3.0 ± 0.3)    Minimum   20, 20 - T/2   20, 20 - T/2     60 + nT, (60 + T/2) + nT   10   0   8   8   Frogrammed to use the or CSD1.

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## 19.3.5 Chip-Select Timing Trim

measure for this figure are found in Table 19-7. For detailed information about the individual signals, see Chapter 6, "Chip-Select Logic." Figure 19-5 shows the timing diagram for the chip-select timing trim. The signal values and units of

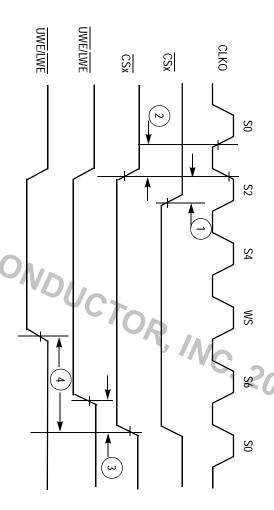


Figure 19-5. Chip-Select Timing Trim Timing Diagram

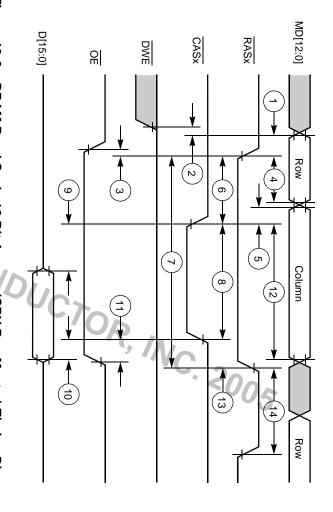
Table 19-7. Chip-Select Timing Trim Timing Parameters

Number	Characteristic	$(3.0 \pm 0.3) \text{ V}$	0.3) V	Uni <del>i</del>
2	4	Minimum	Maximum	
_	CLKO high to CSx asserted (bit ECDS = 0)	I	10	ns
2	CLKO low to $\overline{\text{CSx}}$ asserted (bit ECDS = 1)	I	10	ns
3	$\overline{\text{UWE}/\text{LWE}}$ negated before $\overline{\text{CSx}}$ is negated (bit WPEXT = 0)	10	20	ns
4	$\overline{\text{UWE/LWE}}$ negated before $\overline{\text{CSx}}$ is negated (bit WPEXT = 1)	40	50	ns

#### 19.3.6 **DRAM Read Cycle 16-Bit Access** (CPU Bus Master)

information about the operation of individual signals can be found in Chapter 7, "DRAM Controller," and The signal values and units of measure for this figure are found in Table 19-8 on page 19-9. Detailed Figure 19-6 on page 19-9 shows the DRAM read cycle timing diagram for 16-bit access (CPU bus master). Chapter 6, "Chip-Select Logic."





DRAM Read Cycle 16-Bit Access (CPU Bus Master) Timing Diagram

Table 19-8.

DRAM Read Cycle 16-Bit Access (CPU Bus Master) Timing Parameters

Number	Characteristic	(3.	(3.0 ± 0.3) V
	, (	Minimum	Maximum
_	Row address valid to RASx asserted	40	1
2	DWE negated before row address valid	0	1
3	OE asserted before RASx is asserted	0	1
4	$\overline{RASx}$ asserted before row address invalid (MSW = 0,1)	12,27	I
5	Column address valid to CASx asserted (MSW = 0,1)	10,25	I
6	$\overline{RASx}$ asserted to $\overline{CASx}$ asserted (MSW = 0,1)	28,58	32
7	$\overline{RASx}$ pulse width (SLW = 0,1)	90,120	I
8	CASx pulse width (BC[1:0] = 00,01,10,11)	28,58,88,118	I
9	CASx asserted to data-in valid (BC[1:0] = 00,01,10,11 for FPM)	I	15,45,75,105 (FPM) 20 (EDO)
10	Data-in hold after CASx is negated	0 (FPM) 30 (EDO)	I
1	OE negated after CASx is negated	0 (FPM) 30 (EDO)	35

Table 19-8. DRAM Read Cycle 16-Bit Access (CPU Bus Master) Timing Parameters (Continued)

Number	Characteristic	(3.0	$(3.0 \pm 0.3) \text{ V}$	llnit
	Gran actor is no	Minimum	Maximum	Ollik
12	CASx asserted before column address invalid	50	- -	su
13	RASx negated after CASx is negated	28	-	ns
14	RASx precharge time (SLW= 0,1)	58,118		ns
 Note: RASx	Note: RASx stands for RAS0 and RAS1. CASx stands for CAS0 and CAS1.	AS0 and CAS1.		

**Note:** MSW is bit 5, SLW is bit 3, and BC[1:0] comprises bits 13–12 in the DRAMC register. When the table identifies these bits, the sequence of their listed values corresponds to the sequence of timing data provided.

### 19.3.7 DRAM Write Cycle 16-Bit Access (CPU Bus Master)

values and units of measure for this figure are found in Table 19-9 on page 19-11. Detailed information about the operation of individual signals can be found in Chapter 7, "DRAM Controller," and Chapter 6, Figure 19-7 shows the DRAM write cycle timing diagram for 16-bit access (CPU bus master). The signal "Chip-Select Logic."

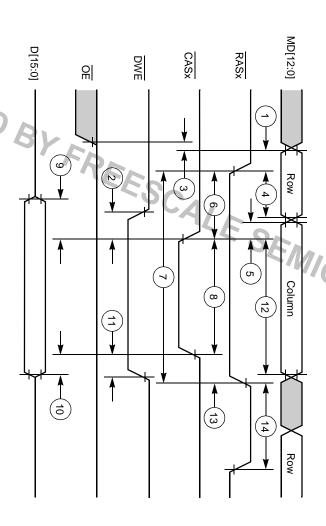


Figure 19-7. DRAM Write Cycle 16-Bit Access (CPU Bus Master) Timing Diagram

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Table 19-9. DRAM Write Cycle 16-Bit Access (CPU Bus Master) Timing Parameters

		$(3.0 \pm 0.3) \text{ V}$	0.3) V	
Number	Characteristic	Minimum	Maximum	Onic
<b>-</b>	Row address valid to RASx asserted	<sup>40</sup>	1	sn
2	DWE asserted before CASx asserted	25	I	su
3	OE negated before RASx asserted	0	I	su
4	RASx asserted before row address invalid (MSW = 0,1)	12,27	I	su
ζī	Column address valid to $\overline{CASx}$ asserted (MSW = 0,1)	10,25	I	su
6	$\overline{RASx}$ asserted to $\overline{CASx}$ asserted (MSW = 0,1)	28,58	I	sn
7	RASx pulse width (SLW = 0,1)	90,120	l	su
8	CASx pulse width (BC[1:0] = 00,01,10,11)	28,58,88,118	l	su
9	Data-out valid before CASx asserted	25	1	su
10	Data-out hold after CASx negated	25	1	su
11	DWE negated after CASx negated	0	l	su
12	CASx asserted before column address invalid	50	l	su
13	RASx negated after CASx negated	28	I	su
14	RASx precharge time (SLW = 0,1)	50,118	l	su
Note: RAS	RASx stands for RAS0 and RAS1. CASx stands for CAS0 and CAS1.	and $\overline{CAS1}$ .	ristor When the to	<u>ב</u>

identifies these bits, the sequence of their listed values corresponds to the sequence of timing data provided. MSW is bit 5, SLW is bit 3, and BC[1:0] comprises bits 13-12 in the DRAMC register. When the table

### 19.3.8 DRAM Hidden Refresh Cycle (Normal Mode)

signal values and units of measure for this figure are found in Table 19-10 on page 19-12. Detailed information about the operation of individual signals can be found in Chapter 7, "DRAM Controller." Figure 19-8 on page 19-12 shows the DRAM hidden refresh cycle timing diagram for normal mode. The ARCHIVEI



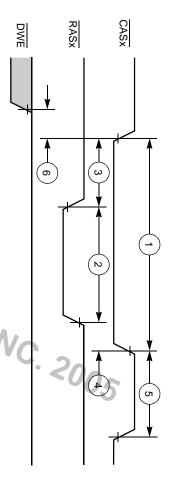


Figure 19-8. DRAM Hidden Refresh Cycle (Normal Mode) Timing Diagram

Table 19-10. DRAM Hidden Refresh Cycle (Normal Mode) Timing Parameters

Number	Characteristic	4	(3.0 ± 0.3) V
	/D		Minimum
_	CASx pulse width		88
2	RASx pulse width		88
3	CASx asserted to RASx asserted		28
4	RASx negated to CASx negated		-28
5	CASx negated to next CASx asserted		88
6	DWE negated before CASx asserted		58
Note: RAS	Note: RASx stands for RAS0 and RAS1. CASx stands for CAS0 and CAS1	۵	CAS1.

### 19.3.9 DRAM Hidden Refresh Cycle (Low-Power Mode)

Figure 19-9 shows the DRAM hidden refresh cycle timing diagram for low-power mode. The signal values and units of measure for this figure are found in Table 19-11 on page 19-13. Detailed information about the operation of individual signals can be found in Chapter 7, "DRAM Controller."

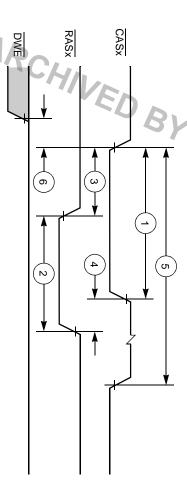


Figure 19-9. DRAM Hidden Refresh Cycle (Low-Power Mode) Timing Diagram

Table 19-11. DRAM Hidden Refresh Cycle (Low-Power Mode) Timing Parameters

Number	Characteristic	(3.0 ±	(3.0 ± 0.3) V	_ 5 <del>*</del>
TAGIIIDGI	Cialacterione	Minimum	Maximum	Ç.
1	CASx pulse width	120	I	ns
2	RASx pulse width	120		sn
3	CASx asserted to RASx asserted	30		ns
4	CASx negated to RASx negated	30	_	ns
5	Refresh cycle (using 32.768 KHz crystal)	15	_	sn
5	Refresh cycle (using 38.400 KHz crystal)	<b>(</b> ) 13	_	sn
9	DWE negated before CASx asserted	58	_	ns
Note: RASx	RASx stands for RAS0 and RAS1. CASx stands for CAS0 and CAS1	S0 and CAS1.		

### LCD SRAM/ROM DMA Cycle 16-Bit Mode Access (1 Wait State)

operation of individual signals can be found in Chapter 7, "DRAM Controller," and Chapter 8, "LCD of measure for this figure are found in Table 19-12 on page 19-14. Detailed information about the Note that WS is the number of wait states in the current memory access cycle. The signal values and units Figure 19-10 shows the LCD SRAM/ROM DMA cycle timing diagram for 16-bit access (1 wait state).

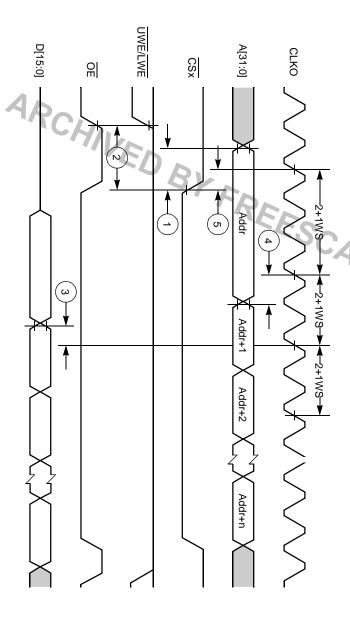


Figure 19-10. LCD SRAM/ROM DMA Cycle 16-Bit Mode Access Timing Diagram

Table 19-12. LCD SRAM/ROM DMA Cycle 16-Bit Mode Access Timing Parameters

Nimber	Characteristic	(3.0 ± 0.3) V	).3) V	_ 5 <del>*</del>
	O INI MANOTE DELLA	Minimum	Maximum	Ş
_	Address valid to CSx asserted	20	I	ns
2	UWE/LWE to CSx asserted	28	1	ns
3	Data setup time	16	1	ns
4	CLKO to address valid	) R	10	ns
51	CLKO high to CSx	7	10	ns

### **LCD DRAM DMA Cycle 16-Bit EDO RAM Mode Access** (LCD Bus Master)

"DRAM Controller," and Chapter 8, on page 19-15. Detailed information about the operation of individual signals can be found in Chapter 7, access (LCD bus master). The signal values and units of measure for this figure are found in Table 19-13 Figure 19-11 shows the timing diagram for the LCD DRAM DMA cycle for 16-bit EDO RAM mode "LCD Controller."

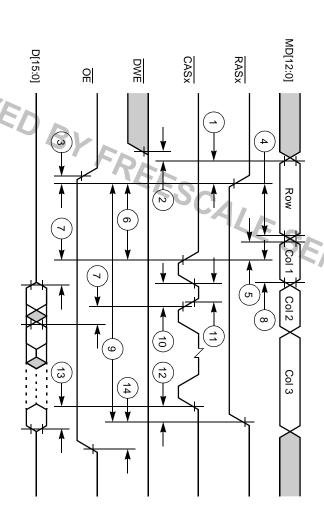


Figure 19-11. LCD DRAM DMA Cycle 16-Bit EDO RAM Mode Access (LCD Bus Master) Timing Diagram

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LCD DRAM DMA Cycle 16-Bit EDO RAM Mode Access (LCD Bus Master)
Timing Parameters

	Note: N is the number T is the system RASX stands fo MSW is bit 5 in second tin	14	13	12	11	10	9	8	7	თ	51	4	3	2	_		Number
ARCHIVEDBY	Note:  N is the number of words in one DMA transfer.  T is the system clock period.  RASx stands for RAS0 and RAS1. CASx stands for CAS0 and CAS1.  MSW is bit 5 in the DRAMC register. When this bit is set to 0, the first timing number applies; when it is set to 1, the second timing number applies.	OE negated after CASx negated	Data-in hold after CASx negated	RASx negated to CASx negated	CASx precharge time	CASx pulse width	RASX pulse width	CASx asserted before column address invalid	CASx asserted to data-in valid	$\overline{RASx}$ asserted to $\overline{CASx}$ asserted (MSW = 0,1)	Column address valid to CASx asserted (MSW = 0,1)	$\overline{RASx}$ asserted before row address invalid (MSW = 0,1)	OE asserted before RASx asserted	DWE negated before row address valid	Row address valid to RASx asserted		Characteristic
	st timing number :	28	30	-28	26	28	(2N + 1)T	20	I	28,58	10,25	12,27	0	\ <u>C</u>	45	Minimum	(3.0 ± 0.3) V
	applies; when it is	32	I	I	I	I	I	I	20	I	I	I	I	I	I	Maximum	0.3) V
	set to 1, the	ns	ns	ns	ns	ns	ns	ns	ns	ns	ns	ns	ns	ns	ns		Unit

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### 19.3.12 LCD DRAM DMA Cycle 16-Bit Fast Page Mode Access (LCD Bus Master)

Controller," and Chapter 8, "LCD Controller." access (LCD bus master). The signal values and units of measure for this figure are found in Table 19-14 Detailed information about the operation of individual signals can be found in Chapter 7, "DRAM shows the timing diagram for the LCD DRAM DMA cycle for 16-bit Fast Page Mode mode

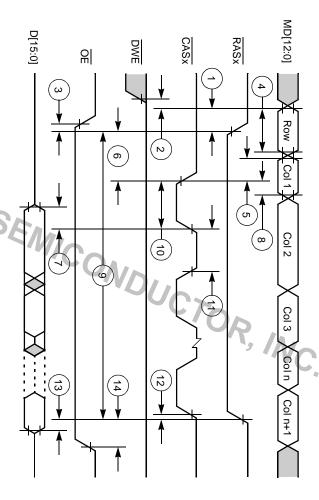


Figure 19-12. LCD DRAM DMA Cycle 16-Bit Fast Page Mode Access (LCD Bus Master) Timing Diagram

LCD DRAM DMA Cycle 16-Bit Fast Page Timing Parameters Mode Access (LCD Bus Master)

Number	2	_	2	3	4	5	6	7	•
Characteristic	Characteristic	Row address valid to RASx asserted	DWE negated before row address valid	OE asserted before RASx asserted	RASx asserted before row address invalid (MSW = 0,1)	Column address valid to $\overline{CASx}$ asserted (MSW = 0,1)	$\overline{RASx}$ asserted to $\overline{CASx}$ asserted (MSW = 0,1)	Data setup time	
$(3.0 \pm 0.3) \text{ V}$	Minimum	45	0	0	12,27	10,25	28,58	15	88
0.3) V	Maximum	I	-	-	1	I	I	I	
l bit	0	ns	su	su	su	su	ns	ns	20

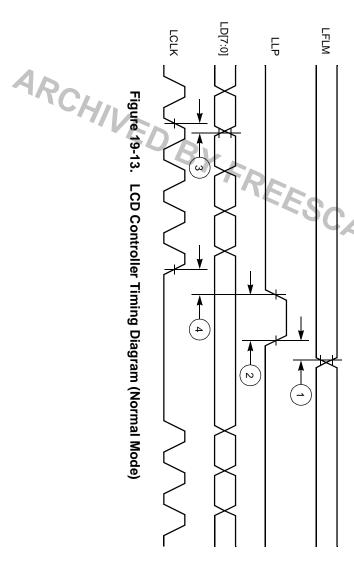
## Freescale Semiconductor,概要 ectrical Characteristics

Table 19-14. LCD DRAM DMA Cycle 16-Bit Fast Page Mode Access (LCD Bus Master) Timing Parameters (Continued)

Number	Characteristic	(3.0 ± 0.3) V	).3) V	= - -
		Minimum	Maximum	
9	RASx pulse width	(2N + 1)T	I	ns
10	CASx pulse width (BC[1:0] = 00,01,10,11 in FPM)	28,58,88,118	I	ns
11	CASx precharge time	26	l	su
12	RASx negated to CASx negated	-28	I	su
13	Data-in hold after CASx negated	0	I	ns
14	OE negated after CASx negated	0	2	ns
Note: N is the number of the system of the s	Note:  N is the number of words in one DMA transfer.  T is the system clock period.  RASx stands for RAS0 and RAS1. CASx stands for CAS0 and CAS1.  MSW is bit 5 and BC[1:0] comprises bits 13–12 in the DRAMC register. When the table identifies these bits, the sequence of their listed values corresponds to the sequence of timing data provided.	1. ter. When the table	identifies these b	oits, the

#### 19.3.13 **LCD Controller Timing**

be found in Chapter 8, "LCD Controller," and Chapter 7, "DRAM Controller." are found in Table 19-15 on page 19-18. Detailed information about the operation of individual signals can displays the timing diagram for self-refresh mode. The signal values and units of measure for both figures Figure 19-13 shows the LCD controller timing diagram for normal mode, and Figure 19-14 on page 19-18



**LCD Controller Timing Diagram (Normal Mode)** 

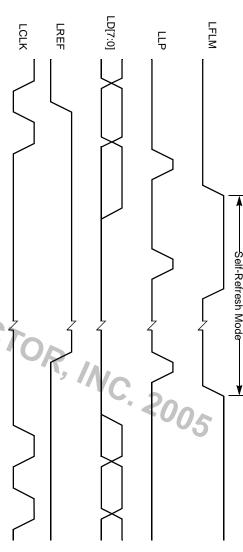


Figure 19-14. LCD Controller Timing Diagram (Self-Refresh Mode)

Table 19-15. **LCD Controller Timing Parameters** 

Nimber	Characteristic	$(3.0 \pm 0.3) \text{ V}$	).3)
	Cital actorion o	Minimum	Maximum
1	Line pulse to frame signal	(4 * pixclk) - 2	_
2	Line pulse width	(4 * pixclk) - 2	
3	LCLK to data valid	-2	2
4	Shift clock to line pulse	(2 * pixclk) - 2 (2 * pixclk) + 2	(2 * pixclk) + 2
Note:	S		

The preceding data is measured by summing the polarity bits LFLM, LLP, and LCLK in the POLCF register. The variable pixclk = LCD\_CLK / (pcd +1).

The self-refresh mode timing between LFRM, LSCLK, LD, and LLP are the same as in normal mode The self-refresh mode is entered and exited on the positive edge of LFRM.

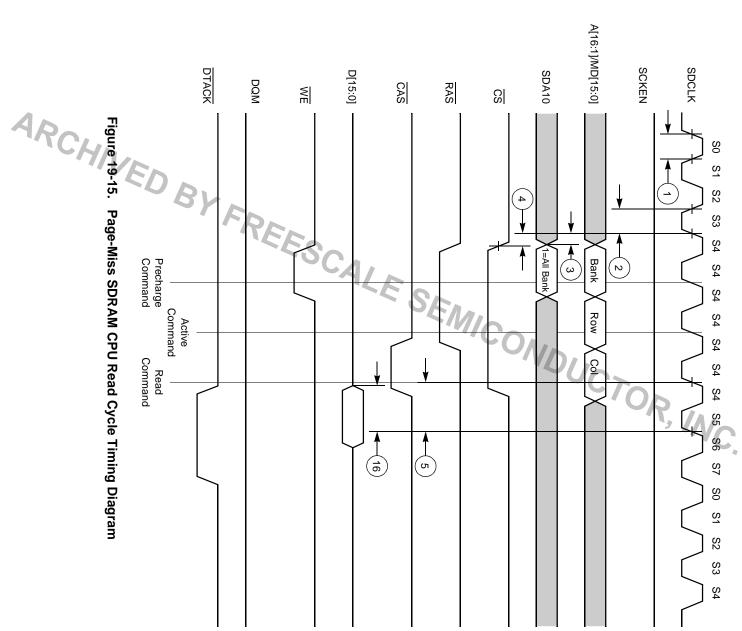
In self-refresh mode, the LFRM and LLP waveforms are identical to the waveforms in normal mode, while LD and



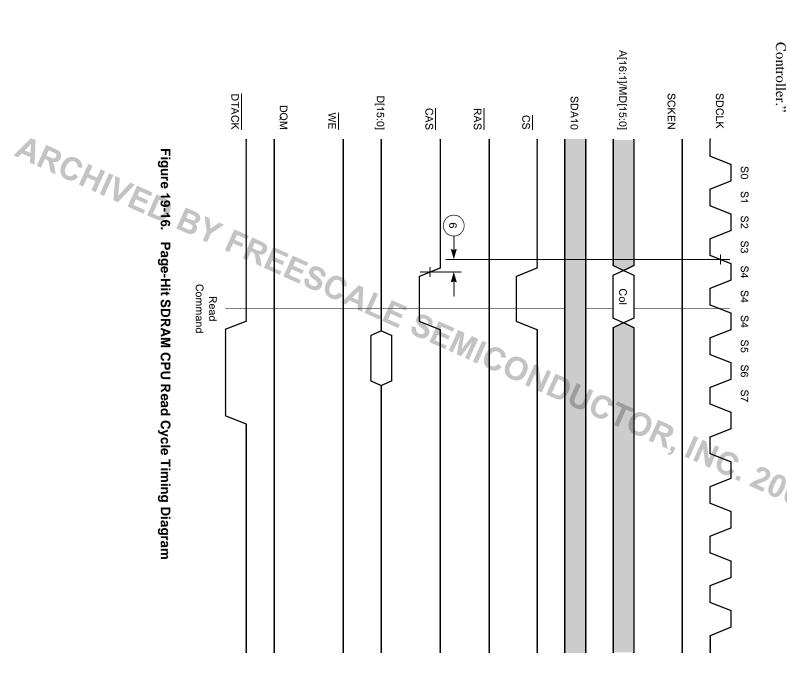
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### Page-Miss SDRAM CPU Read Cycle (CAS .atency = 1)

Figure 19-15 shows the timing diagram for the page-miss SDRAM CPU read cycle. The signal values and units of measure for this figure are found in Table 19-16 on page 19-31. Detailed information about the operation of individual signals can be found in both Chapter 8, "LCD Controller," and Chapter 7, "DRAM" Controller."



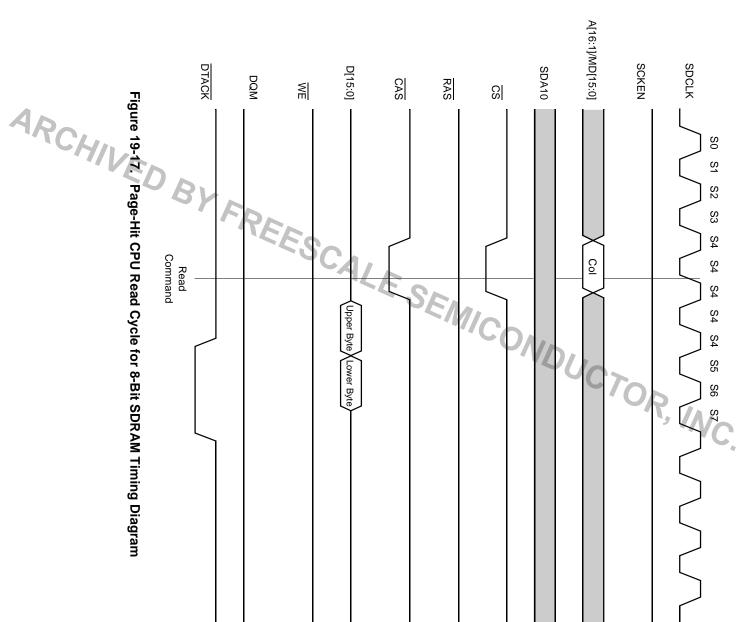
### Figure 19-16 shows the timing diagram for the page-hit SDRAM CPU read cycle. The signal values and units of measure for this figure are found in Table 19-16 on page 19-31. Detailed information about the operation of individual signals can be found in both Chapter 8, "LCD Controller," and Chapter 7, "DRAM 19.3.15 Page-Hit SDRAM CPU Read Cycle (CAS Latency =



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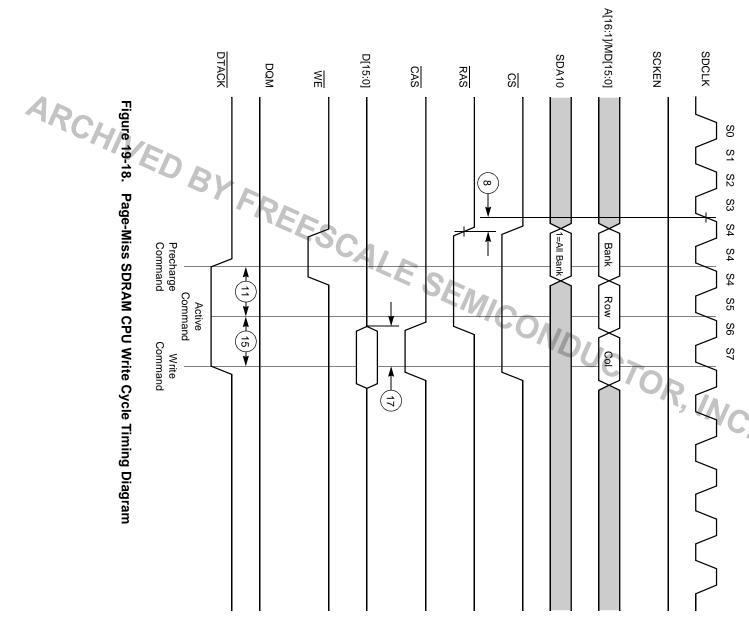
### Page-Hit CPU Read Cycle for 8-Bit SDRAM (CAS .atency = 1)

Figure 19-17 shows the timing diagram for the page-hit CPU read cycle for 8-bit SDRAM. The signal values and units of measure for this figure are found in Table 19-16 on page 19-31. Detailed information about the operation of individual signals can be found in both Chapter 8, "LCD Controller," and Chapter 7, "DRAM Controller" "DRAM Controller."



### 19.3.17 Page-Miss SDRAM CPU Write Cycle (CAS .atency = 1)

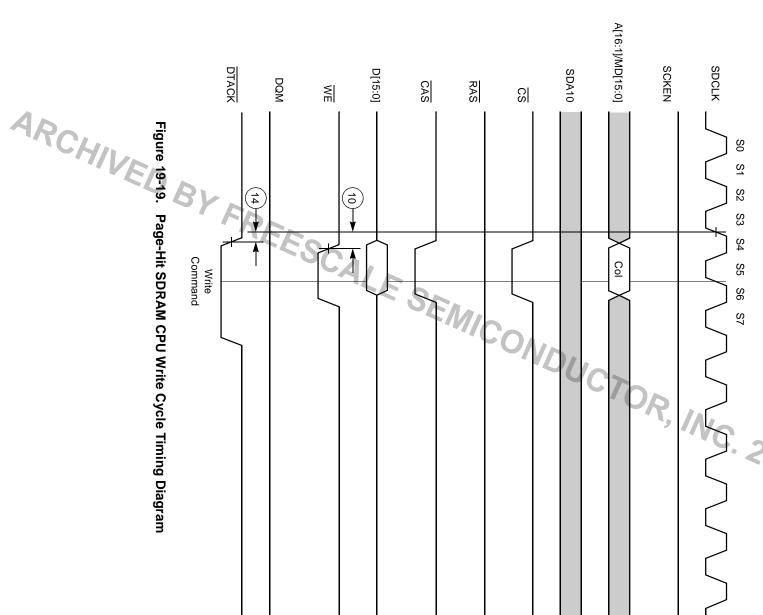
Figure 19-18 shows the timing diagram for the page-miss SDRAM CPU write cycle for 8-bit SDRAM. The signal values and units of measure for this figure are found in Table 19-16 on page 19-31. Detailed and Chapter 7, "DRAM Controller." information about the operation of individual signals can be found in both Chapter 8, "LCD Controller,"



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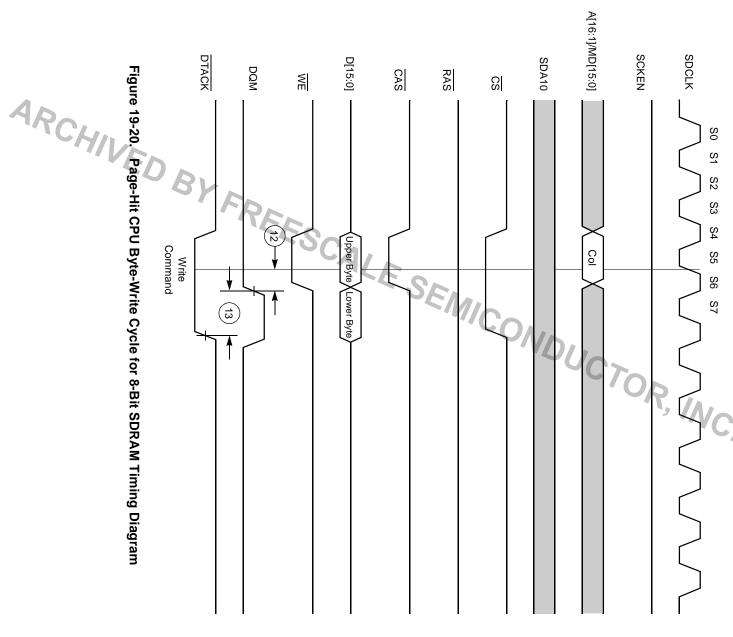
### 19.3.18 Page-Hit SDRAM CPU Write Cycle (CAS Latency = 1)

signal values and units of measure for this figure are found in Table 19-16 on page 19-31. Detailed and Chapter 7, "DRAM Controller." information about the operation of individual signals can be found in both Chapter 8, "LCD Controller," Figure 19-19 shows the timing diagram for the page-hit SDRAM CPU write cycle for 8-bit SDRAM. The



### 19.3.19 Page-Hit CPU Byte-Write Cycle for 8-Bit SDRAM (CAS .atency = 1)

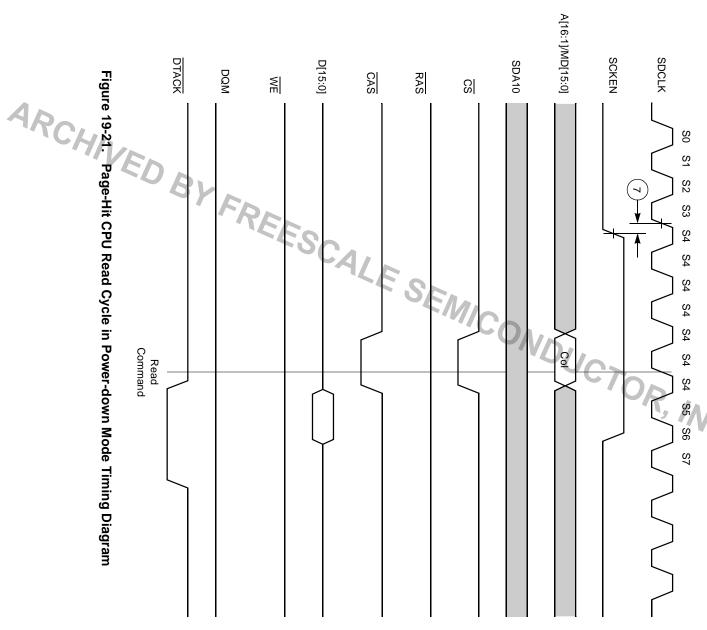
and Chapter 7, "DRAM Controller." information about the operation of individual signals can be found in both Chapter 8, "LCD Controller," The signal values and units of measure for this figure are found in Table 19-16 on page 19-31. Detailed Figure 19-20 shows the timing diagram for the page-hit SDRAM CPU byte-write cycle for 8-bit SDRAM



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#### 19.3.20 Page-Hit CPU Read Cycle in Power-down Mode (CAS Register = 1) Latency = 1, Bit APEN of SDRAM Power-down

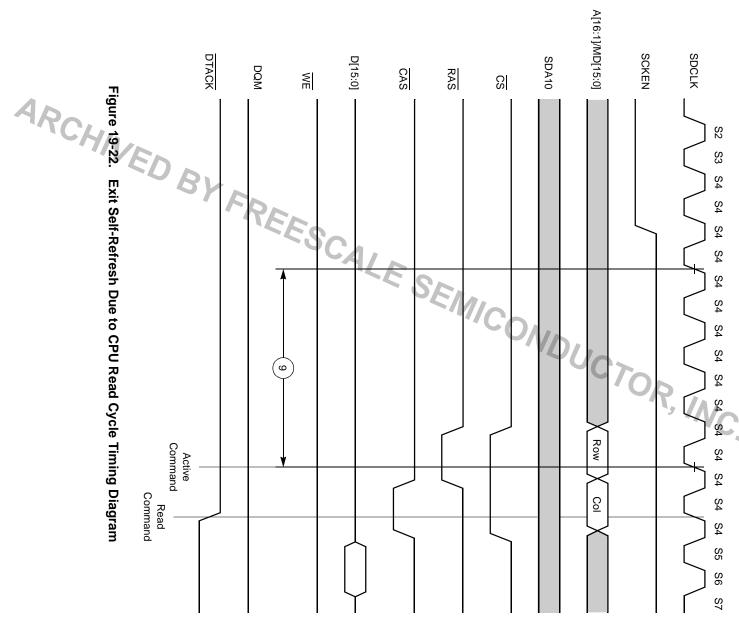
about the operation of individual signals can be found in both Chapter 8 Figure 19-21 shows the timing diagram for the page-hit CPU read cycle in power-down mode. The signal values and units of measure for this figure are found in Table 19-16 on page 19-31. Detailed information about the operation of individual signals can be found in both Chapter 8, "LCD Controller," and Chapter 7, "DRAM Controller."



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### 19.3.21 Exit Self-Refresh Due to CPU Read Cycle (CAS \_atency = 1, Bit RM of DRAM Control Register = 1)

values and units of measure for this figure are found in Table 19-16 on page 19-31. Detailed information about the operation of individual signals can be found in both Chapter 8, "LCD Controller," and Chapter 7, Figure 19-22 shows the timing diagram for the exit self-refresh due to the CPU read cycle. The signal "DRAM Controller."



9-26

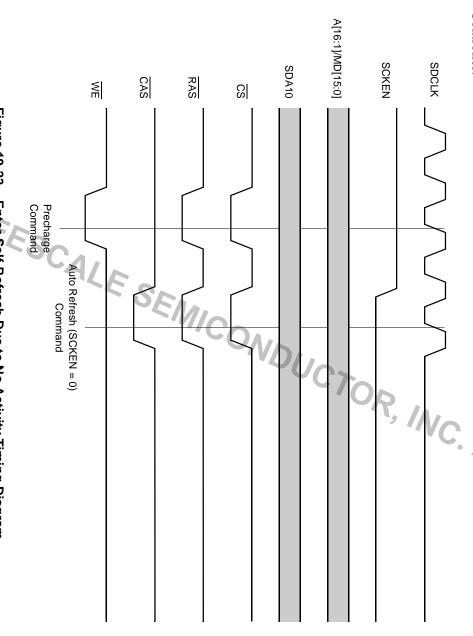
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## Freescale Semiconductor, Interestrical Characteristics

### Enter Self-Refresh Due to No Activity for 64 Clocks Bit RM of DRAM Control Register = 1)

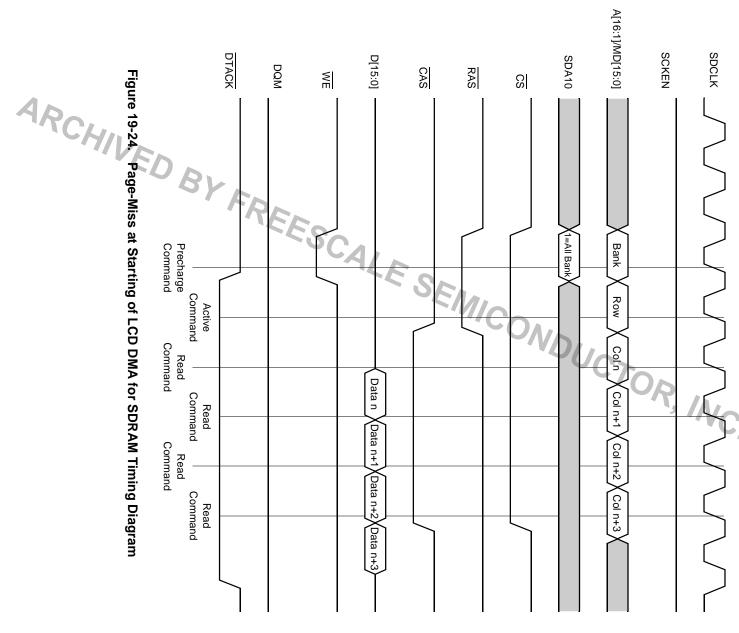
Figure 19-23 shows the timing diagram for enter self-refresh due to no activity. The signal values and units of measure for this figure are found in Table 19-16 on page 19-31. Detailed information about the operation of individual signals can be found in both Chapter 8, "LCD Controller," and Chapter 7, "DRAM Controller."



ARCHIVED BY FRI Enter Self-Refresh Due to No Activity Timing Diagram

#### 19.3.23 Page-Miss at .atency = 1) Starting of LCD DMA for SDRAM (CAS

Figure 19-24 shows the timing diagram for the page-miss at the starting of LCD DMA for SDRAM. The signal values and units of measure for this figure are found in Table 19-16 on page 19-31. Detailed and Chapter 7, "DRAM Controller." information about the operation of individual signals can be found in both Chapter 8, "LCD Controller,"

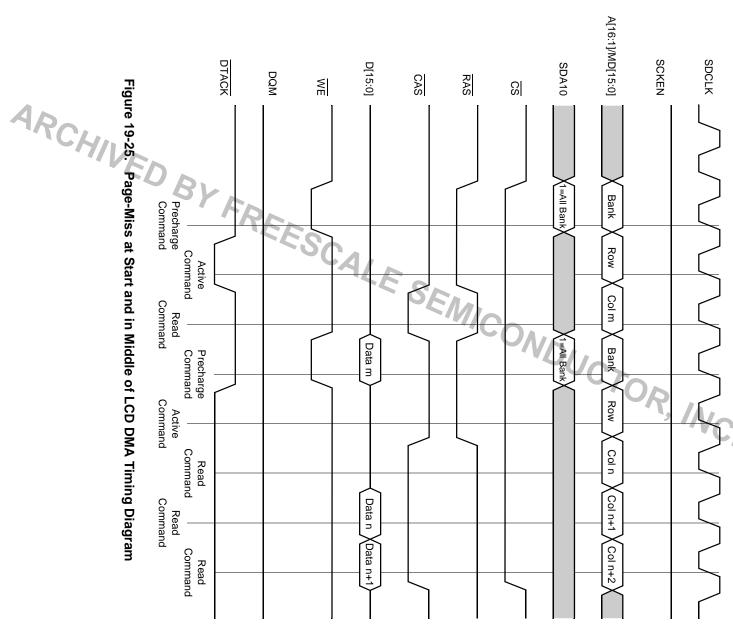




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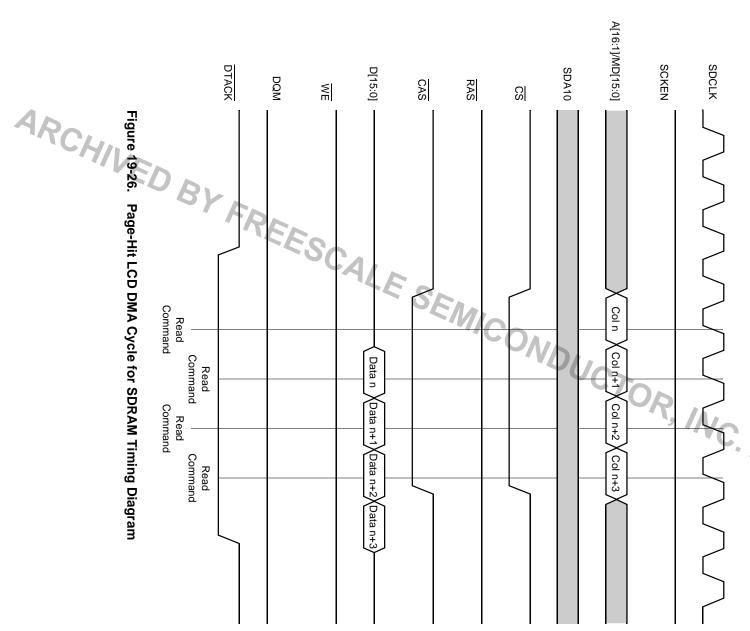
#### 19.3.24 Page-Miss at .atency = 1) Start and in Middle of LCD DMA (CAS

Figure 19-25 shows the timing diagram for the page-miss at the start and in the middle of LCD DMA. The signal values and units of measure for this figure are found in Table 19-16 on page 19-31. Detailed information about the operation of individual signals can be found in both Chapter 8, "LCD Controller," and Chapter 7, "DRAM Controller."



### 19.3.25 Page-Hit LCD DMA Cycle for SDRAM (CAS .atency = 1)

Figure 19-26 shows the timing diagram for the page-hit LCD DMA cycle for SDRAM. The signal values and units of measure for this figure are found in Table 19-16 on page 19-31. Detailed information about the operation of individual signals can be found in both Chapter 8, "LCD Controller," and Chapter 7, "DRAM Controller."



Ф
le 19-16.
Timing
Timing Parameters for Figure 19-15 Through Figure 19-2
for Figure
19-15
Through
Figure 1
9-:

:	<b>!</b>	(3.0 ± 0.3) V	.3) V	:
Number	Cnaracteristic	Minimum	Maximum	Unit
1	Clock high pulse time	12	I	ns
2	Clock low pulse time	13	I	ns
ω	Clock high to address valid	ω (	13	ns
4	Clock high to chip-select	ω	12	ns
Ŋ	Read to data sample latency	CAS latency	I	CLK
6	Clock high to CAS asserted	3	12	ns
7	Clock high to SCKEN asserted	8	12	ns
8	Clock high to RAS asserted	ω	12	ns
9	Self-refresh exit to active command asserted	4 (7)*	I	CLK
10	Clock high to WE asserted	ω	12	ns
11	Precharge command to active command	1 (2)**	I	CLK
12	Clock high to DQM asserted	3	12	ns
13	DQM width asserted	28	l	ns
14	Clock high to DTACK asserted	10	l	ns
15	Active command to read/write command	1 (2)**	l	CLK
16	Data setup time	13	l	ns
17	Data valid to clock high	10		ns
* Note: The va	* Note: The value inside the parentheses is used if the value of bit RACL of the SDRAM control register is 1	٦CL of the SDRAN د	l control register	r is 1.

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## 19.3.26 SPI 1 and SPI 2 Generic Timing

the operation of individual signals can be found in Chapter 13, "Serial Peripheral Interface 1 and 2 Figure 19-27 through Figure 19-32 are found in Table 19-17 on page 19-34. Detailed information about Figure 19-27 shows the timing diagram for SPI 1 and SPI 2. The signal values and units of measure for

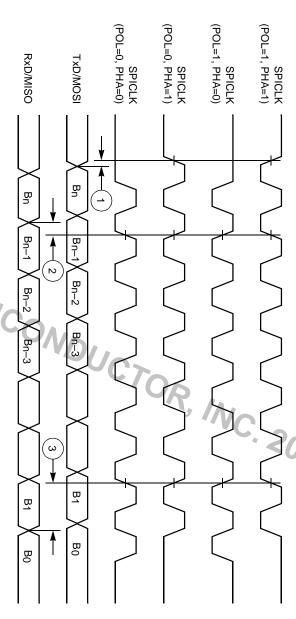


Figure 19-27. SPI 1 and SPI 2 Generic Timing Diagram

#### 19.3.27 **SPI 1 Master Using DATA** READY **Edge Trigger**

signal values and units of measure for Figure 19-27 through Figure 19-32 are found in Table 19-17 on page 19-34. Detailed information about the operation of individual signals can be found in Chapter 13, Figure 19-28 shows the timing diagram for the SPI 1 master using the DATA\_READY edge trigger. The "Serial Peripheral Interface 1 and 2."

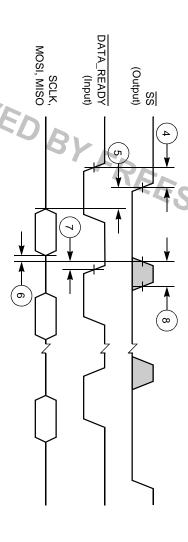


Figure 19-28. SPI 1 Master Using DATA\_READY Edge Trigger Timing Diagram

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### 19.3.28 SPI 1 Master Using DATA\_READY Level Trigger

signal values and units of measure for Figure 19-27 through Figure 19-32 are found in Table 19-17 on page 19-34. Detailed information about the operation of individual signals can be found in Chapter 13 Figure 19-29 shows the timing diagram for the SPI 1 master using the DATA\_READY level trigger. The "Serial Peripheral Interface 1 and 2."

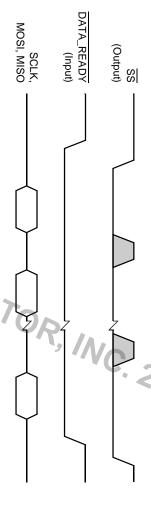
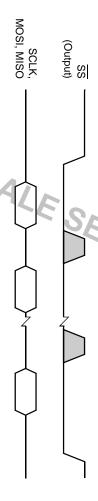


Figure 19-29. SPI 1 Master Using DATA\_READY Level Trigger Timing Diagram

### 19.3.29 SPI 1 Master "Don't Care" DATA READY

Figure 19-30 shows the timing diagram for the SPI 1 master with DATA\_READY "don't care." The signal page 19-34. Detailed information about the operation of individual signals can be found in Chapter 13 values and units of measure for Figure 19-27 through Figure 19-32 are found in Table 19-17 on "Serial Peripheral Interface 1 and 2."



Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently

are not available from Freescale for import or sale in the United States prior to September 2010: MC68VZ328 Product Family

Figure 19-30. SPI 1 Master "Don't Care" DATA\_READY Timing Diagram

### 19.3.30 SPI 1 Slave **FIFO Advanced by Bit Count**

Figure 19-31 shows the timing diagram for the SPI 1 slave FIFO advanced by bit count. The signal values Peripheral Interface 1 and 2." and units of measure for Figure 19-27 through Figure 19-32 are found in Table 19-17 on page 19-34 Detailed information about the operation of individual signals can be found in Chapter 13, "Serial

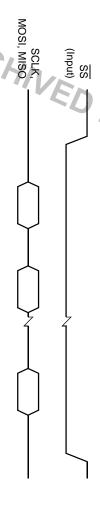


Figure 19-31. SPI 1 Slave FIFO Advanced by Bit Count Timing Diagram



### 19.3.31 SPI 1 Slave FIFO Advanced by SS Rising Edge

information about the operation of individual signals can be found in Chapter 13, "Serial Peripheral values and units of measure for Figure 19-27 through Figure 19-32 are found in Table 19-17. Detailed Figure 19-32 shows the timing diagram for the SPI 1 slave FIFO advanced by  $\overline{SS}$  rising edge. The signal

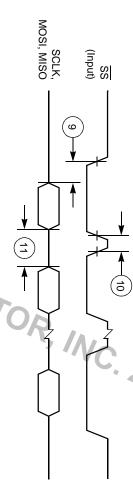


Figure 19-32. SPI 1 Slave FIFO Advanced by SS Rising Edge Timing Diagram

Table 19-17. Timing Parameters for Figure 19-27 Through Figure 19-32

Note: T = SPI clock period WAIT = Number of sysclk or 32.768 KHz clocks per sample period control register	11 Pause between data word	10 SS input pulse width	9 SS input low to first SCLK edge	8 SS output pulse width 2T -	7 SS output high to DATA_READY low	6 Last SCLK edge to SS output high	5 SS output low to first SCLK edge	4 DATA_READY to SS output low	Clock edge to RxD data hold time	2 RxD data ready to clock edge 0	1 Clock edge to TxD data ready		Number Characteristic
mple period control register	0	0	Т	2T + WAIT	Т	Т	2Т	-	0.25T	0.25T		Minimum	
	l	l	ı	ı	ı	l	ı	2T	l	l	0.25T	Maximum	(3.0 ± 0.3) V
	ns	ns	ns	ns	ns	ns	ns	ns	ns	ns	ns	Ç	In i



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### 19.3.32 Normal Mode Timing

and units of measure for Figure 19-33 through Figure 19-35 are found in Table 19-18 on page 19-36 Figure 19-33 shows the timing diagram for normal mode timing of the MC68VZ328. The signal values

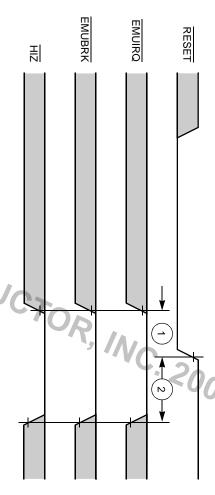


Figure 19-33. Normal Mode Timing Diagram

## 19.3.33 Emulation Mode Timing

and units of measure for Figure 19-33 through Figure 19-35 are found in Table 19-18 on page 19-36. Figure 19-34 shows the timing diagram for emulation mode timing of the MC68VZ328. The signal values

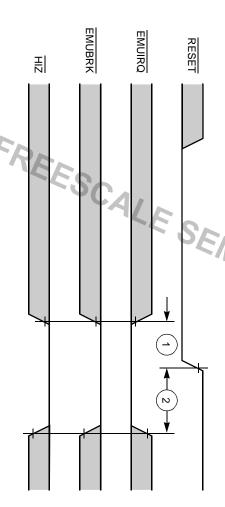


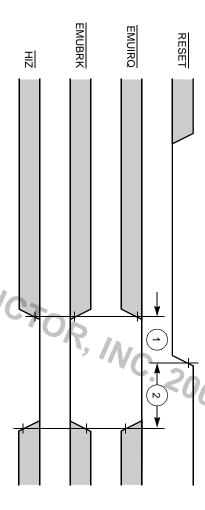
Figure 19-34. Emulation Mode Timing Diagram

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AC Electrical Characteristity eescale Semiconductor, Inc.

#### 19.3.34 **Bootstrap Mode Timing**

and units of measure for Figure 19-33 through Figure 19-35 are found in Table 19-18 Figure 19-35 shows the timing diagram for bootstrap mode timing of the MC68VZ328. The signal values



Timing Parameters for Figure 19-33 Through Figure 19-35

Figure 19-35.

**Bootstrap Mode Timing Diagram** 

	2	1	מווספו	Nimbor	
ARCHIVED BY FREESCA	EMUIRQ, EMUBRK, and HIZ hold time	EMUIRQ, EMUBRK, and HIZ setup time	Cital acter is the		
	20	10	Minimum	(3.0 ±	
		I	Maximum	$(3.0 \pm 0.3) \text{ V}$	
	ns	ns	C		

### Freescale Semiconductor, Inc.

#### Mechanical Chapter ntormation Ordering .C. 2005

This chapter provides mechanical data, including illustrations, and ordering information.

### 20.1 Ordering Information

Table 20-1 provides ordering information for the two package types: the 144-lead, plastic, thin quad flat package (TQFP) and the 144-lead mold array process ball grid array (MAPBGA) package.

Table 20-1. MC68VZ328 Ordering Information

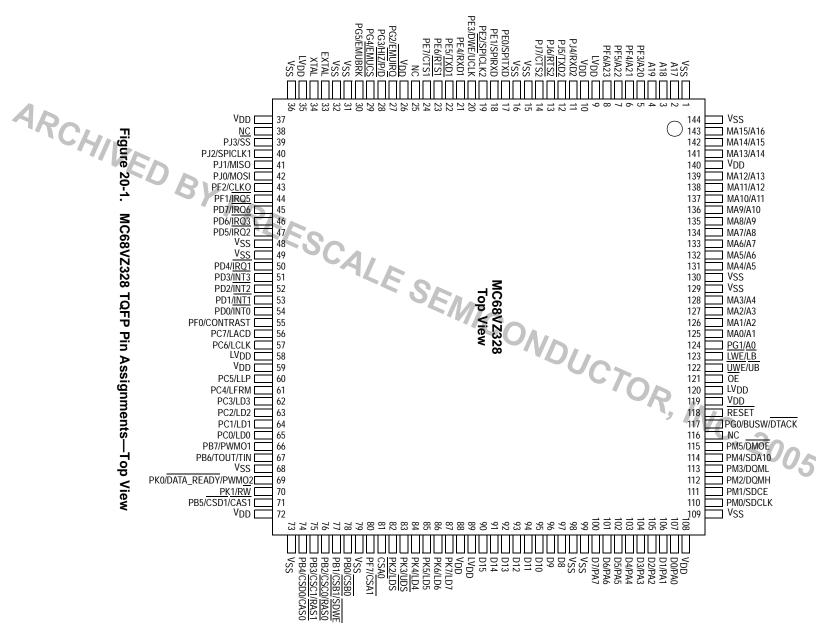
ARCHIVED	144-lead MAPBGA	144-lead TQFP	144-lead MAPBGA	144-lead TQFP	Package Type
ARCHIVED BY FREE	33	33	33	33	Frequency (MHz)
	-40 °C to 85 °C	-40 $^{\circ}$ C to 85 $^{\circ}$ C	0 °C to 70 °C	0 °C to 70 °C	Temperature
	MC68VZ328CVF33V	MC68VZ328CPV33V	MC68VZ328VF33V	MC68VZ328PV33V	Order Number



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#### TQFP Pin ssignments

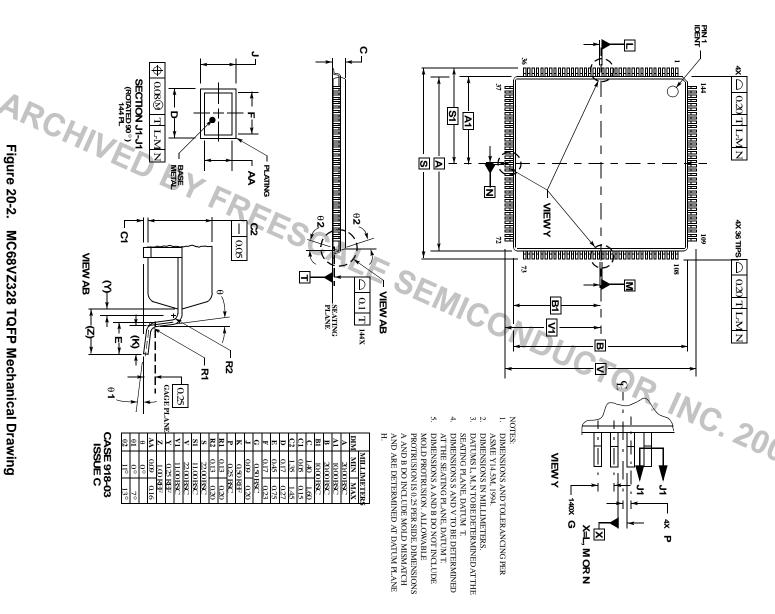
Figure 20-1 provides a top view of TQFP pin assignments



# Freescale Semiconductor, Ing P Package Dimensions

## 20.3 TQFP Package Dimensions

The device designator for the TQFP package is PV Figure 20-2 illustrates the TQFP 20 mm  $\times$  20 mm package, which has 0.5 mm spacing between the pads



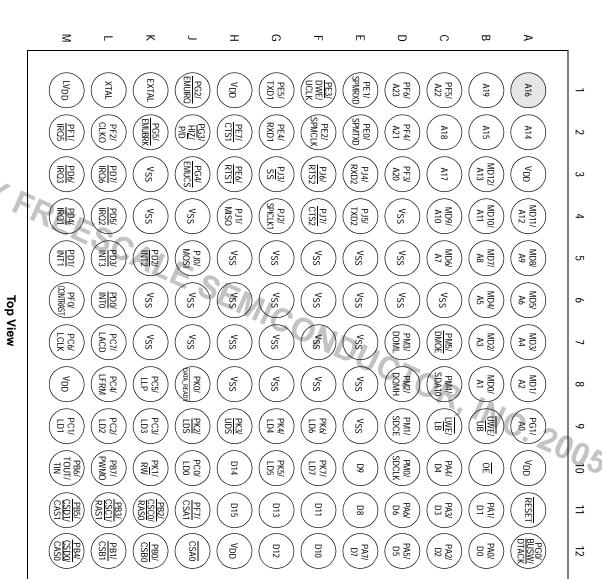
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#### Freescale Semiconductor, Inc.

## 20.4 MAPBGA Pin Assignments

MAPBGA Pin Assignment Freescale Semiconductor, Inc.

Figure 20-3 provides a top view of the MAPBGA pin assignments

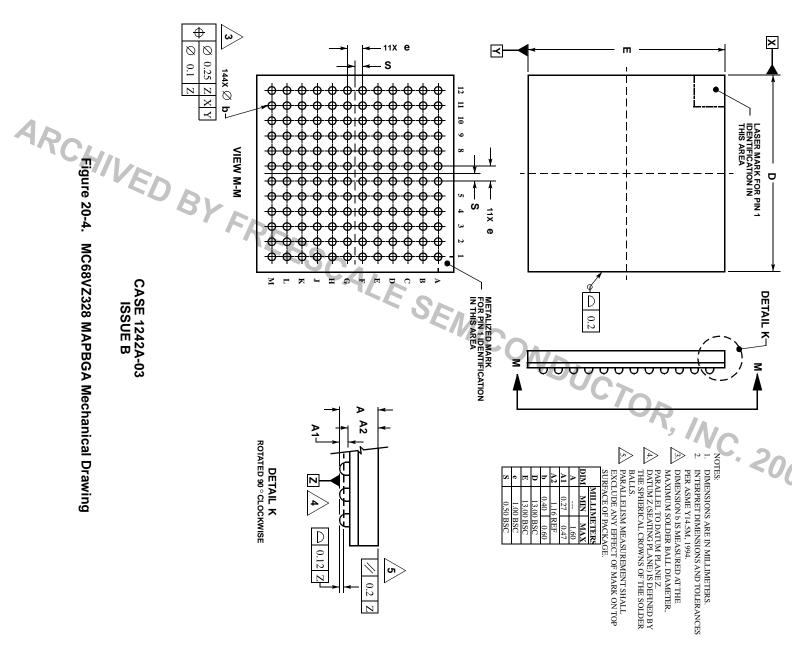


ARCHIVED Figure 20-3. MC68VZ328 MAPBGA Pin Assignments—Top View

# Freescale Semiconductor, Anga Package Dimensions

### **MAPBGA Package Dimensions**

pads. The device designator for the MAPBGA package is VF. Figure 20-4 illustrates the MAPBGA 13 mm × 13 mm package, which has 1 mm spacing between the





#### 20.6 PCB **Finish** Requirement

PCB Finish Requirement Freescale Semiconductor, Inc.

recommended. When EMNI AU finish is used on PCB, brittle intermetallic fractures occasionally occur at For a more reliable BGA assembly process, use HASL finish on PCB. EMNI AU finish is not



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16-Bit SRAM enable bit, see SR16 bit	Baud rate generator
32-bit counter, see cascaded timers 8- or 7-bit bit see 8/7 bit	band rates affected by PLL frequencies, 14-9
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address bits 19–17, see A[19:17] pins	BGBA field, 6-7
address bits 23-20, see A[23:20]/PF[6:3] pins	BIT COUNT field
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MA[15:0]/A[16:1] pins $Part F hits 6-3 sea A[73:70]/DF[6:3] hins$	Bit count overflow bit. see BO bit
Address compare bits 31–0, see ACx bits	Bit count overflow interrupt enable bit, see BOEN bit
Address mask bits 31–0, see AMx bits	BKEN bit, 8-15
AGBA field, 6-6	Blink divisor field, see BDx field
Alternate crystal direction control 6–0 field, see ACDx field	Blink enable bit, <i>see</i> BKEN bit BO bit, 13-9
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overlap Capture event bit, see CAPT bit BUSW/DTACK/PG0 pin, 2-6 CAPTURE field Capture edge field, see CAP field CAP field BWSO bit, 6-17 **BUSY** bit Busy (Tx status) bit, see BUSY bit Bus control signals BUPS2 bit, 6-18 Break characters, generating, Break (character status) bit, see BREAK bit <u>CÁS0/CAS1</u> signal, 6-1 Capture value field, see CAPTURE field Capture events, 12-2 CAPT bit Burst mode BSW bit TSTAT1 register, 12-12
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Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently

are not available from Freescale for import or sale in the United States prior to September 2010: MC68VZ328 Product Family

Semiconductor, Inc.

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