

FLASH MEMORY

CMOS

16M (2M × 8/1M × 16) BIT Dual Operation

MBM29DL16XTD/BD -70/90/12

■ FEATURES

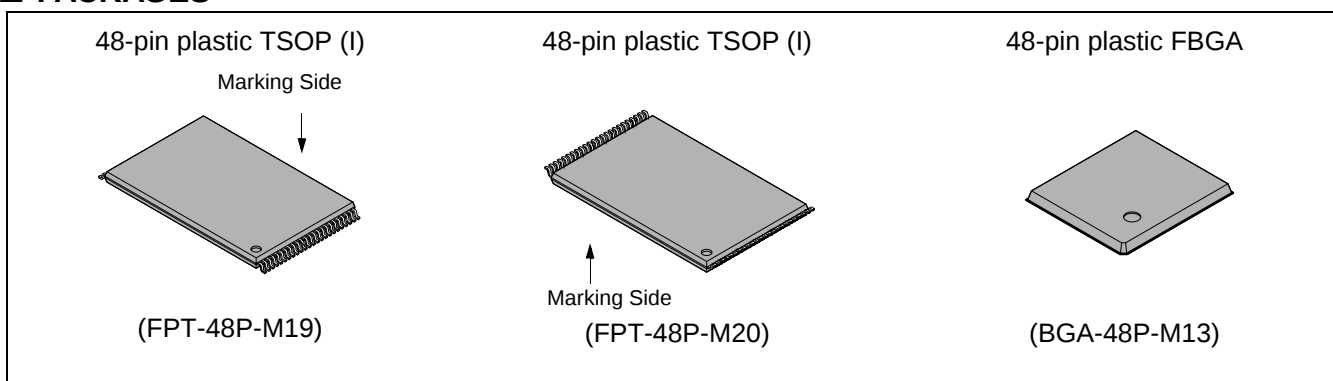
- **0.33 μm Process Technology**
- **Simultaneous Read/Write operations (dual bank)**
Multiple devices available with different bank sizes (Refer to Table 1)
Host system can program or erase in one bank, then immediately and simultaneously read from the other bank
Zero latency between read and write operations
Read-while-erase
Read-while-program
- **Single 3.0 V read, program, and erase**
Minimizes system level power requirements

(Continued)

■ PRODUCT LINE UP

Part No.		MBM29DL16XTD/MBM29DL16XBD		
Ordering Part No.	V _{CC} = 3.3 V ^{+0.3 V} / _{-0.3 V}	70	—	—
	V _{CC} = 3.0 V ^{+0.6 V} / _{-0.3 V}	—	90	12
Max. Address Access Time (ns)		70	90	120
Max. $\overline{\text{CE}}$ Access Time (ns)		70	90	120
Max. $\overline{\text{OE}}$ Access Time (ns)		30	35	50

■ PACKAGES



MBM29DL16XTD/BD-70/90/12

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- **Compatible with JEDEC-standard commands**
Uses same software commands as E²PROMs
- **Compatible with JEDEC-standard world-wide pinouts**
48-pin TSOP(I) (Package suffix: PFTN – Normal Bend Type, PFTR – Reversed Bend Type)
48-ball FBGA (Package suffix: PBT)
- **Minimum 100,000 program/erase cycles**
- **High performance**
70 ns maximum access time
- **Sector erase architecture**
Eight 4K word and thirty one 32K word sectors in word mode
Eight 8K byte and thirty one 64K byte sectors in byte mode
Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Boot Code Sector Architecture**
T = Top sector
B = Bottom sector
- **Hidden ROM (Hi-ROM) region**
64K byte of Hi-ROM, accessible through a new “Hi-ROM Enable” command sequence
Factory serialized and protected to provide a secure electronic serial number (ESN)
- **WPI/ACC input pin**
At V_{IL}, allows protection of boot sectors, regardless of sector protection/unprotection status
At V_{IH}, allows removal of boot sector protection
At V_{ACC}, increases program performance
- **Embedded Erase™ Algorithms**
Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
Automatically writes and verifies data at specified address
- **Data Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready/Busy output (RY/ $\overline{\text{BY}}$)**
Hardware method for detection of program or erase cycle completion
- **Automatic sleep mode**
When addresses remain stable, automatically switch themselves to low power mode.
- **Low V_{CC} write inhibit $\leq 2.5 \text{ V}$**
- **Erase Suspend/Resume**
Suspends the erase operation to allow a read data and/or program in another sector within the same device
- **Sector group protection**
Hardware method disables any combination of sector groups from program or erase operations
- **Sector Group Protection Set function by Extended sector group protection command**
- **Fast Programming Function by Extended Command**
- **Temporary sector group unprotection**
Temporary sector group unprotection via the $\overline{\text{RESET}}$ pin.
- **In accordance with CFI (Common Flash Memory Interface)**

MBM29DL16XTD/BD-70/90/12

■ GENERAL DESCRIPTION

The MBM29DL16XTD/BD are a 16M-bit, 3.0 V-only Flash memory organized as 2M bytes of 8 bits each or 1M words of 16 bits each. The MBM29DL16XTD/BD are offered in a 48-pin TSOP(I) and 48-ball FBGA Package. These devices are designed to be programmed in-system with the standard system 3.0 V V_{CC} supply. 12.0 V V_{PP} and 5.0 V V_{CC} are not required for write or erase operations. The devices can also be reprogrammed in standard EPROM programmers.

MBM29DL16XTD/BD are organized into two banks, Bank 1 and Bank 2, which can be considered to be two separate memory arrays as far as certain operations are concerned. These devices are the same as Fujitsu's standard 3 V only Flash memories with the additional capability of allowing a normal non-delayed read access from a non-busy bank of the array while an embedded write (either a program or an erase) operation is simultaneously taking place on the other bank.

In the MBM29DL16XTD/BD, a new design concept is implemented, so called "Sliding Bank Architecture". Under this concept, the MBM29DL16XTD/BD can be produced a series of devices with different Bank 1/Bank 2 size combinations; 0.5 Mb/15.5 Mb, 2 Mb/14 Mb, 4 Mb/12 Mb, 8 Mb/8 Mb.

The standard MBM29DL16XTD/BD offer access times 70 ns, 90 ns and 120 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the devices have separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$), and output enable ($\overline{OE}$) controls.

The MBM29DL16XTD/BD are pin and command set compatible with JEDEC standard E²PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the devices is similar to reading from 5.0 V and 12.0 V Flash or EPROM devices.

The MBM29DL16XTD/BD are programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in about 0.5 seconds. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the devices automatically time the erase pulse widths and verify proper cell margin.

A sector is typically erased and verified in 1.0 second. (If already completely preprogrammed.)

The devices also feature a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors. The MBM29DL16XTD/BD are erased when shipped from the factory.

The devices feature single 3.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{Data}$ Polling of DQ₇, by the Toggle Bit feature on DQ₆, or the RY/ $\overline{BY}$ output pin. Once the end of a program or erase cycle has been completed, the devices internally reset to the read mode.

Fujitsu's Flash technology combines years of EPROM and E²PROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MBM29DL16XTD/BD memories electrically erase the entire chip or all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The bytes/words are programmed one byte/word at a time using the EPROM programming mechanism of hot electron injection.

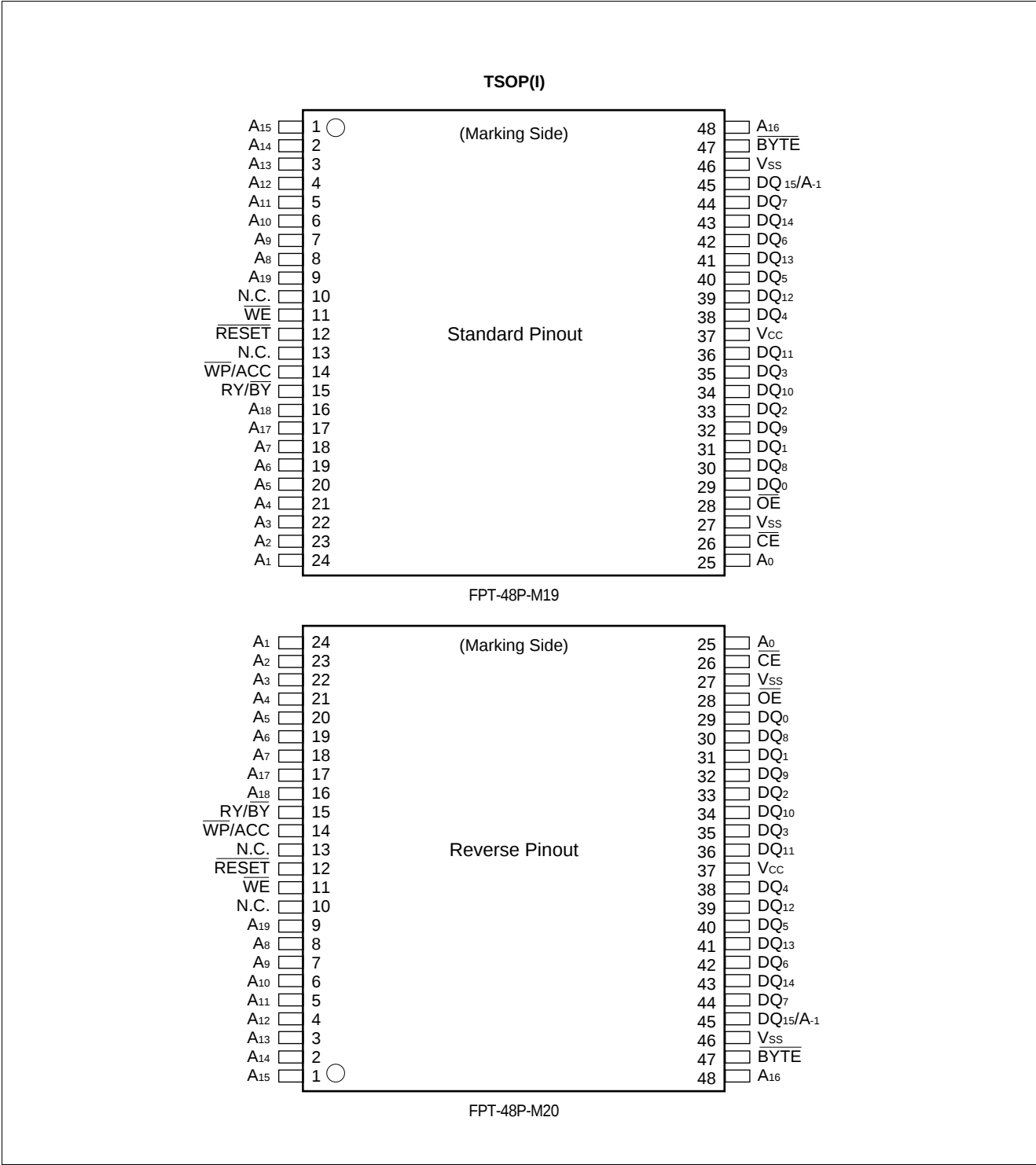
MBM29DL16XTD/BD-70/90/12

Table 1 MBM29DL16XTD/BD Device Bank Divisions

Device Part Number	Organization	Bank 1		Bank 2	
		Megabits	Sector Sizes	Megabits	Sector Sizes
MBM29DL161TD/BD	× 8/× 16	0.5 Mbit	Eight 8K byte/4K word	15.5 Mbit	Thirty-one 64K byte/32K word
MBM29DL162TD/BD		2 Mbit	Eight 8K byte/4K word, three 64K byte/32K word	14 Mbit	Twenty-eight 64K byte/32K word
MBM29DL163TD/BD		4 Mbit	Eight 8K byte/4K word, seven 64K byte/32K word	12 Mbit	Twenty-four 64K byte/32K word
MBM29DL164TD/BD		8 Mbit	Eight 8K byte/4K word, fifteen 64K byte/32K word	8 Mbit	Sixteen 64K byte/32K word

MBM29DL16XTD/BD-70/90/12

PIN ASSIGNMENTS

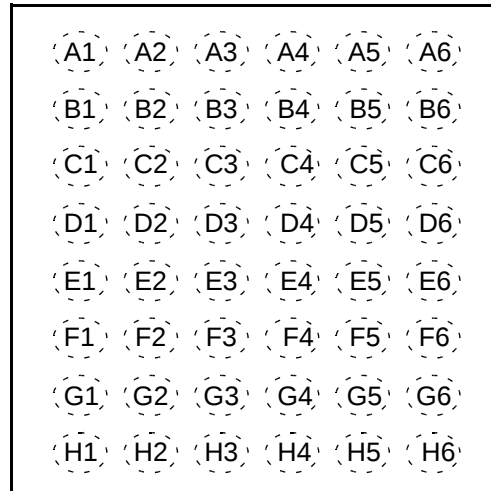


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MBM29DL16XTD/BD-70/90/12

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FBGA
(TOP VIEW)
Marking side

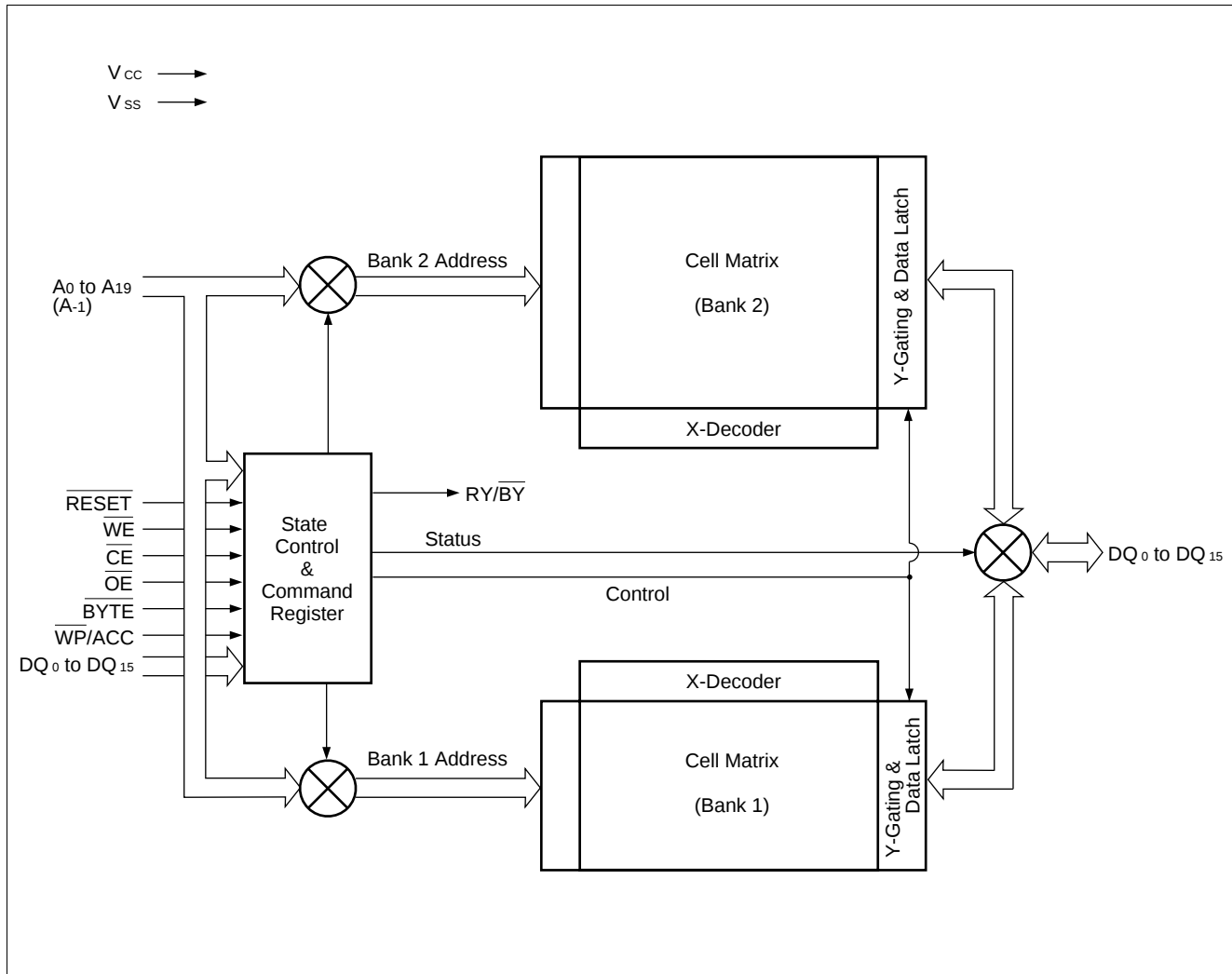


(BGA-48P-M13)

A1	A ₃	A2	A ₇	A3	RY/ $\overline{\text{BY}}$	A4	$\overline{\text{WE}}$	A5	A ₉	A6	A ₁₃
B1	A ₄	B2	A ₁₇	B3	$\overline{\text{WP/ACC}}$	B4	$\overline{\text{RESET}}$	B5	A ₈	B6	A ₁₂
C1	A ₂	C2	A ₆	C3	A ₁₈	C4	N.C.	C5	A ₁₀	C6	A ₁₄
D1	A ₁	D2	A ₅	D3	N.C.	D4	A ₁₉	D5	A ₁₁	D6	A ₁₅
E1	A ₀	E2	DQ ₀	E3	DQ ₂	E4	DQ ₅	E5	DQ ₇	E6	A ₁₆
F1	$\overline{\text{CE}}$	F2	DQ ₈	F3	DQ ₁₀	F4	DQ ₁₂	F5	DQ ₁₄	F6	$\overline{\text{BYTE}}$
G1	$\overline{\text{OE}}$	G2	DQ ₉	G3	DQ ₁₁	G4	V _{CC}	G5	DQ ₁₃	G6	DQ ₁₅ /A ₋₁
H1	V _{SS}	H2	DQ ₁	H3	DQ ₃	H4	DQ ₄	H5	DQ ₆	H6	V _{SS}

MBM29DL16XTD/BD-70/90/12

■ BLOCK DIAGRAM



MBM29DL16XTD/BD-70/90/12

■ LOGIC SYMBOL

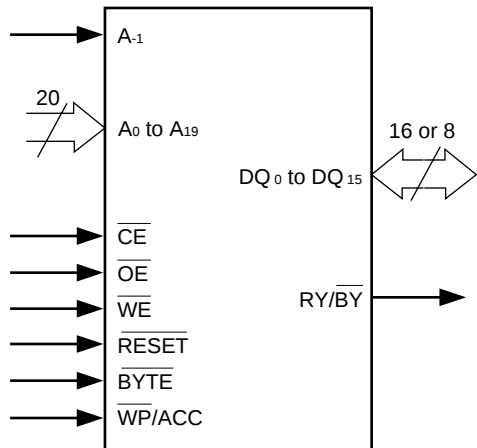


Table 2 MBM29DL16XTD/BD Pin Configuration

Pin	Function
A-1, A0 to A19	Address Inputs
DQ0 to DQ15	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RY/ $\overline{BY}$	Ready/Busy Output
$\overline{RESET}$	Hardware Reset Pin/Temporary Sector Group Unprotection
$\overline{BYTE}$	Selects 8-bit or 16-bit mode
$\overline{WP/ACC}$	Hardware Write Protection/Program Acceleration
N.C.	No Internal Connection
Vss	Device Ground
Vcc	Device Power Supply

MBM29DL16XTD/BD-70/90/12

■ DEVICE BUS OPERATION

Table 3 MBM29DL16XTD/BD User Bus Operations ($\overline{\text{BYTE}} = V_{IH}$)

Operation	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A ₀	A ₁	A ₆	A ₉	DQ ₀ to DQ ₁₅	$\overline{\text{RESET}}$	$\overline{\text{WP/ACC}}$
Auto-Select Manufacturer Code (1)	L	L	H	L	L	L	V _{ID}	Code	H	X
Auto-Select Device Code (1)	L	L	H	H	L	L	V _{ID}	Code	H	X
Read (3)	L	L	H	A ₀	A ₁	A ₆	A ₉	D _{OUT}	H	X
Standby	H	X	X	X	X	X	X	HIGH-Z	H	X
Output Disable	L	H	H	X	X	X	X	HIGH-Z	H	X
Write (Program/Erase)	L	H	L	A ₀	A ₁	A ₆	A ₉	D _{IN}	H	X
Enable Sector Group Protection (2), (4)	L	V _{ID}		L	H	L	V _{ID}	X	H	X
Verify Sector Group Protection (2), (4)	L	L	H	L	H	L	V _{ID}	Code	H	X
Temporary Sector Group Unprotection (5)	X	X	X	X	X	X	X	X	V _{ID}	X
Reset (Hardware)/Standby	X	X	X	X	X	X	X	HIGH-Z	L	X
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	L

Table 4 MBM29DL16XTD/BD User Bus Operations ($\overline{\text{BYTE}} = V_{IL}$)

Operation	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	DQ ₁₅ / A ₋₁	A ₀	A ₁	A ₆	A ₉	DQ ₀ to DQ ₇	$\overline{\text{RESET}}$	$\overline{\text{WP/ACC}}$
Auto-Select Manufacturer Code (1)	L	L	H	L	L	L	L	V _{ID}	Code	H	X
Auto-Select Device Code (1)	L	L	H	L	H	L	L	V _{ID}	Code	H	X
Read (3)	L	L	H	A ₋₁	A ₀	A ₁	A ₆	A ₉	D _{OUT}	H	X
Standby	H	X	X	X	X	X	X	X	HIGH-Z	H	X
Output Disable	L	H	H	X	X	X	X	X	HIGH-Z	H	X
Write (Program/Erase)	L	H	L	A ₋₁	A ₀	A ₁	A ₆	A ₉	D _{IN}	H	X
Enable Sector Group Protection (2), (4)	L	V _{ID}		L	L	H	L	V _{ID}	X	H	X
Verify Sector Group Protection (2), (4)	L	L	H	L	L	H	L	V _{ID}	Code	H	X
Temporary Sector Group Unprotection (5)	X	X	X	X	X	X	X	X	X	V _{ID}	X
Reset (Hardware)/Standby	X	X	X	X	X	X	X	X	HIGH-Z	L	X
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	L

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH},  = Pulse input. See DC Characteristics for voltage levels.

- Notes: 1. Manufacturer and device codes may also be accessed via a command register write sequence. See Table 12.
2. Refer to the section on Sector Group Protection.
3. $\overline{\text{WE}}$ can be V_{IL} if $\overline{\text{OE}}$ is V_{IL}, $\overline{\text{OE}}$ at V_{IH} initiates the write operations.
4. V_{CC} = 3.3 V ± 10%
5. It is also used for the extended sector group protection.

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■ ABSOLUTE MAXIMUM RATINGS(See WARNING)

Parameter	Symbol	Conditions	Rating		Unit
			Min.	Max.	
Storage Temperature	T _{stg}	—	−55	+125	°C
Ambient Temperature with Power Applied	T _A	—	−40	+85	°C
Voltage with respect to Ground All pins except A ₉ , $\overline{\text{OE}}$, $\overline{\text{RESET}}$ (Note 1)	V _{IN} , V _{OUT}	—	−0.5	V _{CC} +0.5	V
Power Supply Voltage (Note 1)	V _{CC}	—	−0.5	+4.0	V
A ₉ , $\overline{\text{OE}}$, and $\overline{\text{RESET}}$ (Note 2)	V _{IN}	—	−0.5	+13.0	V
$\overline{\text{WP/ACC}}$ (Note 3)	V _{IN}	—	−0.5	+10.5	V

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

- Notes: 1. Minimum DC voltage on input or I/O pins are −0.5 V. During voltage transitions, inputs may negative overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins are V_{CC} +0.5 V. During voltage transitions, outputs may positive overshoot to V_{CC} +2.0 V for periods of up to 20 ns.
2. Minimum DC input voltage on A₉, $\overline{\text{OE}}$ and $\overline{\text{RESET}}$ pins are −0.5 V. During voltage transitions, A₉, $\overline{\text{OE}}$ and $\overline{\text{RESET}}$ pins may negative overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC input voltage on A₉, $\overline{\text{OE}}$ and $\overline{\text{RESET}}$ pins are +13.0 V which may positive overshoot to 14.0 V for periods of up to 20 ns. when V_{CC} is applied.
3. Minimum DC input voltage on $\overline{\text{WP/ACC}}$ pin is −0.5 V. During voltage transitions, $\overline{\text{WP/ACC}}$ pin may negative overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC input voltage on $\overline{\text{WP/ACC}}$ pin is when V_{CC} is applied.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value		Unit
			Min.	Max.	
Ambient Temperature	T _A	MBM29DL16XTD/BD-70	−20	+70	°C
		MBM29DL16XTD/BD-90/12	−40	+85	°C
Power Supply Voltage	V _{CC}	MBM29DL16XTD/BD-70	+3.0	+3.6	V
		MBM29DL16XTD/BD-90/12	+2.7	+3.6	V

Operating ranges define those limits between which the functionality of the devices are guaranteed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

MBM29DL16XTD/BD-70/90/12

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

Parameter	Symbol	Conditions	Value		Unit
			Min.	Max.	
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC} , $V_{CC} = V_{CC}$ Max.	-1.0	+1.0	μA
Output Leakage Current	I_{LO}	$V_{OUT} = V_{SS}$ to V_{CC} , $V_{CC} = V_{CC}$ Max.	-1.0	+1.0	μA
A_9 , $\overline{OE}$, $\overline{RESET}$ Inputs Leakage Current	I_{LIT}	$V_{CC} = V_{CC}$ Max. A_9 , $\overline{OE}$, $\overline{RESET} = 12.5$ V	—	35	μA
V _{CC} Active Current (Note 1)	I_{CC1}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, $f = 5$ MHz	—	13	mA
		Byte		15	
		$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, $f = 1$ MHz	—	7	mA
		Word		7	
V _{CC} Active Current (Note 2)	I_{CC2}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	—	35	mA
V _{CC} Current (Standby)	I_{CC3}	$V_{CC} = V_{CC}$ Max., $\overline{CE} = V_{CC} \pm 0.3$ V, $\overline{RESET} = V_{CC} \pm 0.3$ V	—	5	μA
V _{CC} Current (Standby, Reset)	I_{CC4}	$V_{CC} = V_{CC}$ Max., $\overline{WP}/ACC = V_{CC} \pm 0.3$ V, $\overline{RESET} = V_{SS} \pm 0.3$ V	—	5	μA
V _{CC} Current (Automatic Sleep Mode) (Note 3)	I_{CC5}	$V_{CC} = V_{CC}$ Max., $\overline{CE} = V_{SS} \pm 0.3$ V, $\overline{RESET} = V_{CC} \pm 0.3$ V $V_{IN} = V_{CC} \pm 0.3$ V or $V_{SS} \pm 0.3$ V	—	5	μA
V _{CC} Active Current (Note 5) (Read-While-Program)	I_{CC6}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	—	48	mA
		Byte	—	50	
V _{CC} Active Current (Note 5) (Read-While-Erase)	I_{CC7}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	—	48	mA
		Word	—	50	
V _{CC} Active Current (Erase-Suspend-Program)	I_{CC8}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	—	35	mA
ACC Accelerated Program Current	I_{ACC}	$V_{CC} = V_{CC}$ Max. $\overline{WP}/ACC = V_{ACC}$ Max.	—	20	mA
Input Low Level	V_{IL}	—	-0.5	0.6	V
Input High Level	V_{IH}	—	2.0	$V_{CC}+0.3$	V
Voltage for $\overline{WP}/ACC$ Sector Protection/Unprotection and Program Acceleration	V_{ACC}	—	8.5	9.5	V
Voltage for Autoselect and Sector Protection (A_9 , $\overline{OE}$, $\overline{RESET}$) (Note 4)	V_{ID}	—	11.5	12.5	V

(Continued)

- Notes: 1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component.
 2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
 3. Automatic sleep mode enables the low power mode when address remain stable for 150 ns.
 4. Applicable for only V_{CC} applying.
 5. Embedded Algorithm (program or erase) is in progress. (@5 MHz)

MBM29DL16XTD/BD-70/90/12

(Continued)

Parameter	Symbol	Conditions	Value		Unit
			Min.	Max.	
Output Low Voltage Level	V_{OL}	$I_{OL} = 4.0 \text{ mA}$, $V_{CC} = V_{CC} \text{ Min.}$	—	0.45	V
Output High Voltage Level	V_{OH1}	$I_{OH} = -2.0 \text{ mA}$, $V_{CC} = V_{CC} \text{ Min.}$	2.4	—	V
	V_{OH2}	$I_{OH} = -100 \text{ }\mu\text{A}$	$V_{CC}-0.4$	—	V
Low V_{CC} Lock-Out Voltage	V_{LKO}	—	2.3	2.5	V

- Notes: 1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component.
 2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
 3. Automatic sleep mode enables the low power mode when address remain stable for 150 ns.
 4. Applicable for only V_{CC} applying.
 5. Embedded Algorithm (program or erase) is in progress. (@5 MHz)

MBM29DL16XTD/BD-70/90/12

2. AC Characteristics

• Read Only Operations Characteristics

Parameter Symbols		Description	Test Setup		70 (Note)	90 (Note)	12 (Note)	Unit
JEDEC	Standard							
t_{AVAV}	t_{RC}	Read Cycle Time	—	Min.	70	90	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	Max.	70	90	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Max.	70	90	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	—	Max.	30	35	50	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High-Z	—	Max.	25	30	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High-Z	—	Max.	25	30	30	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First	—	Min.	0	0	0	ns
—	t_{READY}	$\overline{RESET}$ Pin Low to Read Mode	—	Max.	20	20	20	μs
—	t_{ELFL} t_{ELFH}	$\overline{CE}$ or $\overline{BYTE}$ Switching Low or High	—	Max.	5	5	5	ns

Note: Test Conditions:

Output Load: 1 TTL gate and 30 pF (MBM29DL16XTD/BD-70)

1 TTL gate and 100 pF (MBM29DL16XTD/BD-90/12)

Input rise and fall times: 5 ns

Input pulse levels: 0.0 V to 3.0 V

Timing measurement reference level

Input: 1.5 V

Output: 1.5 V

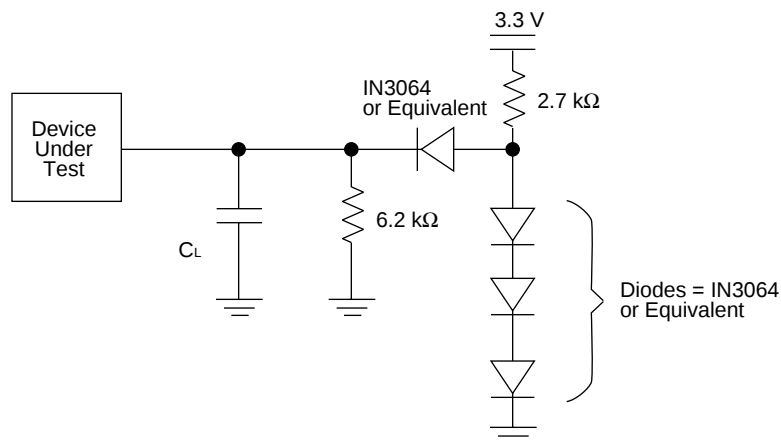


Figure 4 Test Conditions

MBM29DL16XTD/BD-70/90/12

• Write/Erase/Program Operations

Parameter Symbols		Description		70	90	12	Unit
JEDEC	Standard						
t_{AVAV}	t_{WC}	Write Cycle Time	Min.	70	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min.	0	0	0	ns
—	t_{ASO}	Address Setup Time to $\overline{OE}$ Low During Toggle Bit Polling	Min.	12	15	15	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min.	45	45	50	ns
—	t_{AHT}	Address Hold Time from $\overline{CE}$ or $\overline{OE}$ High During Toggle Bit Polling	Min.	0	0	0	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min.	30	35	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min.	0	0	0	ns
—	t_{OEHL}	Output Enable Hold Time	Read	Min.	0	0	ns
			Toggle and Data Polling	Min.	10	10	ns
—	t_{CEPH}	$\overline{CE}$ High During Toggle Bit Polling	Min.	20	20	20	ns
—	t_{OEPH}	$\overline{OE}$ High During Toggle Bit Polling	Min.	20	20	20	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write	Min.	0	0	0	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write	Min.	0	0	0	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup Time	Min.	0	0	0	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time	Min.	0	0	0	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time	Min.	0	0	0	ns
t_{EHWL}	t_{WH}	$\overline{WE}$ Hold Time	Min.	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min.	35	35	50	ns
t_{ELEH}	t_{CP}	$\overline{CE}$ Pulse Width	Min.	35	35	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min.	25	30	30	ns
t_{EHEL}	t_{CPH}	$\overline{CE}$ Pulse Width High	Min.	25	30	30	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	Typ.	8	8	8	μ s
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)	Typ.	1	1	1	sec
—	t_{VCS}	V_{CC} Setup Time	Min.	50	50	50	μ s
—	t_{VIDR}	Rise Time to V_{ID} (Note 2)	Min.	500	500	500	ns
—	t_{VACCR}	Rise Time to V_{ACC} (Note 2)	Min.	500	500	500	ns
—	t_{VLHT}	Voltage Transition Time (Note 2)	Min.	4	4	4	μ s
—	t_{WPP}	Write Pulse Width (Note 2)	Min.	100	100	100	μ s
—	t_{OESP}	$\overline{OE}$ Setup Time to $\overline{WE}$ Active (Note 2)	Min.	4	4	4	μ s

(Continued)

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(Continued)

Parameter Symbols		Description		70	90	12	Unit
JEDEC	Standard						
—	t_{CSP}	$\overline{CE}$ Setup Time to $\overline{WE}$ Active (Note 2)	Min.	4	4	4	μs
—	t_{RB}	Recover Time From $RY/\overline{BY}$	Min.	0	0	0	ns
—	t_{RP}	$\overline{RESET}$ Pulse Width	Min.	500	500	500	ns
—	t_{RH}	$\overline{RESET}$ High Level Period before Read	Min.	200	200	200	ns
—	t_{FLQZ}	$\overline{BYTE}$ Switching Low to Output High-Z	Max.	30	30	40	ns
—	t_{FHQV}	$\overline{BYTE}$ Switching High to Output Active	Max.	70	90	120	ns
—	t_{BUSY}	Program/Erase Valid to $RY/\overline{BY}$ Delay	Max.	90	90	90	ns
—	t_{EOE}	Delay Time from Embedded Output Enable	Max.	70	90	120	ns
—	t_{TOW}	Erase Time-out Time	Min.	50	50	50	μs
—	t_{SPD}	Erase Suspend Transition Time	Max.	20	20	20	μs

Notes: 1. This does not include the preprogramming time.
 2. This timing is for Sector Group Protection operation.

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■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max.		
Sector Erase Time	—	1	10	sec	Excludes programming time prior to erasure
Word Programming Time	—	16	360	μs	Excludes system-level overhead
Byte Programming Time	—	8	300	μs	
Chip Programming Time	—	—	50	sec	Excludes system-level overhead
Program/Erase Cycle	100,000	—	—	cycles	—

■ PIN CAPACITANCE

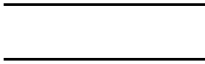
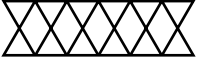
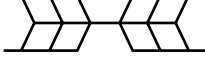
Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0	6	7.5	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0	8.5	12	pF
C _{IN2}	Control Pin Capacitance	V _{IN} = 0	8	10	pF
C _{IN3}	$\overline{WP}/ACC$ Pin Capacitance	V _{IN} = 0	17	18	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHzs

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■ TIMING DIAGRAM

• Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	"H" or "L" Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

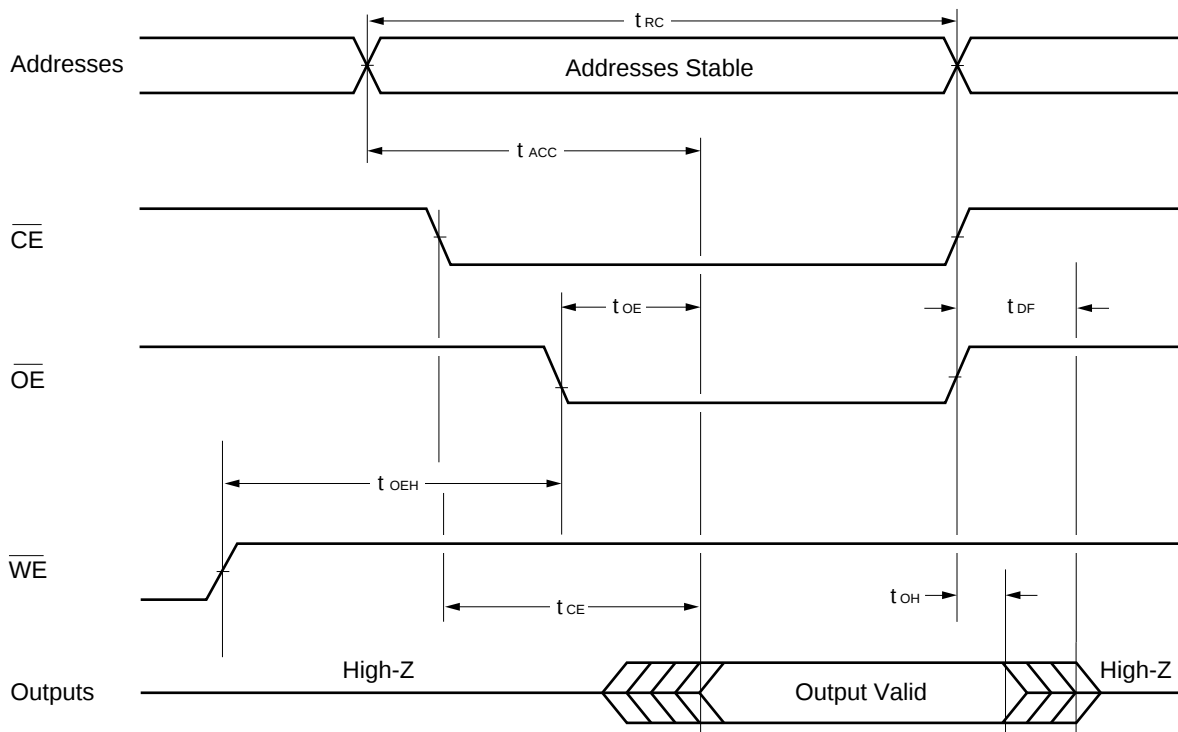
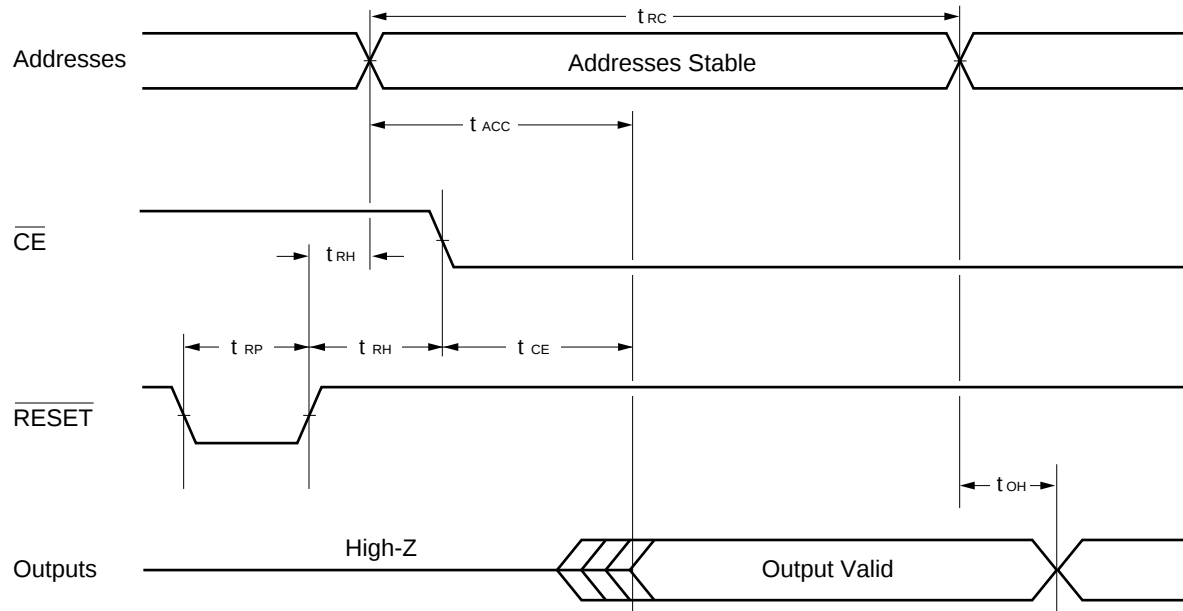
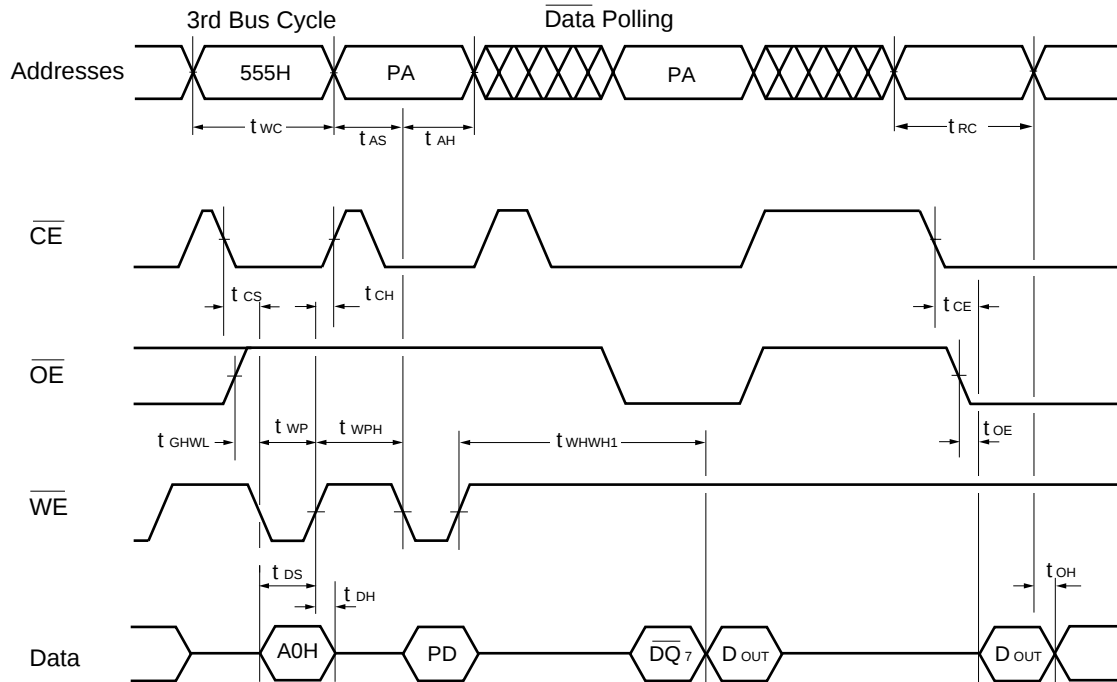


Figure 5.1 AC Waveforms for Read Operations

MBM29DL16XTD/BD-70/90/12**Figure 5.2 AC Waveforms for Hardware Reset/Read Operations**

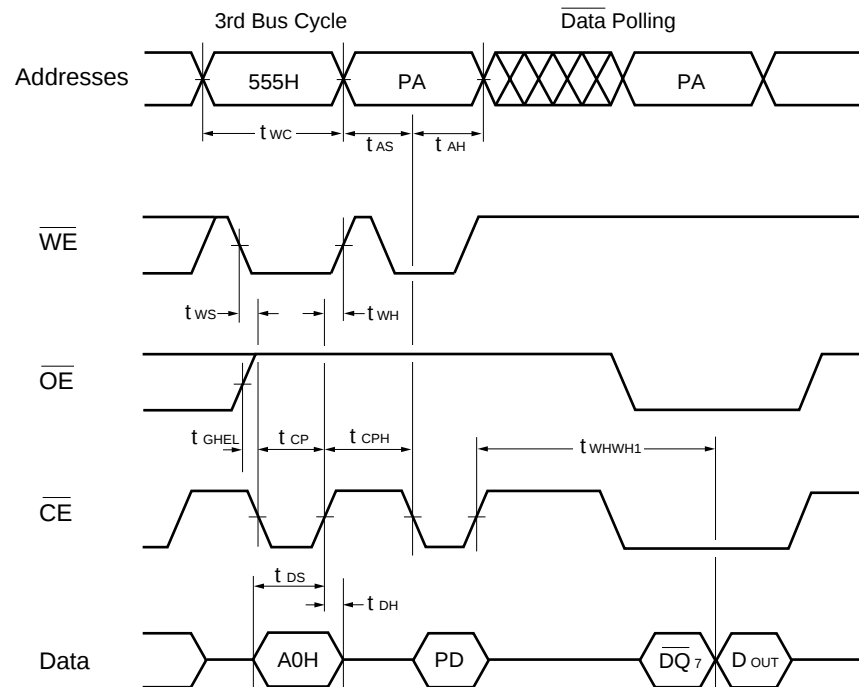
MBM29DL16XTD/BD-70/90/12



- Notes:
1. PA is address of the memory location to be programmed.
 2. PD is data to be programmed at byte address.
 3. $\overline{DQ}_7$ is the output of the complement of the data written to the device.
 4. DOUT is the output of the data written to the device.
 5. Figure indicates last two bus cycles out of four bus cycle sequence.
 6. These waveforms are for the $\times 16$ mode. (The addresses differ from $\times 8$ mode.)

Figure 6 AC Waveforms for Alternate $\overline{WE}$ Controlled Program Operations

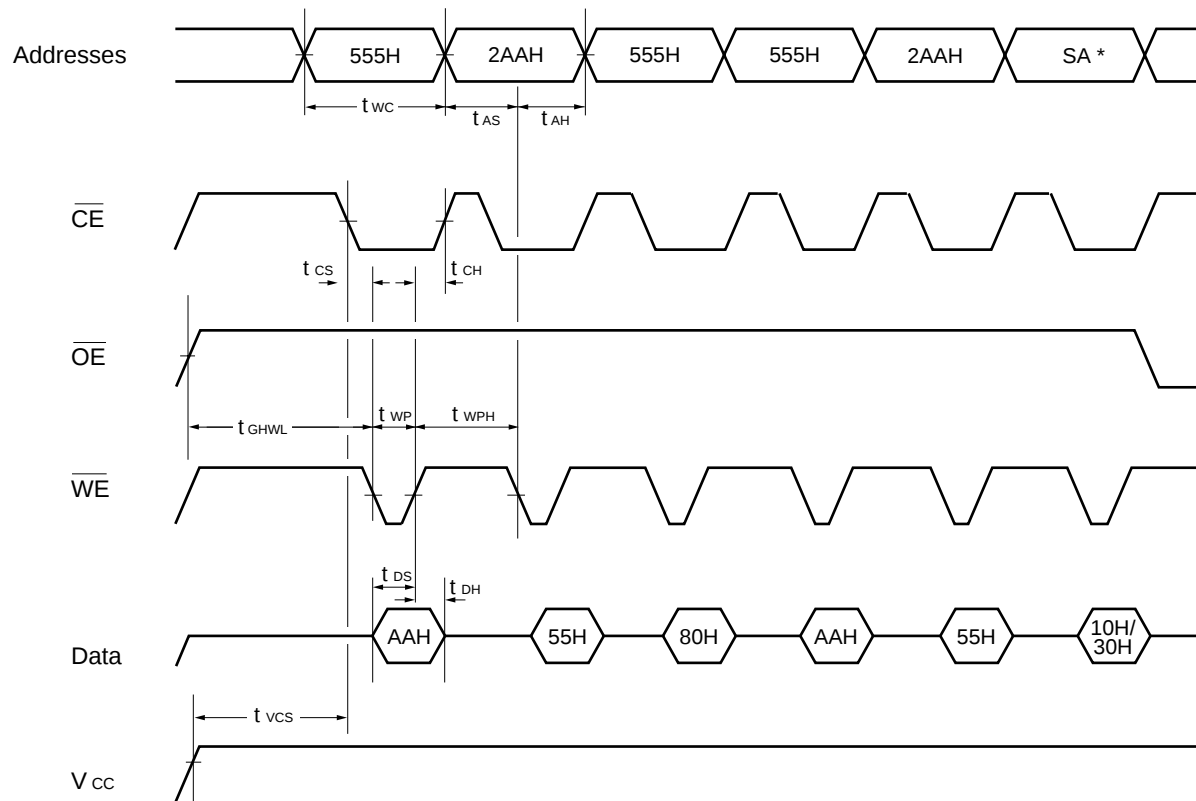
MBM29DL16XTD/BD-70/90/12



- Notes:
1. PA is address of the memory location to be programmed.
 2. PD is data to be programmed at byte address.
 3. $\overline{DQ}_7$ is the output of the complement of the data written to the device.
 4. D_{OUT} is the output of the data written to the device.
 5. Figure indicates last two bus cycles out of four bus cycle sequence.
 6. These waveforms are for the $\times 16$ mode. (The addresses differ from $\times 8$ mode.)

Figure 7 AC Waveforms for Alternate $\overline{CE}$ Controlled Program Operations

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* SA is the sector address for Sector Erase. Addresses = 555H (Word), AAH (Byte) for Chip Erase.

Note: These waveforms are for the $\times 16$ mode. (The addresses differ from $\times 8$ mode.)

Figure 8 AC Waveforms for Chip/Sector Erase Operations

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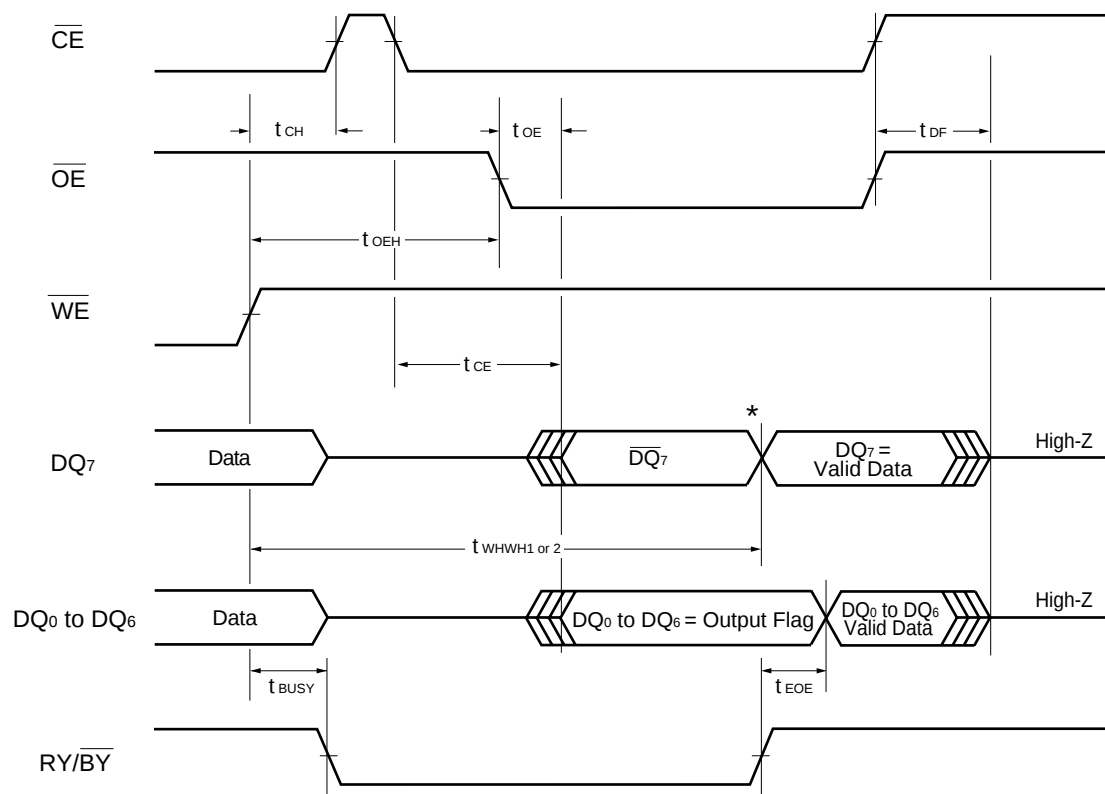
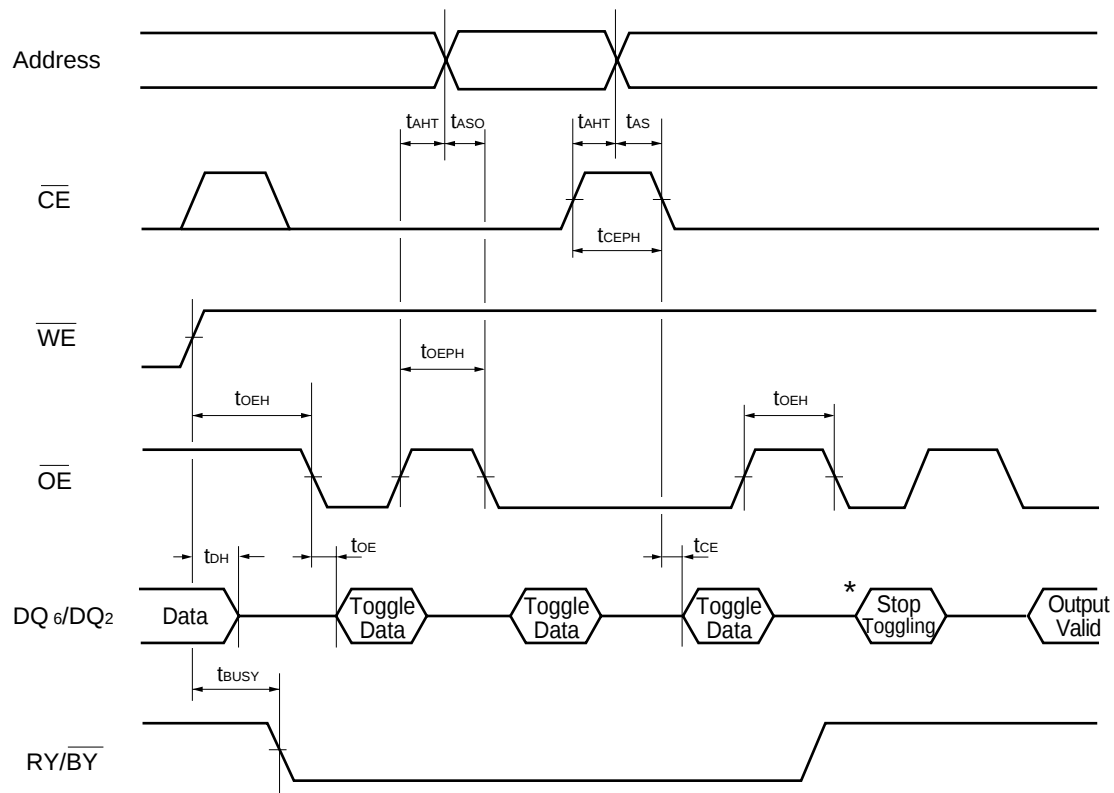


Figure 9 AC Waveforms for $\overline{\text{Data}}$ Polling during Embedded Algorithm Operations

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* : DQ₆ stops toggling (The device has completed the Embedded operation).

Figure 10 AC Waveforms for Toggle Bit I during Embedded Algorithm Operations

MBM29DL16XTD/BD-70/90/12

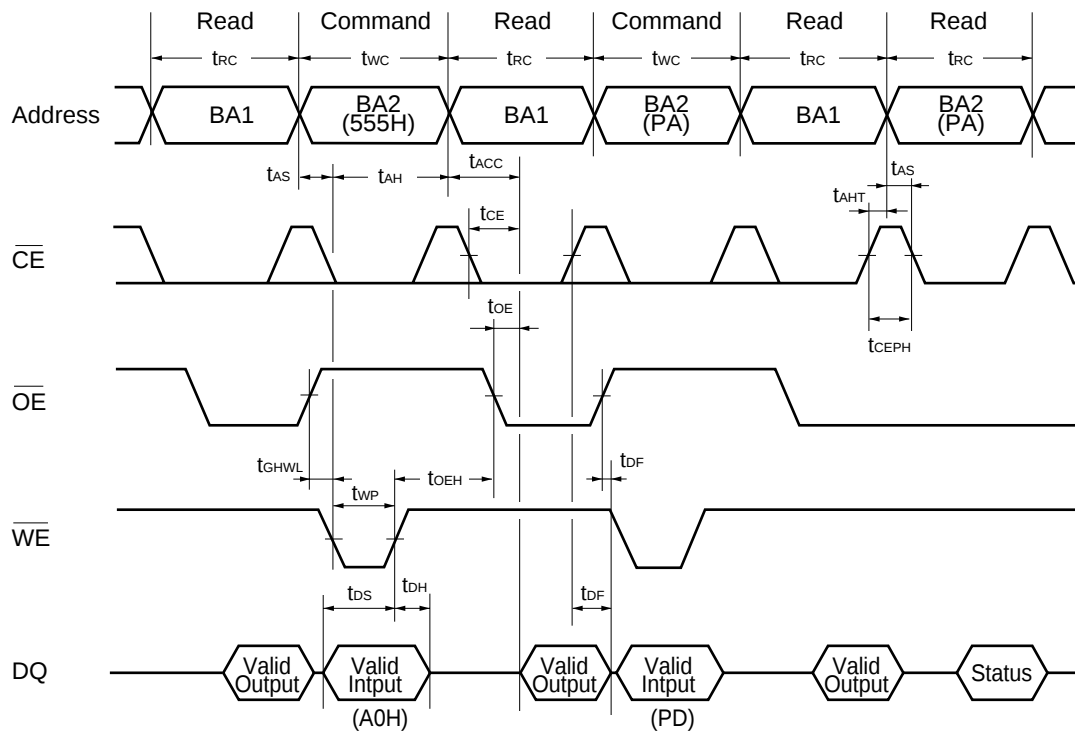
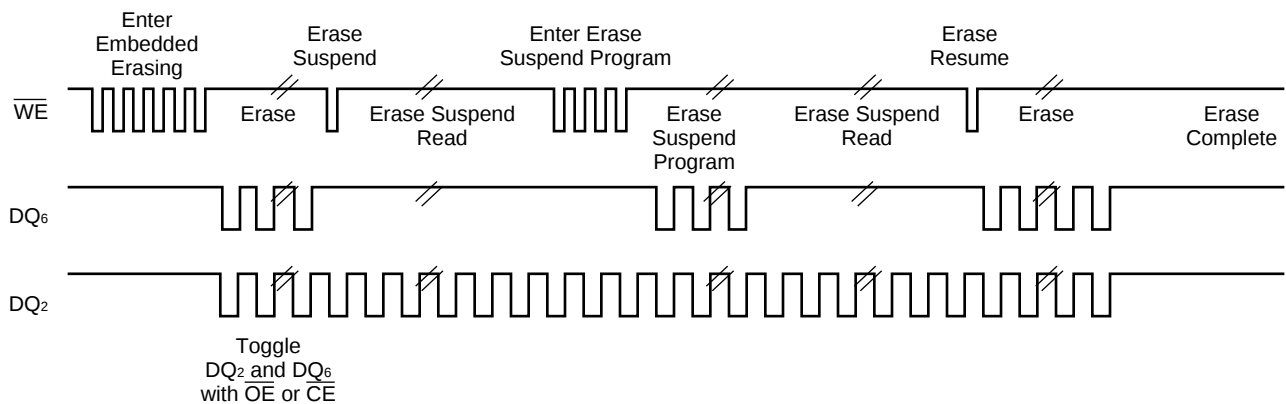


Figure 11 Bank-to-bank Read/Write Timing Diagram

Figure 12 DQ₂ vs. DQ₆

MBM29DL16XTD/BD-70/90/12

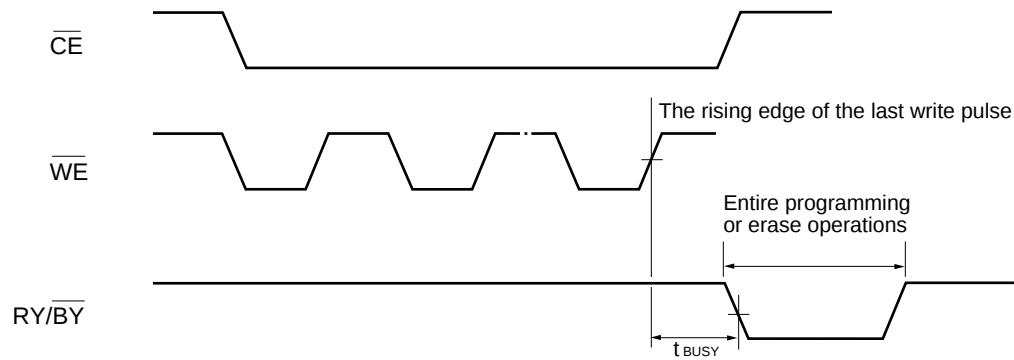


Figure 13 $RY/\overline{BY}$ Timing Diagram during Program/Erase Operations

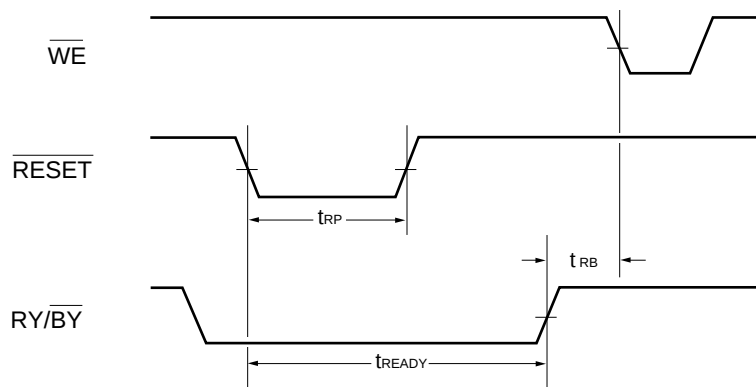
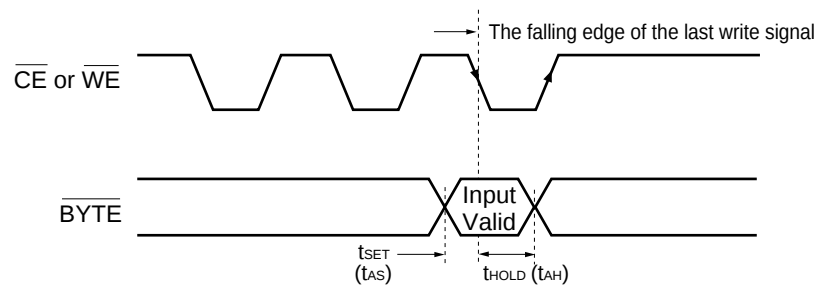
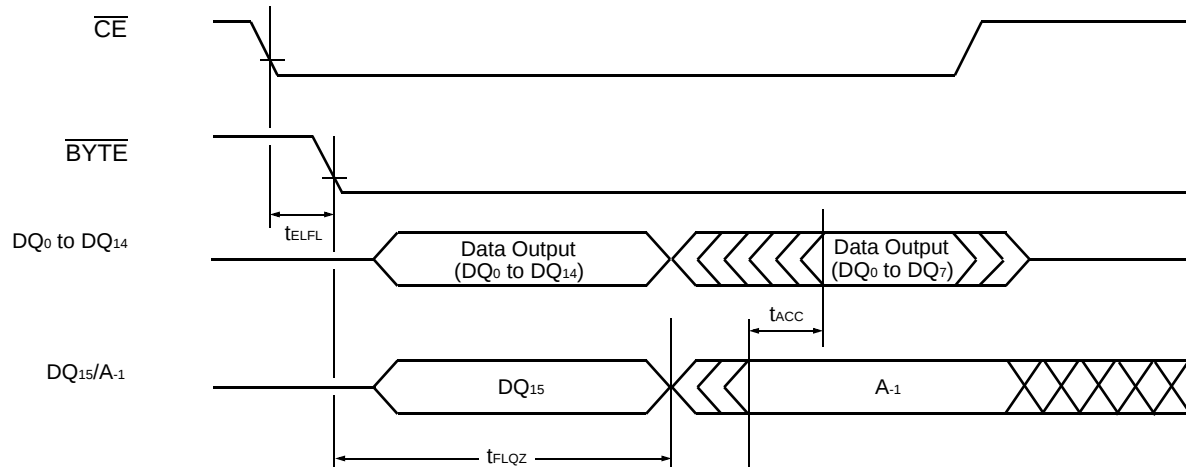
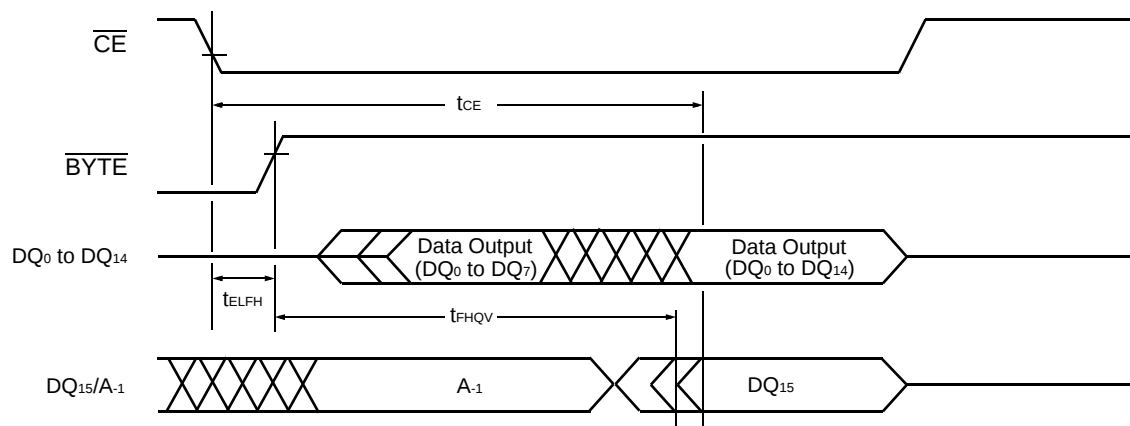
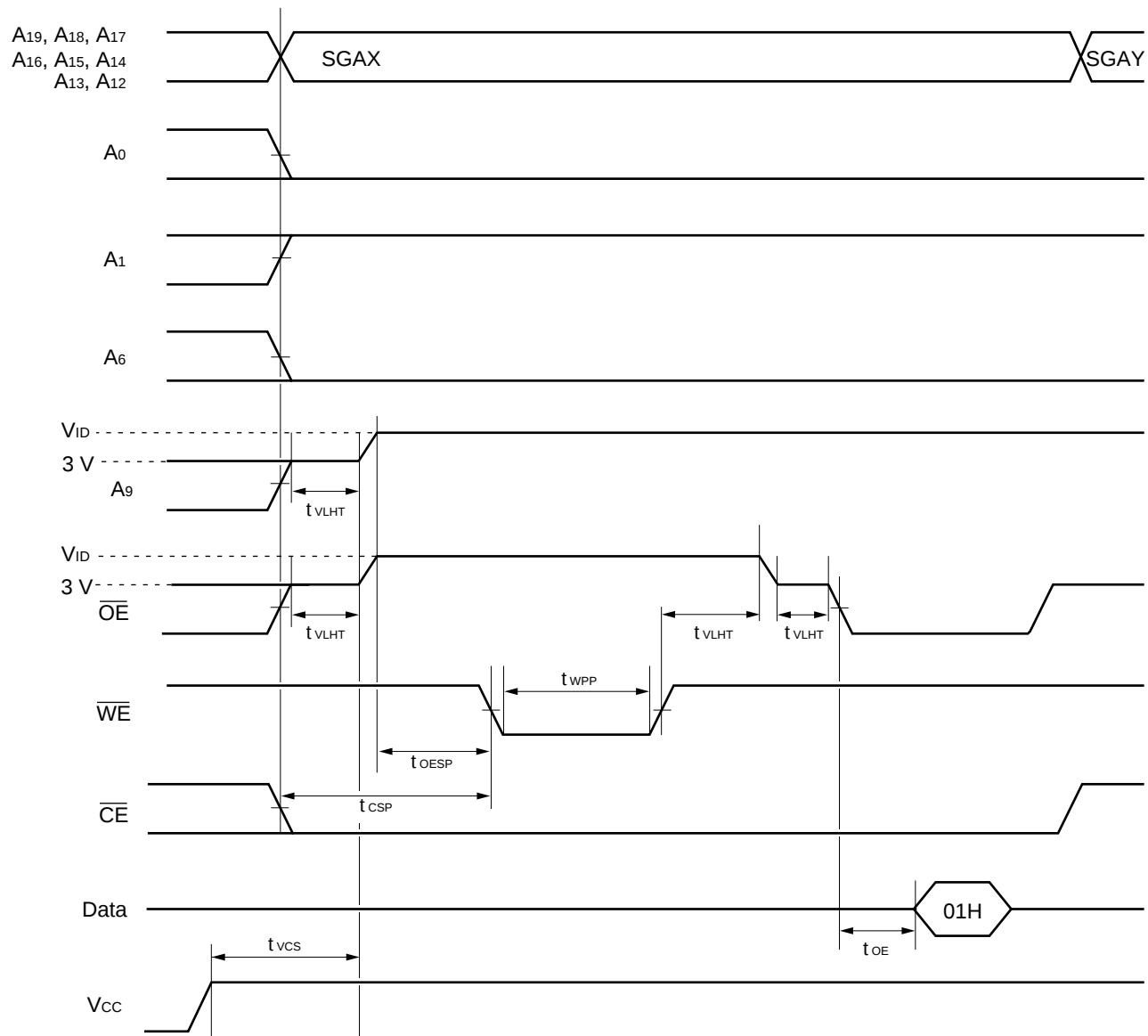


Figure 14 $\overline{RESET}$, $RY/\overline{BY}$ Timing Diagram

MBM29DL16XTD/BD-70/90/12



MBM29DL16XTD/BD-70/90/12



SGAX : Sector Group Address for initial sector

SGAY : Sector Group Address for next sector

Note: A-1 is V_{IL} on byte mode.

Figure 18 AC Waveforms for Sector Group Protection

MBM29DL16XTD/BD-70/90/12

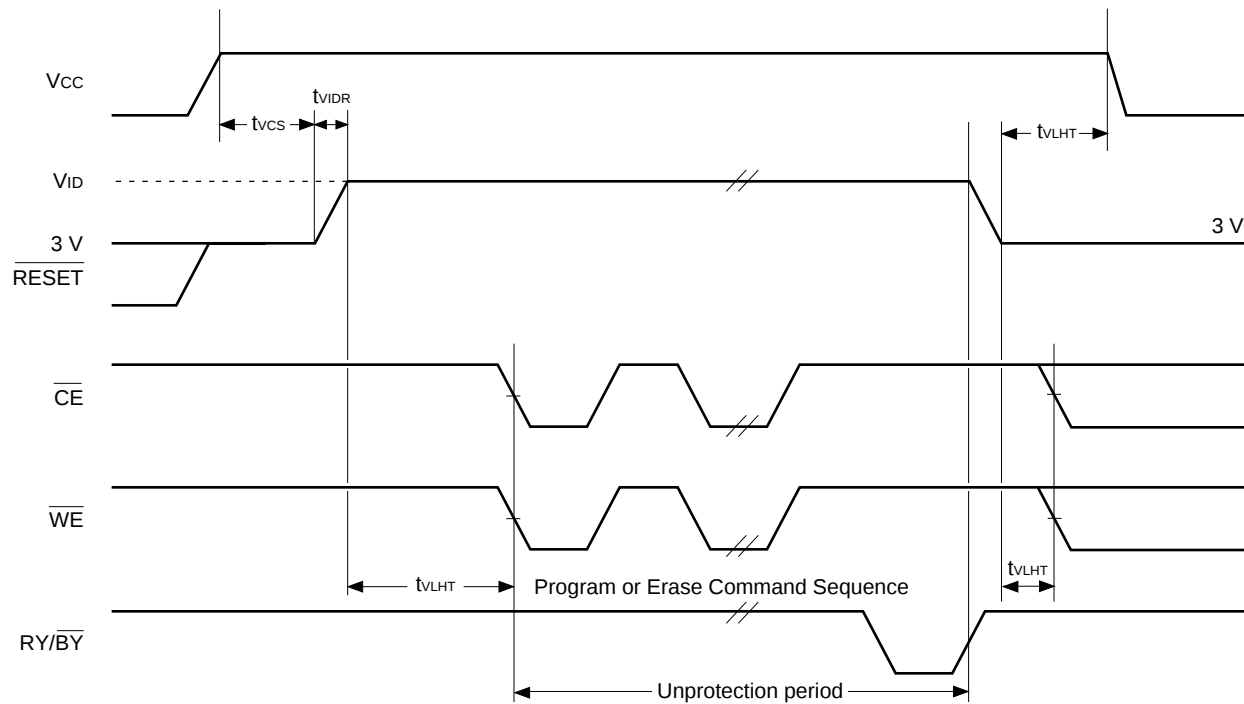
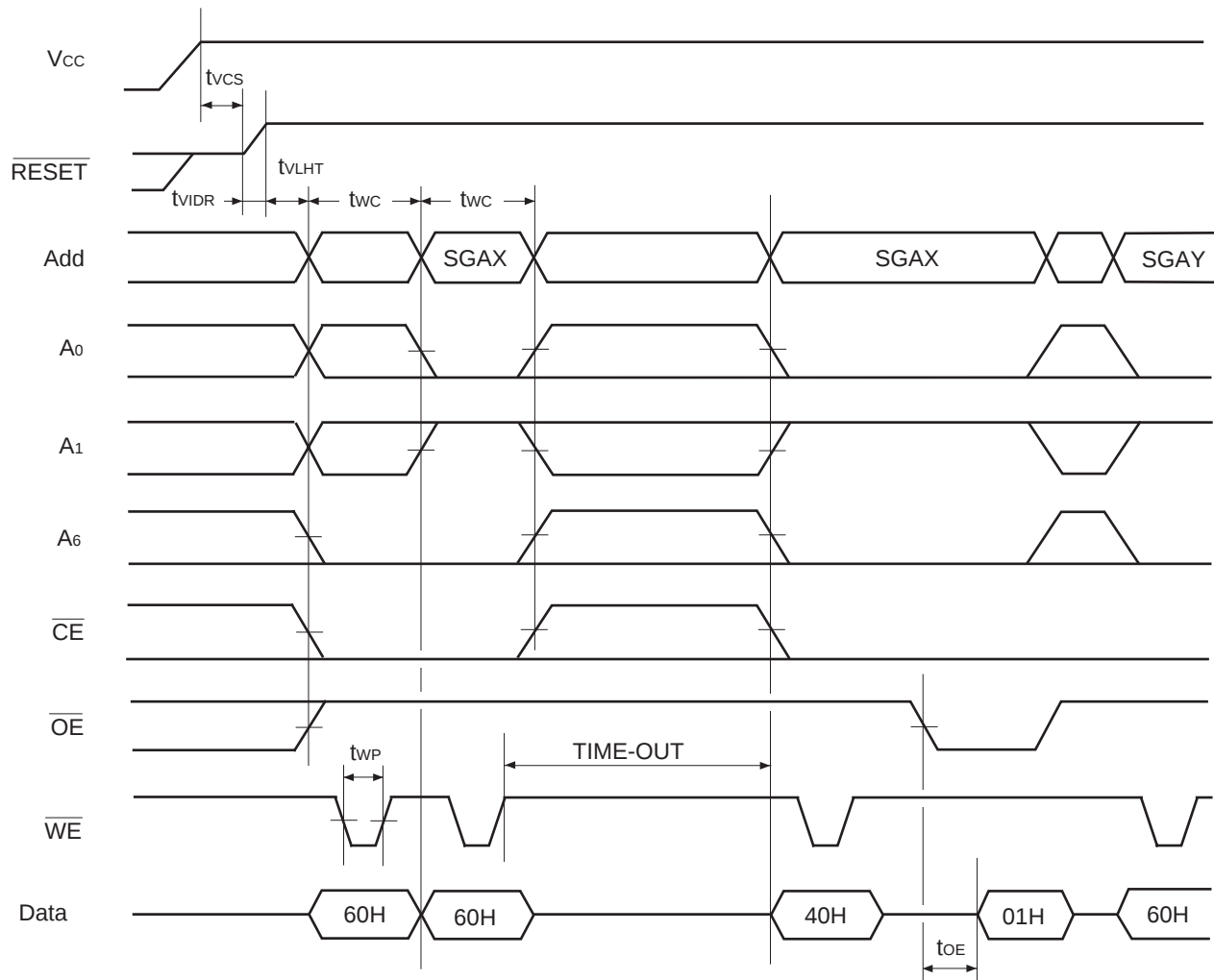


Figure 19 Temporary Sector Group Unprotection Timing Diagram

MBM29DL16XTD/BD-70/90/12



SGAX : Sector Group Address to be protected
 SGAY : Next Sector Group Address to be protected
 TIME-OUT : Time-Out window = 250 μ s (min)

Figure 20 Extended Sector Group Protection Timing Diagram



MBM29DL16XTD/BD-70/90/12

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE

Table 5.1 Sector Address Tables (MBM29DL161TD)

Bank	Sector	Sector Address								Sector Size (Kbytes/ Kwords)	(×8) Address Range	(×16) Address Range
		Bank Address										
		A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅						
Bank 2	SA0	0	0	0	0	0	X	X	X	64/32	000000H to 00FFFFH	000000H to 007FFFH
	SA1	0	0	0	0	1	X	X	X	64/32	010000H to 01FFFFH	008000H to 00FFFFH
	SA2	0	0	0	1	0	X	X	X	64/32	020000H to 02FFFFH	010000H to 017FFFH
	SA3	0	0	0	1	1	X	X	X	64/32	030000H to 03FFFFH	018000H to 01FFFFH
	SA4	0	0	1	0	0	X	X	X	64/32	040000H to 04FFFFH	020000H to 027FFFH
	SA5	0	0	1	0	1	X	X	X	64/32	050000H to 05FFFFH	028000H to 02FFFFH
	SA6	0	0	1	1	0	X	X	X	64/32	060000H to 06FFFFH	030000H to 037FFFH
	SA7	0	0	1	1	1	X	X	X	64/32	070000H to 07FFFFH	038000H to 03FFFFH
	SA8	0	1	0	0	0	X	X	X	64/32	080000H to 08FFFFH	040000H to 047FFFH
	SA9	0	1	0	0	1	X	X	X	64/32	090000H to 09FFFFH	048000H to 04FFFFH
	SA10	0	1	0	1	0	X	X	X	64/32	0A0000H to 0AFFFFH	050000H to 057FFFH
	SA11	0	1	0	1	1	X	X	X	64/32	0B0000H to 0BFFFFH	058000H to 05FFFFH
	SA12	0	1	1	0	0	X	X	X	64/32	0C0000H to 0CFFFFH	060000H to 067FFFH
	SA13	0	1	1	0	1	X	X	X	64/32	0D0000H to 0DFFFFH	068000H to 06FFFFH
	SA14	0	1	1	1	0	X	X	X	64/32	0E0000H to 0EFFFFH	070000H to 077FFFH
	SA15	0	1	1	1	1	X	X	X	64/32	0F0000H to 0FFFFFH	078000H to 07FFFFH
	SA16	1	0	0	0	0	X	X	X	64/32	100000H to 10FFFFH	080000H to 087FFFH
	SA17	1	0	0	0	1	X	X	X	64/32	110000H to 11FFFFH	088000H to 08FFFFH
	SA18	1	0	0	1	0	X	X	X	64/32	120000H to 12FFFFH	090000H to 097FFFH
	SA19	1	0	0	1	1	X	X	X	64/32	130000H to 13FFFFH	098000H to 09FFFFH
	SA20	1	0	1	0	0	X	X	X	64/32	140000H to 14FFFFH	0A0000H to 0A7FFFH
	SA21	1	0	1	0	1	X	X	X	64/32	150000H to 15FFFFH	0A8000H to 0AFFFFH
	SA22	1	0	1	1	0	X	X	X	64/32	160000H to 16FFFFH	0B0000H to 0B7FFFH
	SA23	1	0	1	1	1	X	X	X	64/32	170000H to 17FFFFH	0B8000H to 0BFFFFH
	SA24	1	1	0	0	0	X	X	X	64/32	180000H to 18FFFFH	0C0000H to 0C7FFFH
	SA25	1	1	0	0	1	X	X	X	64/32	190000H to 19FFFFH	0C8000H to 0CFFFFH
	SA26	1	1	0	1	0	X	X	X	64/32	1A0000H to 1AFFFFH	0D0000H to 0D7FFFH
	SA27	1	1	0	1	1	X	X	X	64/32	1B0000H to 1BFFFFH	0D8000H to 0DFFFFH
	SA28	1	1	1	0	0	X	X	X	64/32	1C0000H to 1CFFFFH	0E0000H to 0E7FFFH
	SA29	1	1	1	0	1	X	X	X	64/32	1D0000H to 1DFFFFH	0E8000H to 0EFFFFH
	SA30	1	1	1	1	0	X	X	X	64/32	1E0000H to 1EFFFFH	0F0000H to 0F7FFFH
Bank 1	SA31	1	1	1	1	1	0	0	0	8/4	1F0000H to 1F1FFFH	0F8000H to 0F8FFFH
	SA32	1	1	1	1	1	0	0	1	8/4	1F2000H to 1F3FFFH	0F9000H to 0F9FFFH
	SA33	1	1	1	1	1	0	1	0	8/4	1F4000H to 1F5FFFH	0FA000H to 0FAFFFH
	SA34	1	1	1	1	1	0	1	1	8/4	1F6000H to 1F7FFFH	0FB000H to 0FBFFFH
	SA35	1	1	1	1	1	1	0	0	8/4	1F8000H to 1F9FFFH	0FC000H to 0FCFFFH
	SA36	1	1	1	1	1	1	0	1	8/4	1FA000H to 1FBFFFH	0FD000H to 0FDFFFH
	SA37	1	1	1	1	1	1	1	0	8/4	1FC000H to 1FDFFFH	0FE000H to 0FEFFFH
	SA38	1	1	1	1	1	1	1	1	8/4	1FE000H to 1FFFFFH	0FF000H to 0FFFFFH

Note: The address range is A₁₉: A₁ if in byte mode ($\overline{\text{BYTE}} = V_{\text{IL}}$).
The address range is A₁₉: A₀ if in word mode ($\text{BYTE} = V_{\text{IH}}$)

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Table 5.2 Sector Address Tables (MBM29DL161BD)

Bank	Sector	Sector Address								Sector Size (Kbytes/ Kwords)	(×8) Address Range	(×16) Address Range
		Bank Address					A ₁₄	A ₁₃	A ₁₂			
		A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅						
Bank 2	SA38	1	1	1	1	1	X	X	X	64/32	1F0000H to 1FFFFFFH	0F8000H to 0FFFFFFH
	SA37	1	1	1	1	0	X	X	X	64/32	1E0000H to 1FFFFFFH	0F0000H to 0F7FFFH
	SA36	1	1	1	0	1	X	X	X	64/32	1D0000H to 1DFFFFH	0E8000H to 0EFFFFH
	SA35	1	1	1	0	0	X	X	X	64/32	1C0000H to 1CFFFFH	0E0000H to 0E7FFFH
	SA34	1	1	0	1	1	X	X	X	64/32	1B0000H to 1BFFFFH	0D8000H to 0DFFFFH
	SA33	1	1	0	1	0	X	X	X	64/32	1A0000H to 1AFFFFH	0D0000H to 0D7FFFH
	SA32	1	1	0	0	1	X	X	X	64/32	190000H to 19FFFFH	0C8000H to 0CFFFFH
	SA31	1	1	0	0	0	X	X	X	64/32	180000H to 18FFFFH	0C0000H to 0C7FFFH
	SA30	1	0	1	1	1	X	X	X	64/32	170000H to 17FFFFH	0B8000H to 0BFFFFH
	SA29	1	0	1	1	0	X	X	X	64/32	160000H to 16FFFFH	0B0000H to 0B7FFFH
	SA28	1	0	1	0	1	X	X	X	64/32	150000H to 15FFFFH	0A8000H to 0AFFFFH
	SA27	1	0	1	0	0	X	X	X	64/32	140000H to 14FFFFH	0A0000H to 0A7FFFH
	SA26	1	0	0	1	1	X	X	X	64/32	130000H to 13FFFFH	098000H to 09FFFFH
	SA25	1	0	0	1	0	X	X	X	64/32	120000H to 12FFFFH	090000H to 097FFFH
	SA24	1	0	0	0	X	X	X	X	64/32	110000H to 11FFFFH	088000H to 08FFFFH
	SA23	1	0	0	0	0	X	X	X	64/32	100000H to 10FFFFH	080000H to 087FFFH
	SA22	0	1	1	1	1	X	X	X	64/32	0F0000H to 0FFFFFFH	078000H to 07FFFFH
	SA21	0	1	1	1	0	X	X	X	64/32	0E0000H to 0EFFFFH	070000H to 077FFFH
	SA20	0	1	1	0	1	X	X	X	64/32	0D0000H to 0DFFFFH	068000H to 06FFFFH
	SA19	0	1	1	0	0	X	X	X	64/32	0C0000H to 0CFFFFH	060000H to 067FFFH
	SA18	0	1	0	1	1	X	X	X	64/32	0B0000H to 0BFFFFH	058000H to 05FFFFH
	SA17	0	1	0	1	0	X	X	X	64/32	0A0000H to 0AFFFFH	050000H to 057FFFH
	SA16	0	1	0	0	1	X	X	X	64/32	090000H to 09FFFFH	048000H to 04FFFFH
	SA15	0	1	0	0	0	X	X	X	64/32	080000H to 08FFFFH	040000H to 047FFFH
	SA14	0	0	1	1	1	X	X	X	64/32	070000H to 07FFFFH	038000H to 03FFFFH
	SA13	0	0	1	1	0	X	X	X	64/32	060000H to 06FFFFH	030000H to 037FFFH
	SA12	0	0	1	0	1	X	X	X	64/32	050000H to 05FFFFH	028000H to 02FFFFH
	SA11	0	0	1	0	0	X	X	X	64/32	040000H to 04FFFFH	020000H to 027FFFH
SA10	0	0	0	1	1	X	X	X	64/32	030000H to 03FFFFH	018000H to 01FFFFH	
SA9	0	0	0	1	0	X	X	X	64/32	020000H to 02FFFFH	010000H to 017FFFH	
SA8	0	0	0	0	1	X	X	X	64/32	010000H to 01FFFFH	008000H to 00FFFFH	
Bank 1	SA7	0	0	0	0	0	1	1	1	8/4	00E000H to 00FFFFH	007000H to 007FFFH
	SA6	0	0	0	0	0	1	1	0	8/4	00C000H to 00DFFFH	006000H to 006FFFH
	SA5	0	0	0	0	0	1	0	1	8/4	00A000H to 00BFFFH	005000H to 005FFFH
	SA4	0	0	0	0	0	1	0	0	8/4	008000H to 009FFFH	004000H to 004FFFH
	SA3	0	0	0	0	0	0	1	1	8/4	006000H to 007FFFH	003000H to 003FFFH
	SA2	0	0	0	0	0	0	1	0	8/4	004000H to 005FFFH	002000H to 002FFFH
	SA1	0	0	0	0	0	0	0	1	8/4	002000H to 003FFFH	001000H to 001FFFH
	SA0	0	0	0	0	0	0	0	0	8/4	000000H to 001FFFH	000000H to 000FFFH

Note: The address range is A₁₉: A₋₁ if in byte mode ($\overline{\text{BYTE}} = V_{IL}$).
The address range is A₁₉: A₀ if in word mode ($\text{BYTE} = V_{IH}$).

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Table 6.1 Sector Address Tables (MBM29DL162TD)

Bank	Sector	Sector Address								Sector Size (Kbytes/ Kwords)	(×8) Address Range	(×16) Address Range
		Bank Address			A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂			
		A ₁₉	A ₁₈	A ₁₇								
Bank 2	SA0	0	0	0	0	0	X	X	X	64/32	000000H to 00FFFFH	000000H to 007FFFH
	SA1	0	0	0	0	1	X	X	X	64/32	010000H to 01FFFFH	008000H to 00FFFFH
	SA2	0	0	0	1	0	X	X	X	64/32	020000H to 02FFFFH	010000H to 017FFFH
	SA3	0	0	0	1	1	X	X	X	64/32	030000H to 03FFFFH	018000H to 01FFFFH
	SA4	0	0	1	0	0	X	X	X	64/32	040000H to 04FFFFH	020000H to 027FFFH
	SA5	0	0	1	0	1	X	X	X	64/32	050000H to 05FFFFH	028000H to 02FFFFH
	SA6	0	0	1	1	0	X	X	X	64/32	060000H to 06FFFFH	030000H to 037FFFH
	SA7	0	0	1	1	1	X	X	X	64/32	070000H to 07FFFFH	038000H to 03FFFFH
	SA8	0	1	0	0	0	X	X	X	64/32	080000H to 08FFFFH	040000H to 047FFFH
	SA9	0	1	0	0	1	X	X	X	64/32	090000H to 09FFFFH	048000H to 04FFFFH
	SA10	0	1	0	1	0	X	X	X	64/32	0A0000H to 0AFFFFH	050000H to 057FFFH
	SA11	0	1	0	1	1	X	X	X	64/32	0B0000H to 0BFFFFH	058000H to 05FFFFH
	SA12	0	1	1	0	0	X	X	X	64/32	0C0000H to 0CFFFFH	060000H to 067FFFH
	SA13	0	1	1	0	1	X	X	X	64/32	0D0000H to 0DFFFFH	068000H to 06FFFFH
	SA14	0	1	1	1	0	X	X	X	64/32	0E0000H to 0EFFFFH	070000H to 077FFFH
	SA15	0	1	1	1	1	X	X	X	64/32	0F0000H to 0FFFFFH	078000H to 07FFFFH
	SA16	1	0	0	0	0	X	X	X	64/32	100000H to 10FFFFH	080000H to 087FFFH
	SA17	1	0	0	0	1	X	X	X	64/32	110000H to 11FFFFH	088000H to 08FFFFH
	SA18	1	0	0	1	0	X	X	X	64/32	120000H to 12FFFFH	090000H to 097FFFH
	SA19	1	0	0	1	1	X	X	X	64/32	130000H to 13FFFFH	098000H to 09FFFFH
	SA20	1	0	1	0	0	X	X	X	64/32	140000H to 14FFFFH	0A0000H to 0A7FFFH
	SA21	1	0	1	0	1	X	X	X	64/32	150000H to 15FFFFH	0A8000H to 0AFFFFH
	SA22	1	0	1	1	0	X	X	X	64/32	160000H to 16FFFFH	0B0000H to 0B7FFFH
	SA23	1	0	1	1	1	X	X	X	64/32	170000H to 17FFFFH	0B8000H to 0BFFFFH
	SA24	1	1	0	0	0	X	X	X	64/32	180000H to 18FFFFH	0C0000H to 0C7FFFH
	SA25	1	1	0	0	1	X	X	X	64/32	190000H to 19FFFFH	0C8000H to 0CFFFFH
	SA26	1	1	0	1	0	X	X	X	64/32	1A0000H to 1AFFFFH	0D0000H to 0D7FFFH
	SA27	1	1	0	1	1	X	X	X	64/32	1B0000H to 1BFFFFH	0D8000H to 0DFFFFH
Bank 1	SA28	1	1	1	0	0	X	X	X	64/32	1C0000H to 1CFFFFH	0E0000H to 0E7FFFH
	SA29	1	1	1	0	1	X	X	X	64/32	1D0000H to 1DFFFFH	0E8000H to 0EFFFFH
	SA30	1	1	1	1	0	X	X	X	64/32	1E0000H to 1EFFFFH	0F0000H to 0F7FFFH
	SA31	1	1	1	1	1	0	0	0	8/4	1F0000H to 1F1FFFH	0F8000H to 0F8FFFH
	SA32	1	1	1	1	1	0	0	1	8/4	1F2000H to 1F3FFFH	0F9000H to 0F9FFFH
	SA33	1	1	1	1	1	0	1	0	8/4	1F4000H to 1F5FFFH	0FA000H to 0FAFFFH
	SA34	1	1	1	1	1	0	1	1	8/4	1F6000H to 1F7FFFH	0FB000H to 0FBFFFH
	SA35	1	1	1	1	1	1	0	0	8/4	1F8000H to 1F9FFFH	0FC000H to 0FCFFFH
	SA36	1	1	1	1	1	1	0	1	8/4	1FA000H to 1FBFFFH	0FD000H to 0FDFFFH
	SA37	1	1	1	1	1	1	1	0	8/4	1FC000H to 1FDFFFH	0FE000H to 0FEFFFH
	SA38	1	1	1	1	1	1	1	1	8/4	1FE000H to 1FFFFFH	0FF000H to 0FFFFFH

Note: The address range is A₁₉: A₁ if in byte mode ($\overline{\text{BYTE}} = V_{\text{IL}}$).
The address range is A₁₉: A₀ if in word mode ($\text{BYTE} = V_{\text{IH}}$)

MBM29DL16XTD/BD-70/90/12

Table 6.2 Sector Address Tables (MBM29DL162BD)

Bank	Sector	Sector Address								Sector Size (Kbytes/ Kwords)	(×8) Address Range	(×16) Address Range
		Bank Address			A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂			
		A ₁₉	A ₁₈	A ₁₇								
Bank 2	SA38	1	1	1	1	1	X	X	X	64/32	1F0000H to 1FFFFFFH	0F8000H to 0FFFFFFH
	SA37	1	1	1	1	0	X	X	X	64/32	1E0000H to 1FFFFFFH	0F0000H to 0F7FFFH
	SA36	1	1	1	0	1	X	X	X	64/32	1D0000H to 1DFFFFH	0E8000H to 0EFFFFH
	SA35	1	1	1	0	0	X	X	X	64/32	1C0000H to 1CFFFFH	0E0000H to 0E7FFFH
	SA34	1	1	0	1	1	X	X	X	64/32	1B0000H to 1BFFFFH	0D8000H to 0DFFFFH
	SA33	1	1	0	1	0	X	X	X	64/32	1A0000H to 1AFFFFH	0D0000H to 0D7FFFH
	SA32	1	1	0	0	1	X	X	X	64/32	190000H to 19FFFFH	0C8000H to 0CFFFFH
	SA31	1	1	0	0	0	X	X	X	64/32	180000H to 18FFFFH	0C0000H to 0C7FFFH
	SA30	1	0	1	1	1	X	X	X	64/32	170000H to 17FFFFH	0B8000H to 0BFFFFH
	SA29	1	0	1	1	0	X	X	X	64/32	160000H to 16FFFFH	0B0000H to 0B7FFFH
	SA28	1	0	1	0	1	X	X	X	64/32	150000H to 15FFFFH	0A8000H to 0AFFFFH
	SA27	1	0	1	0	0	X	X	X	64/32	140000H to 14FFFFH	0A0000H to 0A7FFFH
	SA26	1	0	0	1	1	X	X	X	64/32	130000H to 13FFFFH	098000H to 09FFFFH
	SA25	1	0	0	1	0	X	X	X	64/32	120000H to 12FFFFH	090000H to 097FFFH
	SA24	1	0	0	0	X	X	X	X	64/32	110000H to 11FFFFH	088000H to 08FFFFH
	SA23	1	0	0	0	0	X	X	X	64/32	100000H to 10FFFFH	080000H to 087FFFH
	SA22	0	1	1	1	1	X	X	X	64/32	0F0000H to 0FFFFFFH	078000H to 07FFFFH
	SA21	0	1	1	1	0	X	X	X	64/32	0E0000H to 0EFFFFH	070000H to 077FFFH
	SA20	0	1	1	0	1	X	X	X	64/32	0D0000H to 0DFFFFH	068000H to 06FFFFH
	SA19	0	1	1	0	0	X	X	X	64/32	0C0000H to 0CFFFFH	060000H to 067FFFH
	SA18	0	1	0	1	1	X	X	X	64/32	0B0000H to 0BFFFFH	058000H to 05FFFFH
	SA17	0	1	0	1	0	X	X	X	64/32	0A0000H to 0AFFFFH	050000H to 057FFFH
	SA16	0	1	0	0	1	X	X	X	64/32	090000H to 09FFFFH	048000H to 04FFFFH
	SA15	0	1	0	0	0	X	X	X	64/32	080000H to 08FFFFH	040000H to 047FFFH
SA14	0	0	1	1	1	X	X	X	64/32	070000H to 07FFFFH	038000H to 03FFFFH	
SA13	0	0	1	1	0	X	X	X	64/32	060000H to 06FFFFH	030000H to 037FFFH	
SA12	0	0	1	0	1	X	X	X	64/32	050000H to 05FFFFH	028000H to 02FFFFH	
SA11	0	0	1	0	0	X	X	X	64/32	040000H to 04FFFFH	020000H to 027FFFH	
Bank 1	SA10	0	0	0	1	1	X	X	X	64/32	030000H to 03FFFFH	018000H to 01FFFFH
	SA9	0	0	0	1	0	X	X	X	64/32	020000H to 02FFFFH	010000H to 017FFFH
	SA8	0	0	0	0	1	X	X	X	64/32	010000H to 01FFFFH	008000H to 00FFFFH
	SA7	0	0	0	0	0	1	1	1	8/4	00E000H to 00FFFFH	007000H to 007FFFH
	SA6	0	0	0	0	0	1	1	0	8/4	00C000H to 00DFFFH	006000H to 006FFFH
	SA5	0	0	0	0	0	1	0	1	8/4	00A000H to 00BFFFH	005000H to 005FFFH
	SA4	0	0	0	0	0	1	0	0	8/4	008000H to 009FFFH	004000H to 004FFFH
	SA3	0	0	0	0	0	0	1	1	8/4	006000H to 007FFFH	003000H to 003FFFH
	SA2	0	0	0	0	0	0	1	0	8/4	004000H to 005FFFH	002000H to 002FFFH
	SA1	0	0	0	0	0	0	0	1	8/4	002000H to 003FFFH	001000H to 001FFFH
	SA0	0	0	0	0	0	0	0	0	8/4	000000H to 001FFFH	000000H to 000FFFH

Note: The address range is A₁₉: A₁ if in byte mode ($\overline{\text{BYTE}} = V_{\text{IL}}$).
The address range is A₁₉: A₀ if in word mode ($\text{BYTE} = V_{\text{IH}}$).

MBM29DL16XTD/BD-70/90/12

Table 7.1 Sector Address Tables (MBM29DL163TD)

Bank	Sector	Sector Address								Sector Size (Kbytes/ Kwords)	(×8) Address Range	(×16) Address Range
		BA		A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂			
		A ₁₉	A ₁₈									
Bank 2	SA0	0	0	0	0	0	X	X	X	64/32	000000H to 00FFFFH	000000H to 007FFFH
	SA1	0	0	0	0	1	X	X	X	64/32	010000H to 01FFFFH	008000H to 00FFFFH
	SA2	0	0	0	1	0	X	X	X	64/32	020000H to 02FFFFH	010000H to 017FFFH
	SA3	0	0	0	1	1	X	X	X	64/32	030000H to 03FFFFH	018000H to 01FFFFH
	SA4	0	0	1	0	0	X	X	X	64/32	040000H to 04FFFFH	020000H to 027FFFH
	SA5	0	0	1	0	1	X	X	X	64/32	050000H to 05FFFFH	028000H to 02FFFFH
	SA6	0	0	1	1	0	X	X	X	64/32	060000H to 06FFFFH	030000H to 037FFFH
	SA7	0	0	1	1	1	X	X	X	64/32	070000H to 07FFFFH	038000H to 03FFFFH
	SA8	0	1	0	0	0	X	X	X	64/32	080000H to 08FFFFH	040000H to 047FFFH
	SA9	0	1	0	0	1	X	X	X	64/32	090000H to 09FFFFH	048000H to 04FFFFH
	SA10	0	1	0	1	0	X	X	X	64/32	0A0000H to 0AFFFFH	050000H to 057FFFH
	SA11	0	1	0	1	1	X	X	X	64/32	0B0000H to 0BFFFFH	058000H to 05FFFFH
	SA12	0	1	1	0	0	X	X	X	64/32	0C0000H to 0CFFFFH	060000H to 067FFFH
	SA13	0	1	1	0	1	X	X	X	64/32	0D0000H to 0DFFFFH	068000H to 06FFFFH
	SA14	0	1	1	1	0	X	X	X	64/32	0E0000H to 0EFFFFH	070000H to 077FFFH
	SA15	0	1	1	1	1	X	X	X	64/32	0F0000H to 0FFFFFH	078000H to 07FFFFH
	SA16	1	0	0	0	0	X	X	X	64/32	100000H to 10FFFFH	080000H to 087FFFH
	SA17	1	0	0	0	1	X	X	X	64/32	110000H to 11FFFFH	088000H to 08FFFFH
	SA18	1	0	0	1	0	X	X	X	64/32	120000H to 12FFFFH	090000H to 097FFFH
	SA19	1	0	0	1	1	X	X	X	64/32	130000H to 13FFFFH	098000H to 09FFFFH
	SA20	1	0	1	0	0	X	X	X	64/32	140000H to 14FFFFH	0A0000H to 0A7FFFH
	SA21	1	0	1	0	1	X	X	X	64/32	150000H to 15FFFFH	0A8000H to 0AFFFFH
	SA22	1	0	1	1	0	X	X	X	64/32	160000H to 16FFFFH	0B0000H to 0B7FFFH
	SA23	1	0	1	1	1	X	X	X	64/32	170000H to 17FFFFH	0B8000H to 0BFFFFH
Bank 1	SA24	1	1	0	0	0	X	X	X	64/32	180000H to 18FFFFH	0C0000H to 0C7FFFH
	SA25	1	1	0	0	1	X	X	X	64/32	190000H to 19FFFFH	0C8000H to 0CFFFFH
	SA26	1	1	0	1	0	X	X	X	64/32	1A0000H to 1AFFFFH	0D0000H to 0D7FFFH
	SA27	1	1	0	1	1	X	X	X	64/32	1B0000H to 1BFFFFH	0D8000H to 0DFFFFH
	SA28	1	1	1	0	0	X	X	X	64/32	1C0000H to 1CFFFFH	0E0000H to 0E7FFFH
	SA29	1	1	1	0	1	X	X	X	64/32	1D0000H to 1DFFFFH	0E8000H to 0EFFFFH
	SA30	1	1	1	1	0	X	X	X	64/32	1E0000H to 1EFFFFH	0F0000H to 0F7FFFH
	SA31	1	1	1	1	1	0	0	0	8/4	1F0000H to 1F1FFFH	0F8000H to 0F8FFFH
	SA32	1	1	1	1	1	0	0	1	8/4	1F2000H to 1F3FFFH	0F9000H to 0F9FFFH
	SA33	1	1	1	1	1	0	1	0	8/4	1F4000H to 1F5FFFH	0FA000H to 0FAFFFH
	SA34	1	1	1	1	1	0	1	1	8/4	1F6000H to 1F7FFFH	0FB000H to 0FBFFFH
	SA35	1	1	1	1	1	1	0	0	8/4	1F8000H to 1F9FFFH	0FC000H to 0FCFFFH
	SA36	1	1	1	1	1	1	0	1	8/4	1FA000H to 1FBFFFH	0FD000H to 0FDFFFH
	SA37	1	1	1	1	1	1	1	0	8/4	1FC000H to 1FDFFFH	0FE000H to 0FEFFFH
	SA38	1	1	1	1	1	1	1	1	8/4	1FE000H to 1FFFFFH	0FF000H to 0FFFFFH

BA: Bank Address

Note: The address range is A₁₉: A₁ if in byte mode ($\overline{\text{BYTE}} = V_{\text{IL}}$).
The address range is A₁₉: A₀ if in word mode ($\text{BYTE} = V_{\text{IH}}$)

MBM29DL16XTD/BD-70/90/12

Table 7.2 Sector Address Tables (MBM29DL163BD)

Bank	Sector	Sector Address								Sector Size (Kbytes/ Kwords)	(×8) Address Range	(×16) Address Range
		BA		A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂			
		A ₁₉	A ₁₈									
Bank 2	SA38	1	1	1	1	1	X	X	X	64/32	1F0000H to 1FFFFFFH	0F8000H to 0FFFFFFH
	SA37	1	1	1	1	0	X	X	X	64/32	1E0000H to 1FFFFFFH	0F0000H to 0F7FFFH
	SA36	1	1	1	0	1	X	X	X	64/32	1D0000H to 1DFFFFH	0E8000H to 0EFFFFH
	SA35	1	1	1	0	0	X	X	X	64/32	1C0000H to 1CFFFFH	0E0000H to 0E7FFFH
	SA34	1	1	0	1	1	X	X	X	64/32	1B0000H to 1BFFFFH	0D8000H to 0DFFFFH
	SA33	1	1	0	1	0	X	X	X	64/32	1A0000H to 1AFFFFH	0D0000H to 0D7FFFH
	SA32	1	1	0	0	1	X	X	X	64/32	190000H to 19FFFFH	0C8000H to 0CFFFFH
	SA31	1	1	0	0	0	X	X	X	64/32	180000H to 18FFFFH	0C0000H to 0C7FFFH
	SA30	1	0	1	1	1	X	X	X	64/32	170000H to 17FFFFH	0B8000H to 0BFFFFH
	SA29	1	0	1	1	0	X	X	X	64/32	160000H to 16FFFFH	0B0000H to 0B7FFFH
	SA28	1	0	1	0	1	X	X	X	64/32	150000H to 15FFFFH	0A8000H to 0AFFFFH
	SA27	1	0	1	0	0	X	X	X	64/32	140000H to 14FFFFH	0A0000H to 0A7FFFH
	SA26	1	0	0	1	1	X	X	X	64/32	130000H to 13FFFFH	098000H to 09FFFFH
	SA25	1	0	0	1	0	X	X	X	64/32	120000H to 12FFFFH	090000H to 097FFFH
	SA24	1	0	0	0	X	X	X	X	64/32	110000H to 11FFFFH	088000H to 08FFFFH
	SA23	1	0	0	0	0	X	X	X	64/32	100000H to 10FFFFH	080000H to 087FFFH
	SA22	0	1	1	1	1	X	X	X	64/32	0F0000H to 0FFFFFFH	078000H to 07FFFFH
	SA21	0	1	1	1	0	X	X	X	64/32	0E0000H to 0EFFFFH	070000H to 077FFFH
	SA20	0	1	1	0	1	X	X	X	64/32	0D0000H to 0DFFFFH	068000H to 06FFFFH
	SA19	0	1	1	0	0	X	X	X	64/32	0C0000H to 0CFFFFH	060000H to 067FFFH
SA18	0	1	0	1	1	X	X	X	64/32	0B0000H to 0BFFFFH	058000H to 05FFFFH	
SA17	0	1	0	1	0	X	X	X	64/32	0A0000H to 0AFFFFH	050000H to 057FFFH	
SA16	0	1	0	0	1	X	X	X	64/32	090000H to 09FFFFH	048000H to 04FFFFH	
SA15	0	1	0	0	0	X	X	X	64/32	080000H to 08FFFFH	040000H to 047FFFH	
Bank 1	SA14	0	0	1	1	1	X	X	X	64/32	070000H to 07FFFFH	038000H to 03FFFFH
	SA13	0	0	1	1	0	X	X	X	64/32	060000H to 06FFFFH	030000H to 037FFFH
	SA12	0	0	1	0	1	X	X	X	64/32	050000H to 05FFFFH	028000H to 02FFFFH
	SA11	0	0	1	0	0	X	X	X	64/32	040000H to 04FFFFH	020000H to 027FFFH
	SA10	0	0	0	1	1	X	X	X	64/32	030000H to 03FFFFH	018000H to 01FFFFH
	SA9	0	0	0	1	0	X	X	X	64/32	020000H to 02FFFFH	010000H to 017FFFH
	SA8	0	0	0	0	1	X	X	X	64/32	010000H to 01FFFFH	008000H to 00FFFFH
	SA7	0	0	0	0	0	1	1	1	8/4	00E000H to 00FFFFH	007000H to 007FFFH
	SA6	0	0	0	0	0	1	1	0	8/4	00C000H to 00DFFFH	006000H to 006FFFH
	SA5	0	0	0	0	0	1	0	1	8/4	00A000H to 00BFFFH	005000H to 005FFFH
	SA4	0	0	0	0	0	1	0	0	8/4	008000H to 009FFFH	004000H to 004FFFH
	SA3	0	0	0	0	0	0	1	1	8/4	006000H to 007FFFH	003000H to 003FFFH
	SA2	0	0	0	0	0	0	1	0	8/4	004000H to 005FFFH	002000H to 002FFFH
	SA1	0	0	0	0	0	0	0	1	8/4	002000H to 003FFFH	001000H to 001FFFH
	SA0	0	0	0	0	0	0	0	0	8/4	000000H to 001FFFH	000000H to 000FFFH

BA: Bank Address

Note: The address range is A₁₉: A₁ if in byte mode ($\overline{\text{BYTE}} = V_{\text{IL}}$).
The address range is A₁₉: A₀ if in word mode ($\text{BYTE} = V_{\text{IH}}$).

MBM29DL16XTD/BD-70/90/12

Table 8.1 Sector Address Tables (MBM29DL164TD)

Bank	Sector	Sector Address								Sector Size (Kbytes/ Kwords)	(×8) Address Range	(×16) Address Range
		BA A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂			
Bank 2	SA0	0	0	0	0	0	X	X	X	64/32	000000H to 00FFFFH	000000H to 007FFFH
	SA1	0	0	0	0	1	X	X	X	64/32	010000H to 01FFFFH	008000H to 00FFFFH
	SA2	0	0	0	1	0	X	X	X	64/32	020000H to 02FFFFH	010000H to 017FFFH
	SA3	0	0	0	1	1	X	X	X	64/32	030000H to 03FFFFH	018000H to 01FFFFH
	SA4	0	0	1	0	0	X	X	X	64/32	040000H to 04FFFFH	020000H to 027FFFH
	SA5	0	0	1	0	1	X	X	X	64/32	050000H to 05FFFFH	028000H to 02FFFFH
	SA6	0	0	1	1	0	X	X	X	64/32	060000H to 06FFFFH	030000H to 037FFFH
	SA7	0	0	1	1	1	X	X	X	64/32	070000H to 07FFFFH	038000H to 03FFFFH
	SA8	0	1	0	0	0	X	X	X	64/32	080000H to 08FFFFH	040000H to 047FFFH
	SA9	0	1	0	0	1	X	X	X	64/32	090000H to 09FFFFH	048000H to 04FFFFH
	SA10	0	1	0	1	0	X	X	X	64/32	0A0000H to 0AFFFFH	050000H to 057FFFH
	SA11	0	1	0	1	1	X	X	X	64/32	0B0000H to 0BFFFFH	058000H to 05FFFFH
	SA12	0	1	1	0	0	X	X	X	64/32	0C0000H to 0CFFFFH	060000H to 067FFFH
	SA13	0	1	1	0	1	X	X	X	64/32	0D0000H to 0DFFFFH	068000H to 06FFFFH
	SA14	0	1	1	1	0	X	X	X	64/32	0E0000H to 0EFFFFH	070000H to 077FFFH
	SA15	0	1	1	1	1	X	X	X	64/32	0F0000H to 0FFFFFH	078000H to 07FFFFH
Bank 1	SA16	1	0	0	0	0	X	X	X	64/32	100000H to 10FFFFH	080000H to 087FFFH
	SA17	1	0	0	0	1	X	X	X	64/32	110000H to 11FFFFH	088000H to 08FFFFH
	SA18	1	0	0	1	0	X	X	X	64/32	120000H to 12FFFFH	090000H to 097FFFH
	SA19	1	0	0	1	1	X	X	X	64/32	130000H to 13FFFFH	098000H to 09FFFFH
	SA20	1	0	1	0	0	X	X	X	64/32	140000H to 14FFFFH	0A0000H to 0A7FFFH
	SA21	1	0	1	0	1	X	X	X	64/32	150000H to 15FFFFH	0A8000H to 0AFFFFH
	SA22	1	0	1	1	0	X	X	X	64/32	160000H to 16FFFFH	0B0000H to 0B7FFFH
	SA23	1	0	1	1	1	X	X	X	64/32	170000H to 17FFFFH	0B8000H to 0BFFFFH
	SA24	1	1	0	0	0	X	X	X	64/32	180000H to 18FFFFH	0C0000H to 0C7FFFH
	SA25	1	1	0	0	1	X	X	X	64/32	190000H to 19FFFFH	0C8000H to 0CFFFFH
	SA26	1	1	0	1	0	X	X	X	64/32	1A0000H to 1AFFFFH	0D0000H to 0D7FFFH
	SA27	1	1	0	1	1	X	X	X	64/32	1B0000H to 1BFFFFH	0D8000H to 0DFFFFH
	SA28	1	1	1	0	0	X	X	X	64/32	1C0000H to 1CFFFFH	0E0000H to 0E7FFFH
	SA29	1	1	1	0	1	X	X	X	64/32	1D0000H to 1DFFFFH	0E8000H to 0EFFFFH
	SA30	1	1	1	1	0	X	X	X	64/32	1E0000H to 1EFFFFH	0F0000H to 0F7FFFH
	SA31	1	1	1	1	1	0	0	0	8/4	1F0000H to 1F1FFFH	0F8000H to 0F8FFFH
	SA32	1	1	1	1	1	0	0	1	8/4	1F2000H to 1F3FFFH	0F9000H to 0F9FFFH
	SA33	1	1	1	1	1	0	1	0	8/4	1F4000H to 1F5FFFH	0FA000H to 0FAFFFH
	SA34	1	1	1	1	1	0	1	1	8/4	1F6000H to 1F7FFFH	0FB000H to 0FBFFFH
	SA35	1	1	1	1	1	1	0	0	8/4	1F8000H to 1F9FFFH	0FC000H to 0FCFFFH
	SA36	1	1	1	1	1	1	0	1	8/4	1FA000H to 1FBFFFH	0FD000H to 0FDFFFH
	SA37	1	1	1	1	1	1	1	0	8/4	1FC000H to 1FDFFFH	0FE000H to 0FEFFFH
	SA38	1	1	1	1	1	1	1	1	8/4	1FE000H to 1FFFFFH	0FF000H to 0FFFFFH

BA: Bank Address

Note: The address range is A₁₉: A₁ if in byte mode ($\overline{\text{BYTE}} = V_{\text{IL}}$).
The address range is A₁₉: A₀ if in word mode ($\text{BYTE} = V_{\text{IH}}$)

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Table 8.2 Sector Address Tables (MBM29DL164BD)

Bank	Sector	Sector Address								Sector Size (Kbytes/ Kwords)	(×8) Address Range	(×16) Address Range
		BA A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂			
Bank 2	SA38	1	1	1	1	1	X	X	X	64/32	1F0000H to 1FFFFFFH	0F8000H to 0FFFFFFH
	SA37	1	1	1	1	0	X	X	X	64/32	1E0000H to 1FFFFFFH	0F0000H to 0F7FFFFH
	SA36	1	1	1	0	1	X	X	X	64/32	1D0000H to 1DFFFFH	0E8000H to 0EFFFFH
	SA35	1	1	1	0	0	X	X	X	64/32	1C0000H to 1CFFFFH	0E0000H to 0E7FFFFH
	SA34	1	1	0	1	1	X	X	X	64/32	1B0000H to 1BFFFFH	0D8000H to 0DFFFFH
	SA33	1	1	0	1	0	X	X	X	64/32	1A0000H to 1AFFFFH	0D0000H to 0D7FFFFH
	SA32	1	1	0	0	1	X	X	X	64/32	190000H to 19FFFFH	0C8000H to 0CFFFFH
	SA31	1	1	0	0	0	X	X	X	64/32	180000H to 18FFFFH	0C0000H to 0C7FFFFH
	SA30	1	0	1	1	1	X	X	X	64/32	170000H to 17FFFFH	0B8000H to 0BFFFFH
	SA29	1	0	1	1	0	X	X	X	64/32	160000H to 16FFFFH	0B0000H to 0B7FFFFH
	SA28	1	0	1	0	1	X	X	X	64/32	150000H to 15FFFFH	0A8000H to 0AFFFFH
	SA27	1	0	1	0	0	X	X	X	64/32	140000H to 14FFFFH	0A0000H to 0A7FFFFH
	SA26	1	0	0	1	1	X	X	X	64/32	130000H to 13FFFFH	098000H to 09FFFFH
	SA25	1	0	0	1	0	X	X	X	64/32	120000H to 12FFFFH	090000H to 097FFFFH
	SA24	1	0	0	0	X	X	X	X	64/32	110000H to 11FFFFH	088000H to 08FFFFH
	SA23	1	0	0	0	0	X	X	X	64/32	100000H to 10FFFFH	080000H to 087FFFFH
Bank 1	SA22	0	1	1	1	1	X	X	X	64/32	0F0000H to 0FFFFFFH	078000H to 07FFFFH
	SA21	0	1	1	1	0	X	X	X	64/32	0E0000H to 0EFFFFH	070000H to 077FFFFH
	SA20	0	1	1	0	1	X	X	X	64/32	0D0000H to 0DFFFFH	068000H to 06FFFFH
	SA19	0	1	1	0	0	X	X	X	64/32	0C0000H to 0CFFFFH	060000H to 067FFFFH
	SA18	0	1	0	1	1	X	X	X	64/32	0B0000H to 0BFFFFH	058000H to 05FFFFH
	SA17	0	1	0	1	0	X	X	X	64/32	0A0000H to 0AFFFFH	050000H to 057FFFFH
	SA16	0	1	0	0	1	X	X	X	64/32	090000H to 09FFFFH	048000H to 04FFFFH
	SA15	0	1	0	0	0	X	X	X	64/32	080000H to 08FFFFH	040000H to 047FFFFH
	SA14	0	0	1	1	1	X	X	X	64/32	070000H to 07FFFFH	038000H to 03FFFFH
	SA13	0	0	1	1	0	X	X	X	64/32	060000H to 06FFFFH	030000H to 037FFFFH
	SA12	0	0	1	0	1	X	X	X	64/32	050000H to 05FFFFH	028000H to 02FFFFH
	SA11	0	0	1	0	0	X	X	X	64/32	040000H to 04FFFFH	020000H to 027FFFFH
	SA10	0	0	0	1	1	X	X	X	64/32	030000H to 03FFFFH	018000H to 01FFFFH
	SA9	0	0	0	1	0	X	X	X	64/32	020000H to 02FFFFH	010000H to 017FFFFH
	SA8	0	0	0	0	1	X	X	X	64/32	010000H to 01FFFFH	008000H to 00FFFFH
	SA7	0	0	0	0	0	1	1	1	8/4	00E000H to 00FFFFH	007000H to 007FFFFH
	SA6	0	0	0	0	0	1	1	0	8/4	00C000H to 00DFFFFH	006000H to 006FFFFH
	SA5	0	0	0	0	0	1	0	1	8/4	00A000H to 00BFFFFH	005000H to 005FFFFH
	SA4	0	0	0	0	0	1	0	0	8/4	008000H to 009FFFFH	004000H to 004FFFFH
	SA3	0	0	0	0	0	0	1	1	8/4	006000H to 007FFFFH	003000H to 003FFFFH
	SA2	0	0	0	0	0	0	1	0	8/4	004000H to 005FFFFH	002000H to 002FFFFH
	SA1	0	0	0	0	0	0	0	1	8/4	002000H to 003FFFFH	001000H to 001FFFFH
	SA0	0	0	0	0	0	0	0	0	8/4	000000H to 001FFFFH	000000H to 000FFFFH

BA: Bank Address

Note: The address range is A₁₉: A₁ if in byte mode ($\overline{\text{BYTE}} = V_{\text{IL}}$).
The address range is A₁₉: A₀ if in word mode ($\text{BYTE} = V_{\text{IH}}$).

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**Table 9.1 Sector Group Addresses (MBM29DL16XTD)
(Top Boot Block)**

Sector Group	A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂	Sectors
SGA0	0	0	0	0	0	X	X	X	SA0
SGA1	0	0	0	0	1	X	X	X	SA1 to SA3
	0	0	0	1	0	X	X	X	
	0	0	0	1	1	X	X	X	
SGA2	0	0	1	X	X	X	X	X	SA4 to SA7
SGA3	0	1	0	X	X	X	X	X	SA8 to SA11
SGA4	0	1	1	X	X	X	X	X	SA12 to SA15
SGA5	1	0	0	X	X	X	X	X	SA16 to SA19
SGA6	1	0	1	X	X	X	X	X	SA20 to SA23
SGA7	1	1	0	X	X	X	X	X	SA24 to SA27
SGA8	1	1	1	0	0	X	X	X	SA28 to SA30
	1	1	1	0	1	X	X	X	
	1	1	1	1	0	X	X	X	
SGA9	1	1	1	1	1	0	0	0	SA31
SGA10	1	1	1	1	1	0	0	1	SA32
SGA11	1	1	1	1	1	0	1	0	SA33
SGA12	1	1	1	1	1	0	1	1	SA34
SGA13	1	1	1	1	1	1	0	0	SA35
SGA14	1	1	1	1	1	1	0	1	SA36
SGA15	1	1	1	1	1	1	1	0	SA37
SGA16	1	1	1	1	1	1	1	1	SA38

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**Table 9.2 Sector Group Addresses (MBM29DL16XBD)
(Bottom Boot Block)**

Sector Group	A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂	Sectors
SGA0	0	0	0	0	0	0	0	0	SA0
SGA1	0	0	0	0	0	0	0	1	SA1
SGA2	0	0	0	0	0	0	1	0	SA2
SGA3	0	0	0	0	0	0	1	1	SA3
SGA4	0	0	0	0	0	1	0	0	SA4
SGA5	0	0	0	0	0	1	0	1	SA5
SGA6	0	0	0	0	0	1	1	0	SA6
SGA7	0	0	0	0	0	1	1	1	SA7
SGA8	0	0	0	0	1	X	X	X	SA8 to SA10
	0	0	0	1	0	X	X	X	
	0	0	0	1	1	X	X	X	
SGA9	0	0	1	X	X	X	X	X	SA11 to SA14
SGA10	0	1	0	X	X	X	X	X	SA15 to SA18
SGA11	0	1	1	X	X	X	X	X	SA19 to SA22
SGA12	1	0	0	X	X	X	X	X	SA23 to SA26
SGA13	1	0	1	X	X	X	X	X	SA27 to SA30
SGA14	1	1	0	X	X	X	X	X	SA31 to SA34
SGA15	1	1	1	0	0	X	X	X	SA35 to SA37
	1	1	1	0	1	X	X	X	
	1	1	1	1	0	X	X	X	
SGA16	1	1	1	1	1	X	X	X	SA38

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■ FUNCTIONAL DESCRIPTION

• Simultaneous Operation

MBM29DL16XTD/BD have feature, which is capability of reading data from one bank of memory while a program or erase operation is in progress in the other bank of memory (simultaneous operation), in addition to the conventional features (read, program, erase, erase-suspend read, and erase-suspend program). The bank selection can be selected by bank address (A_{15} to A_{19}) with zero latency.

The MBM29DL161TD/BD have two banks which contain

Bank 1 (8KB $\times$ eight sectors) and Bank 2 (64KB $\times$ thirty-one sectors).

The MBM29DL162TD/BD have two banks which contain

Bank 1 (8KB $\times$ eight sectors, 64KB $\times$ three sectors) and Bank 2 (64KB $\times$ twenty eight sectors).

The MBM29DL163TD/BD have two banks which contain

Bank 1 (8KB $\times$ eight sectors, 64KB $\times$ seven sectors) and Bank 2 (64KB $\times$ twenty four sectors).

The MBM29DL164TD/BD have two banks which contain

Bank 1 (8KB $\times$ eight sectors, 64KB $\times$ fifteen sectors) and Bank 2 (64KB $\times$ sixteen sectors).

The simultaneous operation can not execute multi-function mode in the same bank. Table 10 shows combination to be possible for simultaneous operation. (Refer to the Figure 11 Bank-to-bank Read/Write Timing Diagram.)

Table 10 Simultaneous Operation

Case	Bank 1 Status	Bank 2 Status
1	Read mode	Read mode
2	Read mode	Autoselect mode
3	Read mode	Program mode
4	Read mode	Erase mode *
5	Autoselect mode	Read mode
6	Program mode	Read mode
7	Erase mode *	Read mode

*: An erase operation may also be suspended to read from or program to a sector not being erased.

• Read Mode

The MBM29DL16XTD/BD have two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for a device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins. (Assuming the addresses have been stable for at least $t_{ACC-tOE}$ time.) When reading out a data without changing addresses after power-up, it is necessary to input hardware reset or to change $\overline{CE}$ pin from "H" or "L"

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• Standby Mode

There are two ways to implement the standby mode on the MBM29DL16XTD/BD devices, one using both the $\overline{CE}$ and $\overline{RESET}$ pins; the other via the $\overline{RESET}$ pin only.

When using both pins, a CMOS standby mode is achieved with $\overline{CE}$ and $\overline{RESET}$ inputs both held at $V_{CC} \pm 0.3$ V. Under this condition the current consumed is less than 5 μ A max. During Embedded Algorithm operation, V_{CC} active current (I_{CC2}) is required even $\overline{CE} = "H"$. The device can be read with standard access time (t_{CE}) from either of these standby modes.

When using the $\overline{RESET}$ pin only, a CMOS standby mode is achieved with $\overline{RESET}$ input held at $V_{SS} \pm 0.3$ V ($\overline{CE} = "H"$ or $"L"$). Under this condition the current is consumed is less than 5 μ A max. Once the $\overline{RESET}$ pin is taken high, the device requires t_{RH} of wake up time before outputs are valid for read access.

In the standby mode the outputs are in the high impedance state, independent of the $\overline{OE}$ input.

• Automatic Sleep Mode

There is a function called automatic sleep mode to restrain power consumption during read-out of MBM29DL16XTD/BD data. This mode can be used effectively with an application requested low power consumption such as handy terminals.

To activate this mode, MBM29DL16XTD/BD automatically switch themselves to low power mode when MBM29DL16XTD/BD addresses remain stably during access time of 150 ns. It is not necessary to control $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ on the mode. Under the mode, the current consumed is typically 1 μ A (CMOS Level).

During simultaneous operation, V_{CC} active current (I_{CC2}) is required.

Since the data are latched during this mode, the data are read-out continuously. If the addresses are changed, the mode is canceled automatically and MBM29DL16XTD/BD read-out the data for changed addresses.

• Output Disable

With the $\overline{OE}$ input at a logic high level (V_{IH}), output from the devices are disabled. This will cause the output pins to be in a high impedance state.

• Autoselect

The autoselect mode allows the reading out of a binary code from the devices and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the devices to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the devices.

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 12.5 V) on address pin A_9 . Two identifier bytes may then be sequenced from the devices outputs by toggling address A_0 from V_{IL} to V_{IH} . All addresses are DON'T CARES except A_0 , A_1 , and A_6 (A_{-1}). (See Tables 3 and 4.)

The manufacturer and device codes may also be read via the command register, for instances when the MBM29DL16XTD/BD are erased or programmed in a system without access to high voltage on the A_9 pin. The command sequence is illustrated in Table 12. (Refer to Autoselect Command section.)

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Byte 0 ($A_0 = V_{IL}$) represents the manufacturer's code (Fujitsu = 04H) and word 1 ($A_0 = V_{IH}$) represents the device identifier code (MBM29DL161TD = 36H and MBM29DL161BD = 39H for $\times 8$ mode; MBM29DL161TD = 2236H and MBM29DL161BD = 2239H for $\times 16$ mode), (MBM29DL162TD = 2DH and MBM29DL162BD = 2EH for $\times 8$ mode; MBM29DL162TD = 222DH and MBM29DL162BD = 222EH for $\times 16$ mode), (MBM29DL163TD = 28H and MBM29DL163BD = 2BH for $\times 8$ mode; MBM29DL163TD = 2228H and MBM29DL163BD = 222BH for $\times 16$ mode), (MBM29DL164TD = 33H and MBM29DL164BD = 35H for $\times 8$ mode; MBM29DL164TD = 2233H and MBM29DL164BD = 2235H for $\times 16$ mode). These two bytes/words are given in the tables 11.1 to 11.8. All identifiers for manufactures and device will exhibit odd parity with DQ_7 defined as the parity bit. In order to read the proper device codes when executing the autoselect, A_1 must be V_{IL} . (See Tables 11.1 to 11.8.)

In case of applying V_{ID} on A_9 , since both Bank 1 and Bank 2 enters Autoselect mode, the simultaneous operation can not be executed.

Table 11.1 MBM29DL161TD/BD Sector Group Protection Verify Autoselect Codes

Type			A ₁₂ to A ₁₉	A ₆	A ₁	A ₀	A ₋₁ *1	Code (HEX)
Manufacture's Code			X	V _{IL}	V _{IL}	V _{IL}	V _{IL}	04H
Device Code	MBM29DL161TD	Byte	X	V _{IL}	V _{IL}	V _{IH}	V _{IL}	36H
		Word					X	2236H
	MBM29DL161BD	Byte	X	V _{IL}	V _{IL}	V _{IH}	V _{IL}	39H
		Word					X	2239H
Sector Group Protection			Sector Group Addresses	V _{IL}	V _{IH}	V _{IL}	V _{IL}	01H*2

*1: A_{-1} is for Byte mode.

*2: Outputs 01H at protected sector group addresses and outputs 00H at unprotected sector group addresses.

Table 11.2 Expanded Autoselect Code Table

Type			Code	DQ ₁₅	DQ ₁₄	DQ ₁₃	DQ ₁₂	DQ ₁₁	DQ ₁₀	DQ ₉	DQ ₈	DQ ₇	DQ ₆	DQ ₅	DQ ₄	DQ ₃	DQ ₂	DQ ₁	DQ ₀
Manufacturer's Code			04H	A-1/0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Device Code	MBM29DL161TD	(B)	36H	A-1	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	0	0	1	1	0	1	1	0
		(W)	2236H	0	0	1	0	0	0	1	0	0	0	1	1	0	1	1	0
	MBM29DL161BD	(B)	39H	A-1	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	0	0	1	1	1	0	0	1
		(W)	2239H	0	0	1	0	0	0	1	0	0	0	1	1	1	0	0	1
Sector Group Protection			01H	A-1/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

(B): Byte mode

(W): Word mode

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Table 11.3 MBM29DL162TD/BD Sector Group Protection Verify Autoselect Codes

Type			A ₁₂ to A ₁₉	A ₆	A ₁	A ₀	A ₋₁ *1	Code (HEX)
Manufacture's Code			X	V _{IL}	V _{IL}	V _{IL}	V _{IL}	04H
Device Code	MBM29DL162TD	Byte	X	V _{IL}	V _{IL}	V _{IH}	V _{IL}	2DH
		Word					X	222DH
	MBM29DL162BD	Byte	X	V _{IL}	V _{IL}	V _{IH}	V _{IL}	2EH
		Word					X	222EH
Sector Group Protection			Sector Group Addresses	V _{IL}	V _{IH}	V _{IL}	V _{IL}	01H*2

*1: A₋₁ is for Byte mode.

*2: Outputs 01H at protected sector group addresses and outputs 00H at unprotected sector group addresses.

Table 11.4 Expanded Autoselect Code Table

Type			Code	DQ ₁₅	DQ ₁₄	DQ ₁₃	DQ ₁₂	DQ ₁₁	DQ ₁₀	DQ ₉	DQ ₈	DQ ₇	DQ ₆	DQ ₅	DQ ₄	DQ ₃	DQ ₂	DQ ₁	DQ ₀
Manufacturer's Code			04H	A-1/0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Device Code	MBM29DL162TD	(B)	2DH	A-1	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	0	0	1	0	1	1	0	1
		(W)	222DH	0	0	1	0	0	0	1	0	0	0	1	0	1	1	0	1
	MBM29DL162BD	(B)	2EH	A-1	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	0	0	1	0	1	1	1	0
		(W)	222EH	0	0	1	0	0	0	1	0	0	0	1	0	1	1	1	0
Sector Group Protection			01H	A-1/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

(B): Byte mode

(W): Word mode

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Table 11.5 MBM29DL163TD/BD Sector Group Protection Verify Autoselect Codes

Type			A ₁₂ to A ₁₉	A ₆	A ₁	A ₀	A ₋₁ *1	Code (HEX)
Manufacture's Code			X	V _{IL}	V _{IL}	V _{IL}	V _{IL}	04H
Device Code	MBM29DL163TD	Byte	X	V _{IL}	V _{IL}	V _{IH}	V _{IL}	28H
		Word					X	2228H
	MBM29DL163BD	Byte	X	V _{IL}	V _{IL}	V _{IH}	V _{IL}	2BH
		Word					X	222BH
Sector Group Protection			Sector Group Addresses	V _{IL}	V _{IH}	V _{IL}	V _{IL}	01H*2

*1: A₋₁ is for Byte mode.

*2: Outputs 01H at protected sector group addresses and outputs 00H at unprotected sector group addresses.

Table 11.6 Expanded Autoselect Code Table

Type			Code	DQ ₁₅	DQ ₁₄	DQ ₁₃	DQ ₁₂	DQ ₁₁	DQ ₁₀	DQ ₉	DQ ₈	DQ ₇	DQ ₆	DQ ₅	DQ ₄	DQ ₃	DQ ₂	DQ ₁	DQ ₀
Manufacturer's Code			04H	A-1/0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Device Code	MBM29DL163TD	(B)	28H	A-1	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	0	0	1	0	1	0	0	0
		(W)	2228H	0	0	1	0	0	0	1	0	0	0	1	0	1	0	0	0
	MBM29DL163BD	(B)	2BH	A-1	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	0	0	1	0	1	0	1	1
		(W)	222BH	0	0	1	0	0	0	1	0	0	0	1	0	1	0	1	1
Sector Group Protection			01H	A-1/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

(B): Byte mode

(W): Word mode

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Table 11.7 MBM29DL164TD/BD Sector Group Protection Verify Autoselect Codes

Type			A ₁₂ to A ₁₉	A ₆	A ₁	A ₀	A ₋₁ *1	Code (HEX)
Manufacture's Code			X	V _{IL}	V _{IL}	V _{IL}	V _{IL}	04H
Device Code	MBM29DL164TD	Byte	X	V _{IL}	V _{IL}	V _{IH}	V _{IL}	33H
		Word					X	2233H
	MBM29DL164BD	Byte	X	V _{IL}	V _{IL}	V _{IH}	V _{IL}	35H
		Word					X	2235H
Sector Group Protection			Sector Group Addresses	V _{IL}	V _{IH}	V _{IL}	V _{IL}	01H*2

*1: A₋₁ is for Byte mode.

*2: Outputs 01H at protected sector group addresses and outputs 00H at unprotected sector group addresses.

Table 11.8 Expanded Autoselect Code Table

Type			Code	DQ ₁₅	DQ ₁₄	DQ ₁₃	DQ ₁₂	DQ ₁₁	DQ ₁₀	DQ ₉	DQ ₈	DQ ₇	DQ ₆	DQ ₅	DQ ₄	DQ ₃	DQ ₂	DQ ₁	DQ ₀
Manufacturer's Code			04H	A-1/0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Device Code	MBM29DL164TD	(B)	33H	A-1	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	0	0	1	1	0	0	1	1
		(W)	2233H	0	0	1	0	0	0	1	0	0	0	1	1	0	0	1	1
	MBM29DL164BD	(B)	35H	A-1	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	0	0	1	1	0	1	0	1
		(W)	2235H	0	0	1	0	0	0	1	0	0	0	1	1	0	1	0	1
Sector Group Protection			01H	A-1/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

(B): Byte mode

(W): Word mode

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• Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL} , while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH} . Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later; while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

• Sector Group Protection

The MBM29DL16XTD/BD feature hardware sector group protection. This feature will disable both program and erase operations in any combination of seventeen sector groups of memory. (See Tables 9.1 and 9.2). The sector group protection feature is enabled using programming equipment at the user's site. The device is shipped with all sector groups unprotected.

To activate this mode, the programming equipment must force V_{ID} on address pin A_9 and control pin $\overline{OE}$, (suggest $V_{ID} = 11.5\text{ V}$), $\overline{CE} = V_{IL}$ and $A_0 = A_6 = V_{IL}$, $A_1 = V_{IH}$. The sector group addresses (A_{19} , A_{18} , A_{17} , A_{16} , A_{15} , A_{14} , A_{13} , and A_{12}) should be set to the sector to be protected. Tables 5.1 to 8.2 define the sector address for each of the thirty nine (39) individual sectors, and tables 9.1 and 9.2 define the sector group address for each of the seventeen (17) individual group sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector group addresses must be held constant during the $\overline{WE}$ pulse. See Figures 18 and 26 for sector group protection waveforms and algorithm.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A_9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH} . Scanning the sector group addresses (A_{19} , A_{18} , A_{17} , A_{16} , A_{15} , A_{14} , A_{13} , and A_{12}) while (A_6 , A_1 , A_0) = (0, 1, 0) will produce a logical "1" code at device output DQ_0 for a protected sector. Otherwise the device will produce "0" for unprotected sector. In this mode, the lower order addresses, except for A_0 , A_1 , and A_6 are DON'T CARES. Address locations with $A_1 = V_{IL}$ are reserved for Autoselect manufacturer and device codes. A_{-1} requires to apply to V_{IL} on byte mode.

It is also possible to determine if a sector group is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02H, where the higher order addresses (A_{19} , A_{18} , A_{17} , A_{16} , A_{15} , A_{14} , A_{13} , and A_{12}) are the desired sector group address will produce a logical "1" at DQ_0 for a protected sector group. See Tables 11.1 to 11.8 for Autoselect codes.

• Temporary Sector Group Unprotection

This feature allows temporary unprotection of previously protected sector groups of the MBM29DL16XTD/BD devices in order to change data. The Sector Group Unprotection mode is activated by setting the $\overline{RESET}$ pin to high voltage (V_{ID}). During this mode, formerly protected sector groups can be programmed or erased by selecting the sector group addresses. Once the V_{ID} is taken away from the $\overline{RESET}$ pin, all the previously protected sector groups will be protected again. Refer to Figures 19 and 27.

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• RESET

Hardware Reset

The MBM29DL16XTD/BD devices may be reset by driving the $\overline{\text{RESET}}$ pin to V_{IL} . The $\overline{\text{RESET}}$ pin has a pulse requirement and has to be kept low (V_{IL}) for at least “ t_{RP} ” in order to properly reset the internal state machine. Any operation in the process of being executed will be terminated and the internal state machine will be reset to the read mode “ t_{READY} ” after the $\overline{\text{RESET}}$ pin is driven low. Furthermore, once the $\overline{\text{RESET}}$ pin goes high, the devices require an additional “ t_{RH} ” before it will allow read access. When the $\overline{\text{RESET}}$ pin is low, the devices will be in the standby mode for the duration of the pulse and all the data output pins will be tri-stated. If a hardware reset occurs during a program or erase operation, the data at that particular location will be corrupted. Please note that the $\text{RY}/\overline{\text{BY}}$ output signal should be ignored during the $\overline{\text{RESET}}$ pulse. See Figure 14 for the timing diagram. Refer to Temporary Sector Group Unprotection for additional functionality.

• Boot Block Sector Protection

The Write Protect function provides a hardware method of protecting certain boot sectors without using V_{ID} . This function is one of two provided by the $\overline{\text{WP}}/\text{ACC}$ pin.

If the system asserts V_{IL} on the $\overline{\text{WP}}/\text{ACC}$ pin, the device disables program and erase functions in the two “outermost” 8K byte boot sectors independently of whether those sectors were protected or unprotected using the method described in “Sector Protection/Unprotection”. The two outermost 8K byte boot sectors are the two sectors containing the lowest addresses in a bottom-boot-configured device, or the two sectors containing the highest addresses in a top-boot-configured device.

(MBM29DL16XTD: SA37 and SA38, MBM29DL16XBD: SA0 and SA1)

If the system asserts V_{IH} on the $\overline{\text{WP}}/\text{ACC}$ pin, the device reverts to whether the two outermost 8K byte boot sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these two sectors depends on whether they were last protected or unprotected using the method described in “Sector protection/unprotection”.

• Accelerated Program Operation

MBM29DL16XTD/BD offers accelerated program operation which enables the programming in high speed.

If the system asserts V_{ACC} to the $\overline{\text{WP}}/\text{ACC}$ pin, the device automatically enters the acceleration mode and the time required for program operation will reduce to about 60%. This function is primarily intended to allow high speed program, so caution is needed as the sector group will temporarily be unprotected.

The system would use a fast program command sequence when programming during acceleration mode. Set command to fast mode and reset command from fast mode are not necessary. When the device enters the acceleration mode, the device automatically set to fast mode. Therefore, the present sequence could be used for programming and detection of completion during acceleration mode.

Removing V_{ACC} from the $\overline{\text{WP}}/\text{ACC}$ pin returns the device to normal operation. Do not remove V_{ACC} from $\overline{\text{WP}}/\text{ACC}$ pin while programming. See Figure 21.

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Table 12 MBM29DL16XTD/BD Command Definitions

Command Sequence		Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
			Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset	Word	1	XXXH	F0H	—	—	—	—	—	—	—	—	—	—
	Byte													
Read/Reset	Word	3	555H	AAH	2AAH	55H	555H	F0H	RA	RD	—	—	—	—
	Byte		AAAH		555H		AAAH							
Autoselect	Word	3	555H	AAH	2AAH	55H	(BA) 555H	90H	—	—	—	—	—	—
	Byte		AAAH		555H		(BA) AAAH							
Program	Word	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD	—	—	—	—
	Byte		AAAH		555H		AAAH							
Program Suspend		1	BA	B0H	—	—	—	—	—	—	—	—	—	—
Program Resume		1	BA	30H	—	—	—	—	—	—	—	—	—	—
Chip Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
	Byte		AAAH		555H		AAAH		AAAH		555H		AAAH	
Sector Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
	Byte		AAAH		555H		AAAH		AAAH		555H			
Erase Suspend		1	BA	B0H	—	—	—	—	—	—	—	—	—	—
Erase Resume		1	BA	30H	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode	Word	3	555H	AAH	2AAH	55H	555H	20H	—	—	—	—	—	—
	Byte		AAAH		555H		AAAH							
Fast Program *1	Word	2	XXXH	A0H	PA	PD	—	—	—	—	—	—	—	—
	Byte		XXXH											
Reset from Fast Mode *1	Word	2	BA	90H	XXXH	F0H	—	—	—	—	—	—	—	—
	Byte		BA		XXXH									
Extended Sector Group Protection *2	Word	4	XXXH	60H	SPA	60H	SPA	40H	SPA	SD	—	—	—	—
	Byte													
Query *3	Word	1	55H	98H	—	—	—	—	—	—	—	—	—	—
	Byte		AAH											
Hi-ROM Entry	Word	3	555H	AAH	2AAH	55H	555H	88H	—	—	—	—	—	—
	Byte		AAAH		555H		AAAH							
Hi-ROM Program *4	Word	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD	—	—	—	—
	Byte		AAAH		555H		AAAH							
Hi-ROM Erase *4	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	HRA	30H
	Byte		AAAH		555H		AAAH		AAAH		555H			
Hi-ROM Exit *4	Word	4	555H	AAH	2AAH	55H	(HRBA) 555H	90H	XXXH	00H	—	—	—	—
	Byte		AAAH		555H		(HRBA) AAAH							

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- Notes:
- Address bits A₁₁ to A₁₉ = X = "H" or "L" for all address commands except or Program Address (PA), Sector Address (SA), and Bank Address (BA).
 - Bus operations are defined in Tables 3 and 4.
 - RA = Address of the memory location to be read
PA = Address of the memory location to be programmed
Addresses are latched on the falling edge of the write pulse.
SA = Address of the sector to be erased. The combination of A₁₉, A₁₈, A₁₇, A₁₆, A₁₅, A₁₄, A₁₃, and A₁₂ will uniquely select any sector.
BA = Bank Address (A₁₅ to A₁₉)
 - RD = Data read from location RA during read operation.
PD = Data to be programmed at location PA. Data is latched on the falling edge of write pulse.
 - SPA = Sector group address to be protected. Set sector group address (SGA) and (A₆, A₁, A₀) = (0, 1, 0).
SD = Sector group protection verify data. Output 01H at protected sector group addresses and output 00H at unprotected sector group addresses.
 - HRA = Address of the Hi-ROM area
29DL16XTD (Top Boot Type) Word Mode: 0F8000H to 0FFFFFFH
Byte Mode: 1F0000H to 1FFFFFFH
29DL16XBD (Bottom Boot Type) Word Mode: 000000H to 007FFFFH
Byte Mode: 000000H to 00FFFFFFH
 - HRBA = Bank Address of the Hi-ROM area
29DL16XTD (Top Boot Type) :A₁₅ = A₁₆ = A₁₇ = A₁₈ = A₁₉ = 1
29DL16XBD (Bottom Boot Type) :A₁₅ = A₁₆ = A₁₇ = A₁₈ = A₁₉ = 0
 - The system should generate the following address patterns:
Word Mode: 555H or 2AAH to addresses A₀ to A₁₀
Byte Mode: AAAH or 555H to addresses A₋₁ and A₀ to A₁₀
 - Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

*1: This command is valid while Fast Mode.

*2: This command is valid while RESET = V_{DD}.

*3: The valid addresses are A₆ to A₀.

*4: This command is valid while Hi-ROM mode.

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■ COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the devices to the read mode. Some commands are required Bank Address (BA) input. When command sequences are inputted to bank being read, the commands have priority than reading. Table 12 defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress. Also the Program Suspend (B0H) and Program Resume (30H) commands are valid only while the Program operation is in progress. Moreover both Read/Reset commands are functionally equivalent, resetting the device to the read mode. Please note that commands are always written at DQ₀ to DQ₇ and DQ₈ to DQ₁₅ bits are ignored.

• Read/Reset Command

In order to return from Autoselect mode or Exceeded Timing Limits (DQ₅ = 1) to Read/Reset mode, the Read/Reset operation is initiated by writing the Read/Reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The devices remain enabled for reads until the command register contents are altered.

The devices will automatically power-up in the Read/Reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

• Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the devices reside in the target system. PROM programmers typically access the signature codes by raising A₉ to a high voltage. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains an Autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the Autoselect command sequence into the command register.

The Autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address (BA) and the Autoselect command. Then the manufacture and device codes can be read from the bank, and an actual data of memory cell can be read from the another bank.

Following the command write, a read cycle from address (BA)00H retrieves the manufacture code of 04H. A read cycle from address (BA)01H for ×16 ((BA)02H for ×8) returns the device code (MBM29DL161TD = 36H and MBM29DL161BD = 39H for ×8 mode; MBM29DL161TD = 2236H and MBM29DL161BD = 2239H for ×16 mode), (MBM29DL162TD = 2DH and MBM29DL162BD = 2EH for ×8 mode; MBM29DL162TD = 222DH and MBM29DL162BD = 222EH for ×16 mode), (MBM29DL163TD = 28H and MBM29DL163BD = 2BH for ×8 mode; MBM29DL163TD = 2228H and MBM29DL163BD = 222BH for ×16 mode), (MBM29DL164TD = 33H and MBM29DL164BD = 35H for ×8 mode; MBM29DL164TD = 2233H and MBM29DL164BD = 2235H for ×16 mode). (See Tables 11.1 to 11.8.)

All manufacturer and device codes will exhibit odd parity with DQ₇ defined as the parity bit. Sector state (protection or unprotection) will be informed by address (BA)02H for ×16 ((BA)04H for ×8). Scanning the sector group addresses (A₁₉, A₁₈, A₁₇, A₁₆, A₁₅, A₁₄, A₁₃, and A₁₂) while (A₆, A₁, A₀) = (0, 1, 0) will produce a logical “1” at device output DQ₀ for a protected sector group. The programming verification should be performed by verify sector group protection on the protected sector. (See Tables 3 and 4.)

The manufacture and device codes can be allowed reading from selected bank. To read the manufacture and device codes and sector protection status from non-selected bank, it is necessary to write Read/Reset command sequence into the register and then Autoselect command should be written into the bank to be read.

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If the software (program code) for Autoselect command is stored into the Flash memory, the device and manufacture codes should be read from the other bank where is not contain the software.

To terminate the operation, it is necessary to write the Read/Reset command sequence into the register, and also to write the Autoselect command during the operation, execute it after writing Read/Reset command sequence.

• Byte/Word Programming

The devices are programmed on a byte-by-byte (or word-by-word) basis. Programming is a four bus cycle operation. There are two “unlock” write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) begins programming. Upon executing the Embedded Program Algorithm command sequence, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The system can determine the status of the program operation by using DQ_7 ($\overline{\text{Data Polling}}$), DQ_6 (Toggle Bit), or $RY/\overline{BY}$. The $\overline{\text{Data Polling}}$ and Toggle Bit must be performed at the memory location which is being programmed.

The automatic programming operation is completed when the data on DQ_7 is equivalent to data written to this bit at which time the devices return to the read mode and addresses are no longer latched. (See Table 13, Hardware Sequence Flags.) Therefore, the devices require that a valid address to the devices be supplied by the system at this particular instance of time. Hence, $\overline{\text{Data Polling}}$ must be performed at the memory location which is being programmed.

Any commands written to the chip during this period will be ignored. If hardware reset occurs during the programming operation, it is impossible to guarantee the data are being written.

Programming is allowed in any sequence and across sector boundaries. Beware that a data “0” cannot be programmed back to a “1”. Attempting to do so may either hang up the device or result in an apparent success according to the data polling algorithm but a read from Read/Reset mode will show that the data is still “0”. Only erase operations can convert “0”s to “1”s.

Figure 22 illustrates the Embedded Program™ Algorithm using typical command strings and bus operations.

• Chip Erase

Chip erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the chip erase command.

Chip erase does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the devices will automatically program and verify the entire memory for an all zero data pattern prior to electrical erase (Preprogram function). The system is not required to provide any controls or timings during these operations.

The system can determine the status of the erase operation by using DQ_7 ($\overline{\text{Data Polling}}$), DQ_6 (Toggle Bit), or $RY/\overline{BY}$. The chip erase begins on the rising edge of the last $\overline{CE}$ or $\overline{WE}$, whichever happens first in the command sequence and terminates when the data on DQ_7 is “1” (See Write Operation Status section.) at which time the device returns to read the mode.

Chip Erase Time; Sector Erase Time $\times$ All sectors + Chip Program Time (Preprogramming)

Figure 23 illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

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• Sector Erase

Sector erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the Sector Erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$ whichever happens later, while the command (Data = 30H) is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$ which happens first. After time-out of “ t_{TOW} ” from the rising edge of the last sector erase command, the sector erase operation will begin.

Multiple sectors may be erased concurrently by writing the six bus cycle operations on Table 12. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than “ t_{TOW} ” otherwise that command will not be accepted and erasure will start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of “ t_{TOW} ” from the rising edge of last $\overline{CE}$ or $\overline{WE}$ whichever happens first will initiate the execution of the Sector Erase command(s). If another falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first occurs within the “ t_{TOW} ” time-out window the timer is reset. (Monitor DQ_3 to determine if the sector erase timer window is still open, see section DQ_3 , Sector Erase Timer.) Any command other than Sector Erase or Erase Suspend during this time-out period will reset the devices to the read mode, ignoring the previous command string. Resetting the devices once execution has begun will corrupt the data in the sector. In that case, restart the erase on those sectors and allow them to complete. (Refer to the Write Operation Status section for Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 38).

Sector erase does not require the user to program the devices prior to erase. The devices automatically program all memory locations in the sector(s) to be erased prior to electrical erase (Preprogram function). When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

The system can determine the status of the erase operation by using DQ_7 ($\overline{Data}$ Polling), DQ_6 (Toggle Bit), or $RY/\overline{BY}$.

The sector erase begins after the “ t_{TOW} ” time out from the rising edge of $\overline{CE}$ or $\overline{WE}$ whichever happens first for the last sector erase command pulse and terminates when the data on DQ_7 is “1” (See Write Operation Status section.) at which time the devices return to the read mode. $\overline{Data}$ polling and Toggle Bit must be performed at an address within any of the sectors being erased.

Multiple Sector Erase Time; [Sector Erase Time + Sector Program Time (Preprogramming)] × Number of Sector Erase

In case of multiple sector erase across bank boundaries, a read from bank (read-while-erase) can not performe.

Figure 23 illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

• Erase Suspend/Resume

The Erase Suspend command allows the user to interrupt a Sector Erase operation and then perform data reads from or programs to a sector not being erased. This command is applicable ONLY during the Sector Erase operation which includes the time-out period for sector erase. The Erase Suspend command will be ignored if written during the Chip Erase operation or Embedded Program Algorithm. Writing the Erase Suspend command (B0H) during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Writing the Erase Resume command (30H) resumes the erase operation. The bank addresses of sector being erasing or suspending should be set when writing the Erase Suspend or Erase Resume command.

When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of “ t_{SPD} ” to suspend the erase operation. When the devices have entered the erase-suspended mode, the

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$\overline{RY/BY}$ output pin will be at Hi-Z and the DQ_7 bit will be at logic "1", and DQ_6 will stop toggling. The user must use the address of the erasing sector for reading DQ_6 and DQ_7 to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation has been suspended, the devices default to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-read mode will cause DQ_2 to toggle. (See the section on DQ_2 .)

After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for Program. This program mode is known as the erase-suspend-program mode. Again, programming in this mode is the same as programming in the regular Program mode except that the data must be programmed to sectors that are not erase-suspended. Successively reading from the erase-suspended sector while the devices are in the erase-suspend-program mode will cause DQ_2 to toggle. The end of the erase-suspended Program operation is detected by the $\overline{RY/BY}$ output pin, $\overline{Data}$ polling of DQ_7 or by the Toggle Bit I (DQ_6) which is the same as the regular Program operation. Note that DQ_7 must be read from the Program address while DQ_6 can be read from any address within bank being erase-suspended.

To resume the operation of Sector Erase, the Resume command (30H) should be written to the bank being erase suspended. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

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• Extended Command

(1) Fast Mode

MBM29DL16XTD/BD has Fast Mode function. This mode dispenses with the initial two unlock cycles required in the standard program command sequence by writing Fast Mode command into the command register. In this mode, the required bus cycle for programming is two cycles instead of four bus cycles in standard program command. (Do not write erase command in this mode.) The read operation is also executed after exiting this mode. To exit this mode, it is necessary to write Fast Mode Reset command into the command register. The first cycle must contain the bank address. (Refer to the Figure 28.) The V_{CC} active current is required even $\overline{CE} = V_{IH}$ during Fast Mode.

(2) Fast Programming

During Fast Mode, the programming can be executed with two bus cycles operation. The Embedded Program Algorithm is executed by writing program set-up command (A0H) and data write cycles (PA/PD). (Refer to the Figure 28.)

(3) Extended Sector Group Protection

In addition to normal sector group protection, the MBM29DL16XTD/BD has Extended Sector Group Protection as extended function. This function enable to protect sector group by forcing V_{ID} on $\overline{RESET}$ pin and write a command sequence. Unlike conventional procedure, it is not necessary to force V_{ID} and control timing for control pins. The only $\overline{RESET}$ pin requires V_{ID} for sector group protection in this mode. The extended sector group protection requires V_{ID} on $\overline{RESET}$ pin. With this condition, the operation is initiated by writing the set-up command (60H) into the command register. Then, the sector group addresses pins ($A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}$ and A_{12}) and (A_6, A_1, A_0) = (0, 1, 0) should be set to the sector group to be protected (recommend to set V_{IL} for the other addresses pins), and write extended sector group protection command (60H). A sector group is typically protected in 250 μs . To verify programming of the protection circuitry, the sector group addresses pins ($A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}$ and A_{12}) and (A_6, A_1, A_0) = (0, 1, 0) should be set and write a command (40H). Following the command write, a logical "1" at device output DQ_0 will produce for protected sector in the read operation. If the output data is logical "0", please repeat to write extended sector group protection command (60H) again. To terminate the operation, it is necessary to set $\overline{RESET}$ pin to V_{IH} . (Refer to the Figures 20 and 29.)

(4) CFI (Common Flash Memory Interface)

The CFI (Common Flash Memory Interface) specification outlines device and host system software interrogation handshake which allows specific vendor-specified software algorithms to be used for entire families of devices. This allows device-independent, JEDEC ID-independent, and forward-and backward-compatible software support for the specified flash device families. Refer to CFI specification in detail.

The operation is initiated by writing the query command (98H) into the command register. The bank address should be set when writing this command. Then the device information can be read from the bank, and an actual data of memory cell be read from the another bank. Following the command write, a read cycle from specific address retrieves device information. Please note that output data of upper byte (DQ_8 to DQ_{15}) is "0" in word mode (16 bit) read. Refer to the CFI code table. To terminate operation, it is necessary to write the read/reset command sequence into the register. (See Table 15.)

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• Hidden ROM (Hi-ROM) Region

The Hi-ROM feature provides a Flash memory region that the system may access through a new command sequence. This is primarily intended for customers who wish to use an Electronic Serial Number (ESN) in the device with the ESN protected against modification. Once the Hi-ROM region is protected, any further modification of that region is impossible. This ensures the security of the ESN once the product is shipped to the field.

The Hi-ROM region is 64K bytes in length and is stored at the same address of the 8KB ×8 sectors. The MBM29DL16XTD occupies the address of the byte mode 1F0000H to 1FFFFFFH (word mode 0F8000H to 0FFFFFFH) and the MBM29DL16XBD type occupies the address of the byte mode 000000H to 00FFFFFFH (word mode 000000H to 007FFFFH). After the system has written the Enter Hi-ROM command sequence, the system may read the Hi-ROM region by using the addresses normally occupied by the boot sectors. That is, the device sends all commands that would normally be sent to the boot sectors to the Hi-ROM region. This mode of operation continues until the system issues the Exit Hi-ROM command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to the boot sectors.

• Hidden ROM (Hi-ROM) Entry Command

MBM29DL16XTD/BD has a Hidden ROM area with One Time Protect function. This area is to enter the security code and to enable the change of the code once set. Program/erase is possible in this area until it is protected. However, once it is protected, it is impossible to unprotect, so please use this with caution.

Hidden ROM area is 64K Byte and in the same address area of 8KB sector. The address of top boot is 1F0000H to 1FFFFFFH at byte mode (0F8000H to 0FFFFFFH at word mode) and the bottom boot is 000000H to 00FFFFFFH at byte mode (000000H to 007FFFFH at word mode). These areas are normally the boot block area (8KB ×8 sector). Therefore, write the Hidden ROM entry command sequence to enter the Hidden ROM area. It is called as Hidden ROM mode when the Hidden ROM area appears.

Sector other than the boot block area could be read during Hidden ROM mode. Read/program/erase of the Hidden ROM area is possible during Hidden ROM mode. Write the Hidden ROM reset command sequence to exit the Hidden ROM mode. The bank address of the Hidden ROM should be set on the third cycle of this reset command sequence.

In case of MBM29DL161TD/BD, whose Bank 1 size is 0.5 Mbit, the simultaneous operation cannot execute multi-function mode between the Hidden ROM area and Bank 2 Region.

• Hidden ROM (Hi-ROM) Program Command

To program the data to the Hidden ROM area, write the Hidden ROM program command sequence during Hidden ROM mode. This command is same as the program command in the past except to write the command during Hidden ROM mode. Therefore the detection of completion method is the same as in the past, using the DQ₇ data poling, DQ₆ toggle bit and RY/ $\overline{\text{BY}}$ pin. Need to pay attention to the address to be programmed. If the address other than the Hidden ROM area is selected to program, the data of the address will be changed.

• Hidden ROM (Hi-ROM) Erase Command

To erase the Hidden ROM area, write the Hidden ROM erase command sequence during Hidden ROM mode. This command is same as the sector erase command in the past except to write the command during Hidden ROM mode. Therefore the detection of completion method is the same as in the past, using the DQ₇ data poling, DQ₆ toggle bit and RY/ $\overline{\text{BY}}$ pin. Need to pay attention to the sector address to be erased. If the sector address other than the Hidden ROM area is selected, the data of the sector will be changed.

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• Hidden ROM (Hi-ROM) Protect Command

There are two methods to protect the Hidden ROM area. One is to write the sector group protect setup command(60H), set the sector address in the Hidden ROM area and (A_6, A_1, A_0) = (0,1,0), and write the sector group protect command(60H) during the Hidden ROM mode. The same command sequence could be used because except that it is in the Hidden ROM mode and that it does not apply high voltage to $\overline{\text{RESET}}$ pin, it is the same as the extension sector group protect in the past. Please refer to "Function Explanation **Extended Command** (3) Extended Sector Group Protection" for details of extension sector group protect setting.

The other is to apply high voltage (V_{ID}) to A_9 and $\overline{\text{OE}}$, set the sector address in the Hidden ROM area and (A_6, A_1, A_0) = (0,1,0), and apply the write pulse during the Hidden ROM mode. To verify the protect circuit, apply high voltage (V_{ID}) to A_9 , specify (A_6, A_1, A_0) = (0,1,0) and the sector address in the Hidden ROM area, and read. When "1" appears to DQ_0 , the protect setting is completed. "0" will appear to DQ_0 if it is not protected. Please apply write pulse again. The same command sequence could be used for the above method because other than the Hidden ROM mode, it is the same as the sector group protect in the past. Please refer to "Function Explanation **Sector Group Protection**" for details of sector group protect setting

Other sector group will be effected if the address other than the Hidden ROM area is selected for the sector group address, so please be careful. Once it is protected, protection can not be cancelled, so please pay closest attention.

• Write Operation Status

Detailed in Table 13 are all the status flags that can determine the status of the bank for the current mode operation. The read operation from the bank where is not operate Embedded Algorithm returns a data of memory cell. These bits offer a method for determining whether a Embedded Algorithm is completed properly. The information on DQ_2 is address sensitive. This means that if an address from an erasing sector is consecutively read, then the DQ_2 bit will toggle. However, DQ_2 will not toggle if an address from a non-erasing sector is consecutively read. This allows the user to determine which sectors are erasing and which are not.

The status flag is not output from bank (non-busy bank) not executing Embedded Algorithm. For example, there is bank (busy bank) which is now executing Embedded Algorithm. When the read sequence is [1] <busy bank>, [2] <non-busy bank>, [3] <busy bank>, the DQ_6 is toggling in the case of [1] and [3]. In case of [2], the data of memory cell is outputted. In the erase-suspend read mode with the same read sequence, DQ_6 will not be toggled in the [1] and [3].

In the erase suspend read mode, DQ_2 is toggled in the [1] and [3]. In case of [2], the data of memory cell is outputted.

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Table 13 Hardware Sequence Flags

Status			DQ ₇	DQ ₆	DQ ₅	DQ ₃	DQ ₂
In Progress	Embedded Program Algorithm		$\overline{DQ}_7$	Toggle	0	0	1
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle*
	Program Suspended Mode	Program Suspend Read (Program Suspended Sector)	Data	Data	Data	Data	Data
		Program Suspend Read (Non-Program Suspended Sector)	Data	Data	Data	Data	Data
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	1	0	0	Toggle
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data
		Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ}_7$	Toggle	0	0	1 *
Exceeded Time Limits	Embedded Program Algorithm		$\overline{DQ}_7$	Toggle	1	0	1
	Embedded Erase Algorithm		0	Toggle	1	1	N/A
	Erase Suspended Mode	Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ}_7$	Toggle	1	0	N/A

* Successive reads from the erasing or erase-suspend sector will cause DQ₂ to toggle. Reading from non-erase suspend sector address will indicate logic "1" at the DQ₂ bit.

Notes: 1. DQ₀ and DQ₁ are reserve pins for future use.

2. DQ₄ is Fujitsu internal use only.

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• DQ₇

Data Polling

The MBM29DL16XTD/BD devices feature $\overline{\text{Data}}$ Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm an attempt to read the devices will produce the complement of the data last written to DQ₇. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ₇. During the Embedded Erase Algorithm, an attempt to read the device will produce a “0” at the DQ₇ output. Upon completion of the Embedded Erase Algorithm an attempt to read the device will produce a “1” at the DQ₇ output. The flowchart for $\overline{\text{Data}}$ Polling (DQ₇) is shown in Figure 24.

For programming, the $\overline{\text{Data}}$ Polling is valid after the rising edge of fourth write pulse in the four write pulse sequence.

For chip erase and sector erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth write pulse in the six write pulse sequence. $\overline{\text{Data}}$ Polling must be performed at sector address within any of the sectors being erased and not a protected sector. Otherwise, the status may not be valid.

If a program address falls within a protected sector, $\overline{\text{Data}}$ Polling on DQ₇ is active for approximately 1 μs , then that bank returns to the read mode. After an erase command sequence is written, if all sectors selected for erasing are protected, $\overline{\text{Data}}$ Polling on DQ₇ is active for approximately 400 μs , then the bank returns to read mode.

Once the Embedded Algorithm operation is close to being completed, the MBM29DL16XTD/BD data pins (DQ₇) may change asynchronously while the output enable ($\overline{\text{OE}}$) is asserted low. This means that the devices are driving status information on DQ₇ at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the DQ₇ output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operation and DQ₇ has a valid data, the data outputs on DQ₀ to DQ₆ may be still invalid. The valid data on DQ₀ to DQ₇ will be read on the successive read attempts.

The $\overline{\text{Data}}$ Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm or sector erase time-out. (See Table 13.)

See Figure 9 for the $\overline{\text{Data}}$ Polling timing specifications and diagrams.

• DQ₆

Toggle Bit I

The MBM29DL16XTD/BD also feature the “Toggle Bit I” as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{\text{OE}}$ toggling) data from the devices will result in DQ₆ toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ₆ will stop toggling and valid data will be read on the next successive attempts. During programming, the Toggle Bit I is valid after the rising edge of the fourth write pulse in the four write pulse sequence. For chip erase and sector erase, the Toggle Bit I is valid after the rising edge of the sixth write pulse in the six write pulse sequence. The Toggle Bit I is active during the sector time out.

In programming, if the sector being written to is protected, the toggle bit will toggle for about 1 μs and then stop toggling without the data having changed. In erase, the devices will erase all the selected sectors except for the ones that are protected. If all selected sectors are protected, the chip will toggle the toggle bit for about 400 μs and then drop back into read mode, having changed none of the data.

Either $\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggling will cause the DQ₆ to toggle. In addition, an Erase Suspend/Resume command will cause the DQ₆ to toggle.

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The system can use DQ₆ to determine whether a sector is actively erasing or is erase-suspended. When a bank is actively erasing (that is, the Embedded Erase Algorithm is in progress), DQ₆ toggles. When a bank enters the Erase Suspend mode, DQ₆ stops toggling. Successive read cycles during the erase-suspend-program cause DQ₆ to toggle.

To operate toggle bit function properly, $\overline{CE}$ or $\overline{OE}$ must be high when bank address is changed.

See Figure 10 for the Toggle Bit I timing specifications and diagrams.

• DQ₅

Exceeded Timing Limits

DQ₅ will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ₅ will produce a “1”. This is a failure condition which indicates that the program or erase cycle was not successfully completed. Data Polling is the only operating function of the devices under this condition. The $\overline{CE}$ circuit will partially power down the device under these conditions (to approximately 2 mA). The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable functions as described in Tables 3 and 4.

The DQ₅ failure condition may also appear if a user tries to program a non blank location without erasing. In this case the devices lock out and never complete the Embedded Algorithm operation. Hence, the system never reads a valid data on DQ₇ bit and DQ₆ never stops toggling. Once the devices have exceeded timing limits, the DQ₅ bit will indicate a “1.” Please note that this is not a device failure condition since the devices were incorrectly used. If this occurs, reset the device with command sequence.

• DQ₃

Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ₃ will remain low until the time-out is complete. Data Polling and Toggle Bit are valid after the initial sector erase command sequence.

If Data Polling or the Toggle Bit I indicates the device has been written with a valid erase command, DQ₃ may be used to determine if the sector erase timer window is still open. If DQ₃ is high (“1”) the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by Data Polling or Toggle Bit I. If DQ₃ is low (“0”), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ₃ prior to and following each subsequent Sector Erase command. If DQ₃ were high on the second status check, the command may not have been accepted.

See Table 13: Hardware Sequence Flags.

• DQ₂

Toggle Bit II

This toggle bit II, along with DQ₆, can be used to determine whether the devices are in the Embedded Erase Algorithm or in Erase Suspend.

Successive reads from the erasing sector will cause DQ₂ to toggle during the Embedded Erase Algorithm. If the devices are in the erase-suspended-read mode, successive reads from the erase-suspended sector will cause DQ₂ to toggle. When the devices are in the erase-suspended-program mode, successive reads from the byte address of the non-erase suspended sector will indicate a logic “1” at the DQ₂ bit.

DQ₆ is different from DQ₂ in that DQ₆ toggles only when the standard program or Erase, or Erase Suspend Program operation is in progress. The behavior of these two status bits, along with that of DQ₇, is summarized as follows:

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For example, DQ₂ and DQ₆ can be used together to determine if the erase-suspend-read mode is in progress. (DQ₂ toggles while DQ₆ does not.) See also Table 14 and Figure 12.

Furthermore, DQ₂ can also be used to determine which sector is being erased. When the device is in the erase mode, DQ₂ toggles if this bit is read from an erasing sector.

To operate toggle bit function properly, $\overline{CE}$ or $\overline{OE}$ must be high when bank address is changed.

Table 14 Toggle Bit Status

Mode	DQ ₇	DQ ₆	DQ ₂
Program	$\overline{DQ_7}$	Toggle	1
Erase	0	Toggle	Toggle (Note)
Erase-Suspend Read (Erase-Suspended Sector)	1	1	Toggle
Erase-Suspend Program	$\overline{DQ_7}$	Toggle	1 (Note)

Note: Successive reads from the erasing or erase-suspend sector will cause DQ₂ to toggle. Reading from non-erase suspend sector address will indicate logic "1" at the DQ₂ bit.

• RY/ $\overline{BY}$

Ready/Busy

The MBM29DL16XTD/BD provide a RY/ $\overline{BY}$ open-drain output pin as a way to indicate to the host system that the Embedded Algorithms are either in progress or has been completed. If the output is low, the devices are busy with either a program or erase operation. If the output is high, the devices are ready to accept any read/write or erase operation. When the RY/ $\overline{BY}$ pin is low, the devices will not accept any additional program or erase commands. If the MBM29DL16XTD/BD are placed in an Erase Suspend mode, the RY/ $\overline{BY}$ output will be high.

During programming, the RY/ $\overline{BY}$ pin is driven low after the rising edge of the fourth write pulse. During an erase operation, the RY/ $\overline{BY}$ pin is driven low after the rising edge of the sixth write pulse. The RY/ $\overline{BY}$ pin will indicate a busy condition during the $\overline{RESET}$ pulse. Refer to Figures 13 and 14 for a detailed timing diagram. The RY/ $\overline{BY}$ pin is pulled high in standby mode.

Since this is an open-drain output, RY/ $\overline{BY}$ pins can be tied together in parallel with a pull-up resistor to V_{CC}.

• Byte/Word Configuration

The $\overline{BYTE}$ pin selects the byte (8-bit) mode or word (16-bit) mode for the MBM29DL16XTD/BD devices. When this pin is driven high, the devices operate in the word (16-bit) mode. The data is read and programmed at DQ₀ to DQ₁₅. When this pin is driven low, the devices operate in byte (8-bit) mode. Under this mode, the DQ_{15/A-1} pin becomes the lowest address bit and DQ₈ to DQ₁₄ bits are tri-stated. However, the command bus cycle is always an 8-bit operation and hence commands are written at DQ₀ to DQ₇ and the DQ₈ to DQ₁₅ bits are ignored. Refer to Figures 15, 16 and 17 for the timing diagram.

• Data Protection

The MBM29DL16XTD/BD are designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the devices automatically reset the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The devices also incorporate several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

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- **Low V_{CC} Write Inhibit**

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than V_{LKO} (min). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO} . It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above V_{LKO} (min).

If Embedded Erase Algorithm is interrupted, there is possibility that the erasing sector(s) cannot be used.

- **Write Pulse “Glitch” Protection**

Noise pulses of less than 5 ns (typical) on $\overline{OE}$, $\overline{CE}$, or $\overline{WE}$ will not initiate a write cycle.

- **Logical Inhibit**

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$, or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

- **Power-Up Write Inhibit**

Power-up of the devices with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

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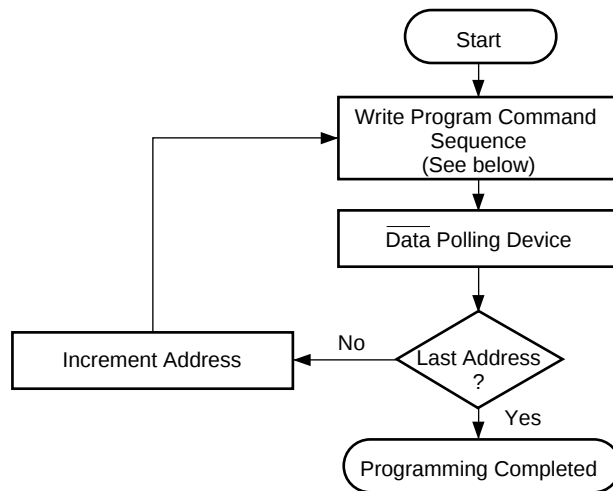
Table 15 Common Flash Memory Interface Code

Description	A ₀ to A ₆	DQ ₀ to DQ ₁₅	Description	A ₀ to A ₆	DQ ₀ to DQ ₁₅
Query-unique ASCII string "QRY"	10h 11h 12h	0051h 0052h 0059h	Query-unique ASCII string "PRI"	40h 41h 42h	0050h 0052h 0049h
Primary OEM Command Set 2h: AMD/FJ standard type	13h 14h	0002h 0000h	Major version number, ASCII	43h	0031h
Address for Primary Extended Table	15h 16h	0040h 0000h	Minor version number, ASCII	44h	0031h
Alternate OEM Command Set (00h = not applicable)	17h 18h	0000h 0000h	Address Sensitive Unlock 0h = Required 1h = Not Required	45h	0000h
Address for Alternate OEM Extended Table	19h 1Ah	0000h 0000h	Erase Suspend 0h = Not Supported 1h = To Read Only 2h = To Read & Write	46h	0002h
V _{CC} Min. (write/erase) D7-4: volt, D3-0: 100 mvolt	1Bh	0027h	Sector Protection 0h = Not Supported X = Number of sectors in per group	47h	0001h
V _{CC} Max. (write/erase) D7-4: volt, D3-0: 100 mvolt	1Ch	0036h	Sector Temporary Unprotection 00h = Not Supported 01h = Supported	48h	0001h
V _{PP} Min. voltage	1Dh	0000h	Sector Protection Algorithm	49h	0004h
V _{PP} Max. voltage	1Eh	0000h	Number of Sector for Bank 2 00h = Not Supported 3Fh = MBM29DL161TD 38h = MBM29DL162TD 30h = MBM29DL163TD 20h = MBM29DL164TD 3Fh = MBM29DL161BD 38h = MBM29DL162BD 30h = MBM29DL163BD 20h = MBM29DL164BD	4Ah	00XXh
Typical timeout per single byte/word write 2 ^N μS	1Fh	0004h	Burst Mode Type 00h = Not Supported	4Bh	0000h
Typical timeout for Min. size buffer write 2 ^N μS	20h	0000h	Page Mode Type 00h = Not Supported	4Ch	0000h
Typical timeout per individual block erase 2 ^N mS	21h	000Ah	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-4: volt, D3-0: 100 mvolt	4Dh	0085h
Typical timeout for full chip erase 2 ^N mS	22h	0000h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-4: volt, D3-0: 100 mvolt	4Eh	0095h
Max. timeout for byte/word write 2 ^N times typical	23h	0005h	Boot Type 02h = MBM29DL16XBD 03h = MBM29DL16XTD	4Fh	00XXh
Max. timeout for buffer write 2 ^N times typical	24h	0000h			
Max. timeout per individual block erase 2 ^N times typical	25h	0004h			
Max. timeout for full chip erase 2 ^N times typical	26h	0000h			
Device Size = 2 ^N byte	27h	0015h			
Flash Device Interface description	28h 29h	0002h 0000h			
Max. number of byte in multi-byte write = 2 ^N	2Ah 2Bh	0000h 0000h			
Number of Erase Block Regions within device	2Ch	0002h			
Erase Block Region 1 Information	2Dh 2Eh 2Fh 30h	0007h 0000h 0020h 0000h			
Erase Block Region 2 Information	31h 32h 33h 34h	001Eh 0000h 0000h 0001h			

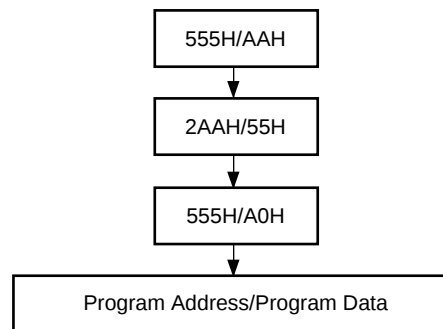
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■ FLOW CHART

EMBEDDED ALGORITHMS



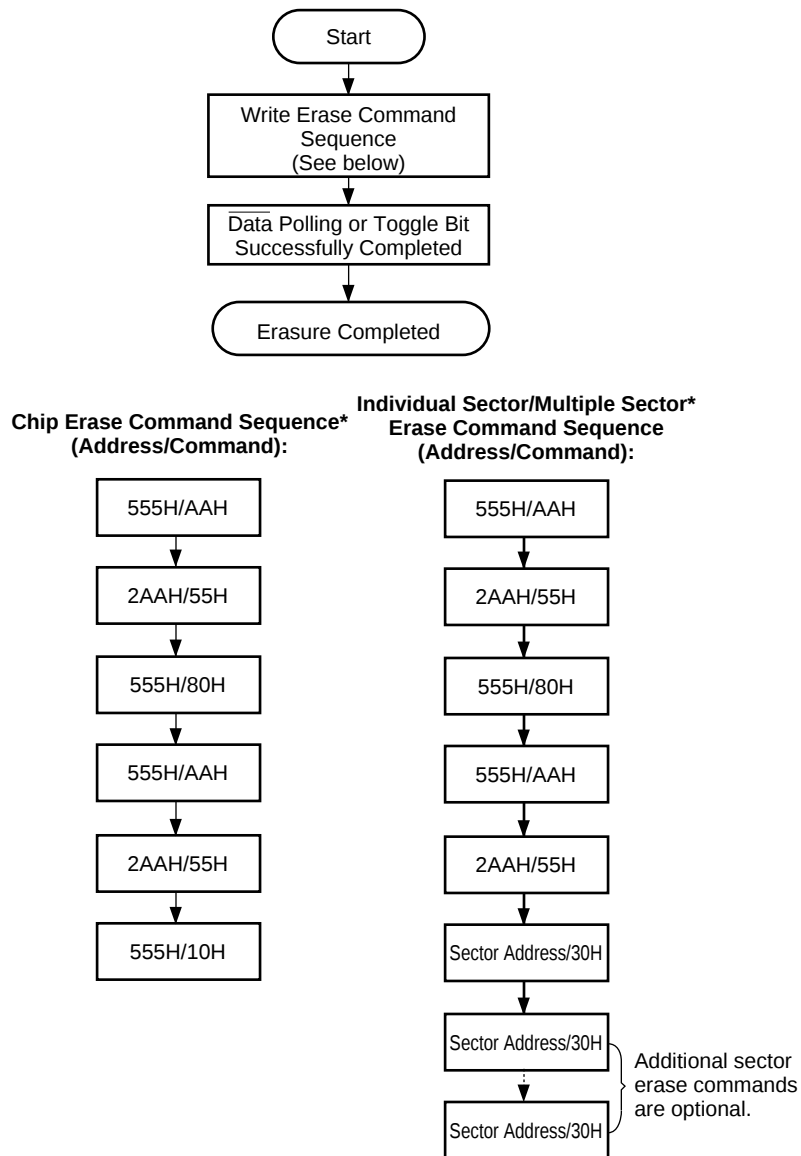
Program Command Sequence* (Address/Command):



* : The sequence is applied for $\times 16$ mode.
The addresses differ from $\times 8$ mode.

Figure 22 Embedded Program™ Algorithm

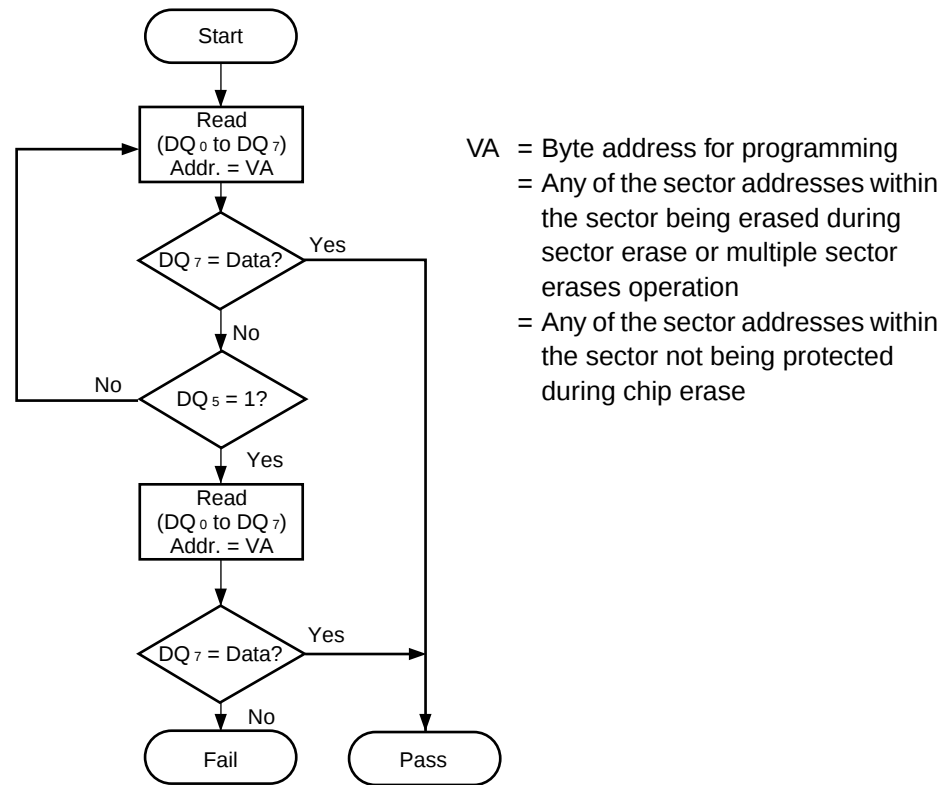
EMBEDDED ALGORITHMS



* : The sequence is applied for $\times 16$ mode.
The addresses differ from $\times 8$ mode.

Figure 23 Embedded Erase™ Algorithm

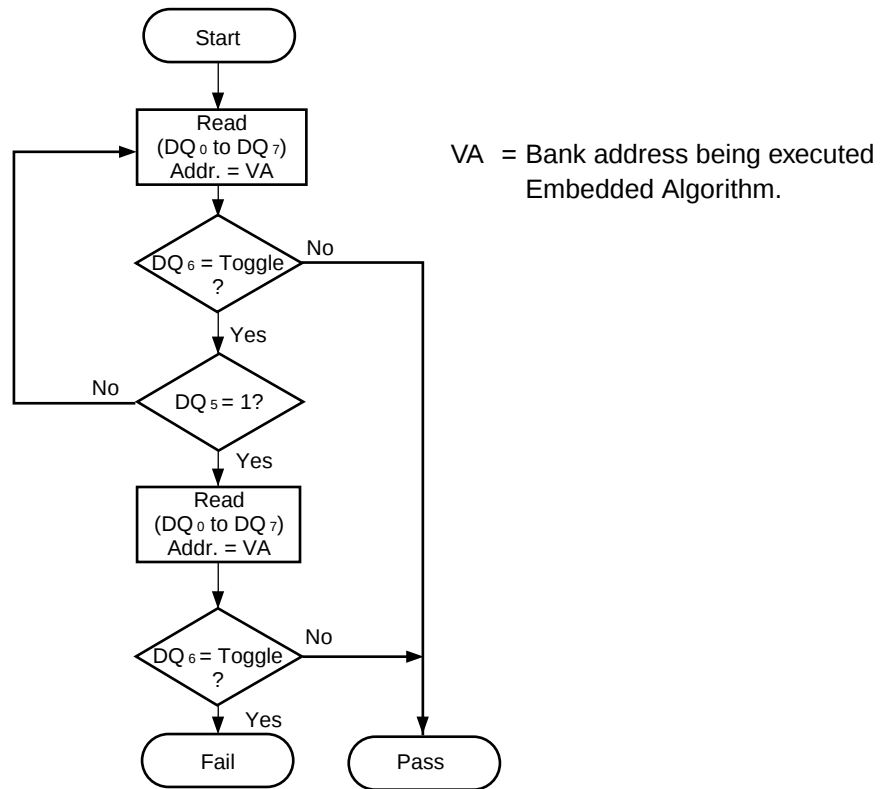
MBM29DL16XTD/BD-70/90/12



Note: DQ₇ is rechecked even if DQ₅ = "1" because DQ₇ may change simultaneously with DQ₅.

Figure 24 Data Polling Algorithm

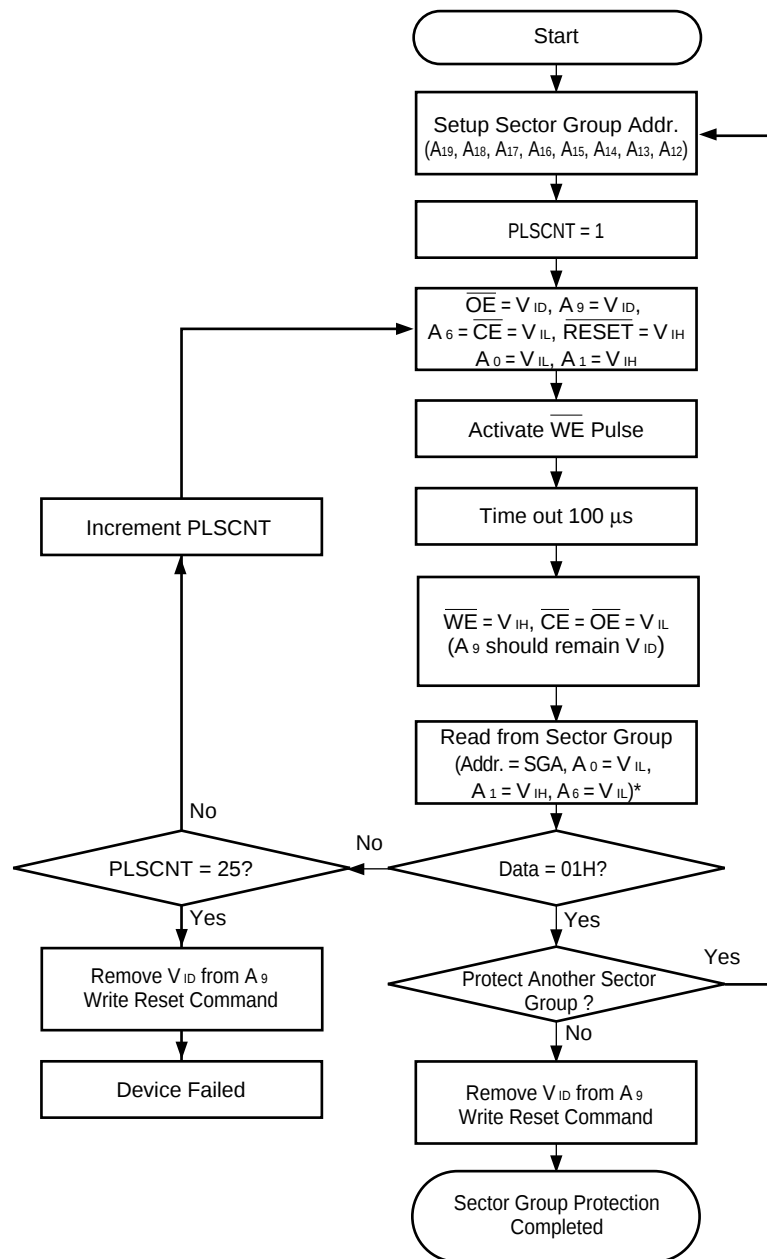
MBM29DL16XTD/BD-70/90/12



Note: DQ₆ is rechecked even if DQ₅ = "1" because DQ₆ may stop toggling at the same time as DQ₅ changing to "1".

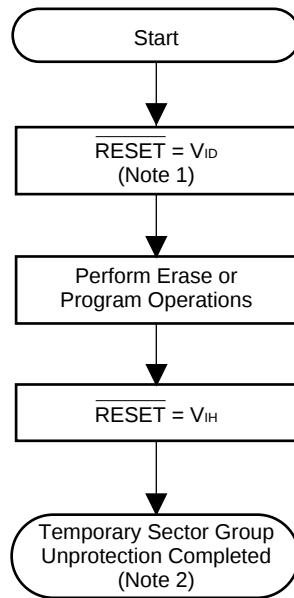
Figure 25 Toggle Bit Algorithm

MBM29DL16XTD/BD-70/90/12



* : A-1 is V_{IL} on byte mode.

Figure 26 Sector Group Protection Algorithm

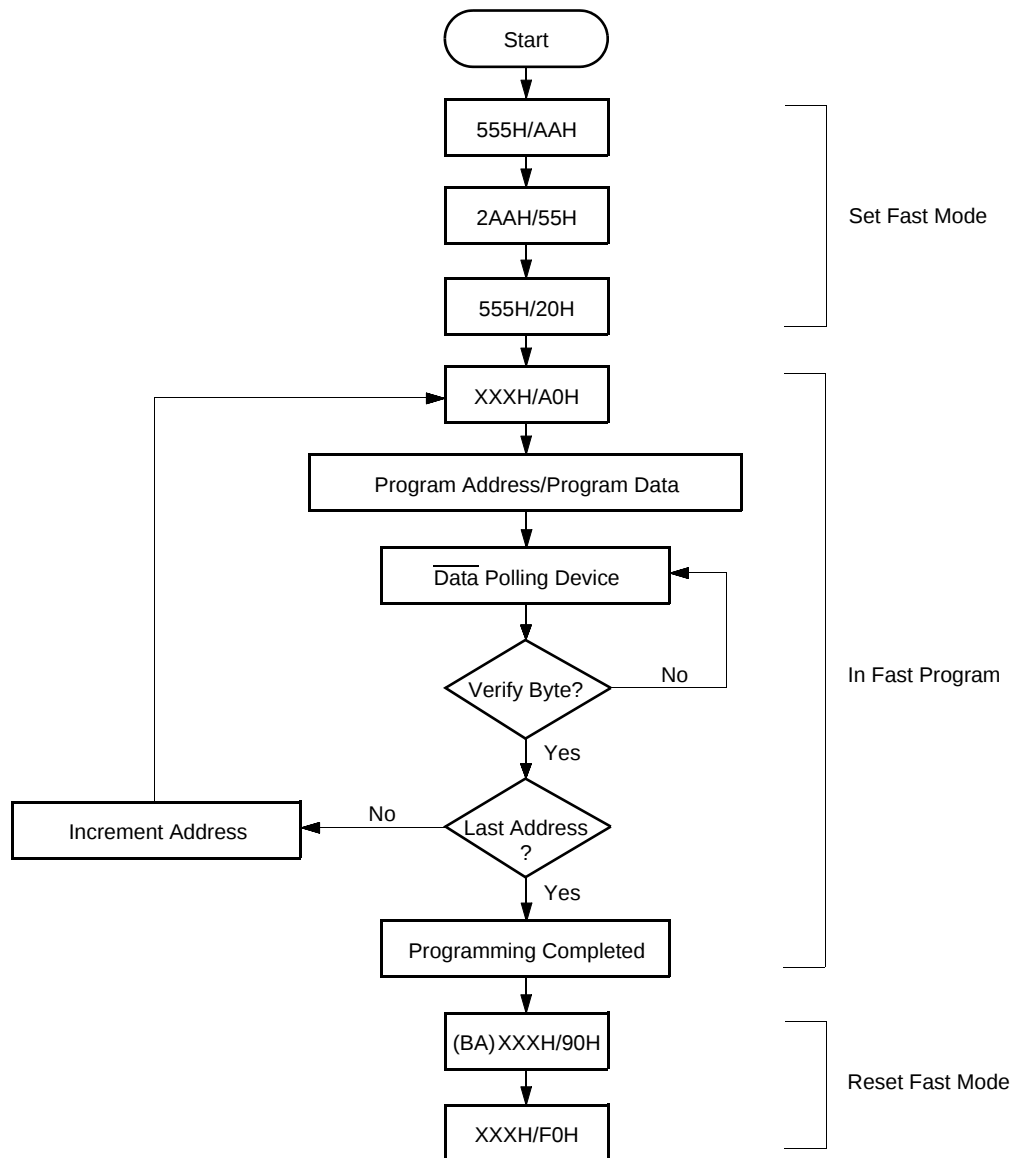
MBM29DL16XTD/BD-70/90/12

- Notes: 1. All protected sector groups are unprotected.
2. All previously protected sector groups are protected once again.

Figure 27 Temporary Sector Group Unprotection Algorithm

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FAST MODE ALGORITHM



Note: The sequence is applied for $\times 16$ mode.
The addresses differ from $\times 8$ mode.

Figure 28 Embedded Program™ Algorithm for Fast Mode

MBM29DL16XTD/BD-70/90/12

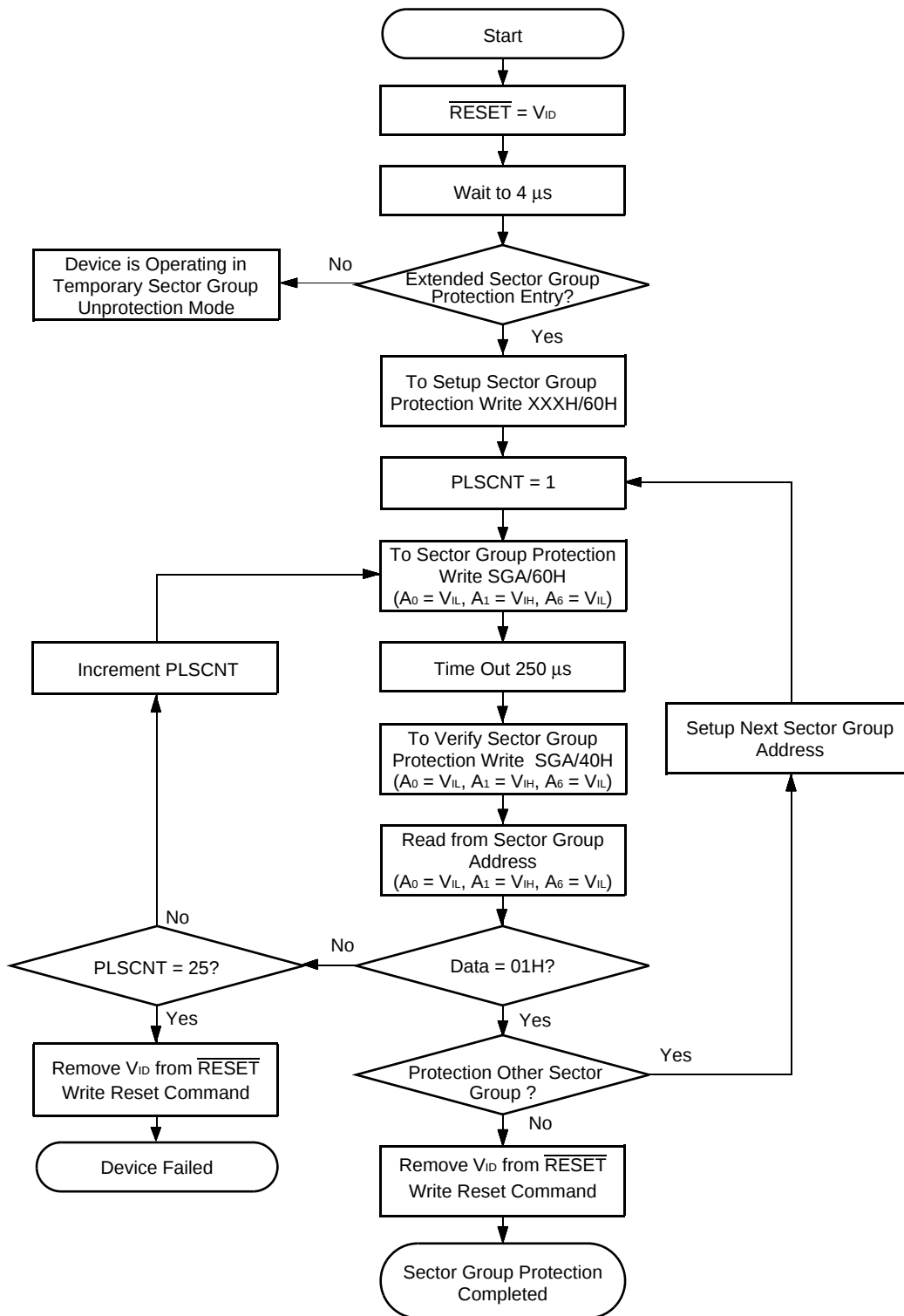


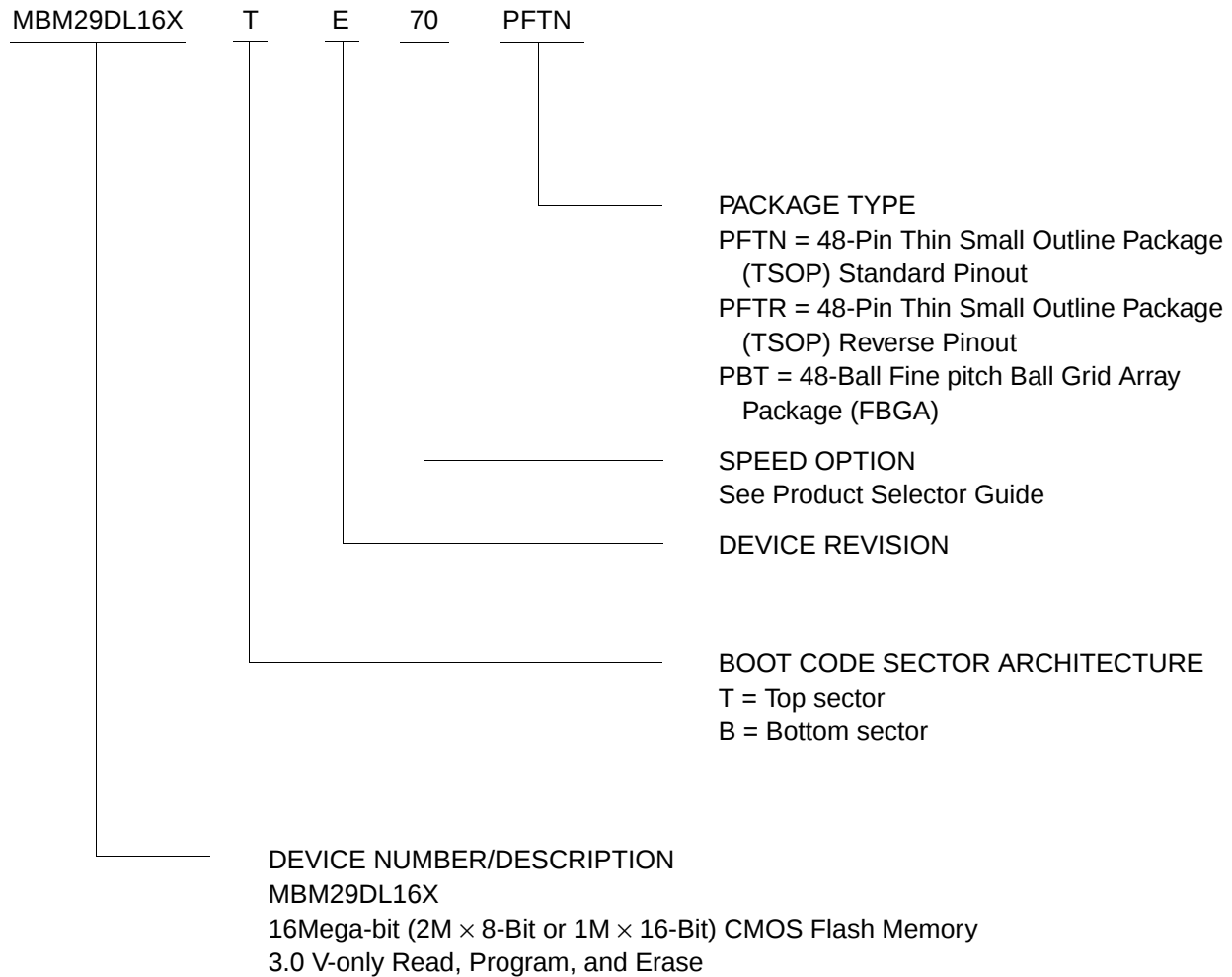
Figure 29 Extended Sector Group Protection Algorithm

MBM29DL16XTD/BD-70/90/12

■ ORDERING INFORMATION

Standard Products

Fujitsu standard products are available in several packages. The order number is formed by a combination of:



Valid Combinations		
MBM29DL161TD/BD	70 90 12	PFTN PFTR PBT
MBM29DL162TD/BD		
MBM29DL163TD/BD		
MBM29DL164TD/BD		

Valid Combinations

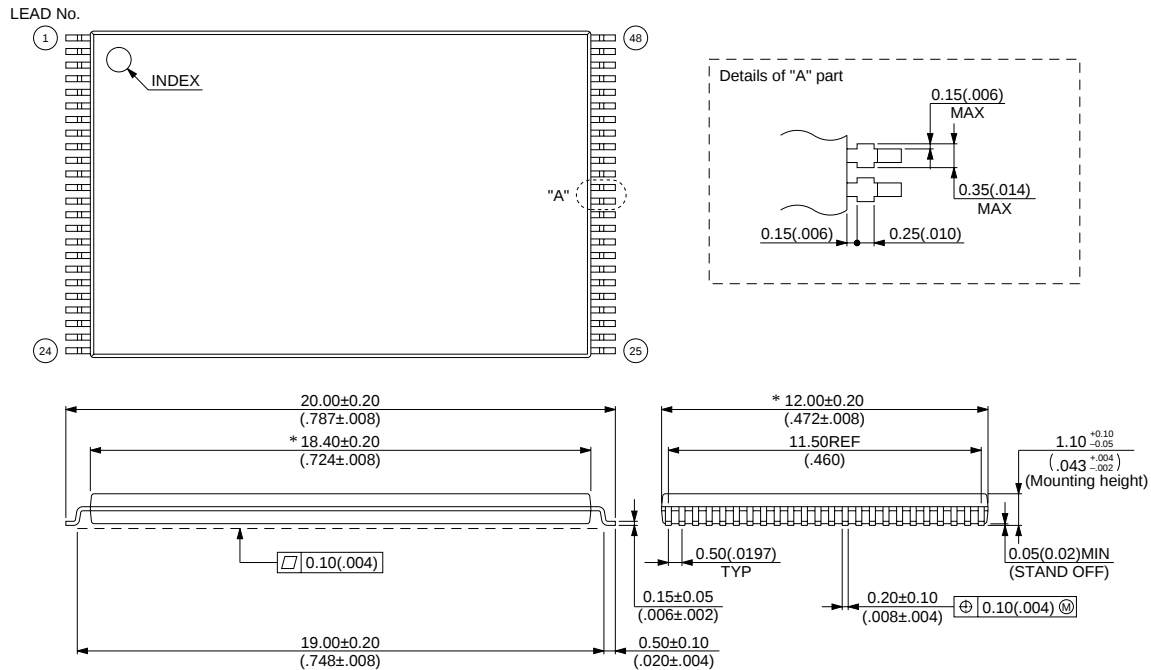
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Fujitsu sales office to confirm availability of specific valid combinations and to check on newly released combinations.

MBM29DL16XTD/BD-70/90/12

■ PACKAGE DIMENSIONS

48-pin plastic TSOP(I)
(FPT-48P-M19)

* Resin Protrusion. (Each Side: 0.15 (.006)Max)

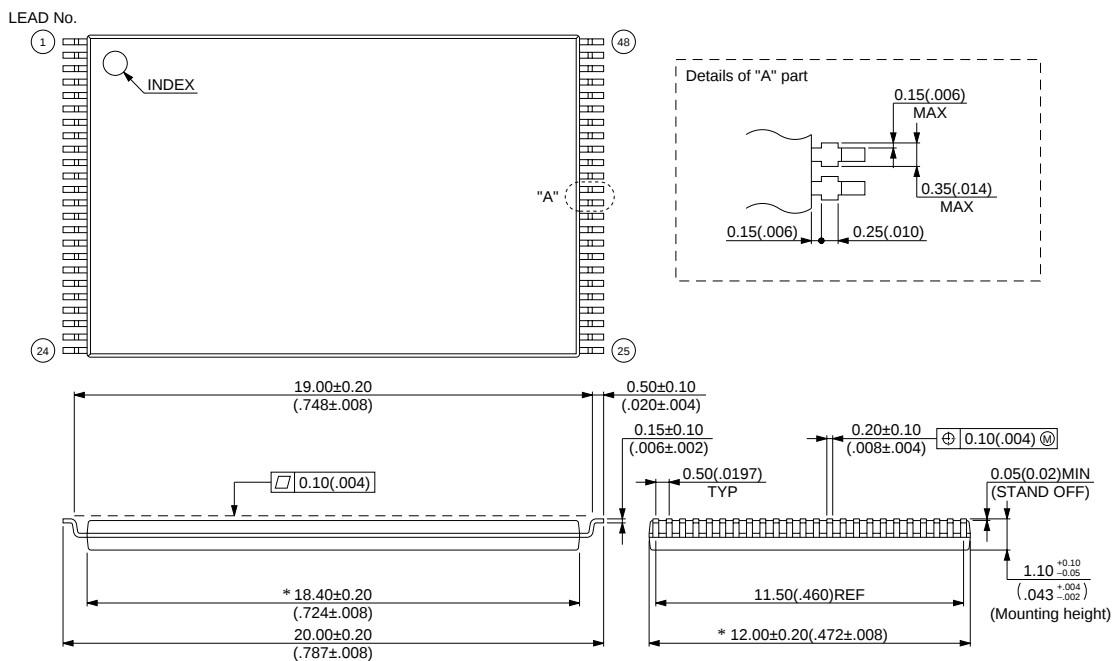


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Dimensions in mm (inches)

48-pin plastic TSOP(I)
(FPT-48P-M20)

* Resin Protrusion. (Each Side: 0.15 (.006)Max)



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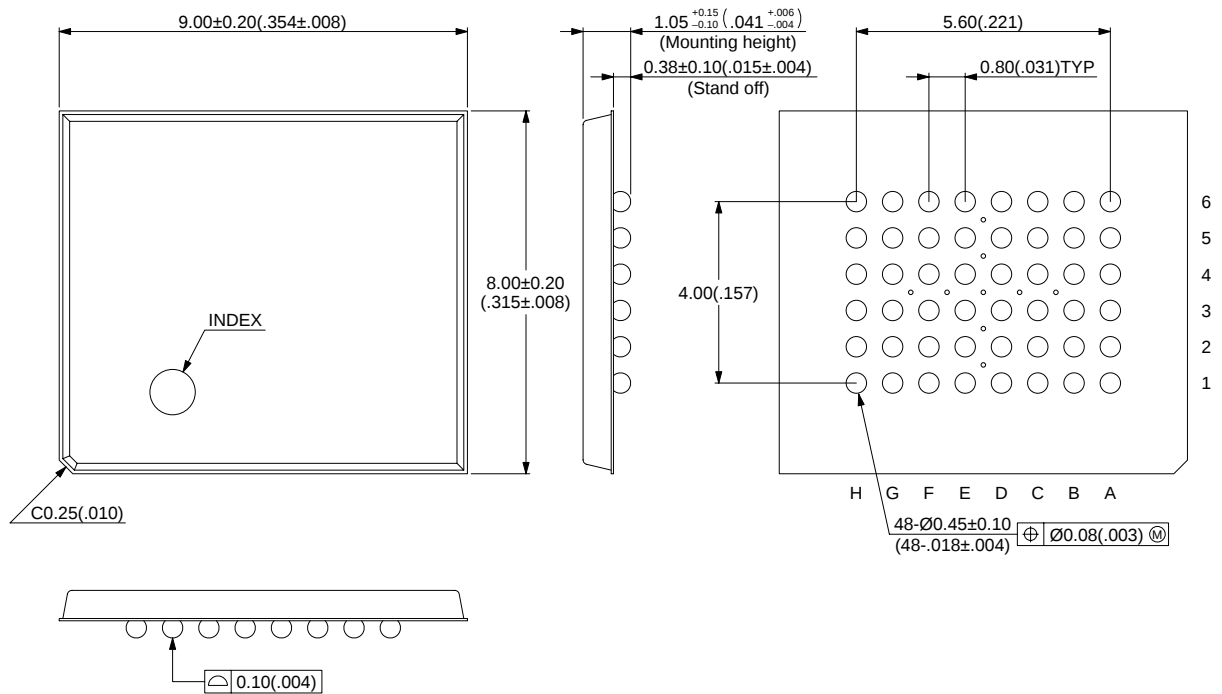
Dimensions in mm (inches)

(Continued)

MBM29DL16XTD/BD-70/90/12

(Continued)

48-pin plastic FBGA
(BGA-48P-M13)



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Dimensions in mm (inches)

MBM29DL16XTD/BD-70/90/12

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