

FlipKY[®], Chip Scale Package Schottky Barrier Rectifier, 0.5 A



FlipKY[®]

FEATURES

- Ultra low V_F to footprint area
- Very low profile (< 0.6 mm)
- Low thermal resistance
- Supplied tested and on tape and reel
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT

APPLICATIONS

- Reverse polarity protection
- Current steering
- Freewheeling
- Flyback
- Oring

DESCRIPTION

Vishay's FlipKY[®] product family utilizes wafer level chip scale packaging to deliver Schottky diodes with the lowest V_F to PCB footprint area in industry. The three pad 0.9 mm x 1.2 mm devices can deliver up to 0.5 A and occupy only 1.08 mm² of board space. The anode and cathode connections are made through solder bump pads on one side of the silicon enabling designers to strategically place the diodes on the PCB. This design not only minimizes board space but also reduces thermal resistance and inductance, which can improve overall circuit efficiency.

Typical applications include hand-held, portable equipment such as cell phones, MP3 players, bluetooth, GPS, PDAs, and portable hard disk drives where space savings and performance are crucial.

PRODUCT SUMMARY

$I_{F(AV)}$	0.5 A
V_R	40 V
V_F at I_F	0.42 V
I_{RM} max. at 25 °C	10 μ A
I_{RM} max. at 125 °C	2 mA
T_J max.	150 °C
E_{AS}	5 mJ

MAJOR RATINGS AND CHARACTERISTICS

SYMBOL	CHARACTERISTICS	MAX.	UNITS
V_{RRM}		40	V
$I_{F(AV)}$	Rectangular waveform	0.5	A
I_{FSM}		190	
V_F	0.5 A _{pk} , $T_J = 125$ °C	0.42	V
T_J		- 55 to 150	°C

VOLTAGE RATINGS

PARAMETER	SYMBOL	VS-FCSP05H40TR	UNITS
Maximum DC reverse voltage	V_R	40	V
Maximum working peak reverse voltage	V_{RWM}		

**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum average forward current	$I_{F(AV)}$	50 % duty cycle at $T_{PCB} = 114\text{ }^{\circ}\text{C}$, rectangular waveform	0.5	A
Maximum peak one cycle non-repetitive surge current at $25\text{ }^{\circ}\text{C}$	I_{FSM}	5 μs sine or 3 μs rect. pulse	190	
		10 ms sine or 6 ms rect. pulse	10	
Non-repetitive avalanche energy	E_{AS}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_{AS} = 2.0\text{ A}$, $L = 5.0\text{ mH}$	5	mJ
Repetitive avalanche current	I_{AR}	Current decaying linearly to zero in 1 μs Frequency limited by T_J maximum $V_A = 1.5 \times V_R$ typical	0.5	A

ELECTRICAL SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		TYP.	MAX.	UNITS
Maximum forward voltage drop See fig. 1	V _{FM} ⁽¹⁾	0.5 A	T _J = 25 °C	0.48	0.52	V
		1 A		0.54	0.58	
		0.5 A	T _J = 125 °C	0.38	0.42	
		1 A		0.46	0.50	
Maximum reverse leakage current See fig. 2	I _{RM} ⁽¹⁾	T _J = 25 °C	V _R = Rated V _R	1	10	μA
			V _R = 20 V	0.2	0.5	
			V _R = 10 V	0.08	0.25	
			V _R = 5 V	0.05	0.15	
		T _J = 125 °C	V _R = Rated V _R	0.5	2	mA
			V _R = 20 V	0.2	1	
			V _R = 10 V	0.15	0.8	
			V _R = 5 V	0.125	0.5	
Maximum junction capacitance	C _T	V _R = 5 V _{DC} (test signal range 100 kHz to 1 MHz), 25 °C		-	90	pF
Maximum voltage rate of charge	dV/dt	Rated V _R		-	10 000	V/μs

Note(1) Pulse width < 300 μs , duty cycle < 2 %**THERMAL - MECHANICAL SPECIFICATIONS**

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction and storage temperature range	$T_J^{(1)}$, T_{Stg}		- 55 to 150	$^{\circ}\text{C}$
Typical thermal resistance, junction to PCB	$R_{thJL}^{(2)}$	DC operation	35	$^{\circ}\text{C/W}$
Maximum thermal resistance, junction to ambient	R_{thJA}		150	

Notes(1) $\frac{dP_{tot}}{dT_J} < \frac{1}{R_{thJA}}$ thermal runaway condition for a diode on its own heatsink

(2) Mounted on minimum footprint PCB

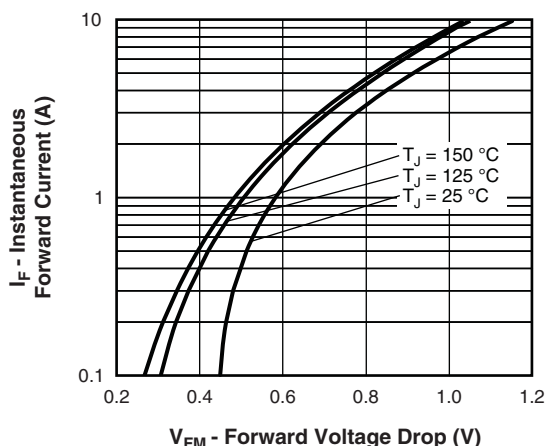


Fig. 1 - Maximum Forward Voltage Drop Characteristics (Per Leg)

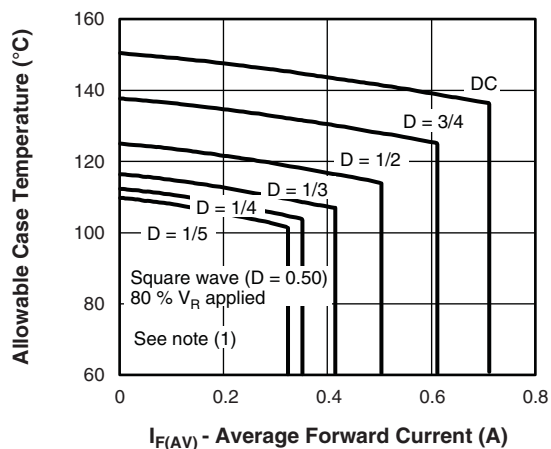


Fig. 4 - Maximum Allowable Case Temperature vs. Average Forward Current (Per Leg)

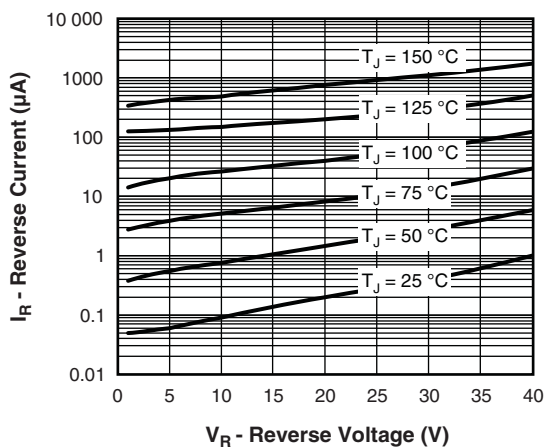


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage (Per Leg)

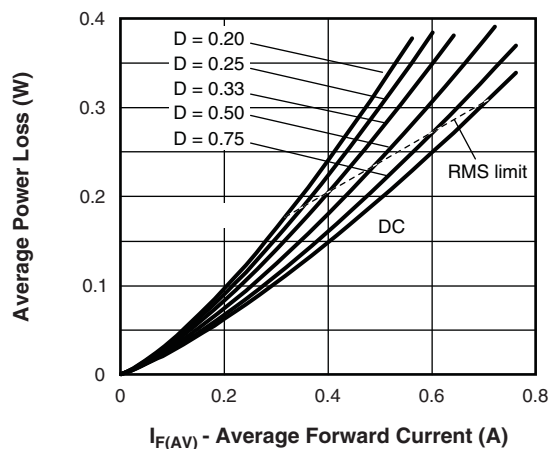


Fig. 5 - Forward Power Loss Characteristics (Per Leg)

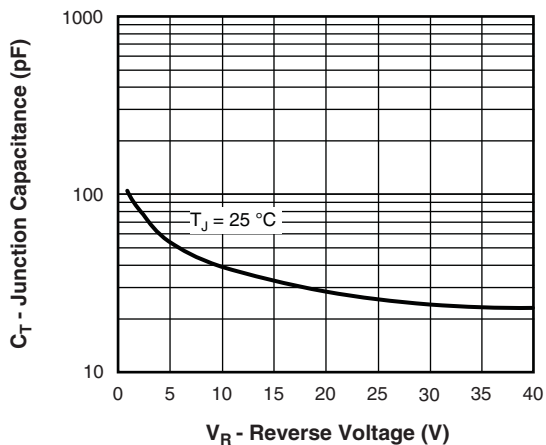


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage (Per Leg)

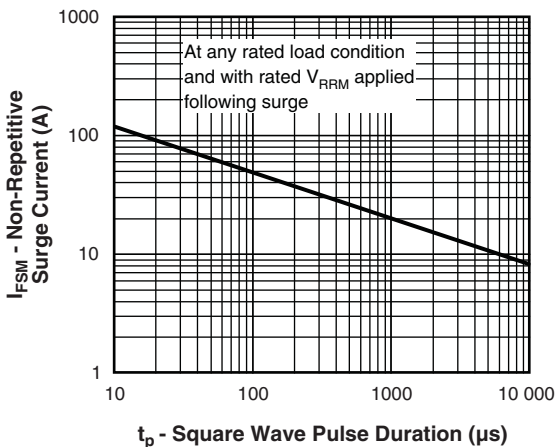


Fig. 6 - Maximum Non-Repetitive Surge Current (Per Leg)

Note

- (1) Formula used: $T_C = T_J - (P_d + P_{dREV}) \times R_{thJC}$
 P_d = Forward power loss = $I_{F(AV)} \times V_{FM}$ at $(I_{F(AV)}/D)$ (see fig. 6); P_{dREV} = Inverse power loss = $V_{R1} \times I_R (1 - D)$; I_R at 80 % V_R applied

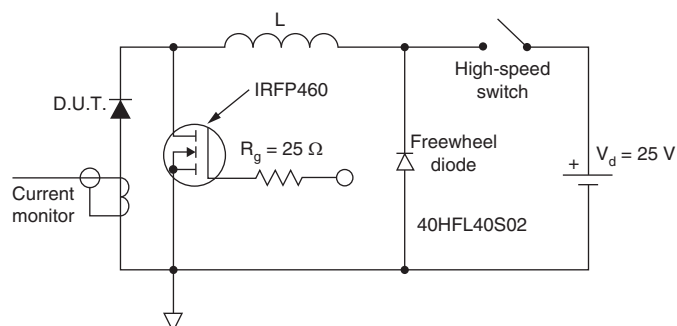
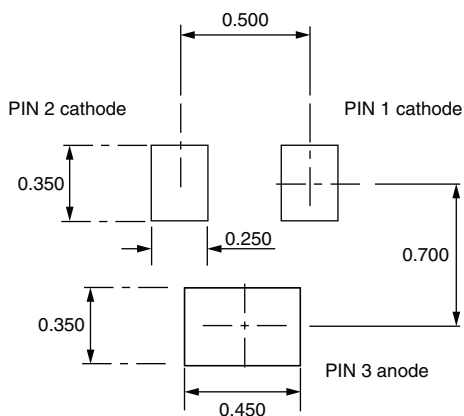
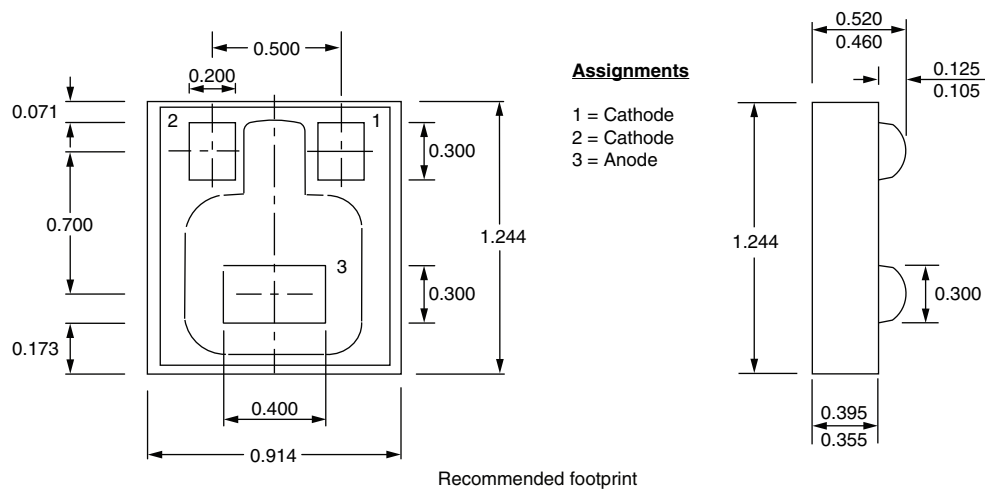


Fig. 7 - Unclamped Inductive Test Circuit

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95049
Part marking information	www.vishay.com/doc?95060
Packaging information	www.vishay.com/doc?95062
SPICE model	www.vishay.com/doc?95318

FlipKY® 0.5 A/0.75 A

DIMENSIONS in millimeters



Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Controlling dimension: millimeter



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