

HN27C256AG Series

32768-word × 8-bit UV Erasable and Programmable ROM

This Hitachi HN27C256AG is a 256-kbit ultraviolet erasable and electrically programmable ROM, featuring high speed and low power dissipation.

Fabricated on advanced fine process and high speed circuitry technique, the HN27C256AG makes high speed access time possible for 16 bit microprocessors such as the 8086 and 68000. And low power dissipation in active and standby modes matches our CMOS 256-kbit EPROM.

In programming operation, the HN27C256AG realizes faster programming times than our conventional 256-kbit EPROM by Hitachi's Fast High-Reliability Programming Algorithm.

Pin arrangement, pin configuration and programming voltage are compatible with our 256-kbit EPROM series, therefore existing programmers can be used with the HN27C256AG.

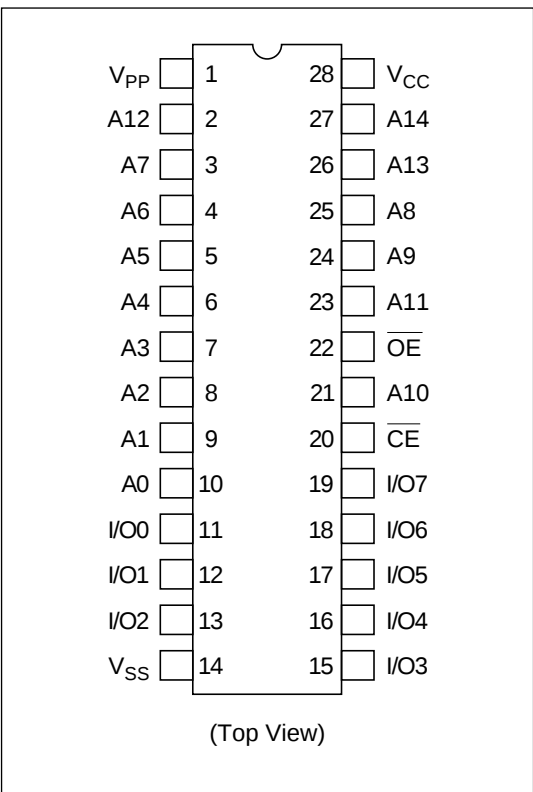
Features

- High speed
Access time: 100/120/150 ns (max)
- Low power dissipation
Active mode: 25 mW (typ) (f = 1 MHz)
Standby mode: 5 μ W (typ)
- High reliability and fast programming
Programming voltage: +12.5 V DC
Fast High-Reliability Programming Algorithm available
- Device identifier mode
Manufacturer code and device code

Ordering Information

Type No.	Access time	Package
HN27C256AG-10	100 ns	600-mil 28-pin cerdip (DG-28)
HN27C256AG-12	120 ns	
HN27C256AG-15	150 ns	

Pin Arrangement

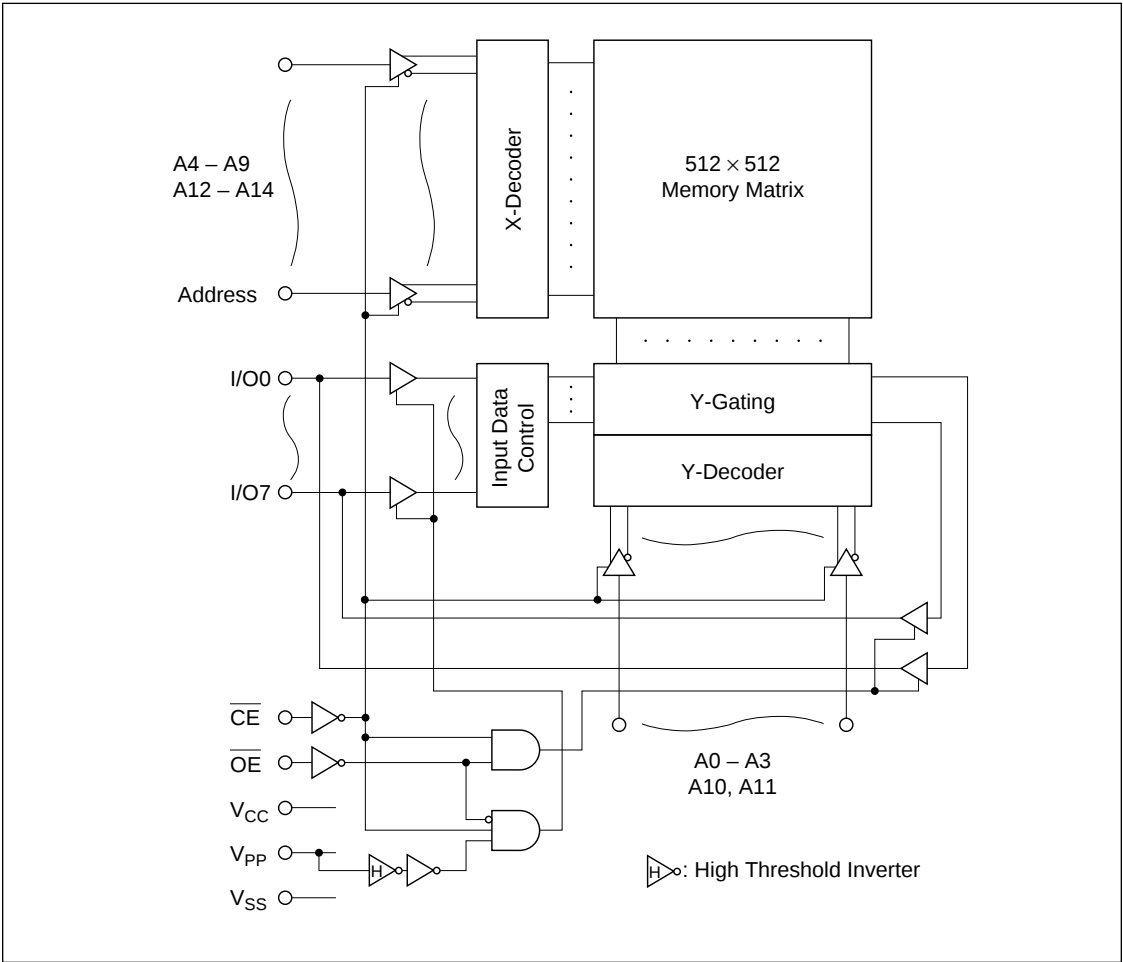


Pin Description

Pin name	Function
A0 – A14	Address
I/O0 – I/O7	Input/output
$\overline{\text{CE}}$	Chip enable
$\overline{\text{OE}}$	Output enable

Pin name	Function
V _{CC}	Power supply
V _{PP}	Programming power supply
V _{SS}	Ground

Block Diagram



Mode Selection

	$\overline{\text{CE}}$	$\overline{\text{OE}}$	A9	V _{PP}	V _{CC}	I/O
Mode	(20)	(22)	(24)	(1)	(28)	(11 – 13, 15 – 19)
Read	V _{IL}	V _{IL}	X	V _{CC}	V _{CC}	Dout
Output disable	V _{IL}	V _{IH}	X	V _{CC}	V _{CC}	High-Z
Standby	V _{IH}	X	X	V _{CC}	V _{CC}	High-Z
Program	V _{IL}	V _{IH}	X	V _{PP}	V _{CC}	Din
Program verify	V _{IH}	V _{IL}	X	V _{PP}	V _{CC}	Dout
Optional verify	V _{IL}	V _{IL}	X	V _{PP}	V _{CC}	Dout
Program inhibit	V _{IH}	V _{IH}	X	V _{PP}	V _{CC}	High-Z
Identifier	V _{IL}	V _{IL}	V _H *2	V _{CC}	V _{CC}	Code

Notes: 1. X : Don't care.

2. V_H : 12.0 V ± 0.5 V.**Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
All input and output voltage*1	V _{in} , V _{out}	–0.6*2 to +7.0	V
A9 input voltage*1	V _{ID}	–0.6*2 to +13.5	V
V _{PP} voltage*1	V _{PP}	–0.6 to +13.5	V
V _{CC} voltage*1	V _{CC}	–0.6 to +7.0	V
Operating temperature range	T _{opr}	0 to +70	°C
Storage temperature range	T _{stg}	–65 to +125	°C
Storage temperature range under bias	T _{bias}	–10 to +80	°C

Notes: 1. Relative to V_{SS}.2. V_{in}, V_{out}, V_{ID} min = –1.0 V for pulse width ≤ 50 ns.

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	C _{in}	—	4	8	pF	V _{in} = 0 V
Output capacitance	C _{out}	—	8	12	pF	V _{out} = 0 V

Read Operation**DC Characteristics** ($T_a = 0\text{ to }+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{PP} = V_{CC}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I _{LI}	—	—	2	μA	V _{in} = 0 V to V _{CC}
Output leakage current	I _{LO}	—	—	2	μA	V _{out} = 0 V to V _{CC}
V _{PP} current	I _{PP1}	—	1	20	μA	V _{PP} = 5.5 V
Standby V _{CC} current	I _{SB1}	—	—	1	mA	$\overline{CE} = V_{IH}$
	I _{SB2}	—	1	20	μA	$\overline{CE} = V_{CC} \pm 0.3\text{ V}$
Operating V _{CC} current	I _{CC1}	—	—	30	mA	$\overline{CE} = V_{IL}$, I _{out} = 0 mA
	I _{CC2}	—	—	30	mA	f = 10 MHz, I _{out} = 0 mA
	I _{CC3}	—	5	15	mA	f = 1 MHz, I _{out} = 0 mA
Input low voltage*3	V _{IL}	-0.3*1	—	0.8	V	
Input high voltage*3	V _{IH}	2.2	—	V _{CC} + 1.0*2	V	
Output low voltage	V _{OL}	—	—	0.45	V	I _{OL} = 2.1 mA
Output high voltage	V _{OH1}	2.4	—	—	V	I _{OH} = -1.0 mA
	V _{OH2}	V _{CC} - 0.7	—	—	V	I _{OH} = -100 μA

Notes: 1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns.

2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns.

If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

3. Only defined for DC function test. V_{IL} max = 0.45 V, V_{IH} min = 2.4 V for AC function test.

AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{PP} = V_{CC}$)

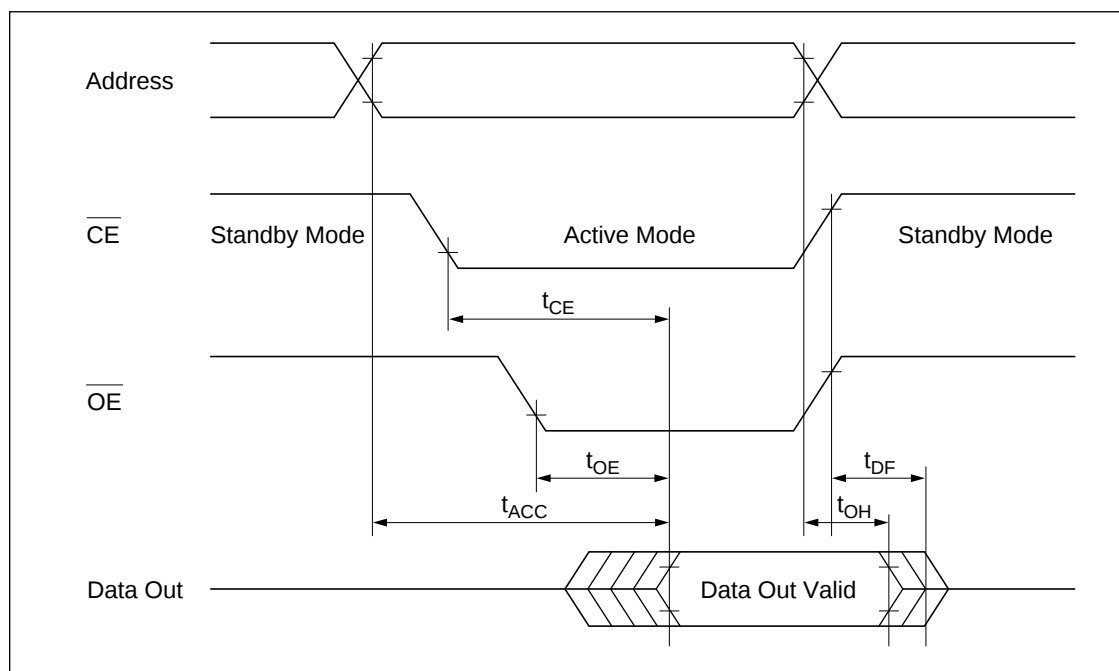
Test Conditions

- Input pulse levels: 0.45 V to 2.4 V
- Input rise and fall times: $\leq 10\text{ ns}$
- Output load: 1TTL gate + 100 pF
- Reference levels for measuring timing: Inputs; 0.8 V and 2.0 V
Outputs; 0.8 V and 2.0 V

Parameter	Symbol	HN27C256AG-10		HN27C256AG-12		HN27C256AG-15		Unit	Test conditions
		Min	Max	Min	Max	Min	Max		
Address to output delay	t_{ACC}	—	100	—	120	—	150	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to output delay	t_{CE}	—	100	—	120	—	150	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to output delay	t_{OE}	—	60	—	60	—	70	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ high to output float	t_{DF}	0	35	0	40	0	50	ns	$\overline{CE} = V_{IL}$
Address to output hold	t_{OH}	5	—	5	—	5	—	ns	$\overline{CE} = \overline{OE} = V_{IL}$

Note: t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

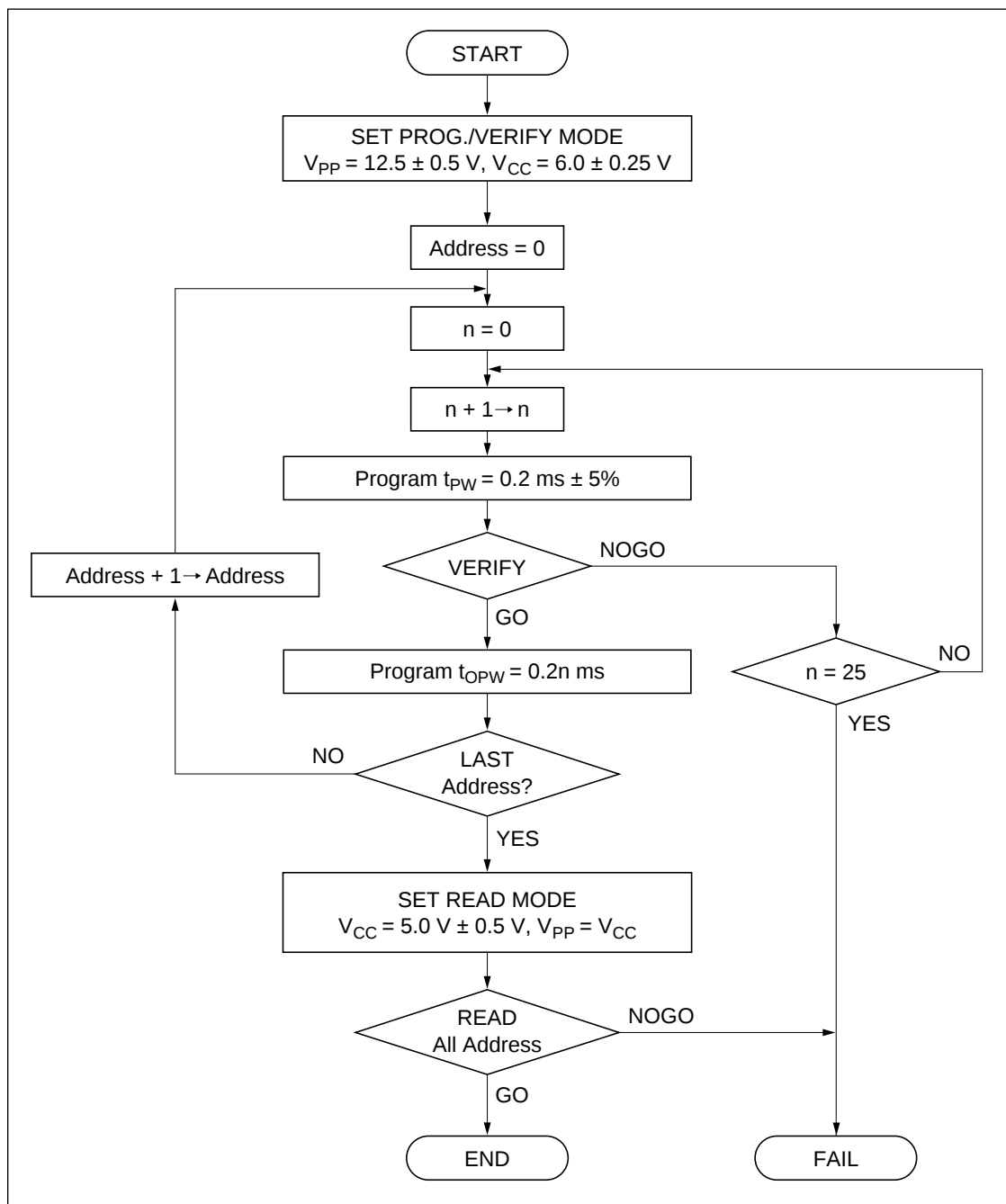
Read Timing Waveform



Fast High-Reliability Programming

This device can be applied the Fast High-Reliability Programming Algorithm shown in following flowchart. This algorithm offers both faster programming time and high reliability data

retention. A theoretical programming time (except blank checking and verifying time) is one-tenth of conventional high performance programming algorithm's. Regarding the model and software version of the programmers available this algorithm, please contact programmer maker.



DC Characteristics ($T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{CC} = 6\text{ V} \pm 0.25\text{ V}$, $V_{PP} = 12.5\text{ V} \pm 0.5\text{ V}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	μA	$V_{in} = 0\text{ V to } V_{CC}$
V_{PP} supply current	I_{PP}	—	—	30	mA	$\overline{CE} = V_{IL}$
Operating V_{CC} current	I_{CC}	—	—	30	mA	
Input low level	V_{IL}	-0.1^{*5}	—	0.8	V	
Input high level	V_{IH}	2.2	—	$V_{CC} + 0.5^{*6}\text{ V}$		
Output low voltage during verify	V_{OL}	—	—	0.45	V	$I_{OL} = 2.1\text{ mA}$
Output high voltage during verify	V_{OH}	2.4	—	—	V	$I_{OH} = -400\text{ }\mu\text{A}$

- Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} .
2. V_{PP} must not exceed 13.5 V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while $V_{PP} = 12.5\text{ V}$.
4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE} = \text{Low}$.
5. V_{IL} min = -0.6 V for pulse width $\leq 20\text{ ns}$.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics ($T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{CC} = 6\text{ V} \pm 0.25\text{ V}$, $V_{PP} = 12.5\text{ V} \pm 0.5\text{ V}$)

Test Conditions

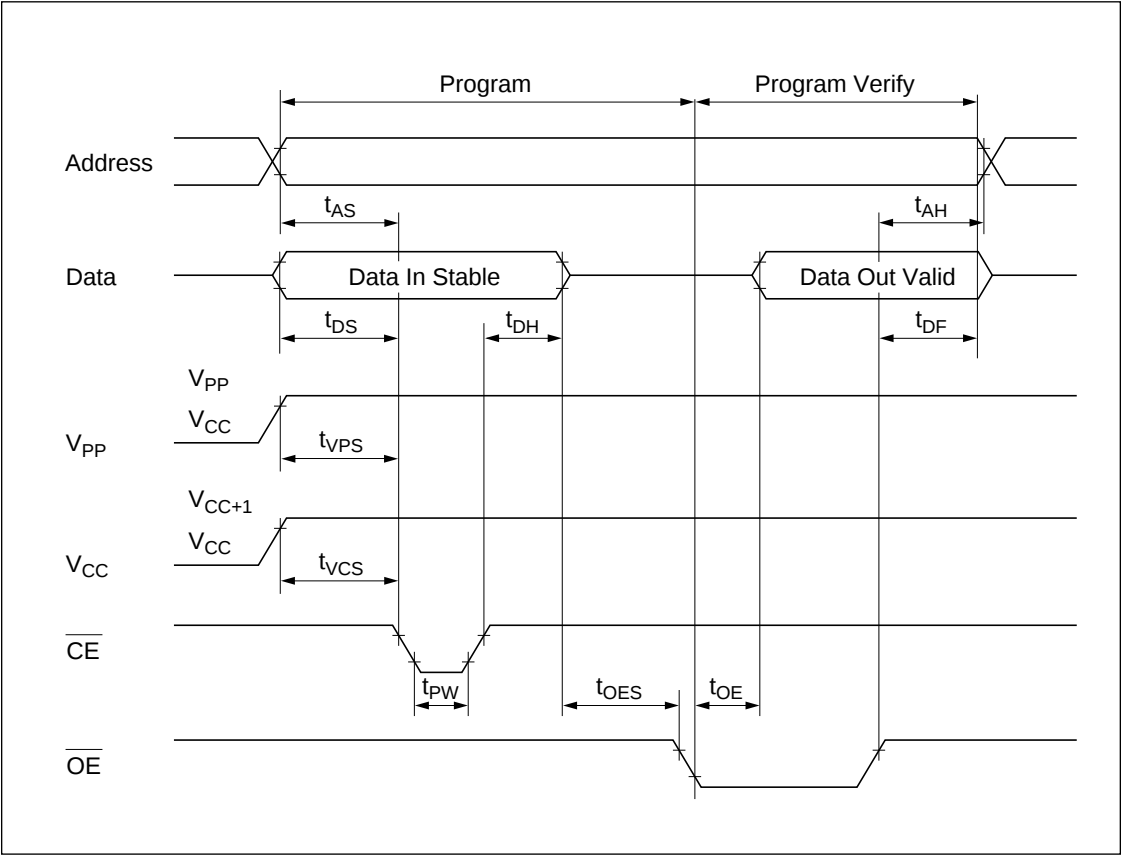
- Input pulse levels: 0.45 V to 2.4 V
- Input rise and fall times: $\leq 20\text{ ns}$
- Reference levels for measuring timing: Inputs; 0.8 V and 2.0 V
Outputs; 0.8 V and 2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	2	—	—	μs	
$\overline{\text{OE}}$ setup time	t_{OES}	2	—	—	μs	
Data setup time	t_{DS}	2	—	—	μs	
Address hold time	t_{AH}	0	—	—	μs	
Data hold time	t_{DH}	2	—	—	μs	
V_{PP} setup time	t_{VPS}	2	—	—	μs	
V_{CC} setup time	t_{VCS}	2	—	—	μs	
$\overline{\text{CE}}$ initial programming pulse width	t_{PW}	0.19	0.20	0.21	ms	
$\overline{\text{CE}}$ over programming pulse width	t_{OPW}^{*1}	0.19	—	5.25	ms	
Data valid from $\overline{\text{OE}}$	t_{OE}	0	—	150	ns	
$\overline{\text{OE}}$ to output float delay	t_{DF}^{*2}	—	—	130	ns	

Notes: 1. Refer to the Fast High-Reliability Programming Flowchart for t_{OPW} .

2. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

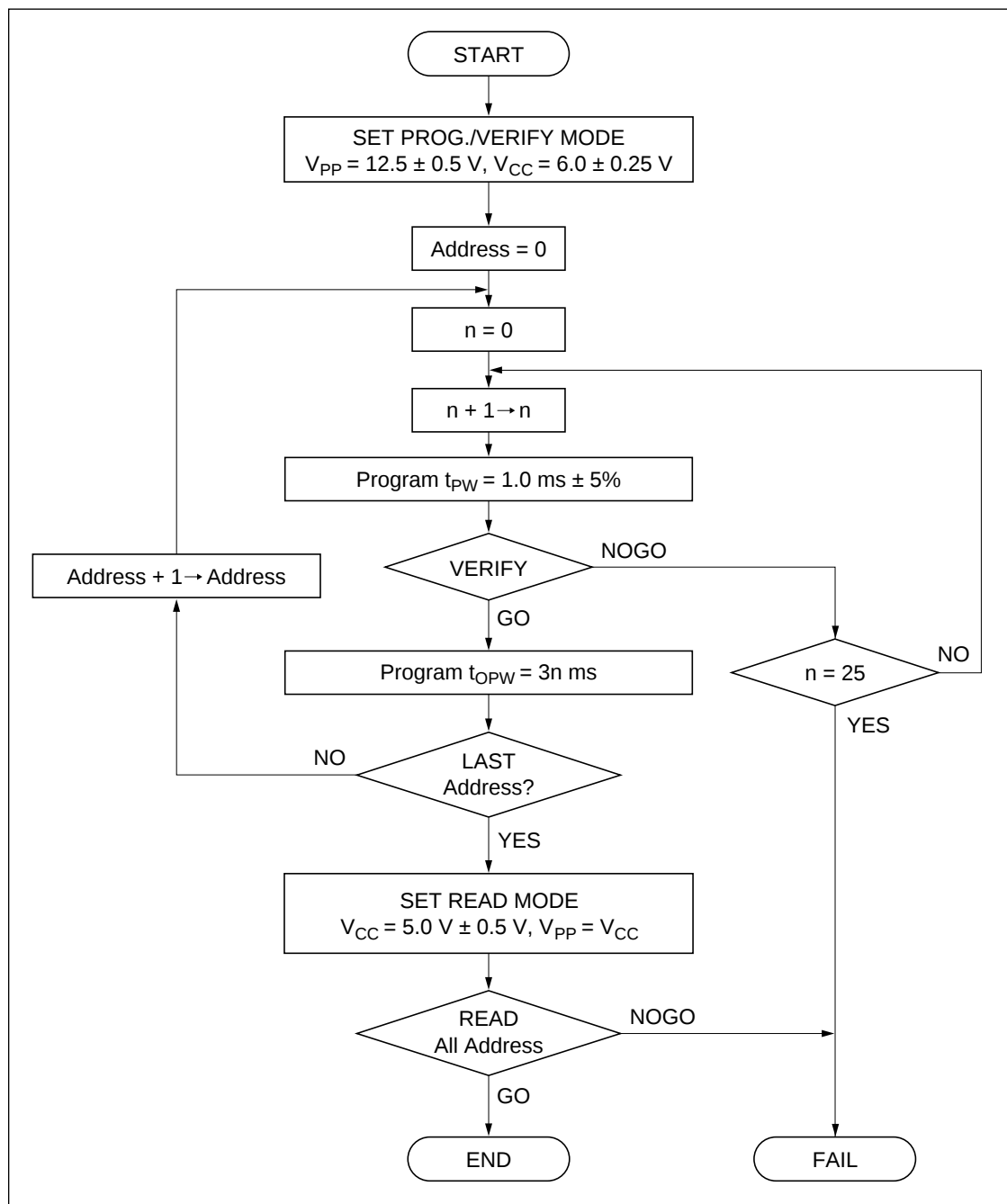
Fast High-Reliability Programming Timing Waveform



High Performance Programming

This device can be applied the high performance programming algorithm shown in following flowchart. This algorithm is as same as our 256-

kbit EPROM series so existing programmers can be used with this device. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



DC Characteristics ($T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{CC} = 6\text{ V} \pm 0.25\text{ V}$, $V_{PP} = 12.5\text{ V} \pm 0.5\text{ V}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	μA	$V_{in} = 0\text{ V to } V_{CC}$
V_{PP} supply current	I_{PP}	—	—	30	mA	$\overline{CE} = V_{IL}$
Operating V_{CC} current	I_{CC}	—	—	30	mA	
Input low level	V_{IL}	-0.1^{*5}	—	0.8	V	
Input high level	V_{IH}	2.2	—	$V_{CC} + 0.5^{*6}\text{ V}$		
Output low voltage during verify	V_{OL}	—	—	0.45	V	$I_{OL} = 2.1\text{ mA}$
Output high voltage during verify	V_{OH}	2.4	—	—	V	$I_{OH} = -400\text{ }\mu\text{A}$

- Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} .
 2. V_{PP} must not exceed 13.5 V including overshoot.
 3. An influence may be had upon device reliability if the device is installed or removed while $V_{PP} = 12.5\text{ V}$.
 4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE} = \text{Low}$.
 5. V_{IL} min = -0.6 V for pulse width $\leq 20\text{ ns}$.
 6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics ($T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{CC} = 6\text{ V} \pm 0.25\text{ V}$, $V_{PP} = 12.5\text{ V} \pm 0.5\text{ V}$)

Test Conditions

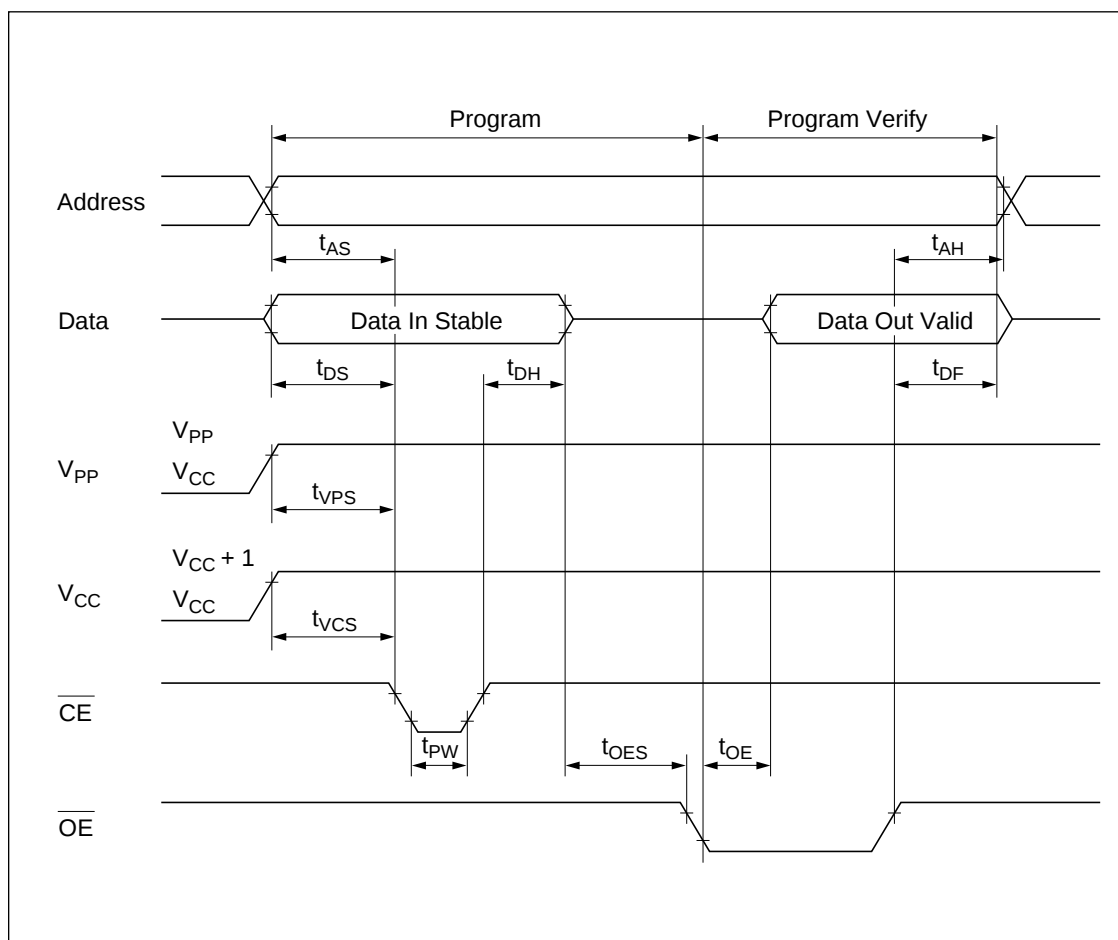
- Input pulse levels: 0.45 V to 2.4 V
- Input rise and fall times: $\leq 20\text{ ns}$
- Reference levels for measuring timing: Inputs; 0.8 V and 2.0 V
Outputs; 0.8 V and 2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	2	—	—	μs	
$\overline{\text{OE}}$ setup time	t_{OES}	2	—	—	μs	
Data setup time	t_{DS}	2	—	—	μs	
Address hold time	t_{AH}	0	—	—	μs	
Data hold time	t_{DH}	2	—	—	μs	
V_{PP} setup time	t_{VPS}	2	—	—	μs	
V_{CC} setup time	t_{VCS}	2	—	—	μs	
$\overline{\text{CE}}$ initial programming pulse width	t_{PW}	0.95	1.0	1.05	ms	
$\overline{\text{CE}}$ over programming pulse width	t_{OPW}^{*1}	2.85	—	78.75	ms	
Data valid from $\overline{\text{OE}}$	t_{OE}	0	—	150	ns	
$\overline{\text{OE}}$ to output float delay	t_{DF}^{*2}	—	—	130	ns	

Notes: 1. Refer to the high performance programming flowchart for t_{OPW} .

2. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

High Performance Programming Timing Waveform



Erase

Erasure of HN27C256AG is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to “1” after this erasure procedure. The minimum integrated dose (i.e. UV intensity × exposure time) for erasure is 15 W•sec/cm².

Mode Description**Device Identifier Mode**

Programming condition of EPROM is various according to EPROM manufacturers and device types. It may cause miss operation. To countermeasure it, some EPROMs provide maker identifier code. Users can write EPROM by reading out write condition coded before shipped. Some commercial programmers can set write condition by recognizing this code. This function enables effective program. Regarding commercial programmers that can recognize this device's identifier code, please contact programmer maker.

HN27C256AG Series Identifier Code

	A0	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Hex
Identifier	(10)	(19)	(18)	(17)	(16)	(15)	(13)	(12)	(11)	data
Manufacturer code	V _{IL}	0	0	0	0	0	1	1	1	07
Device code	V _{IH}	0	0	1	1	0	0	0	1	31

Notes: 1. A9 = 12.0 V ± 0.5 V.

2. A1 – A8, A10 – A14, $\overline{\text{CE}}$, $\overline{\text{OE}}$ = V_{IL}.