



CYPRESS

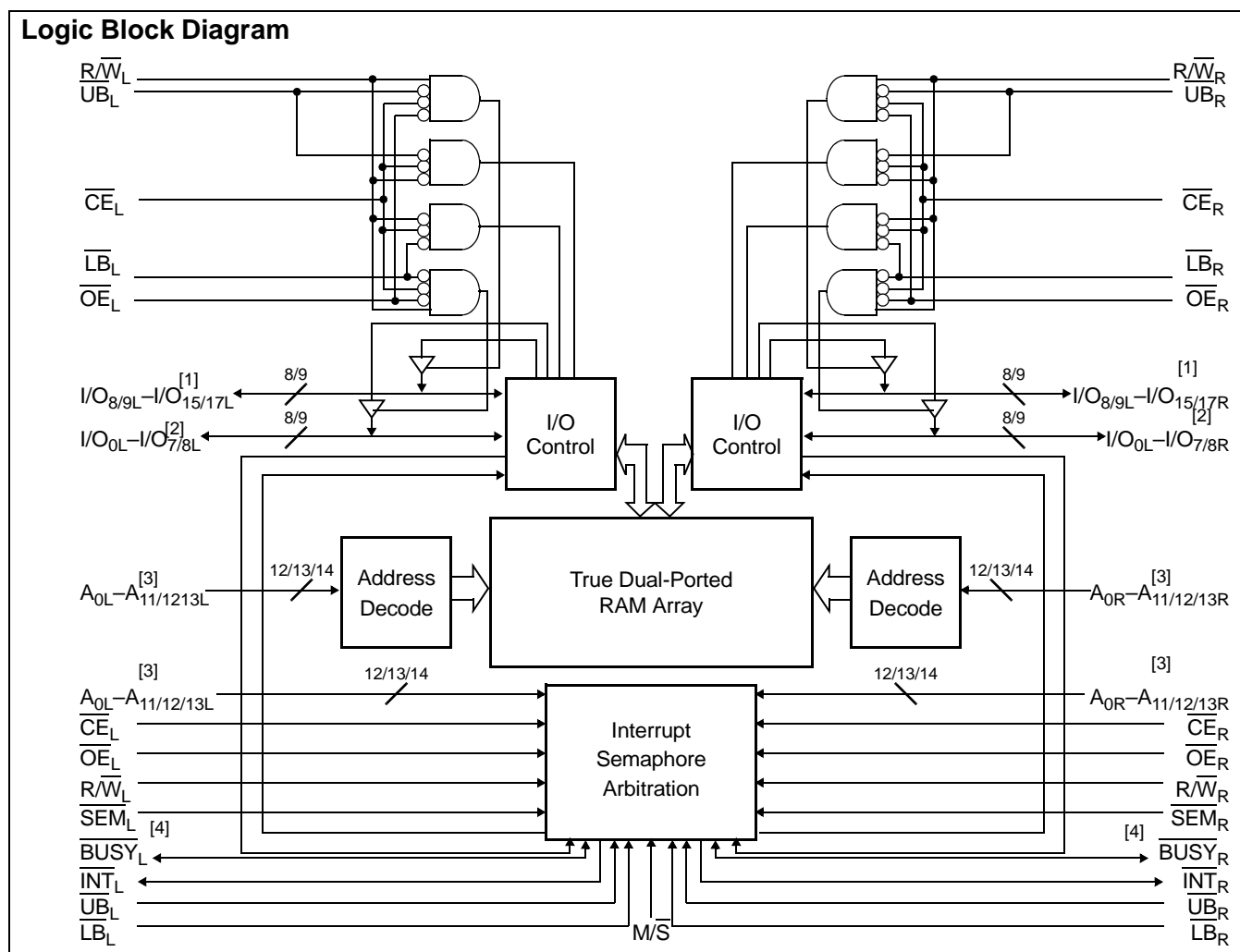
CY7C024AV/025AV/026AV  
CY7C0241AV/0251AV/036AV

3.3V 4K/8K/16K x 16/18 Dual-Port Static RAM

## Features

- True dual-ported memory cells which allow simultaneous access of the same memory location
- 4/8/16K x 16 organization (CY7C024AV/025AV/026AV)
- 4/8K x 18 organization (CY7C0241AV/0251AV)
- 16K x 18 organization (CY7C036AV)
- 0.35-micron CMOS for optimum speed/power
- High-speed access: 20 and 25 ns
- Low operating power
  - Active:  $I_{CC} = 115 \text{ mA}$  (typical)
  - Standby:  $I_{SB3} = 10 \mu\text{A}$  (typical)
- Fully asynchronous operation
- Automatic power-down
- Expandable data bus to 32/36 bits or more using Master/Slave chip select when using more than one device
- On-chip arbitration logic
- Semaphores included to permit software handshaking between ports
- INT flag for port-to-port communication
- Separate upper-byte and lower-byte control
- Pin select for Master or Slave
- Commercial and industrial temperature ranges
- Available in 100-pin TQFP

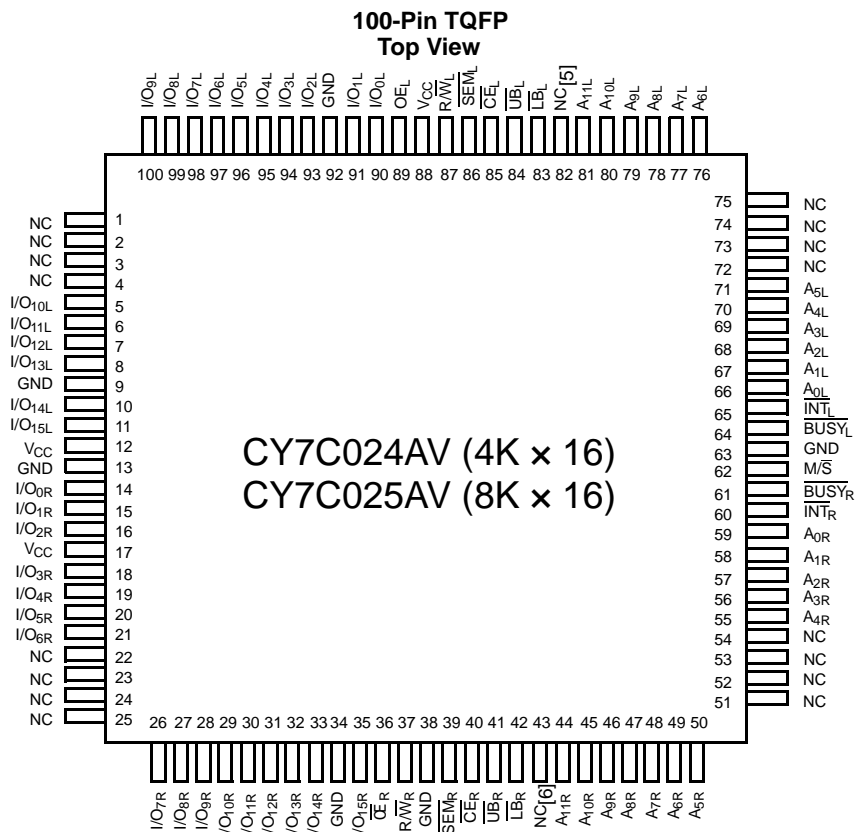
## Logic Block Diagram



### Notes:

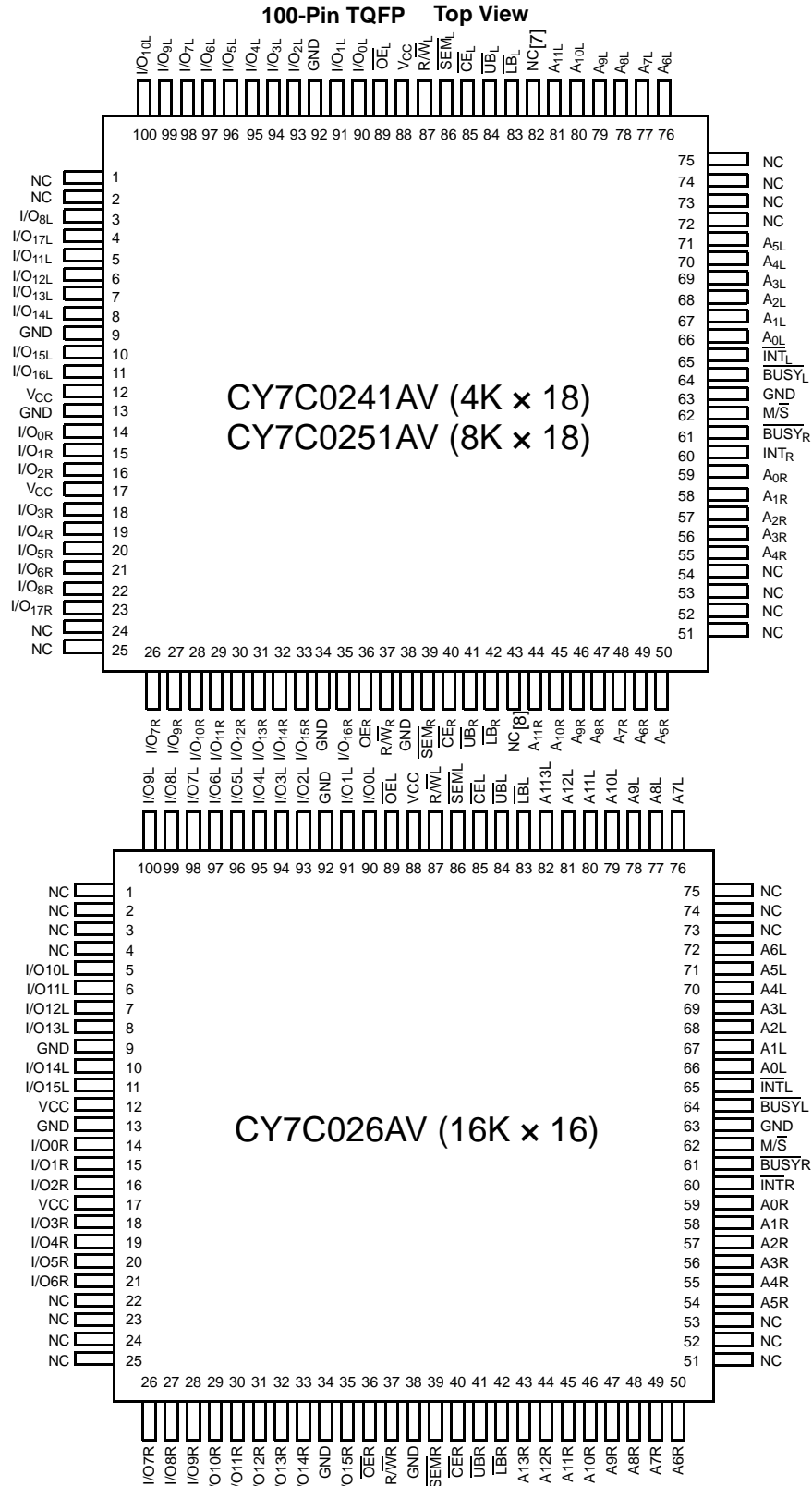
1. I/O<sub>8</sub>-I/O<sub>15</sub> for x16 devices; I/O<sub>9</sub>-I/O<sub>17</sub> for x18 devices.
2. I/O<sub>0</sub>-I/O<sub>7</sub> for x16 devices; I/O<sub>0</sub>-I/O<sub>8</sub> for x18 devices.
3. A<sub>0</sub>-A<sub>11</sub> for 4K devices; A<sub>0</sub>-A<sub>12</sub> for 8K devices; A<sub>0</sub>-A<sub>13</sub> for 16K devices.
4. BUSY is an output in master mode and an input in slave mode.

## Pin Configurations

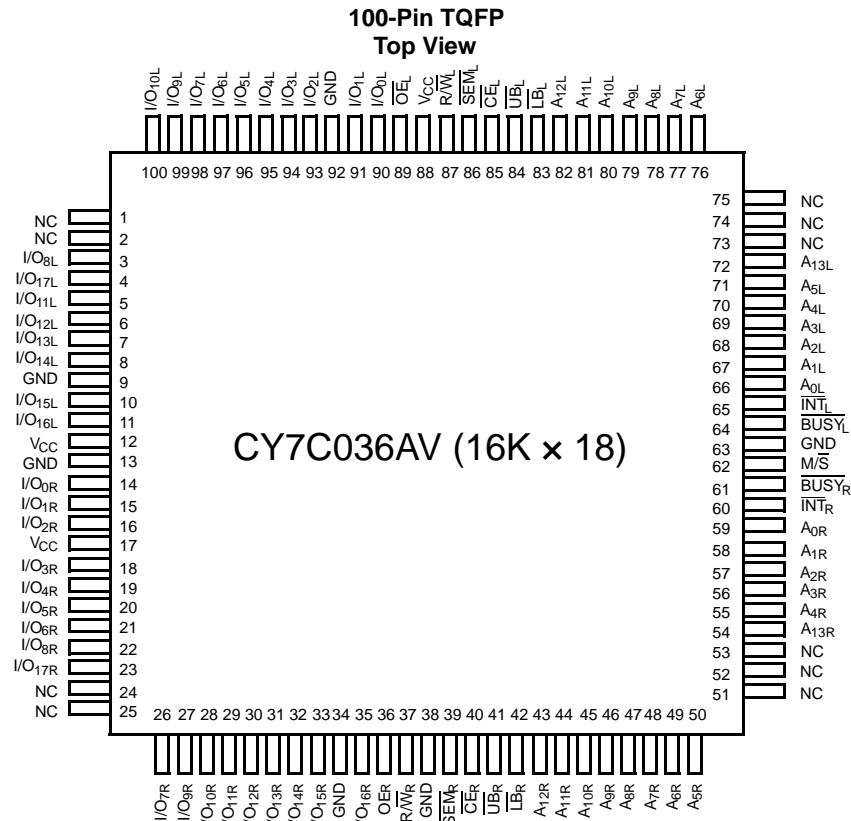


### Notes:

5. A<sub>12L</sub> on the CY7C025AV.
6. A<sub>12R</sub> on the CY7C025AV.

**Pin Configurations (continued)**

**Notes:**

7. A<sub>12L</sub> on the CY7C0251AV.
8. A<sub>12R</sub> on the CY7C0251AVC.

**Pin Configurations (continued)**

**Selection Guide**

	<b>CY7C024AV/025AV/026AV</b> <b>CY7C0241AV/0251AV/036AV</b> <b>-20</b>	<b>CY7C024AV/025AV/026AV</b> <b>CY7C0241AV/0251AV/036AV</b> <b>-25</b>	<b>Unit</b>
Maximum Access Time	20	25	ns
Typical Operating Current	120	115	mA
Typical Standby Current for I <sub>SB1</sub> (Both ports TTL Level)	35	30	mA
Typical Standby Current for I <sub>SB3</sub> (Both ports CMOS Level)	10	10	μA

## Pin Definitions

Left Port	Right Port	Description
CE <sub>L</sub>	CE <sub>R</sub>	Chip Enable.
R/W <sub>L</sub>	R/W <sub>R</sub>	Read/Write Enable.
OE <sub>L</sub>	OE <sub>R</sub>	Output Enable.
A <sub>0L</sub> –A <sub>13L</sub>	A <sub>0R</sub> –A <sub>13R</sub>	Address (A <sub>0</sub> –A <sub>11</sub> for 4K devices; A <sub>0</sub> –A <sub>12</sub> for 8K devices; A <sub>0</sub> –A <sub>13</sub> for 16K).
I/O <sub>0L</sub> –I/O <sub>17L</sub>	I/O <sub>0R</sub> –I/O <sub>17R</sub>	Data Bus Input/Output.
SEM <sub>L</sub>	SEM <sub>R</sub>	Semaphore Enable.
UB <sub>L</sub>	UB <sub>R</sub>	Upper Byte Select (I/O <sub>8</sub> –I/O <sub>15</sub> for x16 devices; I/O <sub>9</sub> –I/O <sub>17</sub> for x18 devices).
LB <sub>L</sub>	LB <sub>R</sub>	Lower Byte Select (I/O <sub>0</sub> –I/O <sub>7</sub> for x16 devices; I/O <sub>0</sub> –I/O <sub>8</sub> for x18 devices).
INT <sub>L</sub>	INT <sub>R</sub>	Interrupt Flag.
BUSY <sub>L</sub>	BUSY <sub>R</sub>	Busy Flag.
M/S		Master or Slave Select.
V <sub>CC</sub>		Power.
GND		Ground.
NC		No Connect.

## Architecture

The CY7C024AV/025AV/026AV and CY7C0241AV/0251AV/036AV consist of an array of 4K, 8K, and 16K words of 16 and 18 bits each of dual-port RAM cells, I/O and address lines, and control signals (CE, OE, R/W). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a BUSY pin is provided on each port. Two Interrupt (INT) pins can be utilized for port-to-port communication. Two Semaphore (SEM) control pins are used for allocating shared resources. With the M/S pin, the devices can function as a master (BUSY pins are outputs) or as a slave (BUSY pins are inputs). The devices also have an automatic power-down feature controlled by CE. Each port is provided with its own output enable control (OE), which allows data to be read from the device.

## Functional Description

The CY7C024AV/025AV/026AV and CY7C0241AV/0251AV/036AV are low-power CMOS 4K, 8K, and 16K x16/18 dual-port static RAMs. Various arbitration schemes are included on the devices to handle situations when multiple processors access the same piece of data. Two ports are provided, permitting independent, asynchronous access for reads and writes to any location in memory. The devices can be utilized as standalone 16/18-bit dual-port static RAMs or multiple devices can be combined in order to function as a 32/36-bit or wider master/slave dual-port static RAM. An M/S pin is provided for implementing 32/36-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: Chip Enable ( $\overline{CE}$ ), Read or Write Enable (R/W), and Output Enable (OE). Two

flags are provided on each port ( $\overline{BUSY}$  and  $\overline{INT}$ ).  $\overline{BUSY}$  signals that the port is trying to access the same location currently being accessed by the other port. The Interrupt flag ( $\overline{INT}$ ) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a Chip Select (CE) pin.

The CY7C024AV/025AV/026AV and CY7C0241AV/0251AV/036AV are available in 100-pin Thin Quad Plastic Flatpacks (TQFP).

### Write Operation

Data must be set up for a duration of  $t_{SD}$  before the rising edge of R/W in order to guarantee a valid write. A write operation is controlled by either the R/W pin (see Write Cycle No. 1 waveform) or the CE pin (see Write Cycle No. 2 waveform). Required inputs for non-contention operations are summarized in Table 1.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must occur before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port  $t_{DD}$  after the data is presented on the other port.

### Read Operation

When reading the device, the user must assert both the  $\overline{OE}$  and  $\overline{CE}$  pins. Data will be available  $t_{ACE}$  after  $\overline{CE}$  or  $t_{DOE}$  after OE is asserted. If the user wishes to access a semaphore flag, then the SEM pin must be asserted instead of the CE pin, and  $\overline{OE}$  must also be asserted.

## Interrupts

The upper two memory locations may be used for message passing. The highest memory location (FFF for the CY7C024AV/41AV, 1FFF for the CY7C025AV/51AV, 3FFF for the CY7C026AV/36AV) is the mailbox for the right port and the second-highest memory location (FFE for the CY7C024AV/41AV, 1FFE for the CY7C025AV/51AV, 3FFE for the CY7C026AV/36AV) is the mailbox for the left port. When one port writes to the other port's mailbox, an interrupt is generated to the owner. The interrupt is reset when the owner reads the contents of the mailbox. The message is user defined.

Each port can read the other port's mailbox without resetting the interrupt. The active state of the busy signal (to a port) prevents the port from setting the interrupt to the winning port. Also, an active busy to a port prevents that port from reading its own mailbox and, thus, resetting the interrupt to it.

If an application does not require message passing, do not connect the interrupt pin to the processor's interrupt request input pin.

The operation of the interrupts and their interaction with Busy are summarized in *Table 2*.

## Busy

The CY7C024AV/025AV/026AV and CY7C0241AV/0251AV/036AV provide on-chip arbitration to resolve simultaneous memory location access (contention). If both ports' CEs are asserted and an address match occurs within  $t_{PS}$  of each other, the busy logic will determine which port has access. If  $t_{PS}$  is violated, one port will definitely gain permission to the location, but it is not predictable which port will get that permission. BUSY will be asserted  $t_{BLA}$  after an address match or  $t_{BLC}$  after CE is taken LOW.

## Master/Slave

A  $\overline{M/\overline{S}}$  pin is provided in order to expand the word width by configuring the device as either a master or a slave. The BUSY output of the master is connected to the BUSY input of the slave. This will allow the device to interface to a master device with no external components. Writing to slave devices must be delayed until after the BUSY input has settled ( $t_{BLC}$  or  $t_{BLA}$ ), otherwise, the slave chip may begin a write cycle during a contention situation. When tied HIGH, the  $\overline{M/\overline{S}}$  pin allows the device to be used as a master and, therefore, the BUSY line is an output. BUSY can then be used to send the arbitration outcome to a slave.

## Semaphore Operation



The CY7C024AV/025AV/026AV and CY7C0241AV/0251AV/036AV provide eight semaphore latches, which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, SEM or OE must be deasserted for  $t_{SOP}$  before attempting to read the semaphore. The semaphore value will be available  $t_{SWRD} + t_{DOE}$  after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control of the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting  $\overline{SEM}$  LOW. The  $\overline{SEM}$  pin functions as a chip select for the semaphore latches (CE must remain HIGH during  $\overline{SEM}$  LOW).  $A_{0-2}$  represents the semaphore address. OE and R/W are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O<sub>0</sub> is used. If a zero is written to the left port of an available semaphore, a one will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore will be set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. *Table 3* shows sample semaphore operations.

When reading a semaphore, all sixteen/eighteen data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within  $t_{SPS}$  of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

**Table 1. Non-Contending Read/Write**

Inputs						Outputs		Operation
CE	R/W	OE	UB	LB	SEM	I/O <sub>9</sub> –I/O <sub>17</sub>	I/O <sub>0</sub> –I/O <sub>8</sub>	
H	X	X	X	X	H	High Z	High Z	Deselected: Power-Down
X	X	X	H	H	H	High Z	High Z	Deselected: Power-Down
L	L	X	L	H	H	Data In	High Z	Write to Upper Byte Only
L	L	X	H	L	H	High Z	Data In	Write to Lower Byte Only
L	L	X	L	L	H	Data In	Data In	Write to Both Bytes
L	H	L	L	H	H	Data Out	High Z	Read Upper Byte Only
L	H	L	H	L	H	High Z	Data Out	Read Lower Byte Only
L	H	L	L	L	H	Data Out	Data Out	Read Both Bytes
X	X	H	X	X	X	High Z	High Z	Outputs Disabled
H	H	L	X	X	L	Data Out	Data Out	Read Data in Semaphore Flag
X	H	L	H	H	L	Data Out	Data Out	Read Data in Semaphore Flag
H		X	X	X	L	Data In	Data In	Write D <sub>IN0</sub> into Semaphore Flag
X		X	H	H	L	Data In	Data In	Write D <sub>IN0</sub> into Semaphore Flag
L	X	X	L	X	L			Not Allowed
L	X	X	X	L	L			Not Allowed

**Table 2. Interrupt Operation Example (assumes  $\overline{\text{BUSY}}_L = \overline{\text{BUSY}}_R = \text{HIGH}$ )<sup>[9]</sup>**

Function	Left Port					Right Port				
	R/W <sub>L</sub>	CE <sub>L</sub>	OE <sub>L</sub>	A <sub>0L–13L</sub>	INT <sub>L</sub>	R/W <sub>R</sub>	CE <sub>R</sub>	OE <sub>R</sub>	A <sub>0R–13R</sub>	INT <sub>R</sub>
Set Right $\overline{\text{INT}}_R$ Flag	L	L	X	FFF <sup>[12]</sup>	X	X	X	X	X	L <sup>[11]</sup>
Reset Right $\overline{\text{INT}}_R$ Flag	X	X	X	X	X	X	L	L	FFF (or 1/3FFF)	H <sup>[10]</sup>
Set Left $\overline{\text{INT}}_L$ Flag	X	X	X	X	L <sup>[10]</sup>	L	L	X	1FFE (or 1/3FFE)	X
Reset Left $\overline{\text{INT}}_L$ Flag	X	L	L	1FFE <sup>[12]</sup>	H <sup>[11]</sup>	X	X	X	X	X

**Table 3. Semaphore Operation Example**

Function	I/O <sub>0</sub> –I/O <sub>17</sub> Left	I/O <sub>0</sub> –I/O <sub>17</sub> Right	Status
No action	1	1	Semaphore-free
Left port writes 0 to semaphore	0	1	Left Port has semaphore token
Right port writes 0 to semaphore	0	1	No change. Right side has no write access to semaphore
Left port writes 1 to semaphore	1	0	Right port obtains semaphore token
Left port writes 0 to semaphore	1	0	No change. Left port has no write access to semaphore
Right port writes 1 to semaphore	0	1	Left port obtains semaphore token
Left port writes 1 to semaphore	1	1	Semaphore-free
Right port writes 0 to semaphore	1	0	Right port has semaphore token
Right port writes 1 to semaphore	1	1	Semaphore free
Left port writes 0 to semaphore	0	1	Left port has semaphore token
Left port writes 1 to semaphore	1	1	Semaphore-free

**Notes:**

9. See Functional Description for specific highest memory locations by device.
10. If  $\overline{\text{BUSY}}_R = \text{L}$ , then no change.
11. If  $\overline{\text{BUSY}}_L = \text{L}$ , then no change.
12. See Functional Description for specific addresses by device.



## Maximum Ratings <sup>[13]</sup>

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with  
 Power Applied..... -55°C to +125°C  
 Supply Voltage to Ground Potential ..... -0.5V to +4.6V  
 DC Voltage Applied to  
 Outputs in High-Z State..... -0.5V to  $V_{CC} + 0.5V$

DC Input Voltage<sup>[14]</sup>..... -0.5V to  $V_{CC} + 0.5V$   
 Output Current into Outputs (LOW)..... 20 mA  
 Static Discharge Voltage..... > 2001V  
 Latch-up Current..... > 200 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$
Commercial	0°C to +70°C	3.3V ± 300 mV
Industrial <sup>[15]</sup>	-40°C to +85°C	3.3V ± 300 mV

## Electrical Characteristics Over the Operating Range

Parameter	Description	CY7C024AV/025AV/026AV CY7C0241AV/0251AV/036AV						Unit	
		-20			-25				
		Min.	Typ.	Max.	Min.	Typ.	Max.		
V <sub>OH</sub>	Output HIGH Voltage (V <sub>CC</sub> =3.3V)	2.4			2.4			V	
V <sub>OL</sub>	Output LOW Voltage			0.4			0.4	V	
V <sub>IH</sub>	Input HIGH Voltage	2.0			2.0			V	
V <sub>IL</sub>	Input LOW Voltage			0.8			0.8	V	
I <sub>OZ</sub>	Output Leakage Current	−10		10	−10		10	μA	
I <sub>IX</sub>	Input Leakage Current	−10		10	−10		10	μA	
I <sub>CC</sub>	Operating Current (V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA) Outputs Disabled	Com'l.		120	175		115	165	mA
		Ind. <sup>[15]</sup>					135	185	mA
I <sub>SB1</sub>	Standby Current (Both Ports TTL Level) CE <sub>L</sub> & CE <sub>R</sub> ≥ V <sub>IH</sub> , f = f <sub>MAX</sub>	Com'l.		35	45		30	40	mA
		Ind. <sup>[15]</sup>					40	50	mA
I <sub>SB2</sub>	Standby Current (One Port TTL Level) CE <sub>L</sub>   CE <sub>R</sub> ≥ V <sub>IH</sub> , f = f <sub>MAX</sub>	Com'l.		75	110		65	95	mA
		Ind. <sup>[15]</sup>					75	105	mA
I <sub>SB3</sub>	Standby Current (Both Ports CMOS Level) CE <sub>L</sub> & CE <sub>R</sub> ≥ V <sub>CC</sub> −0.2V, f = 0	Com'l.		10	500		10	500	μA
		Ind. <sup>[15]</sup>					10	500	μA
I <sub>SB4</sub>	Standby Current (One Port CMOS Level) CE <sub>L</sub>   CE <sub>R</sub> ≥ V <sub>IH</sub> , f = f <sub>MAX</sub> <sup>[16]</sup>	Com'l.		70	95		60	80	mA
		Ind. <sup>[15]</sup>					70	90	mA

## Capacitance<sup>[17]</sup>

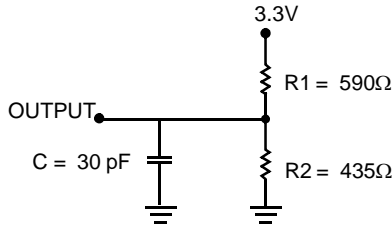
Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1 \text{ MHz}$ , $V_{CC} = 3.3V$	10	pF
$C_{OUT}$	Output Capacitance		10	pF

### Notes:

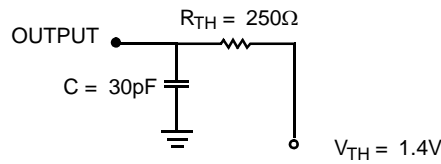
13. The Voltage on any input or I/O pin can not exceed the power pin during power-up.
14. Pulse width < 20 ns.
15. Industrial parts are available in CY7C026AV and CY7C036AV only.
16.  $f_{MAX} = 1/t_{RC}$  = All inputs cycling at  $f = 1/t_{RC}$  (except output enable).  $f = 0$  means no address or control lines change. This applies only to inputs at CMOS level standby  $I_{SB3}$ .
17. Tested initially and after any design or process changes that may affect these parameters.



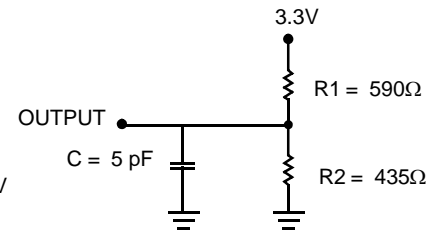
## AC Test Loads and Waveforms



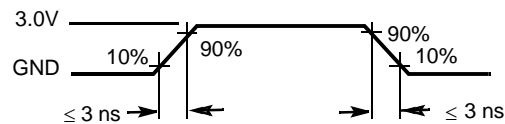
(a) Normal Load (Load 1)



(b) Thévenin Equivalent (Load 1)  
ALL INPUT PULSES



(c) Three-State Delay (Load 2)  
(Used for  $t_{LZ}$ ,  $t_{HZ}$ ,  $t_{HZWE}$ , and  $t_{LZWE}$  including scope and jig)



## Switching Characteristics Over the Operating Range <sup>[18]</sup>

Parameter	Description	CY7C024AV/025AV/026AV CY7C0241AV/0251AV/036AV				Unit
		-20		-25		
		Min.	Max.	Min.	Max.	
Read Cycle						
t <sub>RC</sub>	Read Cycle Time	20		25		ns
t <sub>AA</sub>	Address to Data Valid		20		25	ns
t <sub>OHA</sub>	Output Hold From Address Change	3		3		ns
t <sub>ACE</sub> <sup>[19]</sup>	CE LOW to Data Valid		20		25	ns
t <sub>DOE</sub>	OE LOW to Data Valid		12		13	ns
t <sub>LZOE</sub> <sup>[20, 21, 22]</sup>	OE Low to Low Z	3		3		ns
t <sub>HZOE</sub> <sup>[20, 21, 22]</sup>	OE HIGH to High Z		12		15	ns
t <sub>LZCE</sub> <sup>[20, 21, 22]</sup>	CE LOW to Low Z	3		3		ns
t <sub>HZCE</sub> <sup>[20, 21, 22]</sup>	CE HIGH to High Z		12		15	ns
t <sub>PU</sub> <sup>[22]</sup>	CE LOW to Power-Up	0		0		ns
t <sub>PD</sub> <sup>[22]</sup>	CE HIGH to Power-Down		20		25	ns
t <sub>ABE</sub> <sup>[19]</sup>	Byte Enable Access Time		20		25	ns
Write Cycle						
t <sub>WC</sub>	Write Cycle Time	20		25		ns
t <sub>SCE</sub> <sup>[19]</sup>	CE LOW to Write End	15		20		ns
t <sub>AW</sub>	Address Valid to Write End	15		20		ns
t <sub>HA</sub>	Address Hold From Write End	0		0		ns
t <sub>SA</sub> <sup>[19]</sup>	Address Set-up to Write Start	0		0		ns
t <sub>PWE</sub>	Write Pulse Width	15		20		ns
t <sub>SD</sub>	Data Set-up to Write End	15		15		ns

### Notes:

18. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OH}/I_{OH}$  and 30-pF load capacitance.
19. To access RAM,  $\overline{CE}=L$ ,  $\overline{UB}=L$ ,  $\overline{SEM}=H$ . To access semaphore,  $\overline{CE}=H$  and  $\overline{SEM}=L$ . Either condition must be valid for the entire  $t_{SCE}$  time.
20. At any given temperature and voltage condition for any given device,  $t_{HZCE}$  is less than  $t_{LZCE}$  and  $t_{HZOE}$  is less than  $t_{LZOE}$ .
21. Test conditions used are Load 3.
22. This parameter is guaranteed but not tested. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Busy waveform.

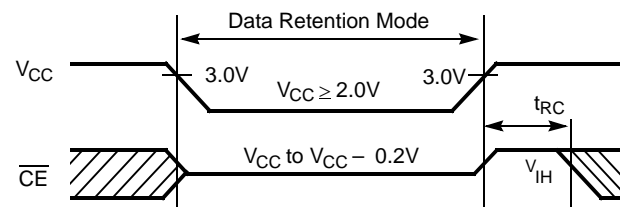
**Switching Characteristics** Over the Operating Range (continued)<sup>[18]</sup>

Parameter	Description	CY7C024AV/025AV/026AV CY7C0241AV/0251AV/036AV				Unit
		-20		-25		
		Min.	Max.	Min.	Max.	
t <sub>HD</sub>	Data Hold From Write End	0		0		ns
t <sub>HZWE</sub> <sup>[21, 22]</sup>	R/W LOW to High Z		12		15	ns
t <sub>LZWE</sub> <sup>[21, 22]</sup>	R/W HIGH to Low Z	3		0		ns
t <sub>WDD</sub> <sup>[23]</sup>	Write Pulse to Data Delay		45		50	ns
t <sub>DDD</sub> <sup>[23]</sup>	Write Data Valid to Read Data Valid		30		35	ns
Busy Timing <sup>[24]</sup>						
t <sub>BLA</sub>	BUS $\overline{Y}$ LOW from Address Match		20		20	ns
t <sub>BHA</sub>	BUS $\overline{Y}$ HIGH from Address Mismatch		20		20	ns
t <sub>BLC</sub>	BUS $\overline{Y}$ LOW from $\overline{CE}$ LOW		20		20	ns
t <sub>BHC</sub>	BUS $\overline{Y}$ HIGH from $\overline{CE}$ HIGH		17		17	ns
t <sub>PS</sub>	Port Set-up for Priority	5		5		ns
t <sub>WB</sub>	R/W HIGH after BUS $\overline{Y}$ (Slave)	0		0		ns
t <sub>WH</sub>	R/W HIGH after BUS $\overline{Y}$ HIGH (Slave)	15		17		ns
t <sub>BDD</sub> <sup>[25]</sup>	BUS $\overline{Y}$ HIGH to Data Valid		20		25	ns
Interrupt Timing <sup>[24]</sup>						
t <sub>INS</sub>	INT Set Time		20		20	ns
t <sub>INR</sub>	INT Reset Time		20		20	ns
Semaphore Timing						
t <sub>SOP</sub>	SEM Flag Update Pulse ( $\overline{OE}$ or SEM)	10		12		ns
t <sub>SWRD</sub>	SEM Flag Write to Read Time	5		5		ns
t <sub>SPS</sub>	SEM Flag Contention Window	5		5		ns
t <sub>SAA</sub>	SEM Address Access Time		20		25	ns

**Data Retention Mode**

The CY7C024AV/025AV/ 026AV and CY7C0241AV/ 0251AV/ 036AV are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

1. Chip Enable ( $\overline{CE}$ ) must be held HIGH during data retention, within  $V_{CC}$  to  $V_{CC} - 0.2V$ .
2.  $\overline{CE}$  must be kept between  $V_{CC} - 0.2V$  and 70% of  $V_{CC}$  during the power-up and power-down transitions.
3. The RAM can begin operation  $>t_{RC}$  after  $V_{CC}$  reaches the minimum operating voltage (3.0V).

**Timing**


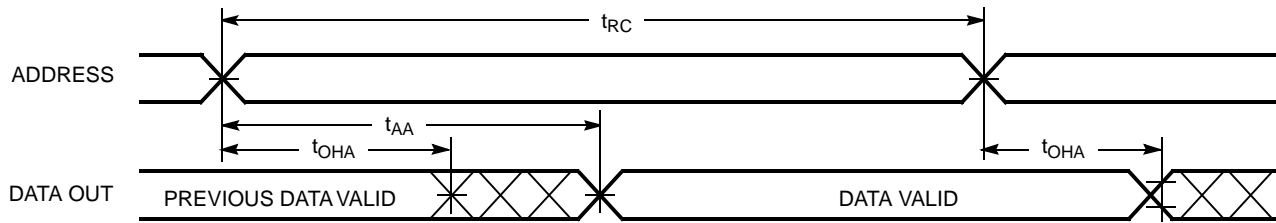
Parameter	Test Conditions <sup>[26]</sup>	Max.	Unit
$ICC_{DR1}$	@ $V_{CCDR} = 2V$	50	$\mu A$

**Notes:**

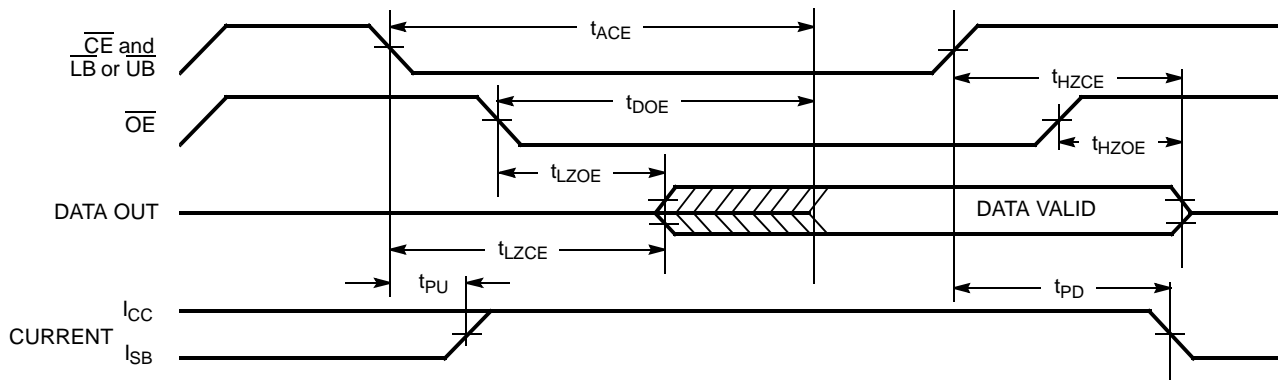
23. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Busy waveform.
24. Test conditions used are Load 2.
25.  $t_{BDD}$  is a calculated parameter and is the greater of  $t_{WDD} - t_{PWE}$  (actual) or  $t_{DDD} - t_{SD}$  (actual).
26.  $CE = V_{CC}$ ,  $V_{in} = GND$  to  $V_{CC}$ ,  $T_A = 25^\circ C$ . This parameter is guaranteed but not tested.

## Switching Waveforms

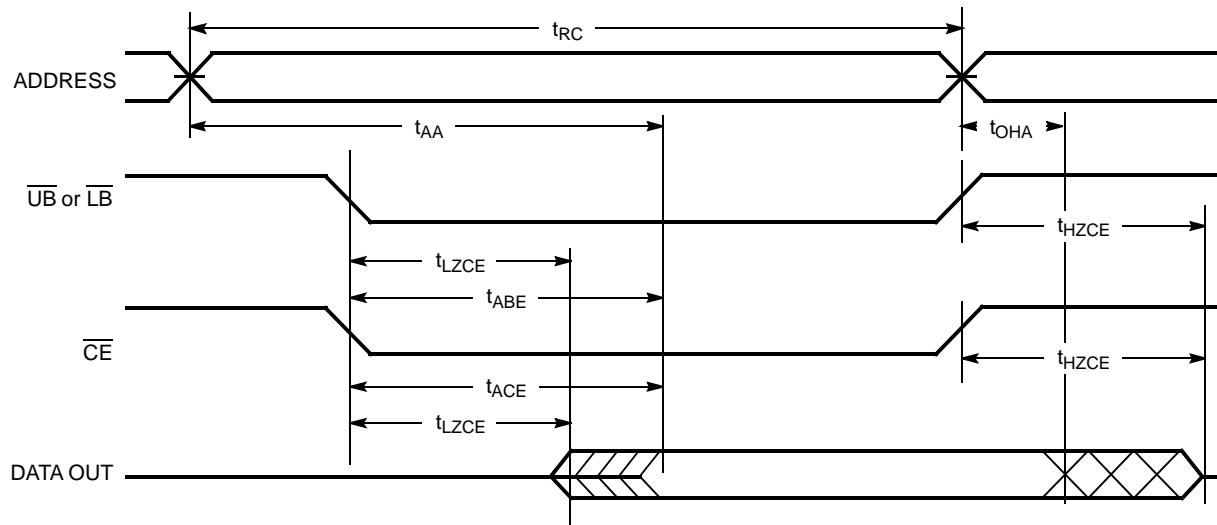
### Read Cycle No.1 (Either Port Address Access)<sup>[27, 28, 29]</sup>



### Read Cycle No.2 (Either Port $\overline{CE}/\overline{OE}$ Access)<sup>[27, 30, 31]</sup>

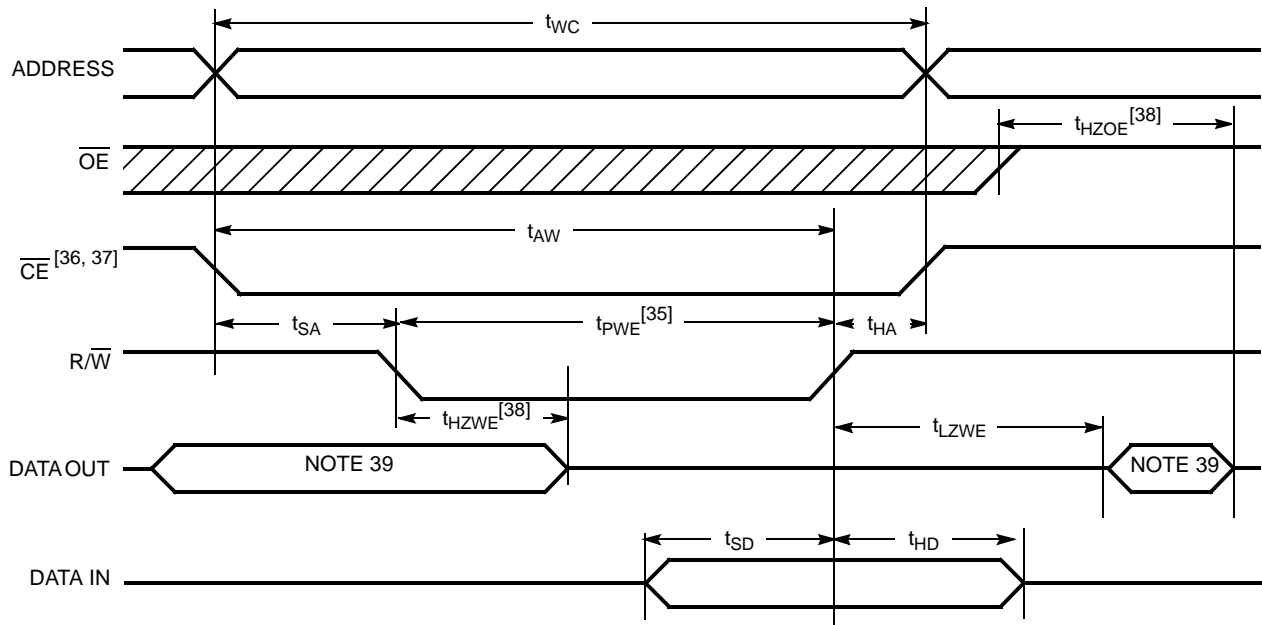
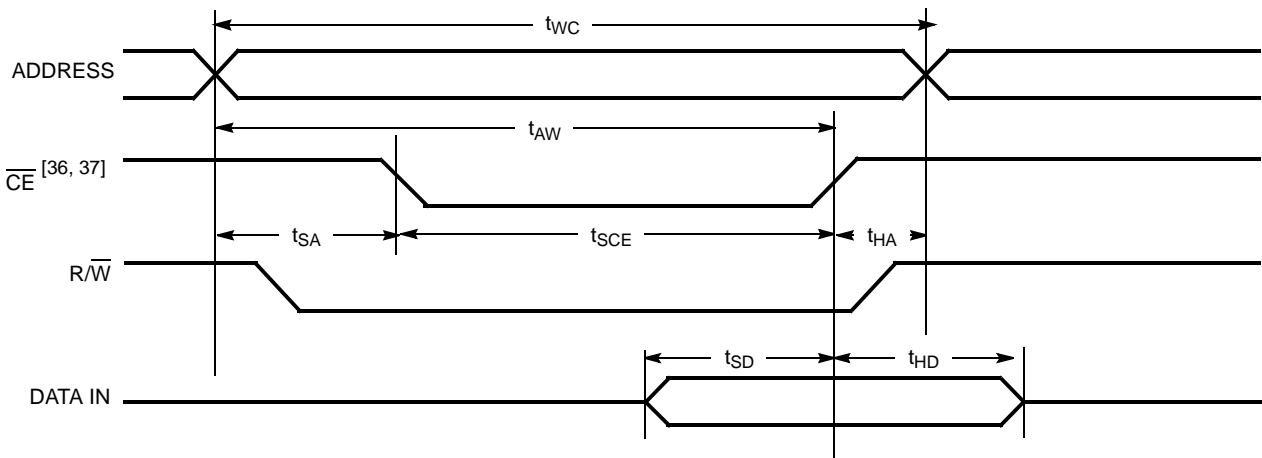


### Read Cycle No. 3 (Either Port)<sup>[27, 29, 30, 31]</sup>

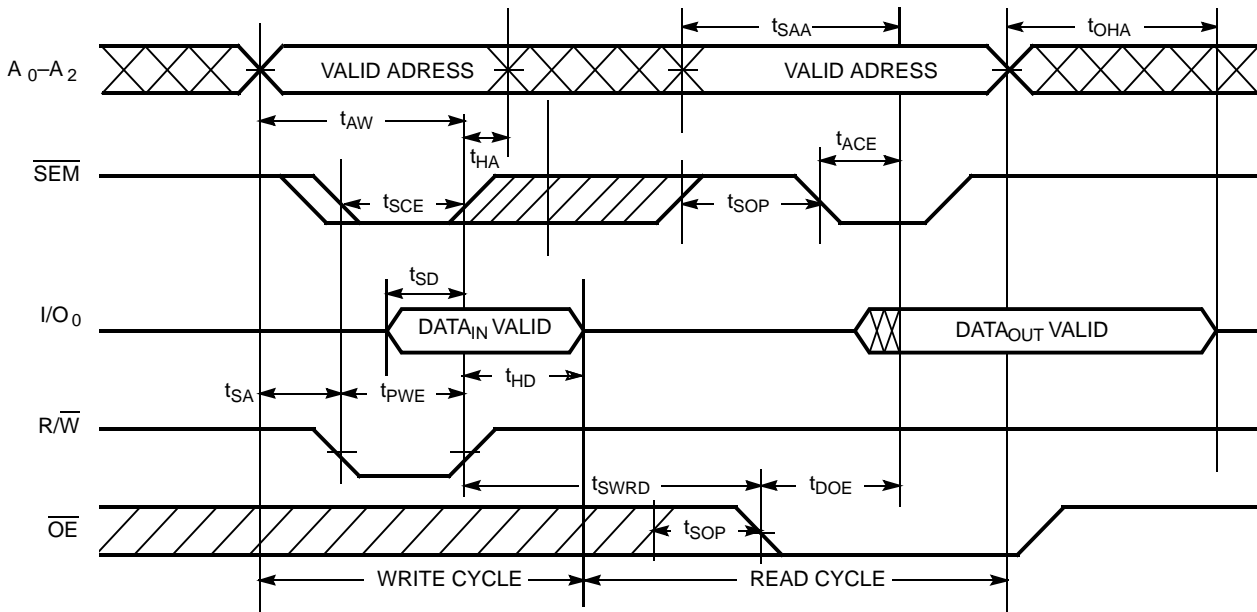
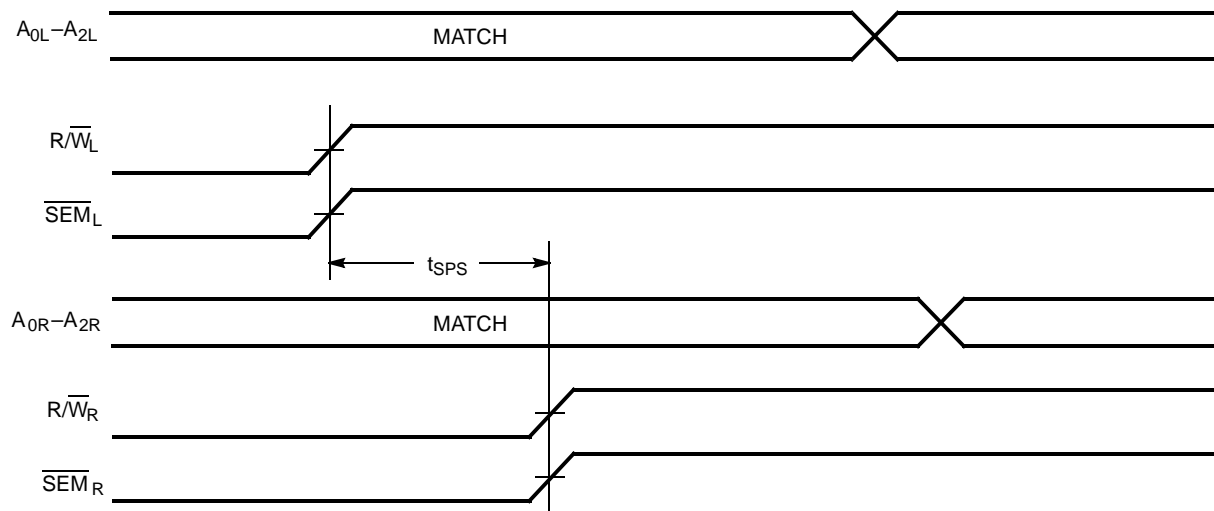


#### Notes:

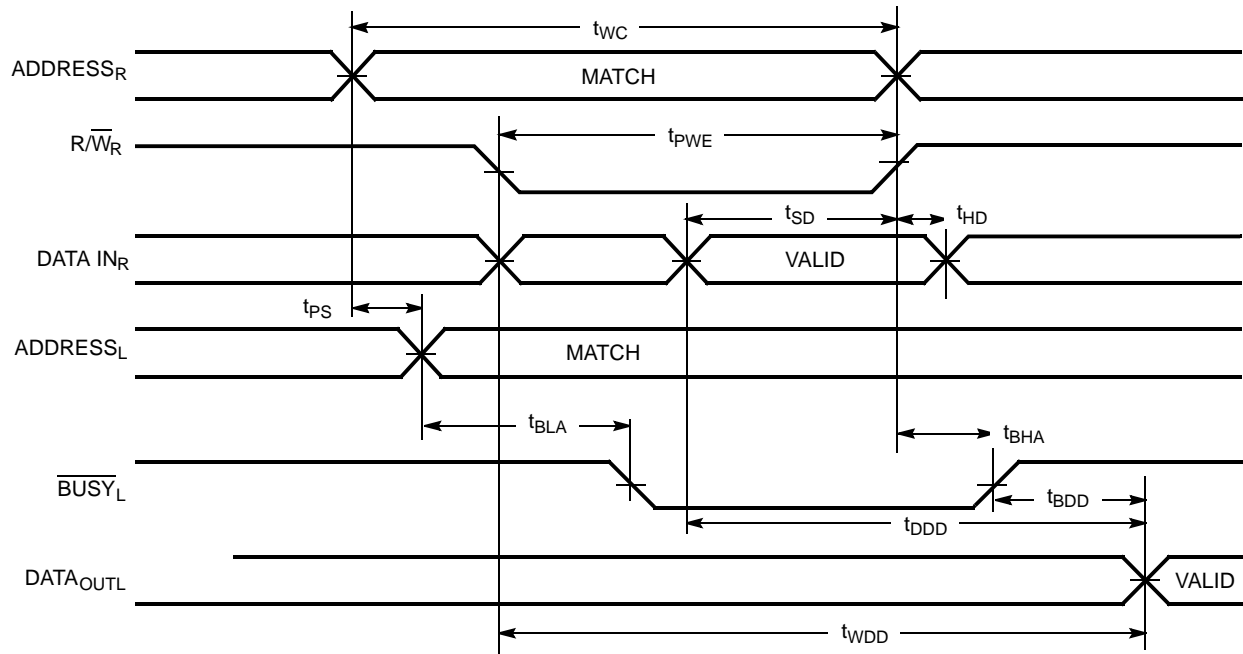
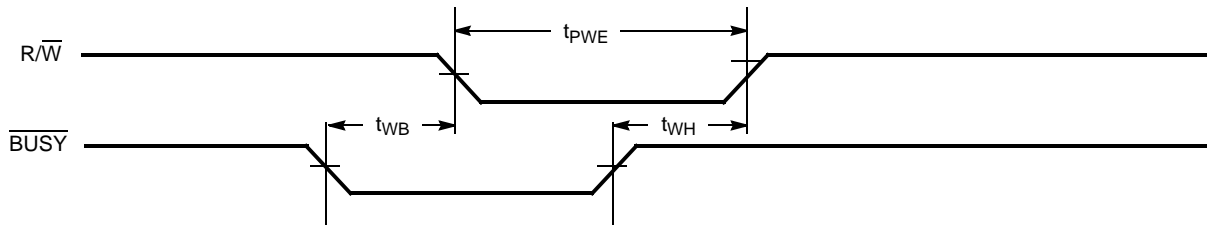
27.  $R/\overline{W}$  is HIGH for read cycles.
28. Device is continuously selected  $\overline{CE} = V_{IL}$  and  $\overline{UB}$  or  $\overline{LB} = V_{IL}$ . This waveform cannot be used for semaphore reads.
29.  $\overline{OE} = V_{IL}$ .
30. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
31. To access RAM,  $\overline{CE} = V_{IL}$ ,  $\overline{UB}$  or  $\overline{LB} = V_{IL}$ ,  $\overline{SEM} = V_{IH}$ . To access semaphore,  $\overline{CE} = V_{IH}$ ,  $\overline{SEM} = V_{IL}$ .

**Switching Waveforms (continued)**
**Write Cycle No.1: R/W Controlled Timing**<sup>[32, 33, 34, 35]</sup>

**Write Cycle No. 2: CE Controlled Timing**<sup>[32, 33, 34, 40]</sup>

**Notes:**

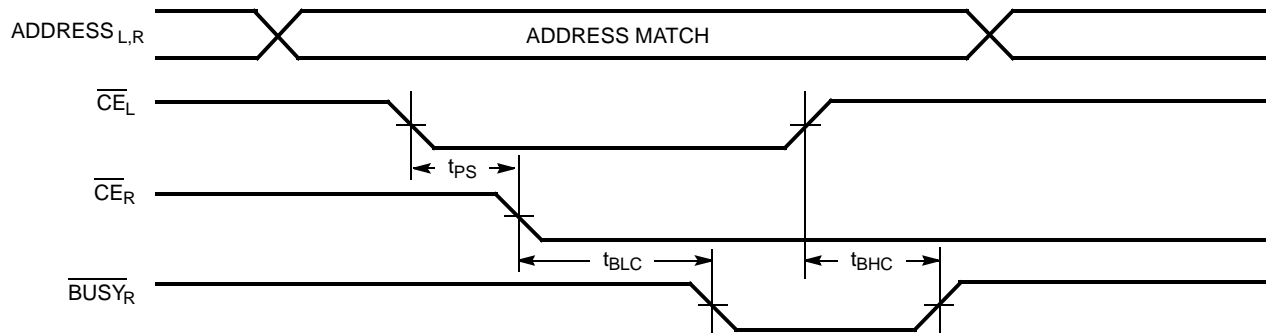
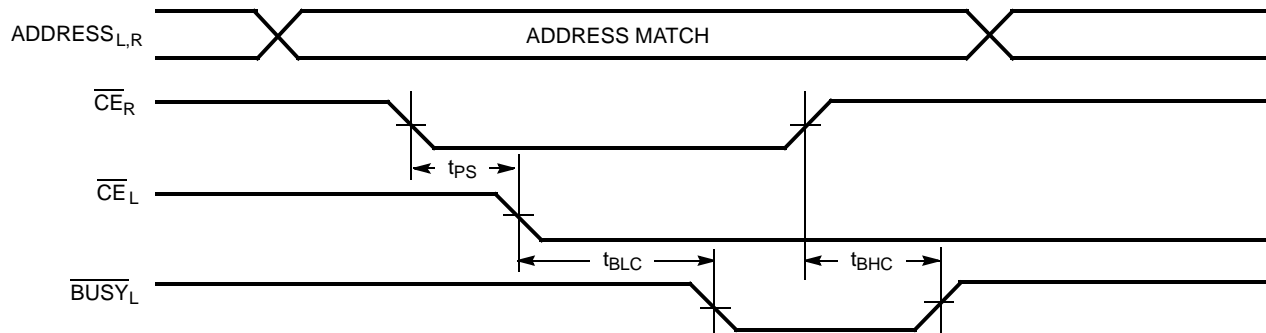
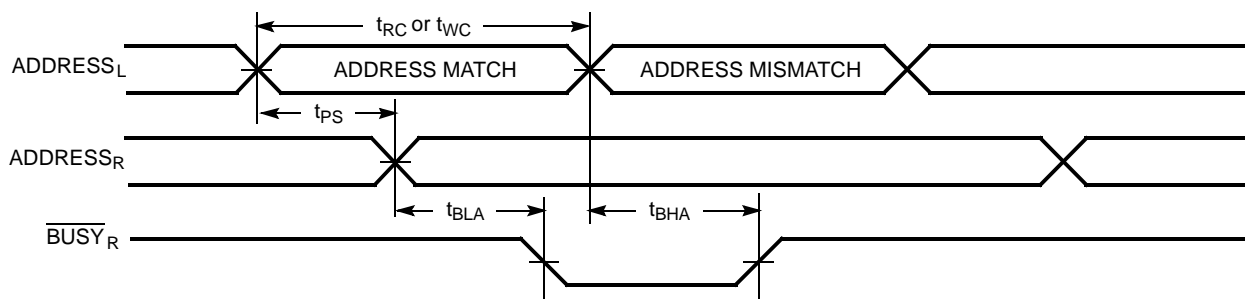
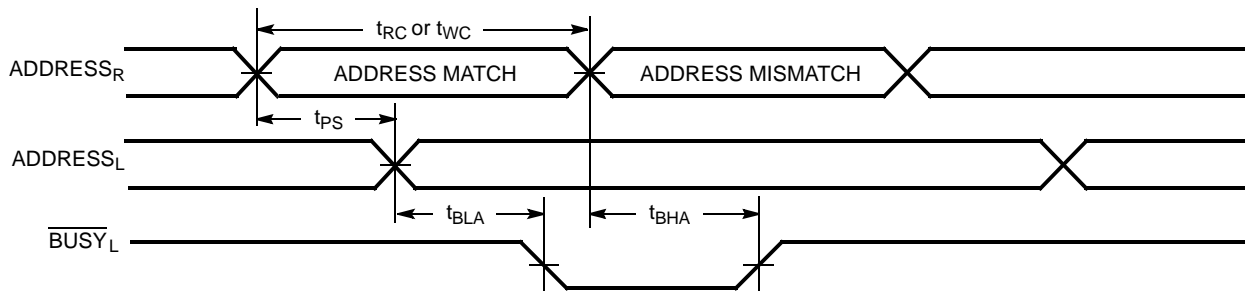
32.  $\overline{R/\overline{W}}$  must be HIGH during all address transitions.
33. A write occurs during the overlap ( $t_{SCE}$  or  $t_{PWE}$ ) of a LOW  $\overline{CE}$  or  $\overline{SEM}$  and a LOW  $\overline{UB}$  or  $\overline{LB}$ .
34.  $t_{HA}$  is measured from the earlier of  $\overline{CE}$  or  $\overline{R/\overline{W}}$  or ( $\overline{SEM}$  or  $\overline{R/\overline{W}}$ ) going HIGH at the end of write cycle.
35. If  $\overline{OE}$  is LOW during a  $\overline{R/\overline{W}}$  controlled write cycle, the write pulse width must be the larger of  $t_{PWE}$  or ( $t_{HZWE} + t_{SD}$ ) to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{SD}$ . If  $\overline{OE}$  is HIGH during an  $\overline{R/\overline{W}}$  controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified  $t_{PWE}$ .
36. To access RAM,  $\overline{CE} = V_{IL}$ ,  $\overline{SEM} = V_{IH}$ .
37. To access upper byte,  $\overline{CE} = V_{IL}$ ,  $\overline{UB} = V_{IL}$ ,  $\overline{SEM} = V_{IH}$ .  
To access lower byte,  $\overline{CE} = V_{IL}$ ,  $\overline{LB} = V_{IL}$ ,  $\overline{SEM} = V_{IH}$ .
38. Transition is measured  $\pm 500$  mV from steady state with a 5-pF load (including scope and jig). This parameter is sampled and not 100% tested.
39. During this period, the I/O pins are in the output state, and input signals must not be applied.
40. If the  $\overline{CE}$  or  $\overline{SEM}$  LOW transition occurs simultaneously with or after the  $\overline{R/\overline{W}}$  LOW transition, the outputs remain in the high-impedance state.

**Switching Waveforms (continued)**
**Semaphore Read After Write Timing, Either Side<sup>[41]</sup>**

**Timing Diagram of Semaphore Contention<sup>[42, 43, 44]</sup>**

**Notes:**

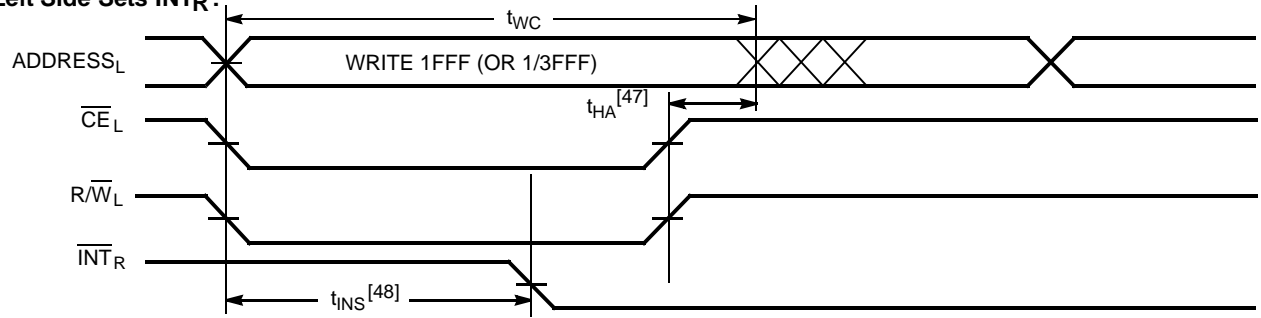
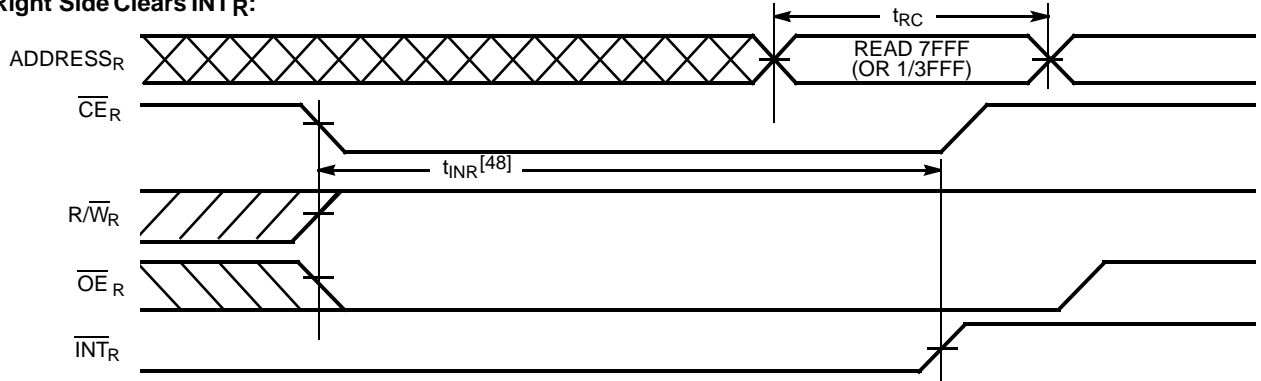
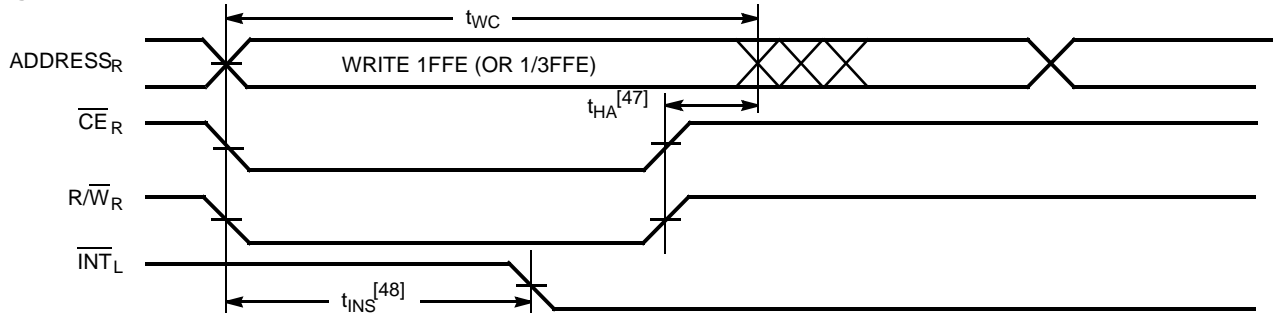
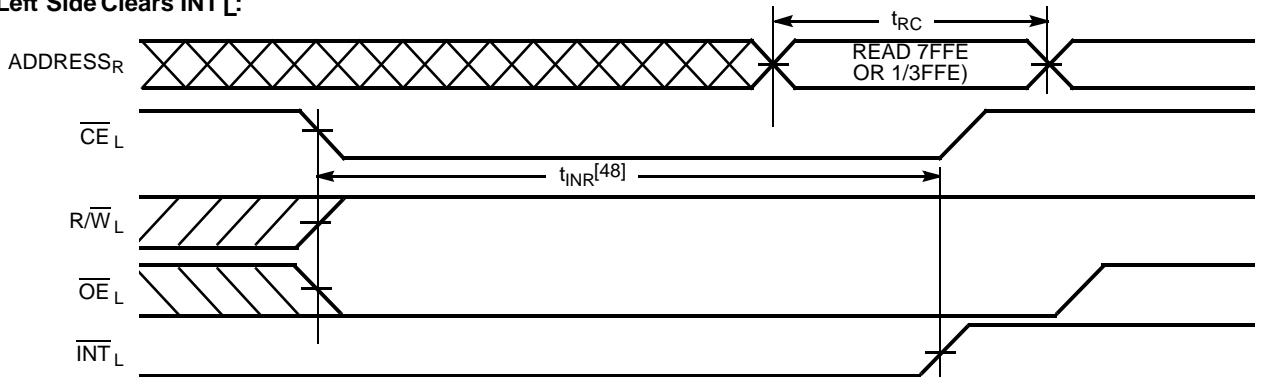
41.  $\overline{CE}$  = HIGH for the duration of the above timing (both write and read cycle).
42.  $I/O_{0R} = I/O_{0L}$  = LOW (request semaphore);  $CE_R = CE_L$  = HIGH.
43. Semaphores are reset (available to both ports) at cycle start.
44. If  $t_{SPS}$  is violated, the semaphore will definitely be obtained by one side or the other, but which side will get the semaphore is unpredictable.

**Switching Waveforms (continued)**
**Timing Diagram of Read with  $\overline{\text{BUSY}}$  ( $\text{M}/\overline{\text{S}}=\text{HIGH}$ )<sup>[45]</sup>**

**Write Timing with Busy Input ( $\text{M}/\overline{\text{S}}=\text{LOW}$ )**

**Note:**

45.  $\overline{\text{CE}}_L = \overline{\text{CE}}_R = \text{LOW}$ .

**Switching Waveforms (continued)**
**Busy Timing Diagram No.1 ( $\overline{CE}$  Arbitration)<sup>[46]</sup>**
 **$\overline{CE}_L$  Valid First:**

 **$\overline{CE}_R$  Valid First:**

**Busy Timing Diagram No.2 (Address Arbitration)<sup>[46]</sup>**
**Left Address Valid First:**

**Right Address Valid First:**

**Note:**

46. If  $t_{PS}$  is violated, the busy signal will be asserted on one side or the other, but there is no guarantee to which side  $\overline{BUSY}$  will be asserted.

**Switching Waveforms (continued)**
**Interrupt Timing Diagrams**
**Left Side Sets  $\overline{\text{INT}}_R$ :**

**Right Side Clears  $\overline{\text{INT}}_R$ :**

**Right Side Sets  $\overline{\text{INT}}_L$ :**

**Left Side Clears  $\overline{\text{INT}}_L$ :**

**Notes:**

47.  $t_{HA}$  depends on which enable pin ( $\overline{\text{CE}}_L$  or  $\overline{\text{R}}/\overline{\text{W}}_L$ ) is deasserted first.  
48.  $t_{INS}$  or  $t_{INR}$  depends on which enable pin ( $\overline{\text{CE}}_L$  or  $\overline{\text{R}}/\overline{\text{W}}_L$ ) is asserted last.





## Ordering Information

### 4K x16 3.3V Asynchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C024AV-20AC	A100	100-Pin Thin Quad Flat Pack	Commercial
25	CY7C024AV-25AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C024AV-25AI	A100	100-Pin Thin Quad Flat Pack	Industrial

### 8K x16 3.3V Asynchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C025AV-20AC	A100	100-Pin Thin Quad Flat Pack	Commercial
25	CY7C025AV-25AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C025AV-25AI	A100	100-Pin Thin Quad Flat Pack	Industrial

### 16K x16 3.3V Asynchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C026AV-20AC	A100	100-Pin Thin Quad Flat Pack	Commercial
25	CY7C026AV-25AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C026AV-25AI	A100	100-Pin Thin Quad Flat Pack	Industrial

### 4K x18 3.3V Asynchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C0241AV-20AC	A100	100-Pin Thin Quad Flat Pack	Commercial
25	CY7C0241AV-25AC	A100	100-Pin Thin Quad Flat Pack	Commercial

### 8K x18 3.3V Asynchronous Dual-Port SRAM

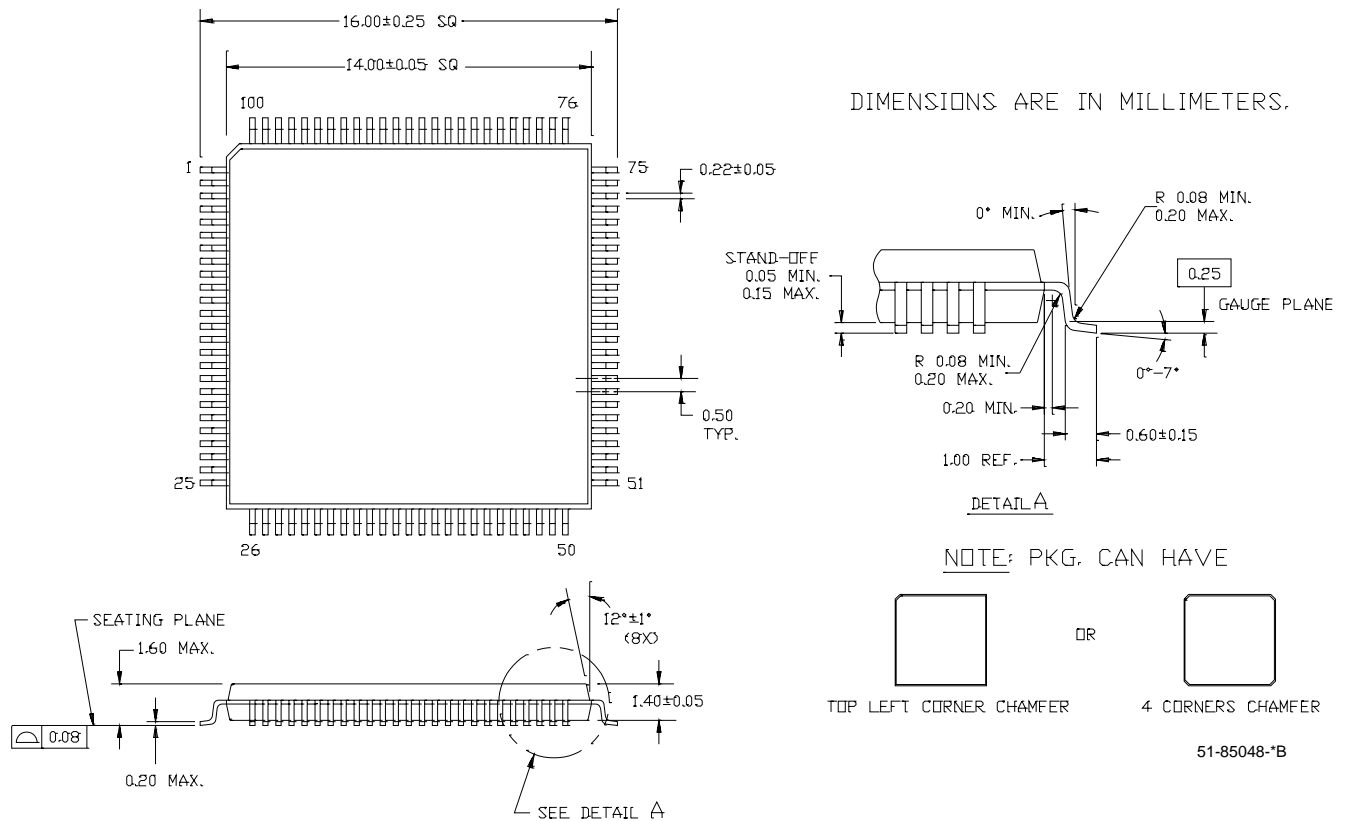
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C0251AV-20AC	A100	100-Pin Thin Quad Flat Pack	Commercial
25	CY7C0251AV-25AC	A100	100-Pin Thin Quad Flat Pack	Commercial

### 16K x18 3.3V Asynchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C036AV-20AC	A100	100-Pin Thin Quad Flat Pack	Commercial
25	CY7C036AV-25AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C036AV-25AI	A100	100-Pin Thin Quad Flat Pack	Industrial

## Package Diagram

### 100-Pin Thin Plastic Quad Flat Pack (TQFP) A100



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**Document History Page**

**Document Title: CY7C024AV/CY7C025AV/CY7C026AV/CY7C0241AV/CY7C0251AV/CY7C036AV 3.3V 4K/8K/16K x 16/18 Dual Port Static RAM**  
**Document Number: 38-06052**

<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	110204	11/11/01	SZV	Change from Spec number: 38-00838 to 38-06052
*A	122302	12/27/02	RBI	Power-up requirements added to Maximum Ratings Information
*B	128958	9/03/03	JFU	Added CY7C025AV-25AI to Ordering Information
*C	237622	See ECN	YDT	Removed cross information from features section
*D	241968	See ECN	WWZ	Added CY7C024AV-25AI to Ordering Information
*E	276451	See ECN	SPN	Corrected x18 for 026AV to x16