AN6554, AN6554NS

Quadruple Operational Amplifiers

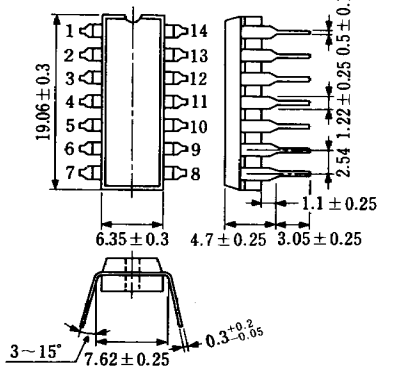
■ Outline

The AN6554 and the AN6554NS are quadruple operational amplifiers with phase compensation circuits built-in.
They are suited for application to various electronic circuits such as active filters and audio preamplifiers.

■ Features

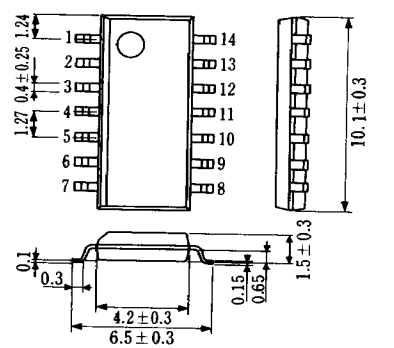
- Phase compensation circuit
- High gain, low noise
- Output short-circuit protection

AN6554 Unit : mm



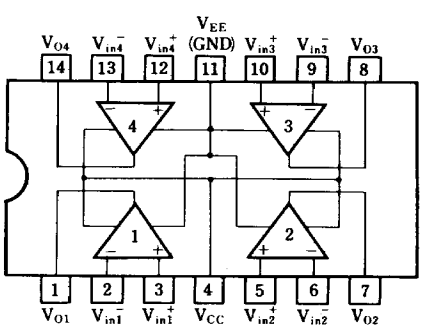
14-Lead DIL Plastic Package

AN6554NS Unit : mm



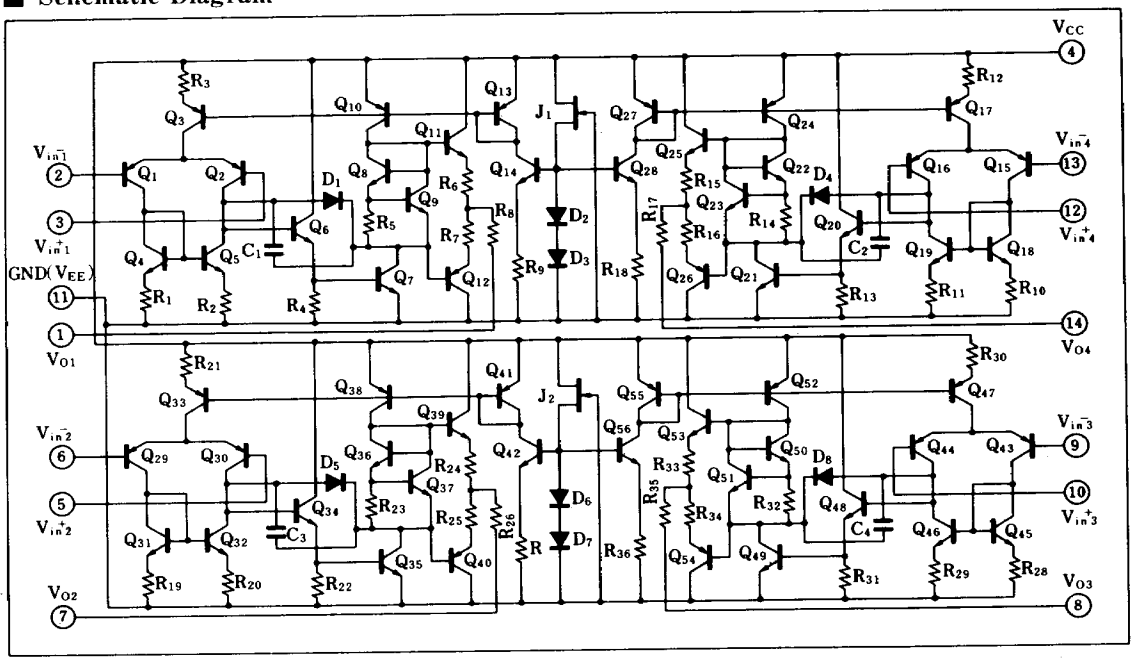
14-Lead PANAFLAT Package(SO-14D)

■ Block Diagram



Panasonic

■ Schematic Diagram



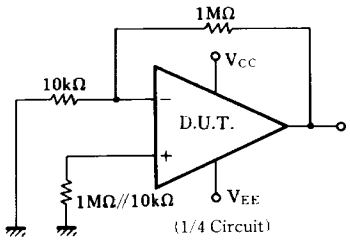
■ Absolute Maximum Ratings (Ta=25℃)

Item			Symbol	Rating	Unit
Voltage	Supply Voltage		V_{CC}	36	V
	Differential Input Voltage		V_{ID}	±30	V
	Common-Mode Input Voltage		V_{ICM}	±15	V
Power Dissipation	AN6554		P_D	570	mW
	AN6554NS			380	
Temperature	Operating Ambient Temperature		T_{opr}	−20～+75	℃
	Storage Temperature	AN6554	T_{stg}	−55～+150	℃
		AN6554NS		−55～+125	

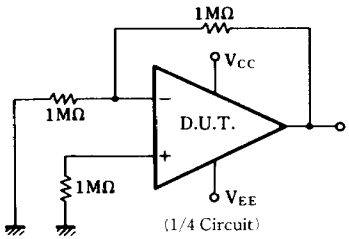
■ Electrical Characteristics (V_{CC}=15V, V_{EE}=−15V, Ta=25℃)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Input Offset Voltage	$V_{I(offset)}$	1	$R_S \leqq 10k\Omega$		0.5	5	mV
Input Offset Current	I_{IO}	2			5	50	nA
Input Bias Current	I_{Bias}	2			100	300	nA
Voltage Gain	G_V	3	$R_L \geqq 2k\Omega$, V_O=±10V	88	100		dB
Maximum Output Voltage	$V_{O(max.1)}$	4	$R_L \geqq 10k\Omega$	±12	±14		V
	$V_{O(max.2)}$	4	$R_L \geqq 2k\Omega$	±10	±13		V
Common-Mode Input Voltage Width	V_{CM}	5		±12	±14		V
Common-Mode Rejection Ratio	CMR	6		70	90		dB
Supply Voltage Rejection Ratio	SVR	7			30	100	μV/V
Power Consumption	P_C	8				240	mW
Slew Rate	SR	9			1.6		V/μs
Input Referred Noise Voltage	V_{ni}	10	R_S=1kΩ, B=10Hz～30kHz		2.5		μV_{rms}
Channel Separation	Sep	11	f=10kHz		110		dB

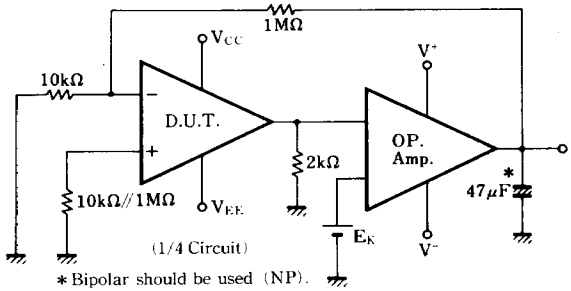
Test Circuit 1 ($V_{I(offset)}$)



Test Circuit 2 (I_{IO}, I_{Bias})

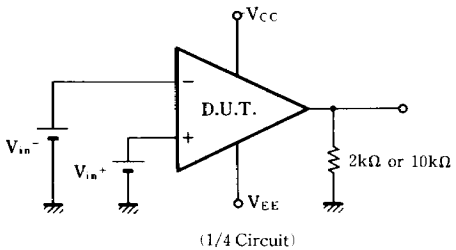


Test Circuit 3 (G_V)

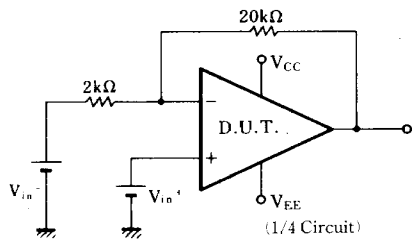


* Bipolar should be used (NP).

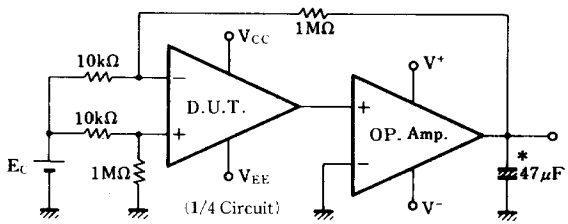
Test Circuit 4 ($V_{O(max.1)}$, $V_{O(max.2)}$)



Test Circuit 5 (V_{CM})

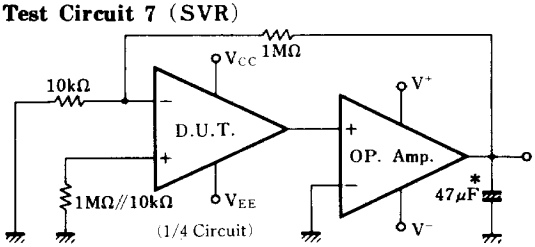


Test Circuit 6 (CMR)



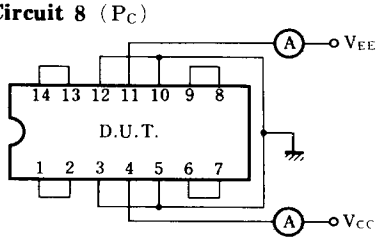
* Bipolar should be used (NP).

Test Circuit 7 (SVR)

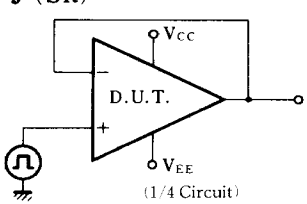


* Bipolar should be used (NP).

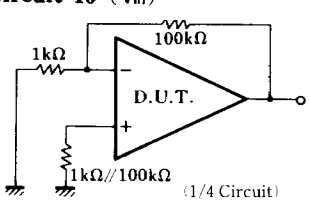
Test Circuit 8 (P_C)



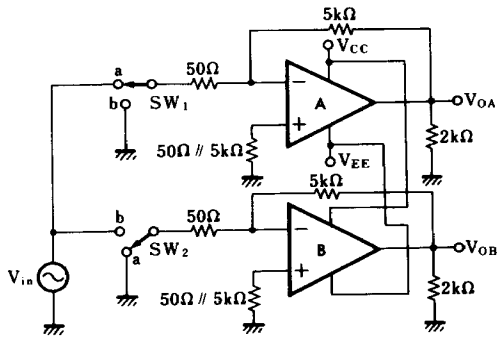
Test Circuit 9 (SR)



Test Circuit 10 (V_{ni})



Test Circuit 11 (Sep)



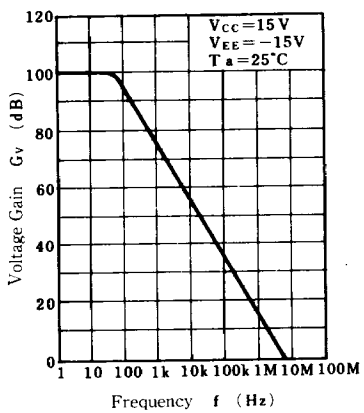
- When SW_1 and SW_2 are set to 'a' side,

$$Sep(A \rightarrow B) = 20\log\frac{100V_{OA}}{V_{OB}}$$

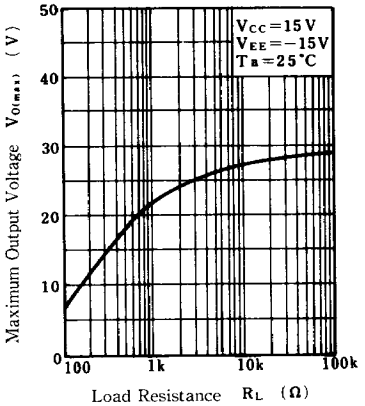
- When SW_1 and SW_2 are set to 'b' side,

$$Sep(B \rightarrow A) = 20\log\frac{100V_{OB}}{V_{OA}}$$

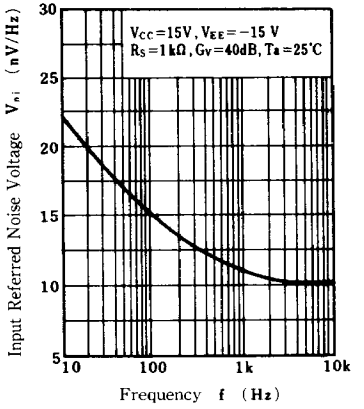
$G_V - f$



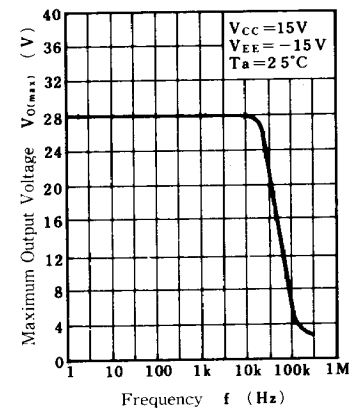
$V_{O(max)} - R_L$



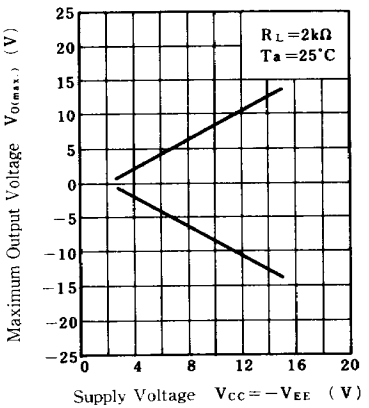
$V_{ni} - f$



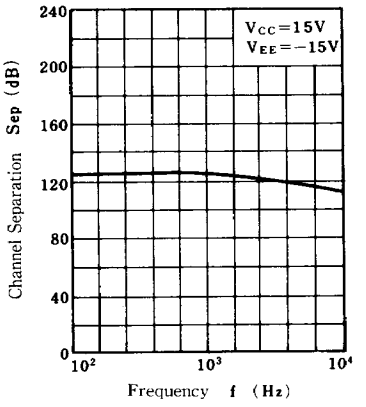
$V_{O(max.)} - f$

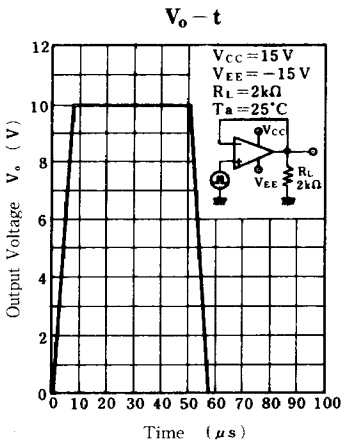


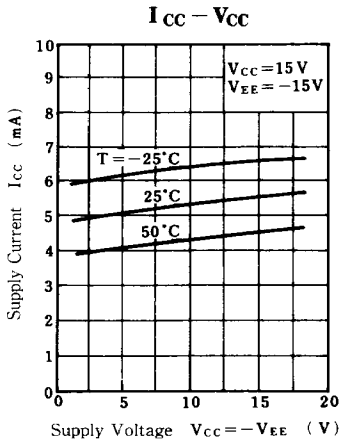
$V_{O(max.)} - V_{CC}, V_{EE}$



$Sep - f$







■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	Ch. 1 Output	8	Ch. 3 Output
2	Ch. 1 Invert Input	9	Ch. 3 Invert Input
3	Ch. 3 Non Invert Input	10	Ch. 3 Non Invert Input
4	V_{CC}	11	V_{EE} (GND)
5	Ch. 2 Non Invert Input	12	Ch. 4 Non Invert Input
6	Ch. 2 Invert Input	13	Ch. 4 Invert Input
7	Ch. 2 Output	14	Ch. 4 Output