Negative Voltage Hot Swap Controllers

FEATURES

- **Allows Safe Board Insertion and Removal from a Live –48V Backplane**
- **Floating Topology Permits Very High Voltage Operation**
- **Current Limit With Circuit Breaker Timer**
- **Fast Response Time Limits Peak Fault Current**
- **Programmable Soft-Start Current Limit**
- **Programmable Timer with Drain Voltage Accelerated Response**
- **±1% Undervoltage/Overvoltage Threshold (LTC4252C)**
- **Improved Ruggedness Shunt Regulator**
- Adjustable Undervoltage/Overvoltage Protection
- LTC4252B-1/LTC4252C-1: Latch Off After Fault
- LTC4252B-2/LTC4252C-2: Automatic Retry After Fault
- Available in 8-Pin and 10-Pin MSOP Packages

APPLICATIONS

- Hot Board Insertion
- Electronic Circuit Breaker
- –48V Distributed Power Systems
- Negative Power Supply Control
- Central Office Switching
- High Availability Servers
- ATCA

DESCRIPTION

The LTC®4252 negative voltage Hot Swap™ controller allows a board to be safely inserted and removed from a live backplane. Output current is controlled by three stages of current limiting: a timed circuit breaker, active current limiting and a fast feedforward path that limits peak current under worst-case catastrophic fault conditions.

Adjustable undervoltage and overvoltage detectors disconnect the load whenever the input supply exceeds the desired operating range. The LTC4252's supply input is shunt regulated, allowing safe operation with very high supply voltages. A multifunction timer delays initial start-up and controls the circuit breaker's response time. The circuit breaker's response time is accelerated by sensing excessive MOSFET drain voltage, keeping the MOSFET within its safe operating area (SOA). An adjustable soft-start circuit controls MOSFET inrush current at start-up.

The LTC4252-2 provides automatic retry after a fault. The LTC4252C-1/LTC4252C-2 feature tight ±1% undervoltage/overvoltage threshold accuracy. The LTC4252 is available in either an 8-pin or 10-pin MSOP.

The LTC4252B and LTC4252C improve the ruggedness of the shunt regulator in the LTC4252 and LTC4252A.

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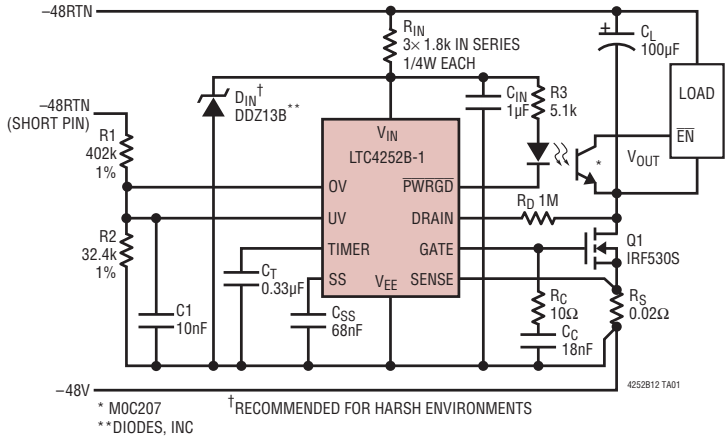
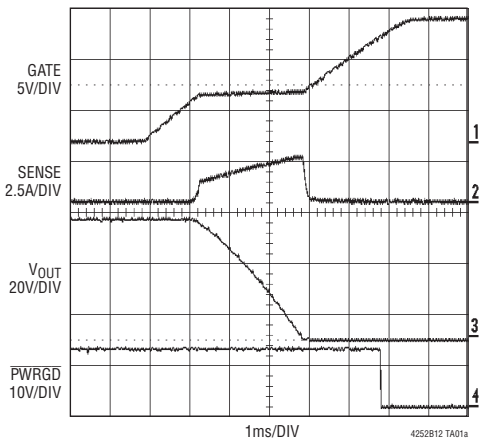
TYPICAL APPLICATION

–48V/2.5A Hot Swap Controller



Start-Up Behavior



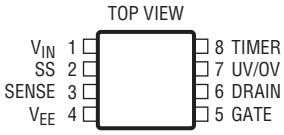
ABSOLUTE MAXIMUM RATINGS

All Voltages Referred to V_{EE} (Note 1)

Current into V_{IN} (100µs Pulse) 100mA
V_{IN}, DRAIN Pin Minimum Voltage..... –0.3V
Input/Output Pins
(Except SENSE and DRAIN) Voltage ..... –0.3V to 16V
SENSE Pin Voltage..... –0.6V to 16V
Current Out of SENSE Pin (20µs Pulse) ..... –200mA
Current into DRAIN Pin (100µs Pulse) 20mA
Maximum Junction Temperature ..... 125°C

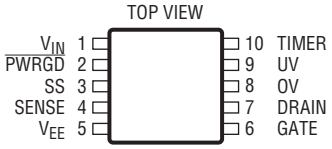
Operating Temperature Range
LTC4252BC-1/LTC4252BC-2
LTC4252CC-1/LTC4252CC-2..... 0°C to 70°C
LTC4252BI-1/LTC4252BI-2
LTC4252CI-1/LTC4252CI-2 ..... –40°C to 85°C
Storage Temperature Range .....–65°C to 150°C
Lead Temperature (Soldering, 10 sec).....300°C

PIN CONFIGURATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 160°C/W



MS PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 160°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4252BCMS8-1#PBF	LTC4252BCMS8-1#TRPBF	LTGDX	8-Lead Plastic MSOP	0°C to 70°C
LTC4252BCMS8-2#PBF	LTC4252BCMS8-2#TRPBF	LTGDZ	8-Lead Plastic MSOP	0°C to 70°C
LTC4252BIMS8-1#PBF	LTC4252BIMS8-1#TRPBF	LTGDX	8-Lead Plastic MSOP	–40°C to 85°C
LTC4252BIMS8-2#PBF	LTC4252BIMS8-2#TRPBF	LTGDZ	8-Lead Plastic MSOP	–40°C to 85°C
LTC4252BCMS-1#PBF	LTC4252BCMS-1#TRPBF	LTGDY	10-Lead Plastic MSOP	0°C to 70°C
LTC4252BCMS-2#PBF	LTC4252BCMS-2#TRPBF	LTGFB	10-Lead Plastic MSOP	0°C to 70°C
LTC4252BIMS-1#PBF	LTC4252BIMS-1#TRPBF	LTGDY	10-Lead Plastic MSOP	–40°C to 85°C
LTC4252BIMS-2#PBF	LTC4252BIMS-2#TRPBF	LTGFB	10-Lead Plastic MSOP	–40°C to 85°C
LTC4252CCMS-1#PBF	LTC4252CCMS-1#TRPBF	LTGFC	10-Lead Plastic MSOP	0°C to 70°C
LTC4252CCMS-2#PBF	LTC4252CCMS-2#TRPBF	LTGFD	10-Lead Plastic MSOP	0°C to 70°C
LTC4252CIMS-1#PBF	LTC4252CIMS-1#TRPBF	LTGFC	10-Lead Plastic MSOP	–40°C to 85°C
LTC4252CIMS-2#PBF	LTC4252CIMS-2#TRPBF	LTGFD	10-Lead Plastic MSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		LTC4252B-1/-2 MIN	LTC4252B-1/-2 TYP	LTC4252B-1/-2 MAX	LTC4252C-1/-2 MIN	LTC4252C-1/-2 TYP	LTC4252C-1/-2 MAX	UNITS
V_Z	V_{IN} – V_{EE} Zener Voltage	I_{IN} = 2mA	●	11.5	13	14.5	11.5	13	14.5	V
r_Z	V_{IN} – V_{EE} Zener Dynamic Impedance	I_{IN} = 2mA to 30mA			5			5		Ω
I_{IN}	V_{IN} Supply Current	UV = OV = 4V, V_{IN} = (V_Z – 0.3V)	●		0.8	2		0.9	2	mA
V_{LKO}	V_{IN} Undervoltage Lockout	Coming Out of UVLO (Rising V_{IN})	●		9.2	11.5		9	10	V
V_{LKH}	V_{IN} Undervoltage Lockout Hysteresis				1			0.5		V
V_{CB}	Circuit Breaker Current Limit Voltage	V_{CB} = (V_{SENSE} – V_{EE})	●	40	50	60	45	50	55	mV
V_{ACL}	Analog Current Limit Voltage	V_{ACL} = (V_{SENSE} – V_{EE}), SS = Open or 2.2V	●	80	100	120				mV
V_{ACL}/ V_{CB}	Analog Current Limit Voltage/ Circuit Breaker Voltage	V_{ACL} = (V_{SENSE} – V_{EE}), SS = Open or 1.4V	●				1.05	1.20	1.38	V/V
V_{FCL}	Fast Current Limit Voltage	V_{FCL} = (V_{SENSE} – V_{EE})	●	150	200	300	150	200	300	mV
V_{SS}	SS Voltage	After End of SS Timing Cycle			2.2			1.4		V
R_{SS}	SS Output Impedance				100			50		kΩ
I_{SS}	SS Pin Current	UV = OV = 4V, V_{SENSE} = V_{EE}, V_{SS} = 0V (Sourcing)			22			28		μA
		UV = OV = 0V, V_{SENSE} = V_{EE}, V_{SS} = 2V (Sinking)			28			28		mA
V_{OS}	Analog Current Limit Offset Voltage				10			10		mV
V_{ACL}+V_{OS}/ V_{SS}	Ratio (V_{ACL} + V_{OS}) to SS Voltage				0.05			0.05		V/V
I_{GATE}	GATE Pin Output Current	UV = OV = 4V, V_{SENSE} = V_{EE}, V_{GATE} = 0V (Sourcing)	●	40	58	80	40	58	80	μA
		UV = OV = 4V, V_{SENSE} – V_{EE} = 0.15V, V_{GATE} = 3V (Sinking)			17			17		mA
		UV = OV = 4V, V_{SENSE} – V_{EE} = 0.3V, V_{GATE} = 1V (Sinking)			190			190		mA
V_{GATE}	External MOSFET Gate Drive	V_{GATE} – V_{EE}, I_{IN} = 2mA	●	10	12	V_Z	10	12	V_Z	V
V_{GATEH}	Gate High Threshold	V_{GATEH} = V_{IN} – V_{GATE}, I_{IN} = 2mA, for PWRGD Status (MS Only)			2.8			2.8		V
V_{GATEL}	Gate Low Threshold	(Before Gate Ramp-Up)			0.5			0.5		V
V_{UVHI}	UV Pin Threshold HIGH		●	3.075	3.225	3.375				V
V_{UVLO}	UV Pin Threshold LOW		●	2.775	2.925	3.075				V
V_{UV}	UV Pin Threshold	Low-to-High Transition	●				3.05	3.08	3.11	V
V_{UVHST}	UV Pin Hysteresis	(● for LTC4252C Only)	●		300		292	324	356	mV
V_{OVHI}	OV Pin Threshold HIGH		●	5.85	6.15	6.45				V
V_{OVLO}	OV Pin Threshold LOW		●	5.25	5.55	5.85				V
V_{OV}	OV Pin Threshold	Low-to-High Transition	●				5.04	5.09	5.14	V
V_{OVHST}	OV Pin Hysteresis	(● for LTC4252C Only)	●		600		82	102	122	mV
I_{SENSE}	SENSE Pin Input Current	UV = OV = 4V, V_{SENSE} = 50mV	●		–15	–30		–15	–30	μA
I_{INP}	UV, OV Pin Input Current	UV = OV = 4V	●		±0.1	±1		±0.1	±1	μA
V_{TMRH}	TIMER Pin Voltage High Threshold				4			4		V
V_{TMRL}	TIMER Pin Voltage Low Threshold				1			1		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

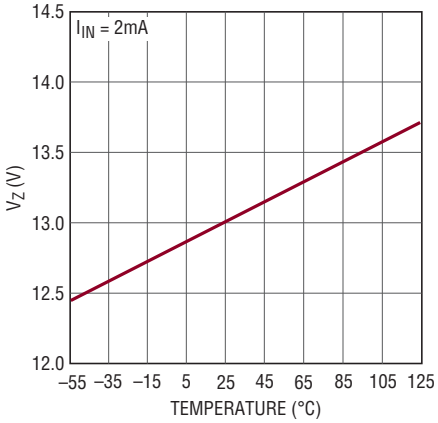
SYMBOL	PARAMETER	CONDITIONS		LTC4252B-1/-2 MIN	LTC4252B-1/-2 TYP	LTC4252B-1/-2 MAX	LTC4252C-1/-2 MIN	LTC4252C-1/-2 TYP	LTC4252C-1/-2 MAX	UNITS
I_{TMR}	TIMER Pin Current	Timer On (Initial Cycle/Latchoff/ Shutdown Cooling, Sourcing), V_{TMR} = 2V			5.8			5.8		µA
		Timer Off (Initial Cycle, Sinking), V_{TMR} = 2V			28			28		mA
		Timer On (Circuit Breaker, Sourcing, I_{DRN} = 0µA), V_{TMR} = 2V			230			230		µA
		Timer On (Circuit Breaker, Sourcing, I_{DRN} = 50µA), V_{TMR} = 2V			630			630		µA
		Timer Off (Circuit Breaker/ Shutdown Cooling, Sinking), V_{TMR} = 2V			5.8			5.8		µA
$\Delta I_{TMRACC}/\Delta I_{DRN}$	[(I_{TMR} at I_{DRN} = 50µA) – (I_{TMR} at I_{DRN} = 0µA)]/ΔI_{DRN}	Timer On (Circuit Breaker with I_{DRN} = 50µA)			8			8		µA/µA
V_{DRNL}	DRAIN Pin Voltage Low Threshold	For $\overline{PWRGD}$ Status (MS Only)			2.385			2.385		V
I_{DRNL}	DRAIN Leakage Current	V_{DRAIN} = 5V (4V for LTC4252C)			±0.1	±1		±0.1	±1	µA
V_{DRNCL}	DRAIN Pin Clamp Voltage	I_{DRN} = 50µA			7			6		V
V_{PGL}	$\overline{PWRGD}$ Output Low Voltage	I_{PG} = 1.6mA (MS Only) I_{PG} = 5mA (MS Only)	● ●		0.2	0.4 1.1		0.2	0.4 1.1	V V
I_{PGH}	$\overline{PWRGD}$ Pull-Up Current	$V_{\overline{PWRGD}}$ = 0V (Sourcing) (MS Only)	●	40	58	80	40	58	80	µA
t_{SS}	SS Default Ramp Period	SS Pin Floating, V_{SS} Ramps from 0.2V to 2V			180					µs
		SS Pin Floating, V_{SS} Ramps from 0.1V to 0.9V						230		µs
t_{PLLUG}	UV Low to Gate Low				0.4			0.4		µs
t_{PHLOG}	OV High to Gate Low				0.4			0.4		µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to V_{EE} unless otherwise specified.

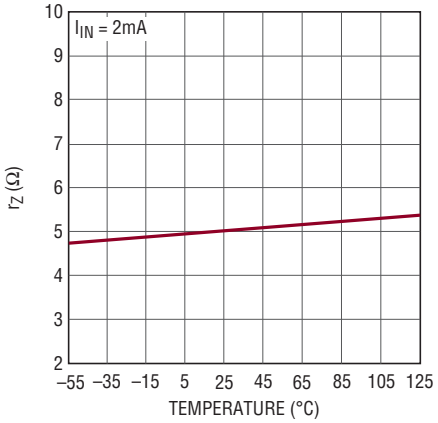
TYPICAL PERFORMANCE CHARACTERISTICS

V_Z vs Temperature



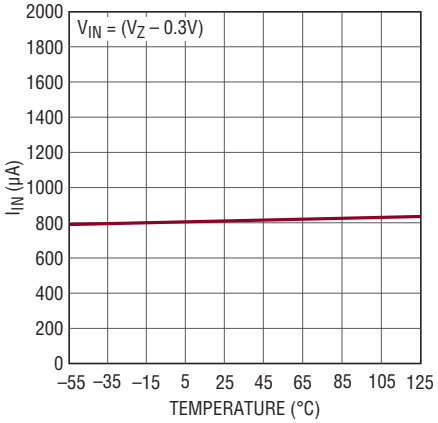
4252B12 G01

r_Z vs Temperature



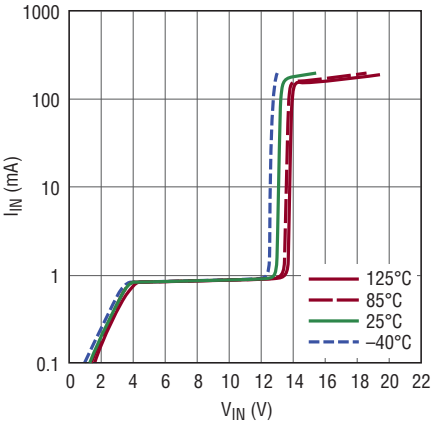
4252B12 G02

I_{IN} vs Temperature



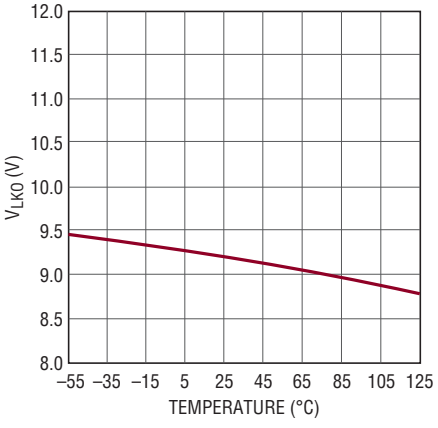
4252B12 G03

I_{IN} vs V_{IN}



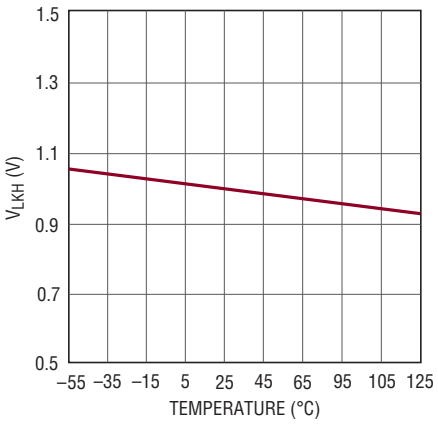
4252B12 G04

Undervoltage Lockout V_{LKO} vs Temperature



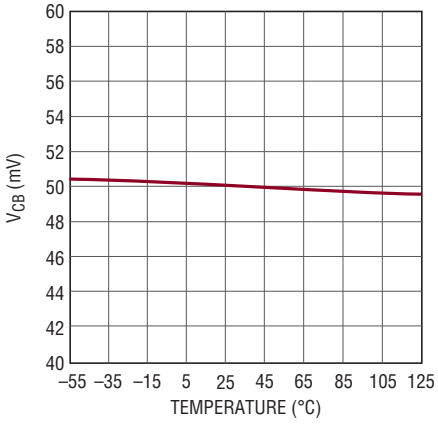
4252B12 G05

Undervoltage Lockout Hysteresis V_{LKH} vs Temperature



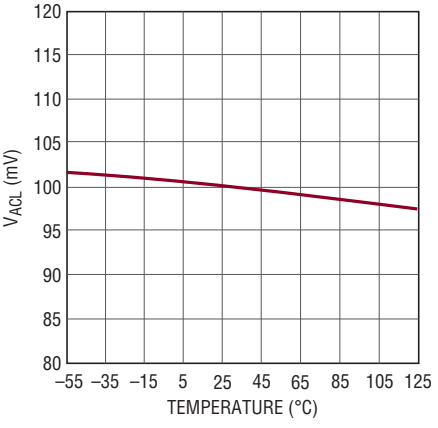
4252B12 G06

Circuit Breaker Current Limit Voltage V_{CB} vs Temperature



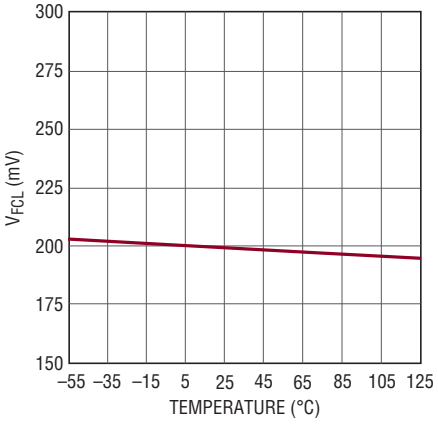
4252B12 G07

Analog Current Limit Voltage V_{ACL} vs Temperature



4252B12 G08

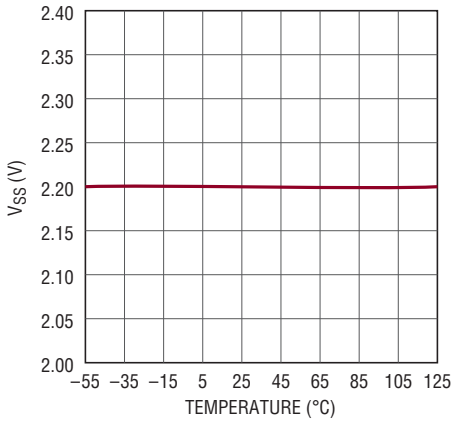
Fast Current Limit Voltage V_{FCL} vs Temperature



4252B12 G09

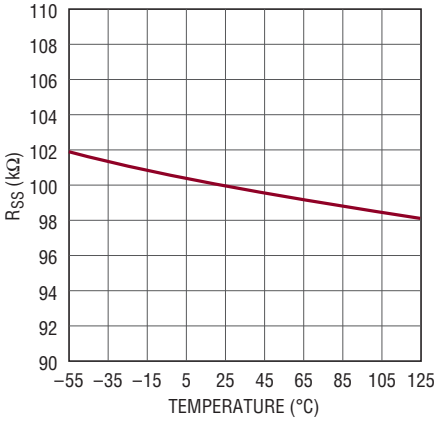
TYPICAL PERFORMANCE CHARACTERISTICS

V_{SS} vs Temperature



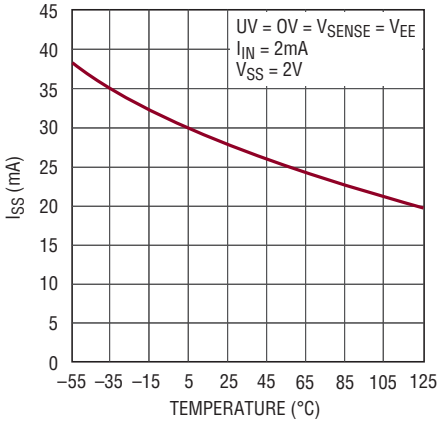
4252B12 G10

R_{SS} vs Temperature



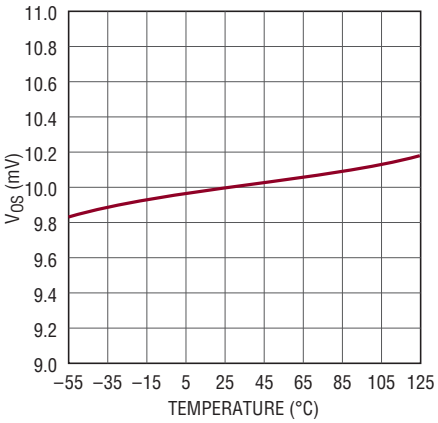
4252B12 G11

I_{SS} (Sinking) vs Temperature



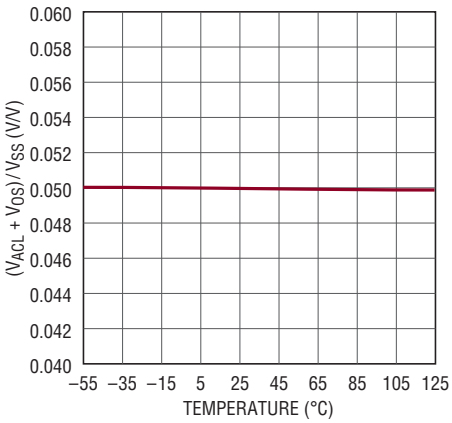
4252B12 G12

V_{OS} vs Temperature



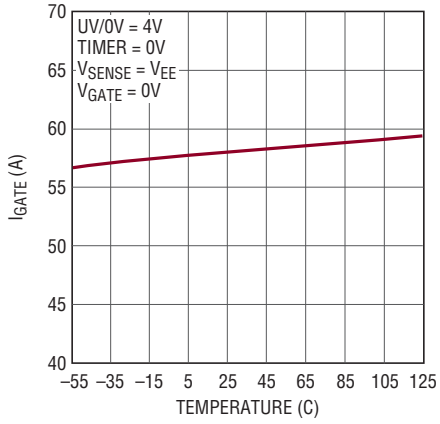
4252B12 G13

$(V_{ACL} + V_{OS})/V_{SS}$ vs Temperature



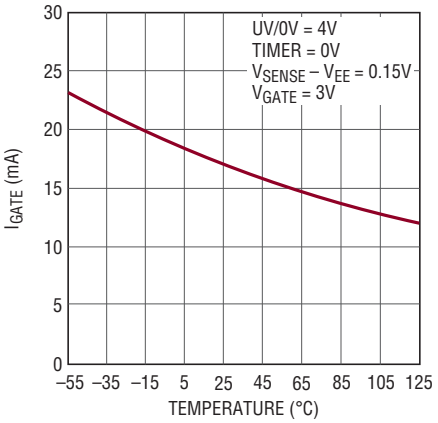
4252B12 G14

I_{GATE} (Sourcing) vs Temperature



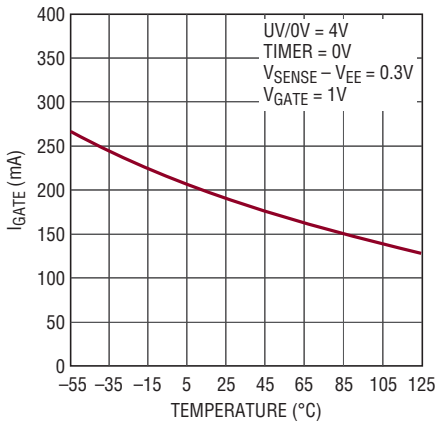
4252B12 G15

I_{GATE} (ACL, Sinking) vs Temperature



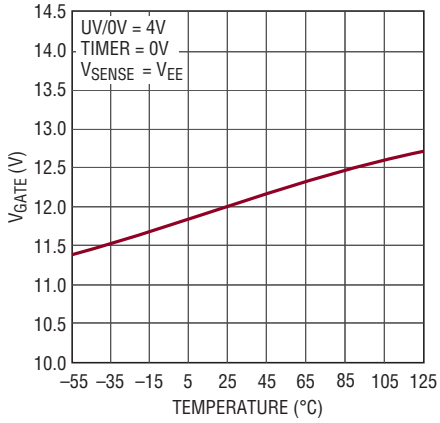
4252B12 G16

I_{GATE} (FCL, Sinking) vs Temperature



4252B12 G17

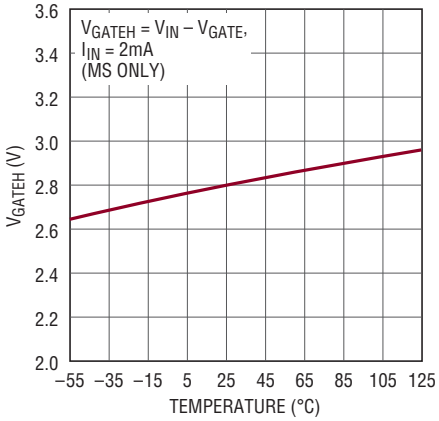
V_{GATE} vs Temperature



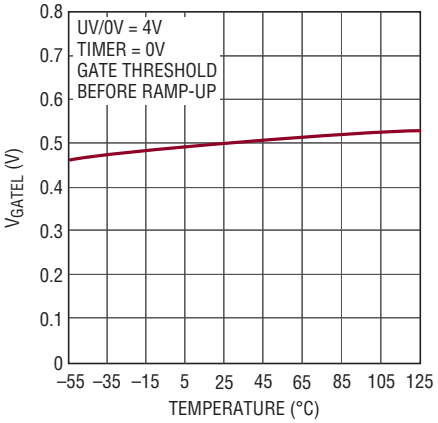
4252B12 G18

TYPICAL PERFORMANCE CHARACTERISTICS

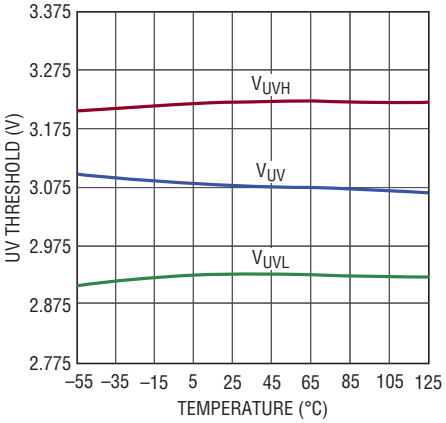
V_{GATEH} vs Temperature



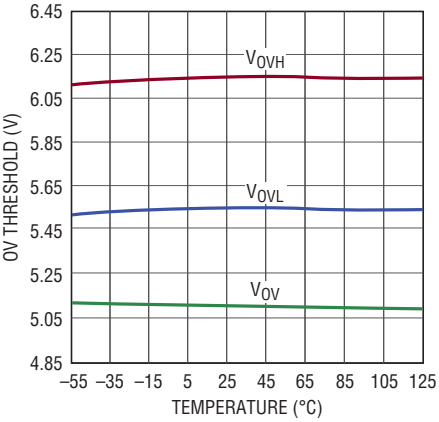
V_{GATEL} vs Temperature



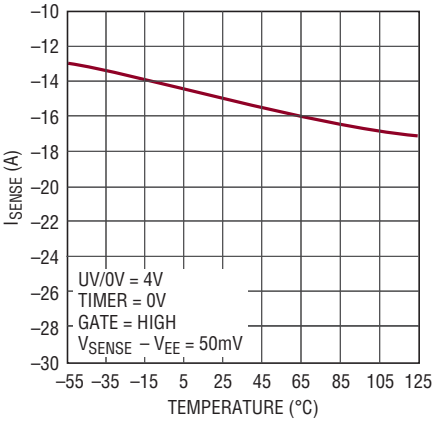
UV Threshold vs Temperature



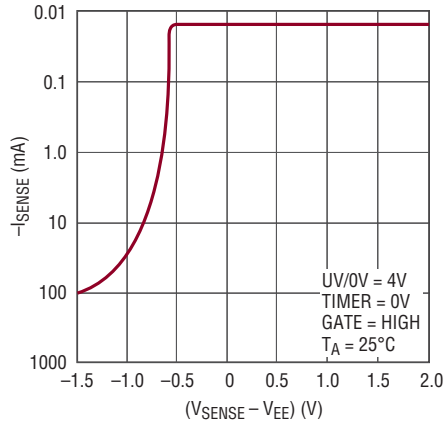
OV Threshold vs Temperature



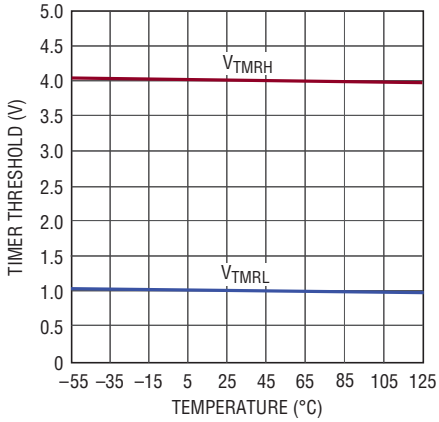
I_{SENSE} vs Temperature



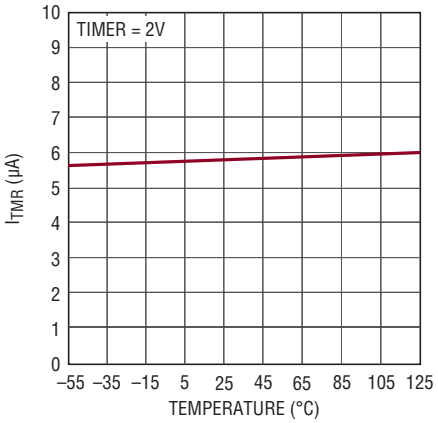
I_{SENSE} vs ($V_{SENSE} – V_{EE}$)



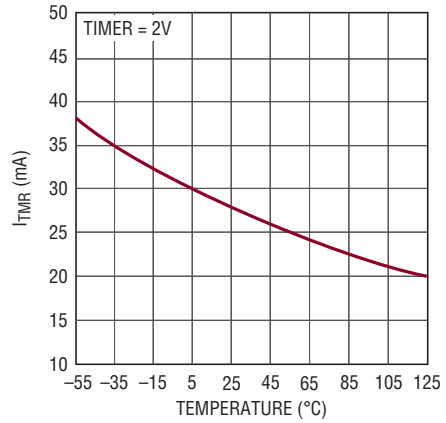
TIMER Threshold vs Temperature



I_{TMR} (Initial Cycle, Sourcing) vs Temperature

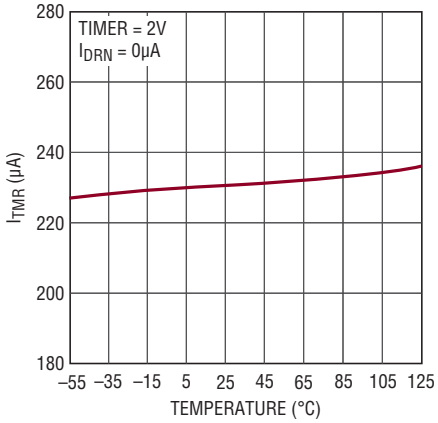


I_{TMR} (Initial Cycle, Sinking) vs Temperature

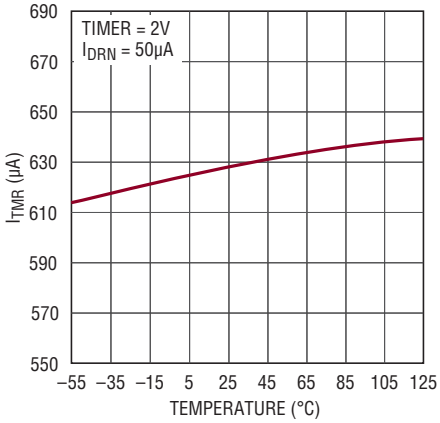


TYPICAL PERFORMANCE CHARACTERISTICS

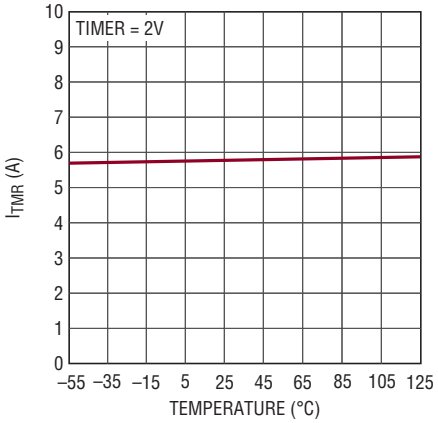
I_{TMR} (Circuit Breaker, Sourcing) vs Temperature



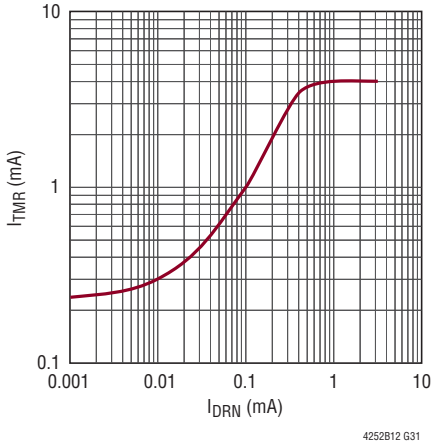
I_{TMR} (Circuit Breaker, I_{DRN} = 50µA, Sourcing) vs Temperature



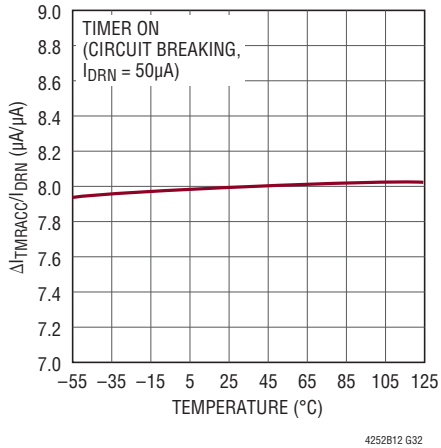
I_{TMR} (Cooling Cycle, Sinking) vs Temperature



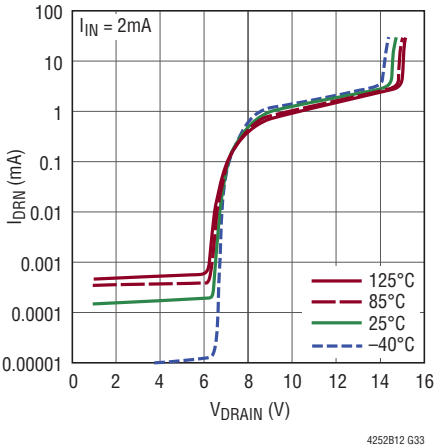
I_{TMR} vs I_{DRN}



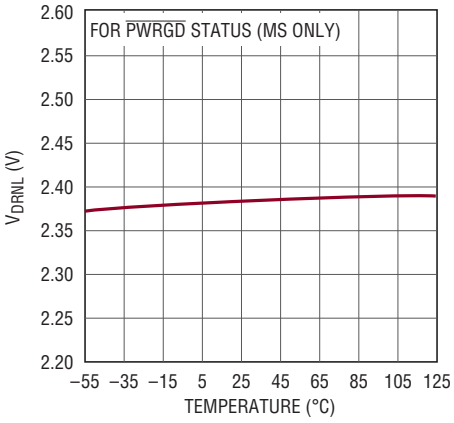
$\Delta I_{TMRACC}/\Delta I_{DRN}$ vs Temperature



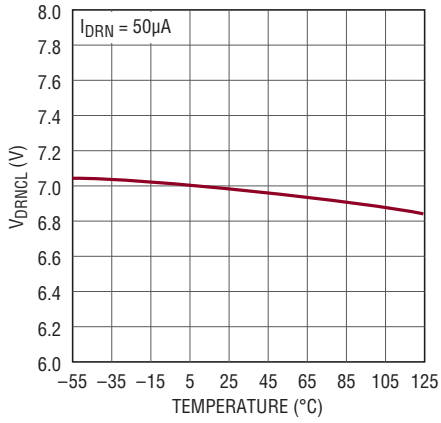
I_{DRN} vs V_{DRAIN}



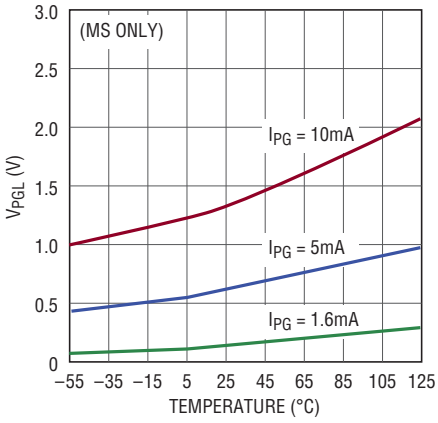
V_{DRNL} vs Temperature



V_{DRNCL} vs Temperature

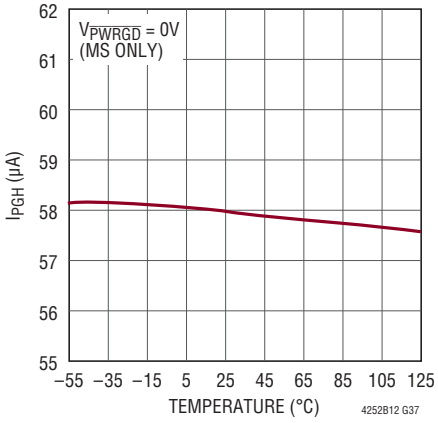


V_{PGL} vs Temperature

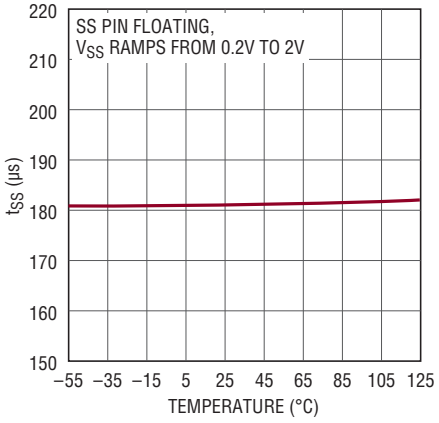


TYPICAL PERFORMANCE CHARACTERISTICS

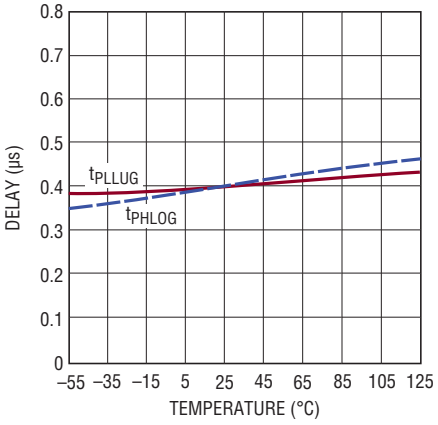
I_{PGH} vs Temperature



t_{SS} vs Temperature



t_{PLLUG} and t_{PHLOG} vs Temperature



PIN FUNCTIONS (MS/MS8)

V_{IN} (Pin 1/Pin 1): Positive Supply Input. Connect this pin to the positive side of the supply through a dropping resistor. A shunt regulator clamps V_{IN} at 13V. An internal undervoltage lockout (UVLO) circuit holds GATE low until the V_{IN} pin is greater than V_{LKO}, overriding UV and OV. If UV is high, OV is low and V_{IN} comes out of UVLO, TIMER starts an initial timing cycle before initiating a GATE ramp-up. If V_{IN} drops below approximately 8.2V, GATE pulls low immediately.

$\overline{PWRGD}$ (Pin 2/Not Available): Power Good Status Output (MS only). At start-up, $\overline{PWRGD}$ latches low if DRAIN is below 2.385V and GATE is within 2.8V of V_{IN}. $\overline{PWRGD}$ status is reset by UV, V_{IN} (UVLO) or a circuit breaker fault timeout. This pin is internally pulled high by a 58µA current source.

SS (Pin 3/Pin 2): Soft-Start Pin. This pin is used to ramp inrush current during start up, thereby effecting control over di/dt. A 20x attenuated version of the SS pin voltage is presented to the current limit amplifier. This attenuated voltage limits the MOSFET's drain current through the sense resistor during the soft-start current limiting. At the beginning of a start-up cycle, the SS capacitor (C_{SS}) is ramped by a 22µA (28µA for the LTC4252C) current source. The GATE pin is held low until SS exceeds 20 • V_{OS} = 0.2V. SS is internally shunted by a 100k resistor (R_{SS}) which limits the SS pin voltage to 2.2V (50k resistor and 1.4V for the LTC4252C). This corresponds to an analog current limit SENSE voltage of 100mV (60mV for the LTC4252C). If the SS capacitor is omitted, the SS pin ramps up in about 180µs. The SS pin is pulled low under any of the following conditions: in UVLO, in an undervoltage condition, in an overvoltage condition, during the initial timing cycle or when the circuit breaker fault times out.

SENSE (Pin 4/Pin 3): Circuit Breaker/Current Limit Sense Pin. Load current is monitored by a sense resistor R_S connected between SENSE and V_{EE}, and controlled in three steps. If SENSE exceeds V_{CB} (50mV), the circuit breaker comparator activates a (230µA + 8 • I_{DRN}) TIMER pull-up current. If SENSE exceeds V_{ACL}, the analog current limit amplifier pulls GATE down to regulate the MOSFET current at V_{ACL}/R_S. In the event of a catastrophic short-circuit, SENSE may overshoot. If SENSE reaches V_{FCL} (200mV), the fast current limit comparator pulls GATE low with a strong pull-down. To disable the circuit breaker and current limit functions, connect SENSE to V_{EE}.

PIN FUNCTIONS (MS/MS8)

V_{EE} (Pin 5/Pin 4): Negative Supply Voltage Input. Connect this pin to the negative side of the power supply.

GATE (Pin 6/Pin 5): N-Channel MOSFET Gate Drive Output. This pin is pulled high by a 58µA current source. GATE is pulled low by invalid conditions at V_{IN} (UVLO), UV, OV, or a circuit breaker fault timeout. GATE is actively servoed to control the fault current as measured at SENSE. A compensation capacitor at GATE stabilizes this loop. A comparator monitors GATE to ensure that it is low before allowing an initial timing cycle, GATE ramp-up after an overvoltage event or restart after a current limit fault. During GATE start-up, a second comparator detects if GATE is within 2.8V of V_{IN} before $\overline{PWRGD}$ is set (MS package only).

DRAIN (Pin 7/Pin 6): Drain Sense Input. Connecting an external resistor, R_D, between this pin and the MOSFET's drain (V_{OUT}) allows voltage sensing below 6.15V (5V for LTC4252C) and current feedback to TIMER. A comparator detects if DRAIN is below 2.385V and together with the GATE high comparator sets the $\overline{PWRGD}$ flag. If V_{OUT} is above V_{DRNCL}, DRAIN clamps at approximately V_{DRNCL}. The current through R_D is internally multiplied by 8 and added to TIMER's 230µA pull-up current during a circuit breaker fault cycle. This reduces the fault time and MOSFET heating.

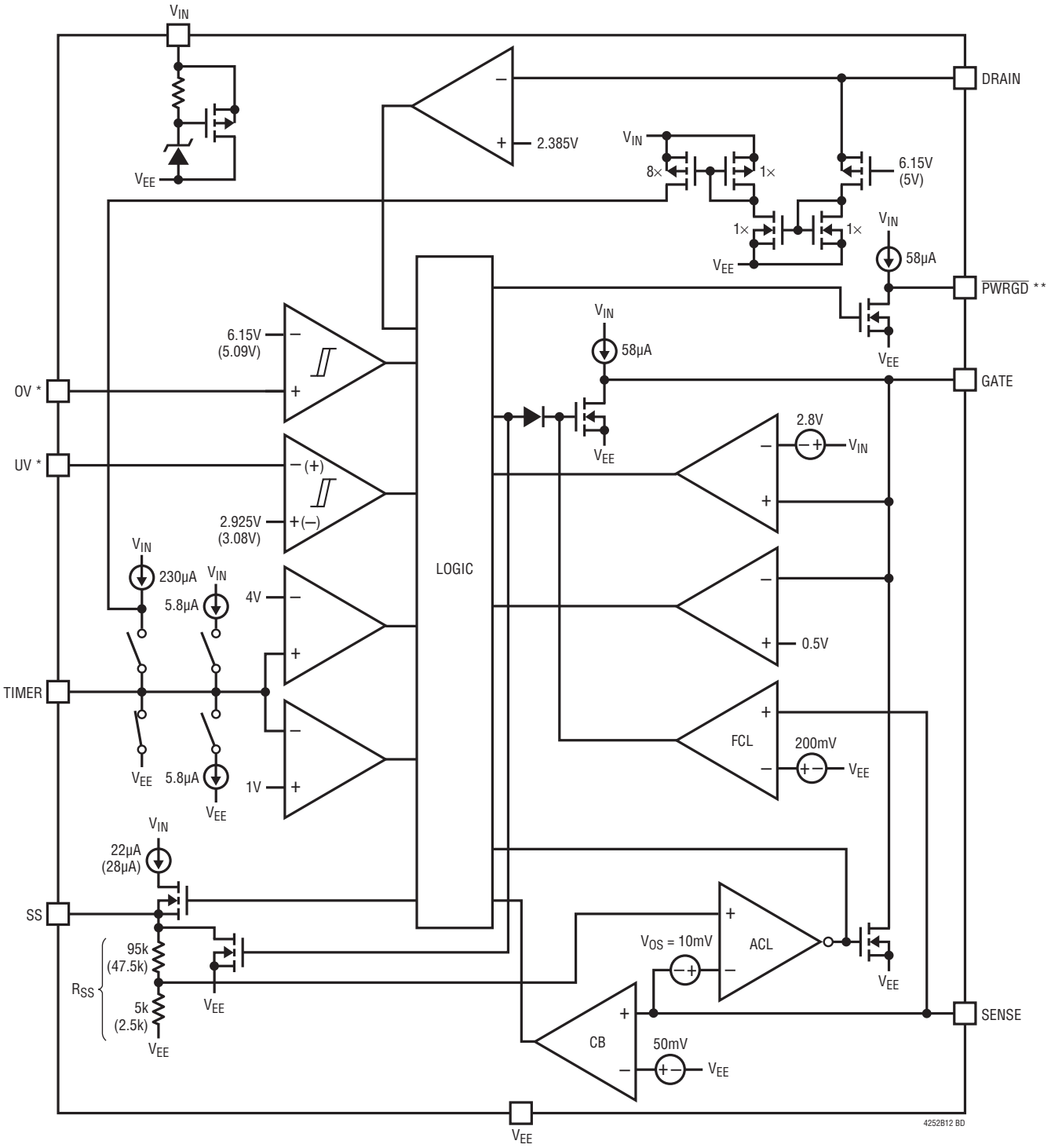
OV (Pin 8/Pin 7): Overvoltage Input. The active high threshold at the OV pin is set at 6.15V with 0.6V hysteresis. If OV > 6.15V, GATE pulls low. When OV returns below 5.55V, GATE start-up begins without an initial timing cycle. The LTC4252C OV pin is set at 5.09V with 102mV hysteresis. If OV > 5.09V, GATE pulls low. When OV returns below 4.988V, GATE start-up begins without an initial timing cycle. If an overvoltage condition occurs in the middle of an initial timing cycle, the initial timing cycle is restarted after the overvoltage condition goes away. An overvoltage condition does not reset the $\overline{PWRGD}$ flag. The internal UVLO at V_{IN} always overrides OV. A 1nF to 10nF capacitor at OV prevents transients and switching noise from affecting the OV thresholds and prevents glitches at the GATE pin.

UV (Pin 9/Pin 7): Undervoltage Input. The active low threshold at the UV pin is set at 2.925V with 0.3V hysteresis. If UV < 2.925V, $\overline{PWRGD}$ pulls high, both GATE and TIMER pull low. If UV rises above 3.225V, this initiates an initial timing cycle followed by GATE start-up. The LTC4252C UV pin is set at 3.08V with 324mV hysteresis. If UV < 2.756V, $\overline{PWRGD}$ pulls high, both GATE and TIMER pull low. If UV rises above 3.08V, this initiates an initial timing cycle followed by GATE start-up. The internal UVLO at V_{IN} always overrides UV. A low at UV resets an internal fault latch. A 1nF to 10nF capacitor at UV prevents transients and switching noise from affecting the UV thresholds and prevents glitches at the GATE pin.

TIMER (Pin 10/Pin 8): Timer Input. TIMER is used to generate an initial timing delay at start-up and to delay shutdown in the event of an output overload (circuit breaker fault). TIMER starts an initial timing cycle when the following conditions are met: UV is high, OV is low, V_{IN} clears UVLO, TIMER pin is low, GATE is lower than V_{GATEL}, SS < 0.2V, and $V_{SENSE} - V_{EE} < V_{CB}$. A pull-up current of 5.8µA then charges C_T, generating a time delay. If C_T charges to V_{TMRH} (4V), the timing cycle terminates, TIMER quickly pulls low and GATE is activated.

If SENSE exceeds 50mV while GATE is high, a circuit breaker cycle begins with a 230µA pull-up current charging C_T. If DRAIN is approximately 7V (6V for LTC4252C) during this cycle, the timer pull-up has an additional current of 8 • I_{DRN}. If SENSE drops below 50mV before TIMER reaches 4V, a 5.8µA pull-down current slowly discharges the C_T. In the event that C_T eventually integrates up to the V_{TMRH} threshold, the circuit breaker trips, GATE quickly pulls low and $\overline{PWRGD}$ pulls high. The LTC4252-1 TIMER pin latches high with a 5.8µA pull-up source. This latched fault is cleared by either pulling TIMER low with an external device or by pulling UV below V_{UVLO}. The LTC4252-2 starts a shutdown cooling cycle following an overcurrent fault. This cycle consists of 4 discharging ramps and 3 charging ramps. The charging and discharging currents are 5.8µA and TIMER ramps between its 1V and 4V thresholds. At the completion of a shutdown cooling cycle, the LTC4252-2 attempts a start-up cycle.

BLOCK DIAGRAM



*OV AND UV ARE TIED TOGETHER ON THE MS8 PACKAGE. OV AND UV ARE SEPARATE PINS ON THE MS PACKAGE
** ONLY AVAILABLE IN THE MS PACKAGE
FOR COMPONENTS, CURRENT AND VOLTAGE WITH TWO VALUES, VALUES IN PARENTHESES REFER TO THE LTC4252C. VALUES WITHOUT PARENTHESES REFER TO THE LTC4252B

OPERATION

Hot Circuit Insertion

When circuit boards are inserted into a live backplane, the supply bypass capacitors can draw huge transient currents from the power bus as they charge. The flow of current damages the connector pins and glitches the power bus, causing other boards in the system to reset. The LTC4252 is designed to turn on a circuit board supply in a controlled manner, allowing insertion or removal without glitches or connector damage.

Initial Start-Up

The LTC4252 resides on a removable circuit board and controls the path between the connector and load or power conversion circuitry with an external MOSFET switch (see Figure 1). Both inrush control and short-circuit protection are provided by the MOSFET.

A detailed schematic for the LTC4252C is shown in Figure 2. –48V and –48RTN receive power through the longest connector pins and are the first to connect when the board is inserted. The GATE pin holds the MOSFET off during this time. UV and OV determine whether or not the MOSFET should be turned on based upon internal high accuracy thresholds and an external divider. UV and OV do double duty by also monitoring whether or not the connector is seated. The top of the divider detects –48RTN by way of a short connector pin that is the last to mate during the insertion sequence.

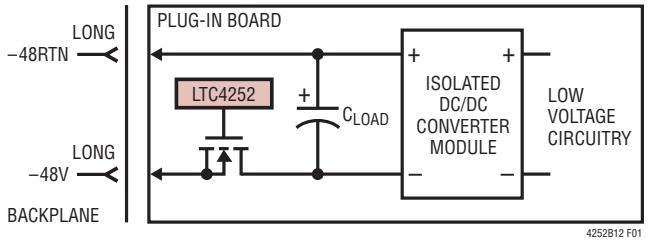


Figure 1. Basic LTC4252 Hot Swap Topology

Interlock Conditions

A start-up sequence commences once these "interlock" conditions are met.

1. The input voltage V_{IN} exceeds V_{LKO} (UVLO).
2. The voltage at UV > V_{UVHI}.
3. The voltage at OV < V_{OVLO}.
4. The (SENSE – V_{EE}) voltage is < 50mV (V_{CB}).
5. The voltage at SS is < 0.2V (20 • V_{OS}).
6. The voltage on the TIMER capacitor (C_T) is < 1V (V_{TMRL}).
7. The voltage at GATE is < 0.5V (V_{GATEL}).

The first three conditions are continuously monitored and the latter four are checked prior to initial timing or GATE ramp-up. Upon exiting an OV condition, the TIMER pin voltage requirement is inhibited. Details are described in the Applications Information, Timing Waveforms section.

TIMER begins the start-up sequence by sourcing 5.8µA into C_T. If V_{IN}, UV or OV falls out of range, the start-up cycle stops and TIMER discharges C_T to less than 1V, then waits until the aforementioned conditions are once again met. If C_T successfully charges to 4V, TIMER pulls low and both SS and GATE pins are released. GATE sources 58µA (I_{GATE}), charging the MOSFET gate and associated capacitance. The SS voltage ramp limits V_{SENSE} to control the inrush current. $\overline{PWRGD}$ pulls active low when GATE is within 2.8V of V_{IN} and DRAIN is lower than V_{DRNL}.

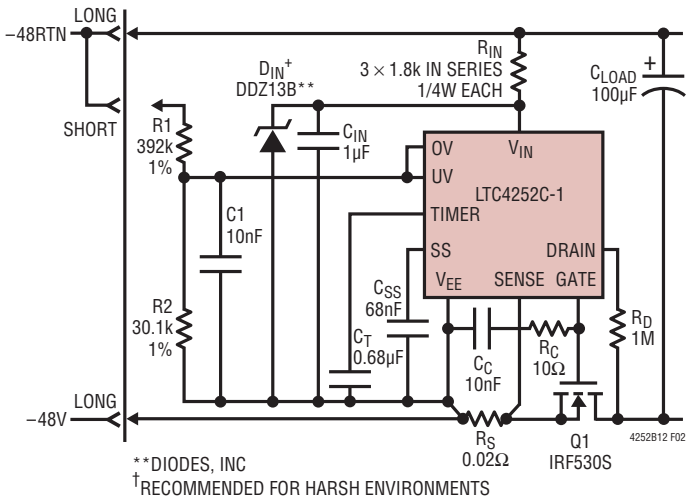


Figure 2. –48V, 2.5A Hot Swap Controller

OPERATION

Two modes of operation are possible during the time the MOSFET is first turning on, depending on the values of external components, MOSFET characteristics and nominal design current. One possibility is that the MOSFET will turn on gradually so that the inrush into the load capacitance remains a low value. The output will simply ramp to –48V and the LTC4252 will fully enhance the MOSFET. A second possibility is that the load current exceeds the soft-start current limit threshold of $[V_{SS}(t)/20 – V_{OS}]/R_S$. In this case the LTC4252 will ramp the output by sourcing soft-start limited current into the load capacitance. If the soft-start voltage is below 1.2V, the circuit breaker TIMER is held low. Above 1.2V, TIMER ramps up. It is important to set the timer delay so that, regardless of which start-up mode is used, the TIMER ramp is less than one circuit breaker delay time. If this condition is not met, the LTC4252-1 may shut down after one circuit breaker delay time whereas the LTC4252-2 may continue to autoretry.

Board Removal

If the board is withdrawn from the card cage, the UV and OV divider is the first to lose connection. This shuts off the MOSFET and commutates the flow of current in the connector. When the power pins subsequently separate, there is no arcing.

Current Control

Three levels of protection handle short-circuit and overload conditions. Load current is monitored by SENSE and resistor R_S. There are three distinct thresholds at SENSE: 50mV for a timed circuit breaker function; 100mV for an analog current limit loop (60mV for the LTC4252C); and 200mV for a fast, feedforward comparator which limits peak current in the event of a catastrophic short-circuit.

If, owing to an output overload, the voltage drop across R_S exceeds 50mV, TIMER sources 230µA into C_T. C_T eventually charges to a 4V threshold and the LTC4252 shuts off. If the overload goes away before C_T reaches 4V and SENSE measures less than 50mV, C_T slowly discharges (5.8µA). In this way the LTC4252's circuit breaker function responds to low duty cycle overloads and accounts for fast heating and slow cooling characteristics of the MOSFET.

Higher overloads are handled by an analog current limit loop. If the drop across R_S reaches V_{ACL}, the current limiting loop servos the MOSFET gate and maintains a constant output current of V_{ACL}/R_S. In current limit mode, V_{OUT} typically rises and this increases MOSFET heating. If $V_{OUT} > V_{DRNCL}$, connecting an external resistor, R_D, between V_{OUT} and DRAIN allows the fault timing cycle to be shortened by accelerating the charging of the TIMER capacitor. The TIMER pull-up current is increased by 8 • I_{DRN}. Note that because SENSE > 50mV, TIMER charges C_T during this time and the LTC4252 will eventually shut down.

Low impedance failures on the load side of the LTC4252 coupled with 48V or more driving potential can produce current slew rates well in excess of 50A/µs. Under these conditions, overshoot is inevitable. A fast SENSE comparator with a threshold of 200mV detects overshoot and pulls GATE low much harder and hence much faster than the weaker current limit loop. The V_{ACL}/R_S current limit loop then takes over and servos the current as previously described. As before, TIMER runs and shuts down the LTC4252 when C_T reaches 4V.

If C_T reaches 4V, the LTC4252-1 latches off with a 5.8µA pull-up current source whereas the LTC4252-2 starts a shutdown cooling cycle. The LTC4252-1 circuit breaker latch is reset by either pulling UV momentarily low or dropping the input voltage V_{IN} below the internal UVLO threshold or pulling TIMER momentarily low with a switch. The LTC4252-2 retries after its shutdown cooling cycle.

Although short-circuits are the most obvious fault type, several operating conditions may invoke overcurrent protection. Noise spikes from the backplane or load, input steps caused by the connection of a second, higher voltage supply, transient currents caused by faults on adjacent circuit boards sharing the same power bus or the insertion of non-hot-swappable products could cause higher than anticipated input current and temporary detection of an overcurrent condition. The action of TIMER and C_T rejects these events allowing the LTC4252 to "ride out" temporary overloads and disturbances that could trip a simple current comparator and, in some cases, blow a fuse.

APPLICATIONS INFORMATION

SHUNT REGULATOR

A fast responding shunt regulator clamps the V_{IN} pin to 13V (VZ). Power is derived from –48RTN by an external current limiting resistor, R_{IN}. A 1µF decoupling capacitor, C_{IN} filters supply transients and contributes a short delay at start-up.

To meet creepage requirements R_{IN} may be split into two or more series connected units. This introduces a wider total spacing than is possible with a single component while at the same time ballasting the potential across the gap under each resistor. The LTC4252 is fundamentally a low voltage device that operates with –48V as its reference ground. To further protect against arc discharge into its pins, the area in and around the LTC4252 and all associated components should be free of any other planes such as chassis ground, return, or secondary-side power and ground planes.

V_{IN} may be biased with additional current up to 30mA to accommodate external loading such as the $\overline{PWRGD}$ optocoupler shown in Figure 23. As an alternative to running higher current, simply buffer V_{IN} with an emitter follower as shown in Figure 3. Another method shown in Figure 19 cascodes the $\overline{PWRGD}$ output.

V_{IN} is rated handle 30mA within the thermal limits of the package, and is tested to survive a 100µs, 100mA pulse. To protect V_{IN} against damage from higher amplitude spikes, clamp V_{IN} to V_{EE} with a 13V Zener diode. Star connect V_{EE} and all V_{EE}-referred components to the sense resistor Kelvin terminal as illustrated in Figure 3, keeping trace lengths between V_{IN}, C_{IN}, D_{IN} and V_{EE} as short as possible.

INTERNAL UNDERVOLTAGE LOCKOUT (UVLO)

A hysteretic comparator, UVLO, monitors V_{IN} for undervoltage. The thresholds are defined by V_{LKO} and its hysteresis, V_{LKH}. When V_{IN} rises above V_{LKO} the chip is enabled; below (V_{LKO} – V_{LKH}) it is disabled and GATE is pulled low. The UVLO function at V_{IN} should not be confused with the UV/OV pin(s). These are completely separate functions.

UV/OV COMPARATORS (LTC4252B)

An UV hysteretic comparator detects undervoltage conditions at the UV pin, with the following thresholds:

UV low-to-high (V_{UVHI}) = 3.225V

UV high-to-low (V_{UVLO}) = 2.925V

An OV hysteretic comparator detects overvoltage conditions at the OV pin, with the following thresholds:

OV low-to-high (V_{OVHI}) = 6.150V

OV high-to-low (V_{OVLO}) = 5.550V

The UV and OV trip point ratio is designed to match the standard telecom operating range of 43V to 82V when connected together as in the typical application. A divider (R1, R2) is used to scale the supply voltage. Using R1 = 402k

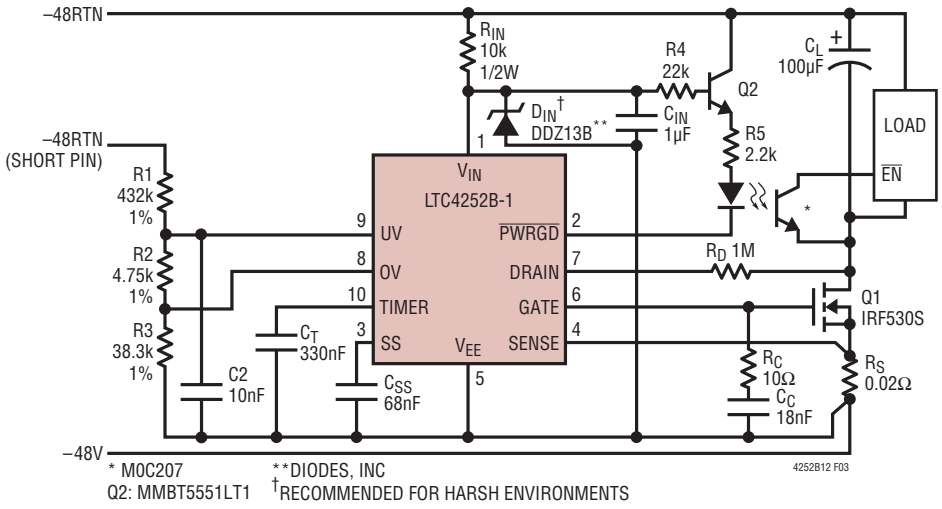


Figure 3. –48V/2.5A Application with Different Input Operating Range

APPLICATIONS INFORMATION

and R2 = 32.4k gives a typical operating range of 43.2V to 82.5V. The undervoltage shutdown and overvoltage recovery thresholds are then 39.2V and 74.4V. 1% divider resistors are recommended to preserve threshold accuracy.

The R1-R2 divider values shown in the Typical Application set a standing current of slightly more than 100µA and define an impedance at UV/OV of 30kΩ. In most applications, 30kΩ impedance coupled with 300mV UV hysteresis makes the LTC4252B insensitive to noise. If more noise immunity is desired, add a 1nF to 10nF filter capacitor from UV/OV to V_{EE}.

Separate UV and OV pins are available in the 10-pin MS package and can be used for a different operating range such as 35.5V to 76V as shown in Figure 3. Other combinations are possible with different resistor arrangements.

UV/OV COMPARATORS (LTC4252C)

A UV hysteretic comparator detects undervoltage conditions at the UV pin, with the following thresholds:

UV low-to-high (V_{UV}) = 3.08V

UV high-to-low ($V_{UV} – V_{UVHST}$) = 2.756V

An OV hysteretic comparator detects overvoltage conditions at the OV pin, with the following thresholds:

OV low-to-high (V_{OV}) = 5.09V

OV high-to-low ($V_{OV} – V_{OVHST}$) = 4.988V

The UV and OV trip point ratio is designed to match the standard telecom operating range of 43V to 71V when connected together as in Figure 2. A divider (R1, R2) is used to scale the supply voltage. Using R1 = 390k and R2 = 30.1k gives a typical operating range of 43V to 71V. The undervoltage shutdown and overvoltage recovery thresholds are then 38.5V and 69.6V respectively. 1% divider resistors are recommended to preserve threshold accuracy.

The R1-R2 divider values shown in Figure 2 set a standing current of slightly more than 100µA and define an impedance at UV/OV of 28kΩ. In most applications, 28kΩ impedance coupled with 324mV UV hysteresis makes the LTC4252C insensitive to noise. If more noise immunity is desired, add a 1nF to 10nF filter capacitor from UV/OV to V_{EE}.

The UV and OV pins can be used for a wider operating range such as 35.5V to 76V as shown in Figure 4. Other combinations are possible with different resistor arrangements.

UV/OV OPERATION

A low input to the UV comparator will reset the chip and pull the GATE and TIMER pins low. A low-to-high UV transition will initiate an initial timing sequence if the other interlock

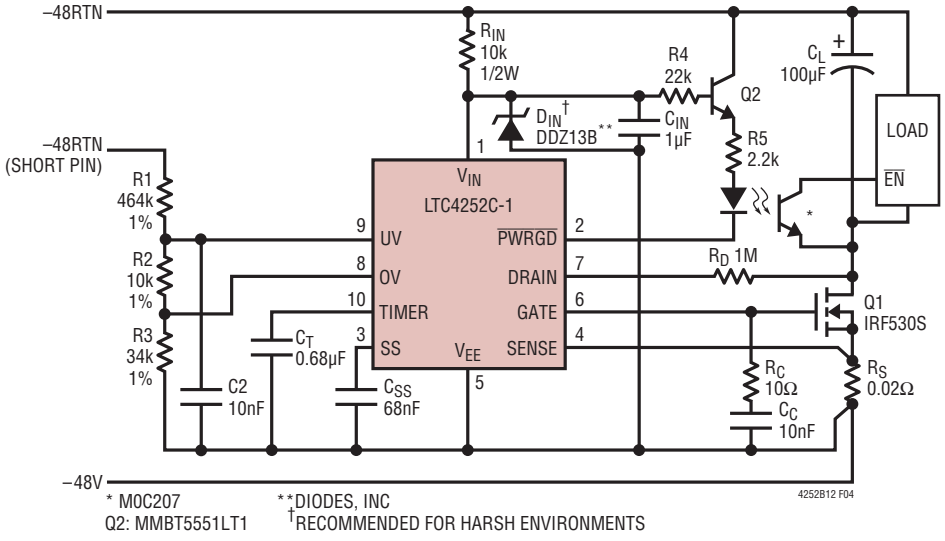


Figure 4. –48V/2.5A Application with Wider Input Operating Range

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conditions are met. A high-to-low transition in the UV comparator immediately shuts down the LTC4252, pulls the MOSFET gate low and resets the latched $\overline{PWRGD}$ high.

Overvoltage conditions detected by the OV comparator will also pull GATE low, thereby shutting down the load. However, it will not reset the circuit breaker TIMER, $\overline{PWRGD}$ flag or shutdown cooling timer. Returning the supply voltage to an acceptable range restarts the GATE pin if all the interlock conditions except TIMER are met. Only during the initial timing cycle does an OV condition reset the TIMER.

DRAIN

Connecting an external resistor, R_D, to the dual function DRAIN pin allows V_{OUT} sensing* without it being damaged by large voltage transients. Below 5V, negligible pin leakage allows a DRAIN low comparator to detect V_{OUT} less than 2.385V (V_{DRNL}). This condition, together with the GATE low comparator, sets the $\overline{PWRGD}$ flag.

If $V_{OUT} > V_{DRNCL}$, the DRAIN pin is clamped at about V_{DRNCL} and the current flowing in R_D is given by:

$$I_{DRN} \approx \frac{V_{OUT} - V_{DRNCL}}{R_D} \quad (1)$$

This current is scaled up 8 times during a circuit breaker fault and is added to the nominal 230µA TIMER current. This accelerates the fault TIMER pull-up when the MOSFET's drain-source voltage exceeds V_{DRNCL} and effectively shortens the MOSFET heating duration.

TIMER

The operation of the TIMER pin is somewhat complex as it handles several key functions. A capacitor C_T is used at TIMER to provide timing for the LTC4252. Four different charging and discharging modes are available at TIMER:

1) A 5.8µA slow charge; initial timing and shutdown cooling delay.

2) A (230µA + 8 • I_{DRN}) fast charge; circuit breaker delay.

3) A 5.8µA slow discharge; circuit breaker "cool off" and shutdown cooling.

4) Low impedance switch; resets the TIMER capacitor after an initial timing delay, in UVLO, in UV and in OV during initial timing.

For initial start-up, the 5.8µA pull-up is used. The low impedance switch is turned off and the 5.8µA current source is enabled when the interlock conditions are met. C_T charges to 4V in a time period given by:

$$t = \frac{4V \bullet C_T}{5.8\mu A} \quad (2)$$

When C_T reaches 4V (V_{TMRH}), the low impedance switch turns on and discharges C_T. A GATE start-up cycle begins and both SS and GATE are released.

CIRCUIT BREAKER TIMER OPERATION

If the SENSE pin detects more than a 50mV drop across R_S, the TIMER pin charges C_T with (230µA + 8 • I_{DRN}). If C_T charges to 4V, the GATE pin pulls low and the LTC4252-1 latches off while the LTC4252-2 starts a shutdown cooling cycle. The LTC4252-1 remains latched off until the UV pin is momentarily pulsed low or TIMER is momentarily discharged low by an external switch or V_{IN} dips below UVLO and is then restored. The circuit breaker timeout period is given by:

$$t = \frac{4V \bullet C_T}{230\mu A + 8 \bullet I_{DRN}} \quad (3)$$

If $V_{OUT} < 5V$, an internal PMOS device isolates any DRAIN pin leakage current, making I_{DRN} = 0µA in Equation (3). If $V_{OUT} > V_{DRNCL}$ during the circuit breaker fault period, the charging of C_T accelerates by 8 • I_{DRN} of Equation (1).

Intermittent overloads may exceed the 50mV threshold at SENSE, but, if their duration is sufficiently short, TIMER will not reach 4V and the LTC4252 will not shut the external MOSFET off. To handle this situation, the TIMER discharges C_T slowly with a 5.8µA pull-down whenever the SENSE voltage is less than 50mV. Therefore, any intermittent overload with $V_{OUT} > 5V$ and an aggregate duty cycle of

*V_{OUT} as viewed by the MOSFET; i.e., V_{DS}.

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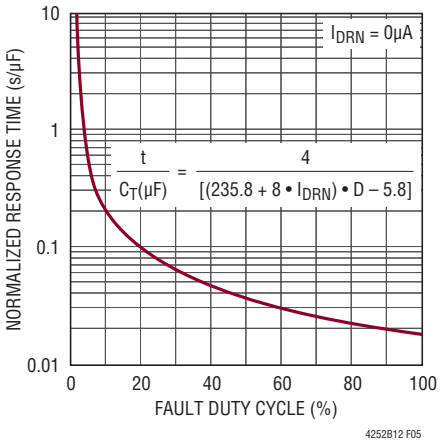

Figure 5. Circuit-Breaker Response Time

2.5% or more will eventually trip the circuit breaker and shut down the LTC4252. Figure 5 shows the circuit breaker response time in seconds normalized to 1µF for I_{DRN} = 0µA. The asymmetric charging and discharging of C_T is a fair gauge of MOSFET heating.

The normalized circuit response time is estimated by

$$\frac{t}{C_T(\mu F)} = \frac{4}{\left[\left(235.8+8\bullet I_{DRN}\right)\bullet D-5.8\right]} \quad (4)$$

SHUTDOWN COOLING CYCLE

For the LTC4252-1 (latchoff version), TIMER latches high with a 5.8µA pull-up after the circuit breaker fault TIMER reaches 4V. For the LTC4252-2 (automatic retry version), a shutdown cooling cycle begins if TIMER reaches the 4V threshold. TIMER starts with a 5.8µA pull-down until it reaches the 1V threshold. Then, the 5.8µA pull-up turns back on until TIMER reaches the 4V threshold. Four 5.8µA pull-down cycles and three 5.8µA pull-up cycles occur between the 1V and 4V thresholds, creating a time interval given by:

$$t_{SHUTDOWN} = \frac{7\bullet 3V\bullet C_T}{5.8\mu A} \quad (5)$$

At the 1V threshold of the last pull-down cycle, a GATE ramp-up is attempted.

SOFT-START

Soft-start limits the inrush current profile during GATE start-up. Unduly long soft-start intervals can exceed the MOSFET's SOA rating if powering up into an active load. If SS floats, an internal current source ramps SS from 0V to 2.2V for the LTC4252B or 0V to 1.4V for the LTC4252C in about 230µs. Connecting an external capacitor C_{SS} from SS to ground modifies the ramp to approximate an RC response of:

$$V_{SS}(t) \approx V_{SS}\bullet\left(1-e^{\left(-\frac{t}{R_{SS}\bullet C_{SS}}\right)}\right) \quad (6)$$

An internal resistive divider (95k/5k for the LTC4252B or 47.5k/2.5k for the LTC4252C) scales $V_{SS}(t)$ down by 20 times to give the analog current limit threshold:

$$V_{ACL}(t) = \frac{V_{SS}(t)}{20} - V_{OS} \quad (7)$$

This allows the inrush current to be limited to $V_{ACL}(t)/R_S$. The offset voltage, V_{OS} (10mV), ensures C_{SS} is sufficiently discharged and the ACL amplifier is in current limit before GATE start-up. SS is pulled low under any of the following conditions: in UVLO, in an undervoltage condition, in an overvoltage condition, during the initial timing cycle or when the circuit breaker fault times out.

GATE

GATE is pulled low to V_{EE} under any of the following conditions: in UVLO, in an undervoltage condition, in an overvoltage condition, during the initial timing cycle or when the circuit breaker fault times out. When GATE turns on, a 58µA current source charges the MOSFET gate and any associated external capacitance. V_{IN} limits the gate drive to no more than 14.5V.

Gate-drain capacitance (C_{GD}) feedthrough at the first abrupt application of power can cause a gate-source voltage sufficient to turn on the MOSFET. A unique circuit pulls GATE low with practically no usable voltage at V_{IN}

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and eliminates current spikes at insertion. A large external gate-source capacitor is thus unnecessary for the purpose of compensating C_{GD}. Instead, a smaller value (≥ 10nF) capacitor C_C is adequate. C_C also provides compensation for the analog current limit loop.

GATE has two comparators: the GATE low comparator looks for < 0.5V threshold prior to initial timing or a GATE start-up cycle; the GATE high comparator looks for < 2.8V relative to V_{IN} and, together with the DRAIN low comparator, sets $\overline{PWRGD}$ status during GATE startup.

SENSE

The SENSE pin is monitored by the circuit breaker (CB) comparator, the analog current limit (ACL) amplifier and the fast current limit (FCL) comparator. Each of these three measures the potential of SENSE relative to V_{EE}. When SENSE exceeds 50mV, the CB comparator activates the 230µA TIMER pull-up. At 100mV (60mV for the LTC4252C), the ACL amplifier servos the MOSFET current and, at 200mV, the FCL comparator abruptly pulls GATE low in an attempt to bring the MOSFET current under control. If any of these conditions persists long enough for TIMER to charge C_T to 4V (see Equation 3), the LTC4252 shuts down and pulls GATE low.

If the SENSE pin encounters a voltage greater than V_{ACL}, the ACL amplifier will servo GATE downwards in an attempt to control the MOSFET current. Since GATE overdrives the MOSFET in normal operation, the ACL amplifier needs time to discharge GATE to the threshold of the MOSFET. For a mild overload the ACL amplifier can control the MOSFET current, but in the event of a severe overload the current may overshoot. At SENSE = 200mV the FCL comparator takes over, quickly discharging the GATE pin to near V_{EE} potential. FCL then releases and the ACL amplifier takes over. All the while TIMER is running. The effect of FCL is to add a nonlinear response to the control loop in favor of reducing MOSFET current.

Owing to inductive effects in the system, FCL typically over corrects the current limit loop and GATE undershoots. A zero in the loop (resistor R_C in series with the gate capacitor) helps the ACL amplifier to recover.

SHORT-CIRCUIT OPERATION

Circuit behavior arising from a load side low impedance short is shown in Figure 6 for the LTC4252. Initially, the current overshoots the fast current limit level of V_{SENSE} = 200mV (Trace 2) as the GATE pin works to bring V_{GS} under control (Trace 3). The overshoot glitches the backplane in the negative direction and when the current is reduced to 100mV/R_S, the backplane responds by glitching in the positive direction.

TIMER commences charging C_T (Trace 4) while the analog current limit loop maintains the fault current at 100mV/R_S, which in this case is 5A (Trace 2). Note that the backplane voltage (Trace 1) sags under load. Timer pull-up is accelerated by V_{OUT}. When C_T reaches 4V, GATE turns off, $\overline{PWRGD}$ pulls high, the load current drops to zero and the backplane rings up to over 100V. The transient associated with the GATE turn off can be controlled with a snubber to reduce ringing and a transient voltage suppressor (such as Diodes Inc. SMAT70A) to clip off large spikes. The choice of RC for the snubber is usually done experimentally. The value of the snubber capacitor is usually chosen between 10 to 100 times the MOSFET C_{OSS}. The value of the snubber resistor is typically between 3Ω to 100Ω.

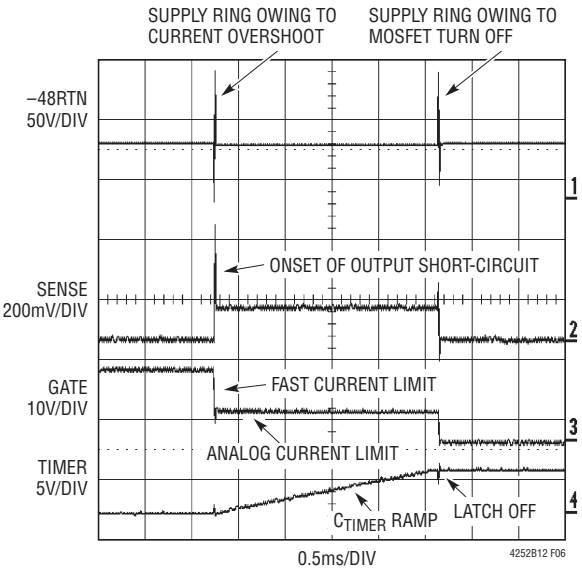

Figure 6. Output Short-Circuit Behavior of LTC4252

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A low impedance short on one card may influence the behavior of others sharing the same backplane. The initial glitch and backplane sag as seen in Figure 6 Trace 1, can rob charge from output capacitors on adjacent cards. When the faulty card shuts down, current flows in to refresh the capacitors. If LTC4252s are used by the other cards, they respond by limiting the inrush current to a value of 100mV/R_S. If C_T is sized correctly, the capacitors will recharge long before C_T times out.

POWER GOOD, $\overline{PWRGD}$

$\overline{PWRGD}$ latches low if GATE charges up to within 2.8V of V_{IN} and DRAIN pulls below V_{DRNL} during start-up. $\overline{PWRGD}$ is reset in UVLO, in a UV condition or if C_T charges up to 4V. An overvoltage condition has no effect on $\overline{PWRGD}$ status. A 58µA current pulls this pin high during reset. Due to voltage transients between the power module and $\overline{PWRGD}$, optoisolation is recommended. This pin provides sufficient drive for an opto-coupler. Figure 19 shows an alternative NPN configuration with a limiting base resistor for the $\overline{PWRGD}$ interface. The module enable input should have protection from the negative input current.

MOSFET SELECTION

The external MOSFET switch must have adequate safe operating area (SOA) to handle short-circuit conditions until TIMER times out. These considerations take precedence over DC current ratings. A MOSFET with adequate SOA for a given application can always handle the required current, but the opposite may not be true. Consult the manufacturer's MOSFET data sheet for safe operating area and effective transient thermal impedance curves.

MOSFET selection is a 3-step process by assuming the absence of a soft-start capacitor. First, R_S is calculated and then the time required to charge the load capacitance is determined. This timing, along with the maximum short-circuit current and maximum input voltage defines an operating point that is checked against the MOSFET's SOA curve.

To begin a design, first specify the required load current and load capacitance, I_L and C_L. The circuit breaker current trip point (V_{CB}/R_S) should be set to accommodate the maximum load current. Note that maximum input current to a DC/DC converter is expected at $V_{SUPPLY(MIN)}$. R_S is given by:

$$R_S = \frac{V_{CB(MIN)}}{I_{L(MAX)}} \quad (8)$$

where $V_{CB(MIN)}$ = 40mV (45mV for LTC4252C) represents the guaranteed minimum circuit breaker threshold.

During the initial charging process, the LTC4252B may operate the MOSFET in current limit, forcing (V_{ACL}) between 80mV to 120mV (V_{ACL} is 54mV to 66mV for LTC4252C) across R_S. The minimum inrush current is given by:

$$I_{INRUSH(MIN)} = \frac{80mV}{R_S} \quad (9)$$

Maximum short-circuit current limit is calculated using the maximum V_{ACL}. This gives

$$I_{SHORTCIRCUIT(MAX)} = \frac{120mV}{R_S} \quad (10)$$

The TIMER capacitor C_T must be selected based on the slowest expected charging rate; otherwise TIMER might time out before the load capacitor is fully charged. A value for C_T is calculated based on the maximum time it takes the load capacitor to charge. That time is given by:

$$t_{CL(CHARGE)} = \frac{C \bullet V}{I} = \frac{C_L \bullet V_{SUPPLY(MAX)}}{I_{INRUSH(MIN)}} \quad (11)$$

The maximum current flowing in the DRAIN pin is given by:

$$I_{DRN(MAX)} = \frac{V_{SUPPLY(MAX)} - V_{DRNCL}}{R_D} \quad (12)$$

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Approximating a linear charging rate as I_{DRN} drops from $I_{DRN(MAX)}$ to zero, the I_{DRN} component in Equation (3) can be approximated with 0.5 • $I_{DRN(MAX)}$. Rearranging equation, TIMER capacitor C_T is given by:

$$C_T = \frac{t_{CL(CHARGE)} \bullet \left(230\mu A + 4 \bullet I_{DRN(MAX)}\right)}{4V} \quad (13)$$

Returning to Equation (3), the TIMER period is calculated and used in conjunction with $V_{SUPPLY(MAX)}$ and $I_{SHORTCIRCUIT(MAX)}$ to check the SOA curves of a prospective MOSFET.

As a numerical design example, consider a 30W load, which requires 1A input current at 36V. If $V_{SUPPLY(MAX)}$ = 72V and C_L = 100µF, R_D = 1MΩ, Equation (8) gives R_S = 40mΩ; Equation (13) gives C_T = 441nF. To account for errors in R_S, C_T, TIMER current (230µA), TIMER threshold (4V), R_D, DRAIN current multiplier and DRAIN voltage clamp (V_{DRNCL}), the calculated value should be multiplied by 1.5, giving the nearest standard value of C_T = 680nF.

If a short-circuit occurs, a current of up to 120mV/40mΩ = 3A will flow in the MOSFET for 5.6ms as dictated by C_T = 680nF in Equation (3). The MOSFET must be selected based on this criterion. The IRF530S can handle 100V and 3A for 10ms and is safe to use in this application.

Computing the maximum soft-start capacitor value during soft-start to a load short is complicated by the nonlinear MOSFET's SOA characteristics and the $R_{SS}C_{SS}$ response. An overly conservative but simple approach begins with the maximum circuit breaker current, given by:

$$I_{CB(MAX)} = \frac{V_{CB(MAX)}}{R_S} \quad (14)$$

where $V_{CB(MAX)}$ = 60mV (55mV for the LTC4252C).

From the SOA curves of a prospective MOSFET, determine the time allowed, $t_{SOA(MAX)}$. C_{SS} is given by:

$$C_{SS} = \frac{t_{SOA(MAX)}}{0.916 \bullet R_{SS}} \quad (15)$$

In the above example, 60mV/40mΩ gives 1.5A. $t_{SOA(MAX)}$ for the IRF530S is 40ms. From Equation (15), C_{SS} = 437nF. Actual board evaluation showed that C_{SS} = 100nF was appropriate. The ratio (R_{SS} • C_{SS}) to $t_{CL(CHARGE)}$ is a good gauge as a large ratio may result in the time-out period expiring. This gauge is determined empirically with board level evaluation.

SUMMARY OF DESIGN FLOW

To summarize the design flow, consider the application shown in Figure 2 with the LTC4252C. It was designed for 80W.

Calculate the maximum load current: 80W/43V = 1.86A; allowing for 83% converter efficiency, $I_{IN(MAX)}$ = 2.2A.

Calculate R_S: from Equation (8) R_S = 20mΩ.

Calculate $I_{SHORTCIRCUIT(MAX)}$: from Equation (10)

$$I_{SHORTCIRCUIT(MAX)} = \frac{66mV}{20m\Omega} = 3.3A$$

Select a MOSFET that can handle 3.3A at 71V: IRF530S.

Calculate C_T: from Equation (13) C_T = 322nF. Select C_T = 680nF, which gives the circuit breaker time-out period t = 5.6ms.

Consult MOSFET SOA curves: the IRF530S can handle 3.3A at 100V for 8.2ms, so it is safe to use in this application.

Calculate C_{SS}: using Equations (14) and (15) select C_{SS} = 68nF.

FREQUENCY COMPENSATION

The LTC4252C typical frequency compensation network for the analog current limit loop is a series R_C (10Ω) and C_C connected to V_{EE}. Figure 7 depicts the relationship between the compensation capacitor C_C and the MOSFET's C_{ISS}. The line in Figure 7 is used to select a starting value for C_C based upon the MOSFET's C_{ISS} specification. Optimized values for C_C are shown for several popular MOSFETs. Differences in the optimized value of C_C versus the starting value are small. Nevertheless, compensation values should be verified by board level short-circuit testing.

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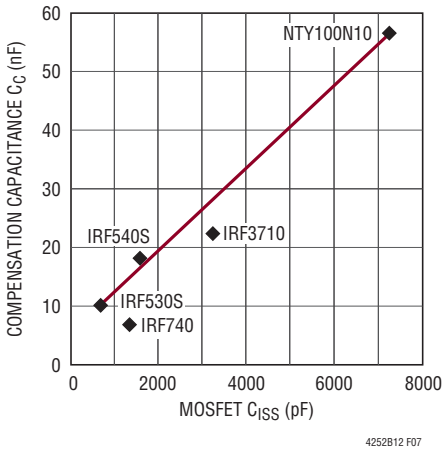

Figure 7. Recommended Compensation Capacitor C_C vs MOSFET C_{ISS}

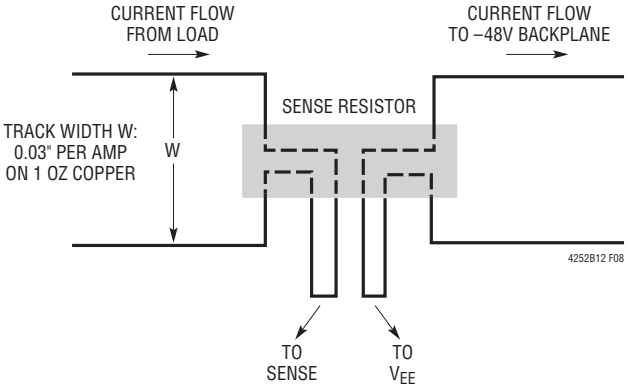

Figure 8. Making PCB Connections to the Sense Resistor

As seen in Figure 6 previously, at the onset of a short-circuit event, the input supply voltage can ring dramatically owing to series inductance. If this voltage avalanches the MOSFET, current continues to flow through the MOSFET to the output. The analog current limit loop cannot control this current flow and therefore the loop undershoots. This effect cannot be eliminated by frequency compensation. A Zener diode is required to clamp the input supply voltage and prevent MOSFET avalanche.

SENSE RESISTOR CONSIDERATIONS

For proper circuit breaker operation, Kelvin-sense PCB connections between the sense resistor and the LTC4252's V_{EE} and SENSE pins are strongly recommended. The drawing in Figure 8 illustrates the correct way of making connections between the LTC4252 and the sense resistor. PCB layout should be balanced and symmetrical to minimize wiring errors. In addition, the PCB layout for the sense resistor should include good thermal management techniques for optimal sense resistor power dissipation.

TIMING WAVEFORMS

System Power-Up

Figure 9 details the timing waveforms for a typical power-up sequence in the case where a board is already installed in the backplane and system power is applied abruptly. At time point 1, the supply ramps up, together with UV/OV, V_{OUT} and DRAIN. V_{IN} and $\overline{PWRGD}$ follow at a slower rate as set by the V_{IN} bypass capacitor. At time point 2, V_{IN} exceeds V_{LKO} and the internal logic checks for UV > V_{UVHI}, OV < V_{OVLO}, GATE < V_{GATEL}, SENSE < V_{CB}, SS < 20 • V_{OS} and TIMER < V_{TMRL}. If all conditions are met, an initial timing cycle starts and the TIMER capacitor is charged by a 5.8µA current source pull-up. At time point 3, TIMER reaches the V_{TMRH} threshold and the initial timing cycle terminates. The TIMER capacitor is quickly discharged. At time point 4, the V_{TMRL} threshold is reached and the conditions of GATE < V_{GATEL}, SENSE < V_{CB} and SS < 20 • V_{OS} must be satisfied before a GATE ramp-up cycle begins. SS ramps up as dictated by R_{SS} • C_{SS} (as in Equation 6); GATE is held low by the analog current limit (ACL) amplifier until SS crosses 20 • V_{OS}. Upon releasing GATE, 58µA sources into the external MOSFET gate and compensation network. When the GATE voltage reaches the MOSFET's threshold, current begins flowing into the load capacitor at time point 5. At time point 6, load current reaches the SS control level and the analog current limit loop activates. Between time points 6 and 8, the GATE voltage is servoed, the SENSE voltage is regulated at $V_{ACL}(t)$ (Equation 7) and soft-start limits the slew rate of the load current. If the SENSE voltage (V_{SENSE} – V_{EE}) reaches the V_{CB} threshold at time point 7, the circuit breaker TIMER activates. The TIMER capacitor, C_T, is charged by a (230µA + 8 • I_{DRN}) current pull-up. As the load capacitor nears full charge, load current begins to decline.

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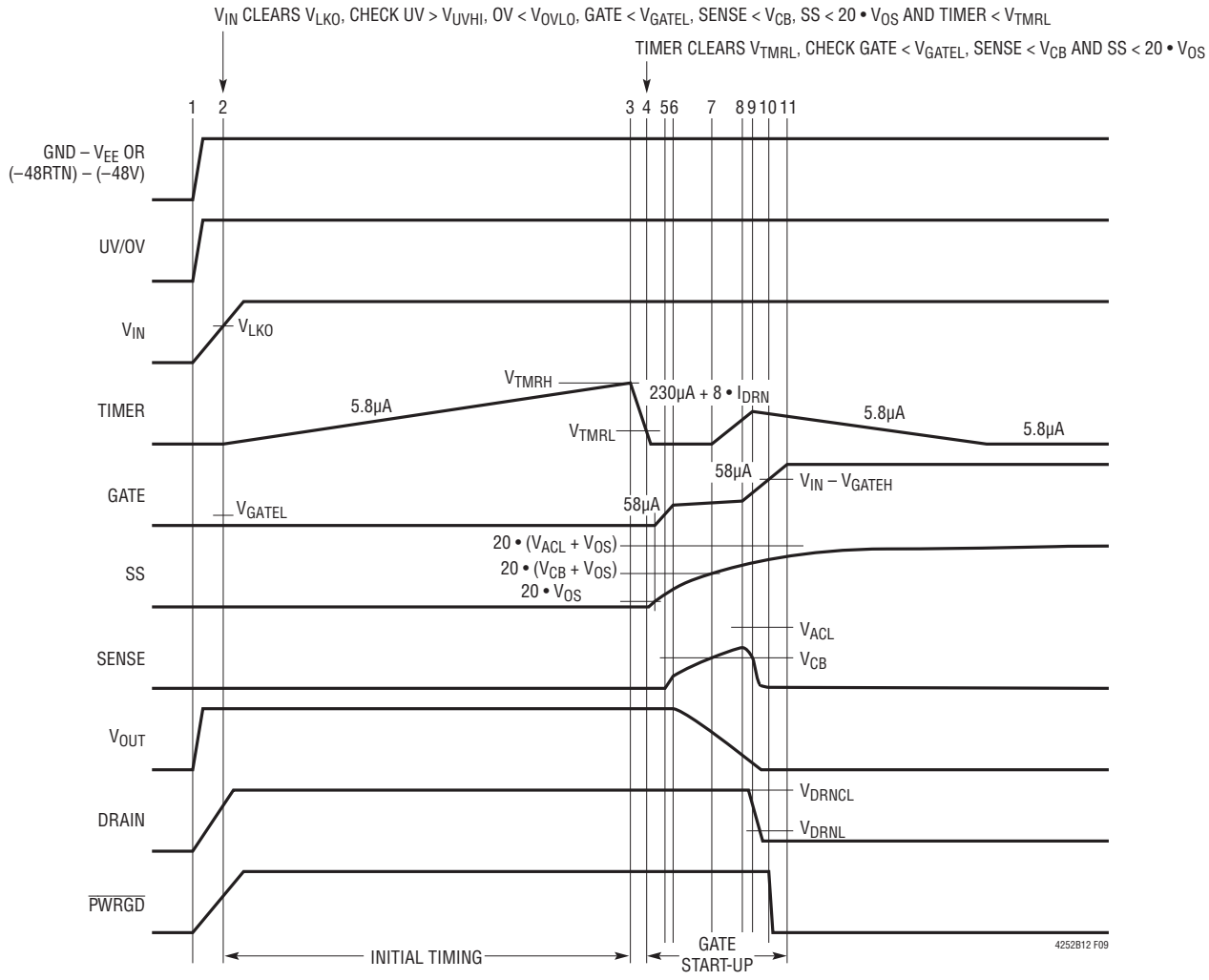

Figure 9. System Power-Up Timing (All Waveforms Are Referenced to V_{EE})

At time point 8, the load current falls and the SENSE voltage drops below $V_{ACL}(t)$. The analog current limit loop shuts off and the GATE pin ramps further. At time point 9, the SENSE voltage drops below V_{CB}, the fault TIMER cycle ends, followed by a 5.8µA discharge cycle (cool off). The duration between time points 7 and 9 must be shorter than one circuit breaker delay to avoid a fault time out during GATE ramp-up. When GATE ramps past the V_{GATEH} threshold at time point 10, $\overline{PWRGD}$ pulls low. At time point 11, GATE reaches its maximum voltage as determined by V_{IN}.

Live Insertion with Short Pin Control of UV/OV

In the example shown in Figure 10, power is delivered through long connector pins whereas the UV/OV divider makes contact through a short pin. This ensures the power connections are firmly established before the LTC4252 is activated. At time point 1, the power pins make contact and V_{IN} ramps through V_{LKO}. At time point 2, the UV/OV divider makes contact and its voltage exceeds V_{UVHI}. In addition, the internal logic checks for OV < V_{OVHI}, GATE < V_{GATEL}, SENSE < V_{CB}, SS < 20 • V_{OS} and TIMER < V_{TMRL}. If all conditions are met, an initial timing cycle starts and the TIMER capacitor is charged by a 5.8µA current source pull-up. At time point 3, TIMER reaches the V_{TMRH} threshold and the initial timing cycle terminates. The TIMER capacitor is quickly discharged. At time point 4, the V_{TMRL} threshold is reached and the conditions of GATE < V_{GATEL}, SENSE < V_{CB} and SS < 20 • V_{OS} must be

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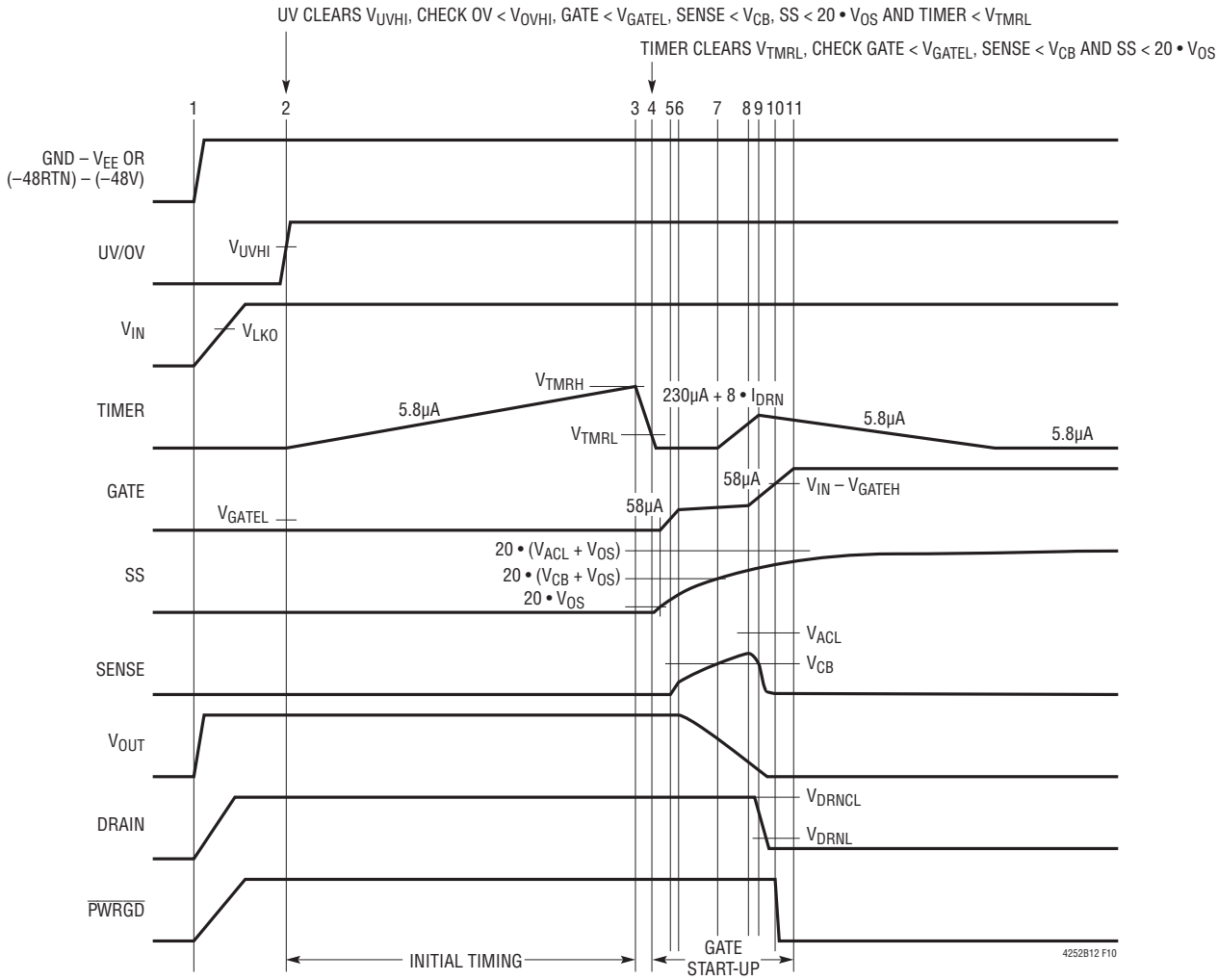

Figure 10. Power-Up Timing with a Short Pin (All Waveforms Are Referenced to V_{EE})

satisfied before a GATE start-up cycle begins. SS ramps up as dictated by R_{SS} • C_{SS}; GATE is held low by the analog current limit amplifier until SS crosses 20 • V_{OS}. Upon releasing GATE, 58µA sources into the external MOSFET gate and compensation network. When the GATE voltage reaches the MOSFET's threshold, current begins flowing into the load capacitor at time point 5. At time point 6, load current reaches the SS control level and the analog current limit loop activates. Between time points 6 and 8, the GATE voltage is servoed, the SENSE voltage is regulated at $V_{ACL}(t)$ and soft-start limits the slew rate of the load current. If the SENSE voltage (V_{SENSE} – V_{EE}) reaches the V_{CB} threshold at time point 7, the circuit breaker TIMER activates. The TIMER capacitor, C_T, is charged by a (230µA + 8 • I_{DRN}) current pull-up. As the load capacitor nears full charge, load current begins to decline. At point 8, the load current falls and the SENSE voltage drops below $V_{ACL}(t)$. The analog current limit loop shuts off and the GATE pin ramps further. At time point 9, the SENSE voltage drops below V_{CB} and the fault TIMER cycle ends, followed by a 5.8µA discharge cycle (cool off). When GATE ramps past V_{GATEH} threshold at time point 10, $\overline{PWRGD}$ pulls low. At time point 11, GATE reaches its maximum voltage as determined by V_{IN}.

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Undervoltage Timing

In Figure 11 when UV pin drops below V_{UVLO} (time point 1), the LTC4252 shuts down with TIMER, SS and GATE all pulling low. If current has been flowing, the SENSE pin voltage decreases to zero as GATE collapses. When UV recovers and clears V_{UVHI} (time point 2), an initial timer cycle begins followed by a GATE start-up cycle.

V_{IN} Undervoltage Lockout Timing

The V_{IN} undervoltage lockout comparator, UVLO, has a similar timing behavior as the UV pin timing except it looks for $V_{IN} < (V_{LKO} – V_{LKH})$ to shut down and $V_{IN} > V_{LKO}$ to start. In an undervoltage lockout condition, both UV and OV comparators are held off. When V_{IN} exits undervoltage lockout, the UV and OV comparators are enabled.

Undervoltage Timing with Overvoltage Glitch

In Figure 12, both UV and OV pins are connected together. When UV clears V_{UVHI} (time point 1), an initial timing cycle starts. If the system bus voltage overshoots V_{OVHI} as shown at time point 2, TIMER discharges. At time point 3, the supply voltage recovers and drops below the V_{OVLO} threshold. The initial timing cycle restarts, followed by a GATE start-up cycle.

Overvoltage Timing

During normal operation, if the OV pin exceeds V_{OVHI} as shown at time point 1 of Figure 13, the TIMER and $\overline{PWRGD}$ status are unaffected. Nevertheless, SS and GATE pull down and the load is disconnected. At time point 2, OV recovers and drops below the V_{OVLO} threshold. A GATE start-up cycle begins. If the overvoltage glitch is long enough to deplete the load capacitor, a full start-up cycle as shown between time points 4 through 7 may occur.

Circuit Breaker Timing

In Figure 14a, the TIMER capacitor charges at 230µA if the SENSE pin exceeds V_{CB} but V_{DRN} is less than 5V. If the SENSE pin drops below V_{CB} before TIMER reaches

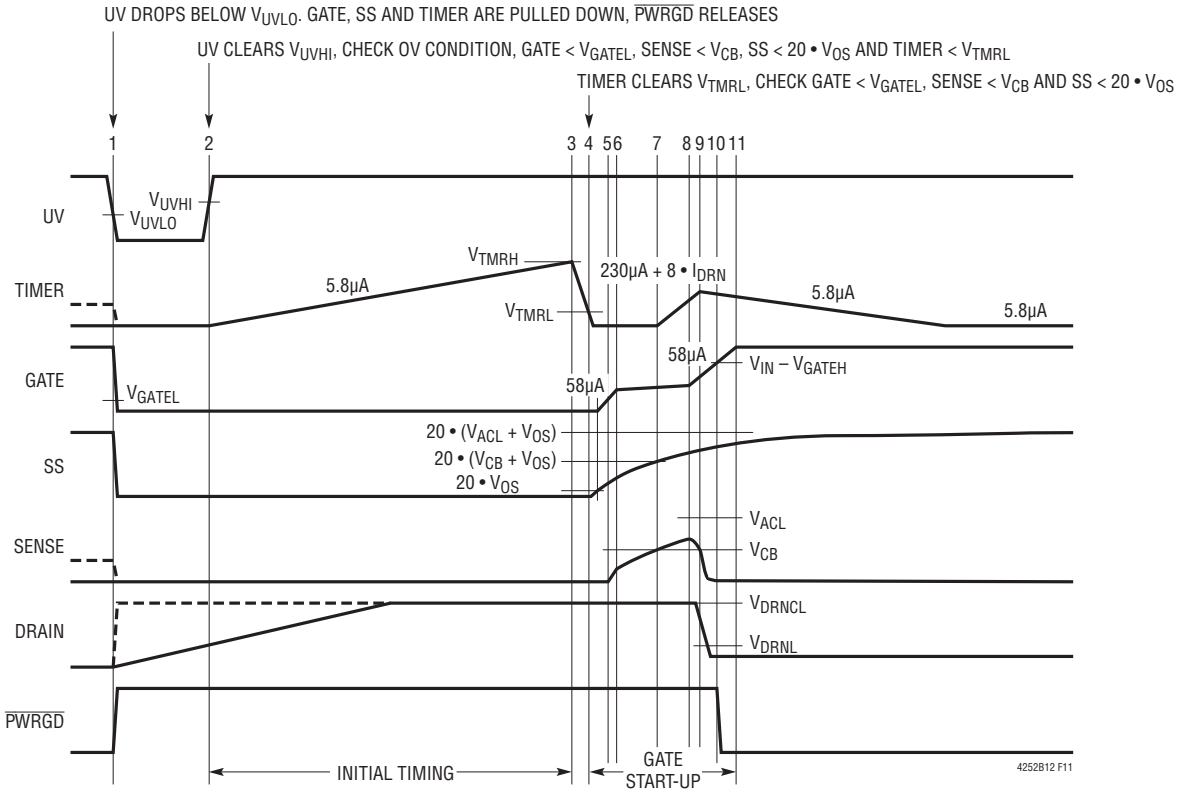


Figure 11. Undervoltage Timing (All Waveforms Are Referenced to V_{EE})

APPLICATIONS INFORMATION

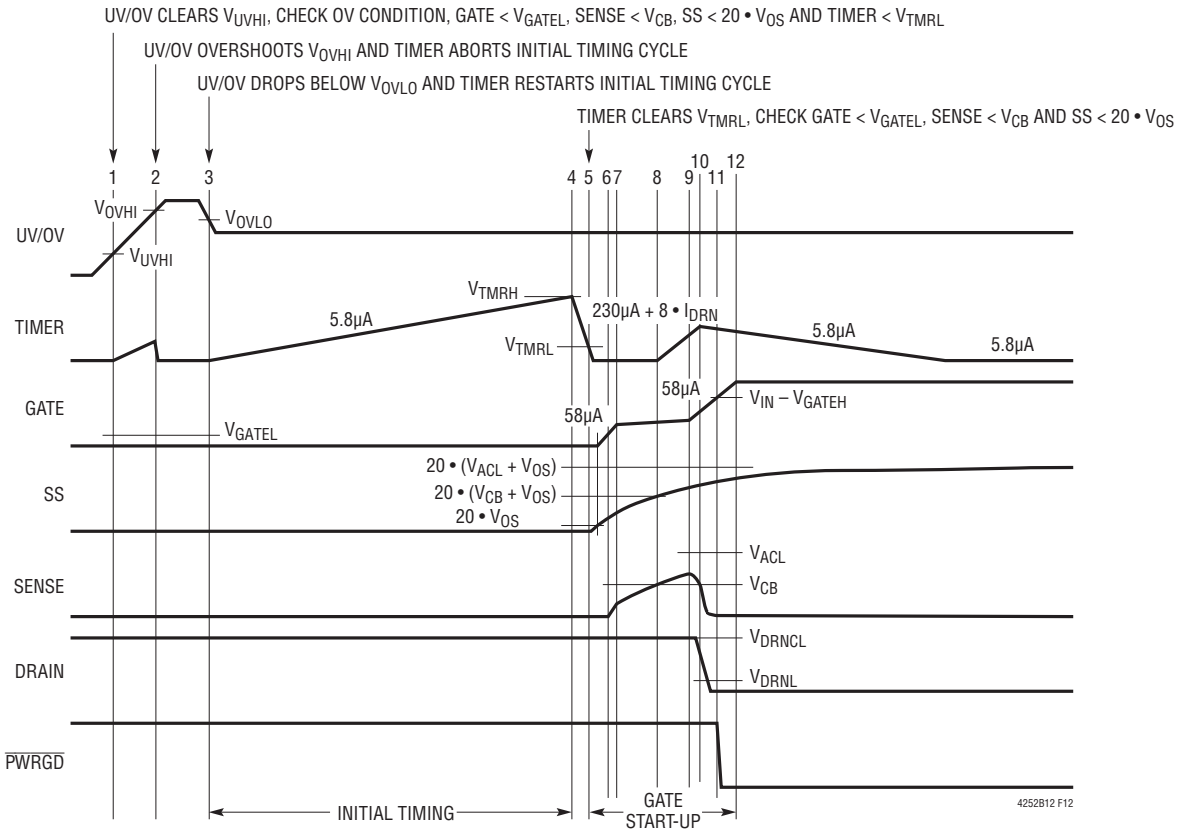


Figure 12. Undervoltage Timing with an Overvoltage Glitch (All Waveforms Are Referenced to V_{EE})

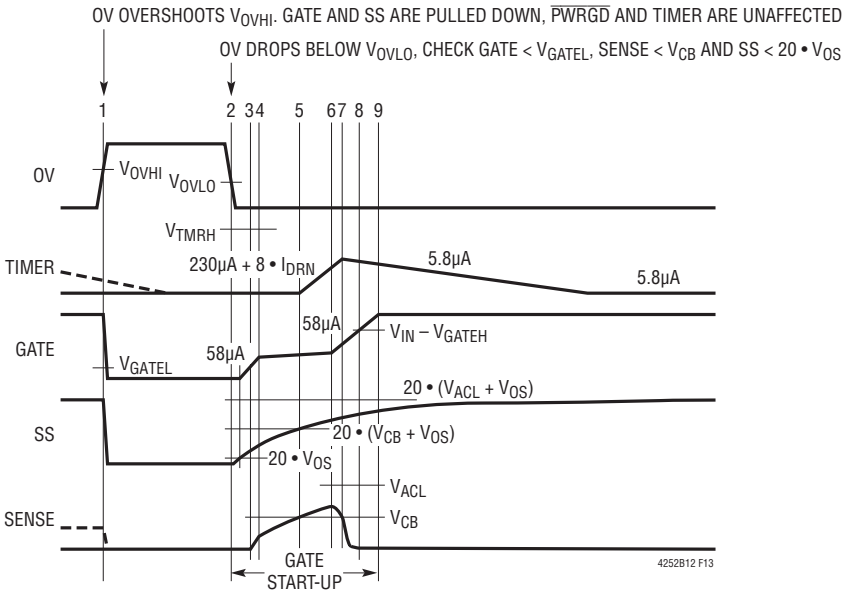
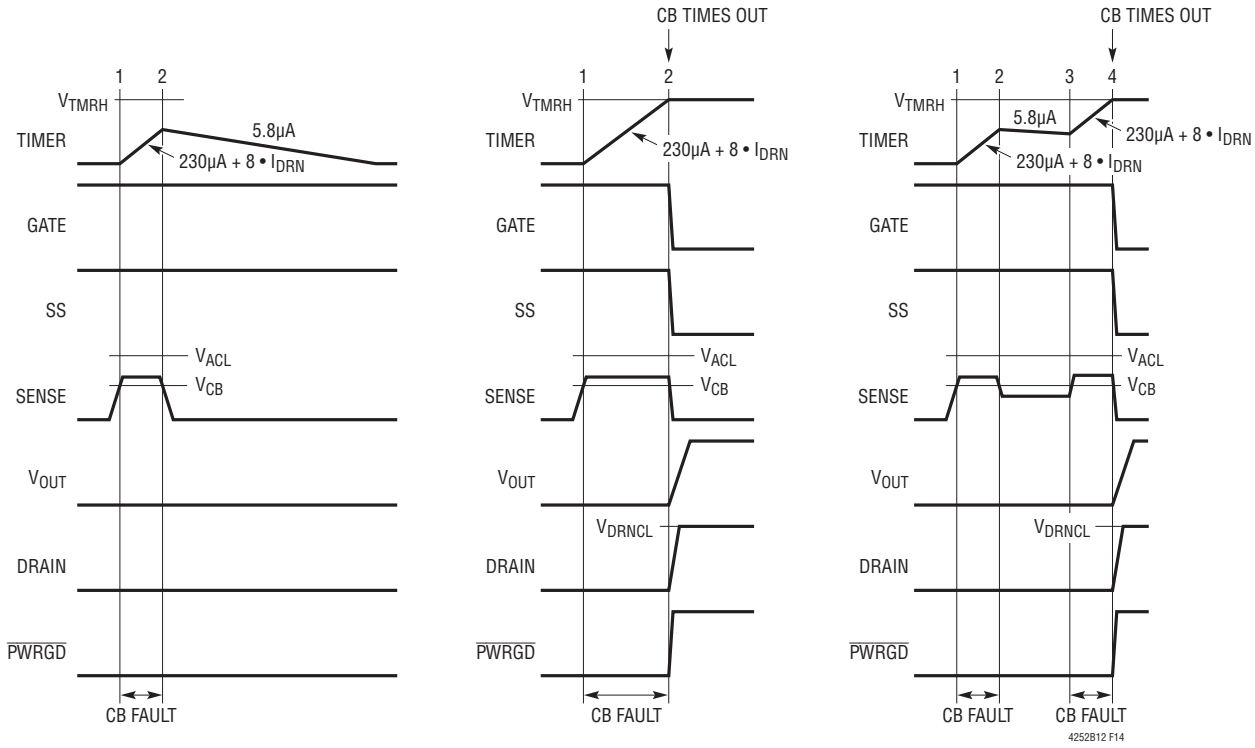


Figure 13. Overvoltage Timing (All Waveforms Are Referenced to V_{EE})

APPLICATIONS INFORMATION



(14a) Momentary Circuit-Breaker Fault **(14b) Circuit-Breaker Time Out** **(14c) Multiple Circuit-Breaker Fault**

Figure 14. Circuit-Breaker Timing Behavior (All Waveforms Are Referenced to V_{EE})

the V_{TMRH} threshold, TIMER is discharged by 5.8µA. In Figure 14b, when TIMER exceeds V_{TMRH}, GATE pulls down immediately and the LTC4252 shuts down. In Figure 14c, multiple momentary faults cause the TIMER capacitor to integrate and reach V_{TMRH}. GATE pull down follows and the LTC4252 shuts down. During shutdown, the LTC4252-1 latches TIMER high with a 5.8µA pull-up current source; the LTC4252-2 activates a shutdown cooling cycle.

Resetting a Fault Latch (LTC4252-1)

The latched circuit breaker fault of LTC4252-1 benefits from long cooling time. It is reset by pulling the UV pin below V_{UVLO} with a switch. Reset is also accomplished by pulling the V_{IN} pin momentarily below ($V_{LKO} – V_{LKH}$). A third reset method involves pulling the TIMER pin below V_{TMRL} as shown in Figure 15. An initial timing cycle is skipped if TIMER is used for reset. An initial timing cycle is generated if reset by the UV pin or the V_{IN} pin.

The duration of the TIMER reset pulse should be smaller than the time taken to reach 0.2V at SS pin. With a single pole mechanical pushbutton switch, this may not be feasible. A double pole, single throw pushbutton switch removes this restriction by connecting the second switch to the SS pin. With this method, both the SS and TIMER pins are released at the same time (see Figure 24).

Shutdown Cooling Cycle (LTC4252-2)

Figure 16 shows the timer behavior of the LTC4252-2. At time point 2, TIMER exceeds V_{TMRH}, GATE pulls down immediately and the LTC4252 shuts down. TIMER starts a shutdown cooling cycle by discharging TIMER with 5.8µA to the V_{TMRL} threshold. TIMER then charges with 5.8µA to the V_{TMRH} threshold. There are four 5.8µA discharge phases and three 5.8µA charge phases in this shutdown cooling cycle spanning time points 2 and 3. At time point 3, the LTC4252 automatic retry occurs with a start-up cycle. Good thermal management techniques are highly recommended; power and thermal dissipation must be carefully evaluated when implementing the automatic retry scheme.

APPLICATIONS INFORMATION

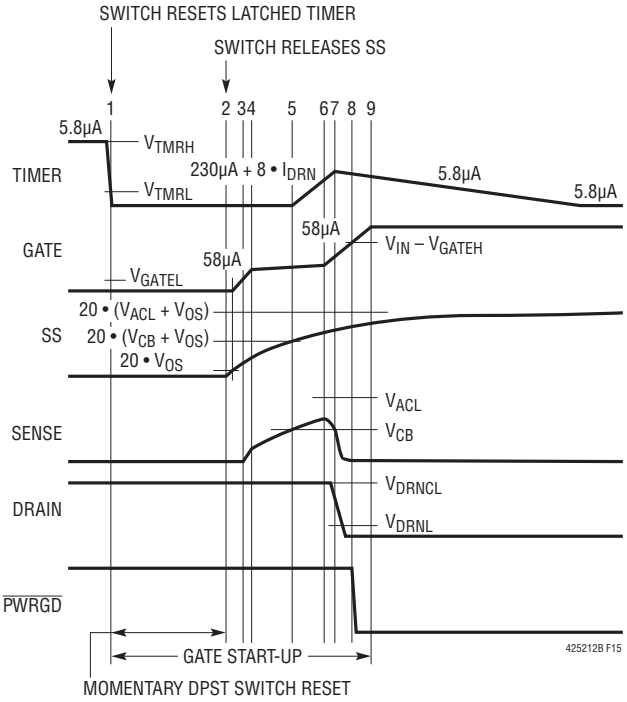


Figure 15. Pushbutton Reset of LTC4252-1's Latched Fault (All Waveforms Are Referenced to V_{EE})

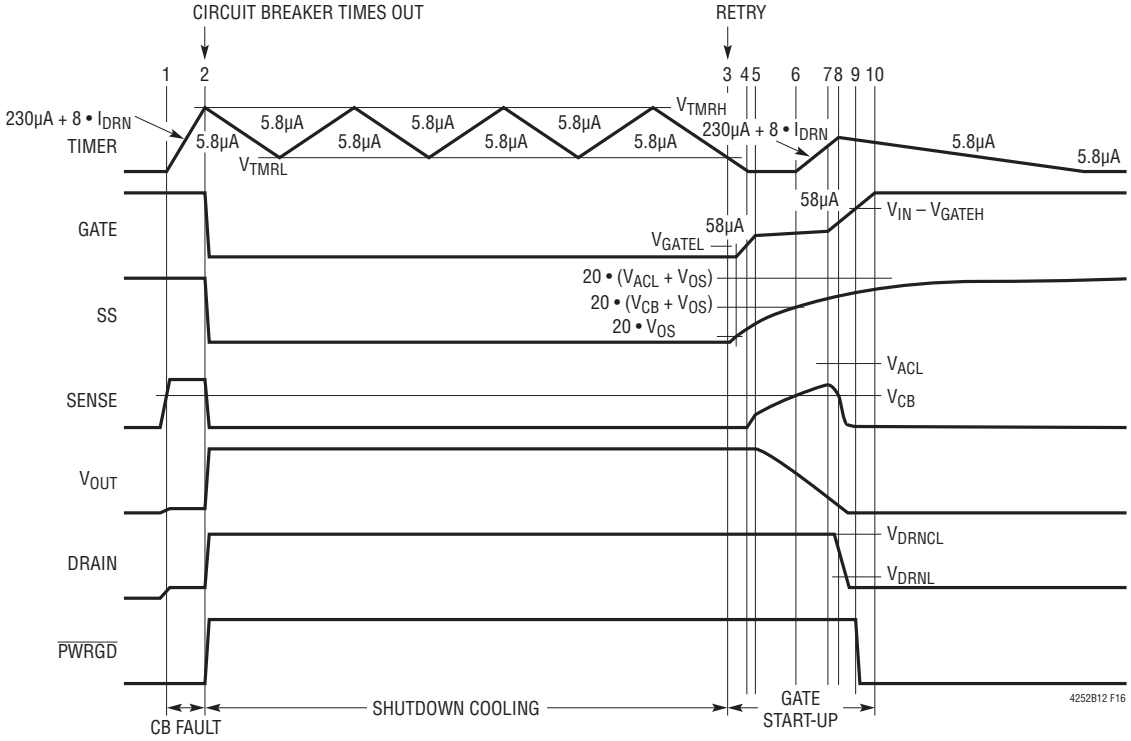


Figure 16. Shutdown Cooling Timing Behavior of LTC4252-2 (All Waveforms Are Referenced to V_{EE})

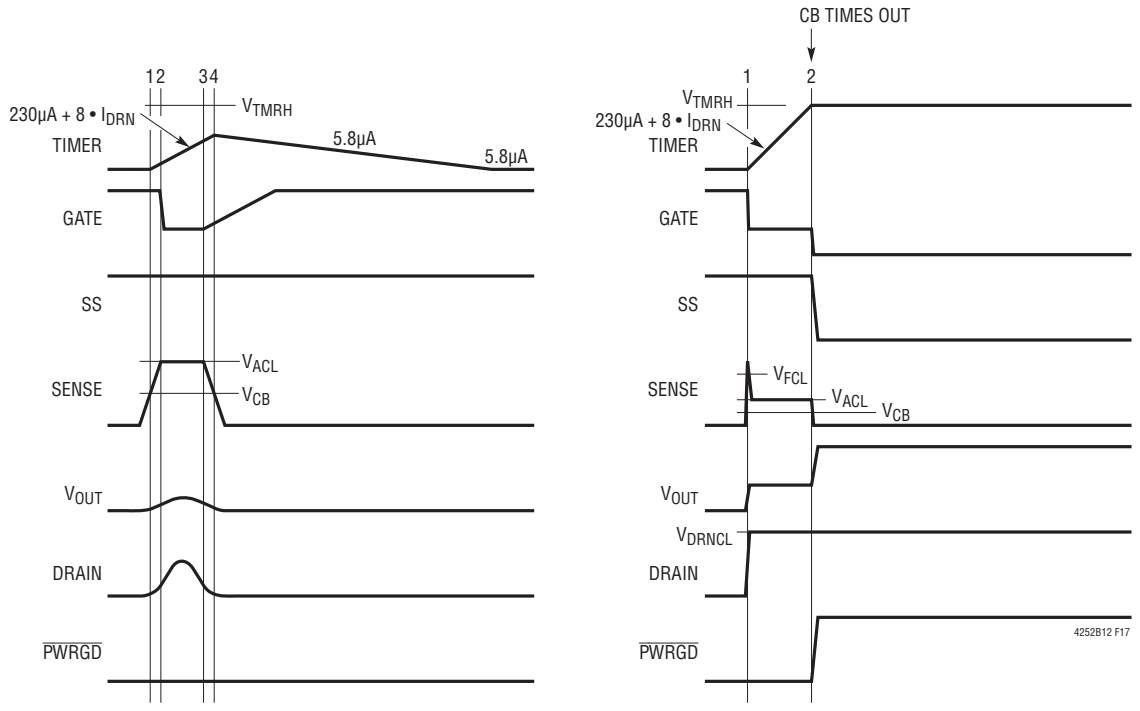
APPLICATIONS INFORMATION

Analog Current Limit and Fast Current Limit

In Figure 17a, when SENSE exceeds V_{ACL}, GATE is regulated by the analog current limit amplifier loop. When SENSE drops below V_{ACL}, GATE is allowed to pull up. In Figure 17b, when a severe fault occurs, SENSE exceeds V_{FCL} and GATE immediately pulls down until the analog current amplifier establishes control. If the severe fault causes V_{OUT} to exceed V_{DRNCL}, the DRAIN pin is clamped at V_{DRNCL}. I_{DRN} flows into the DRAIN pin and is multiplied by 8. This extra current is added to the TIMER pull-up current of 230µA. This accelerated TIMER current of [230µA+8 • I_{DRN}] produces a shorter circuit breaker fault delay. Careful selection of C_T, R_D and MOSFET can help prevent SOA damage in a low impedance fault condition.

Soft-Start

If the SS pin is not connected, this pin defaults to a linear voltage ramp, from 0V to 2.2V in about 180µs (or 0V to 1.4V in 230µs for the LTC4252C) at GATE start-up, as shown in Figure 18a. If a soft-start capacitor, C_{SS}, is connected to this SS pin, the soft-start response is modified from a linear ramp to an RC response (Equation 6), as shown in Figure 18b. This feature allows load current to slowly ramp-up at GATE start-up. Soft-start is initiated at time point 3 by a TIMER transition from V_{TMRH} to V_{TMRL} (time points 1 to 2) or by the OV pin falling below the V_{OVLO} threshold after an OV condition. When the SS pin is below 0.2V, the analog current limit amplifier holds GATE low. Above 0.2V, GATE is released and 58µA ramps up the compensation network and GATE capacitance at time point 4. Meanwhile, the SS pin voltage continues to ramp up. When GATE reaches the MOSFET's threshold, the MOSFET begins to conduct. Due to the MOSFET's high g_m, the MOSFET current quickly reaches the soft-start control value of $V_{ACL}(t)$ (Equation 7). At time point 6, the GATE voltage is controlled by the current limit amplifier. The soft-start control voltage reaches the circuit breaker voltage, V_{CB}, at time point 7 and the circuit breaker TIMER activates. As the load capacitor nears full charge, load

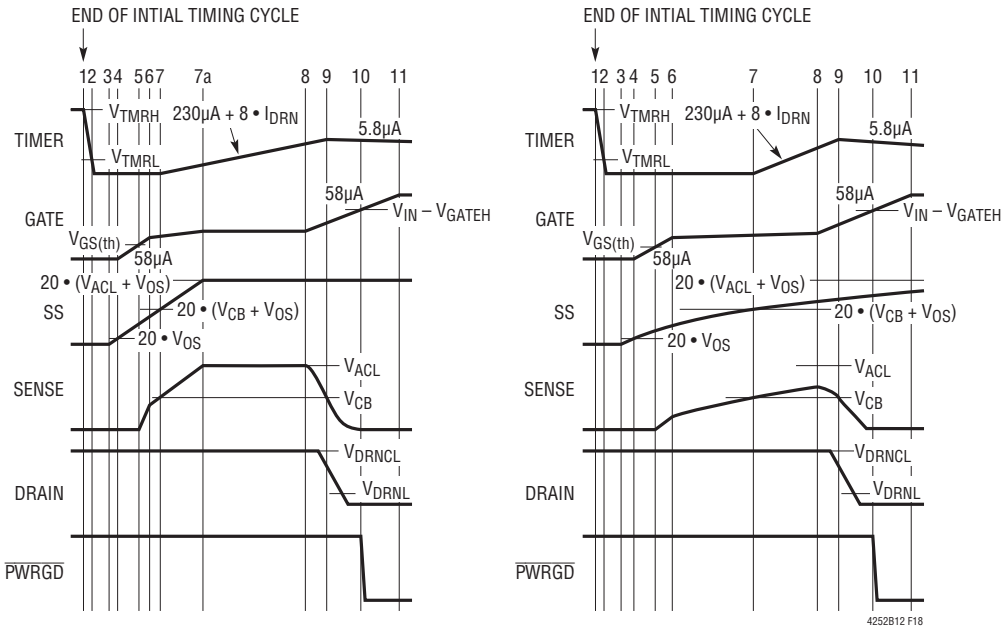


(17a) Analog Current Limit Fault

(17b) Fast Current Limit Fault

Figure 17. Current Limit Behavior (All Waveforms Are Referenced to V_{EE})

APPLICATIONS INFORMATION



(18a) Without External C_{SS} **(18b) With External C_{SS}**

Figure 18. Soft-Start Timing (All Waveforms Are Referenced to V_{EE})

current begins to decline below $V_{ACL}(t)$. The current limit loop shuts off and GATE releases at time point 8. At time point 9, the SENSE voltage falls below V_{CB} and TIMER deactivates.

Large values of C_{SS} can cause premature circuit breaker time out as $V_{ACL}(t)$ may exceed the V_{CB} potential during the circuit breaker delay. The load capacitor is unable to achieve full charge in one GATE start-up cycle. A more serious side effect of large C_{SS} values is SOA duration may be exceeded during soft-start into a low impedance load. A soft-start voltage below V_{CB} will not activate the circuit breaker TIMER.

Power Limit Circuit Breaker

Figure 19 shows the LTC4252C-1 in a power limit circuit breaking application. The SENSE pin is modulated by the board supply voltage, V_{SUPPLY}. The D1 Zener voltage, V_Z is set to be the same as the low supply operating voltage, $V_{SUPPLY(MIN)}$ = 43V. If the goal is to have the high supply operating voltage, $V_{SUPPLY(MAX)}$ = 71V giving the same power at $V_{SUPPLY(MIN)}$, then resistors R4 and R6 are selected using the ratio:

$$\frac{R6}{R4} = \frac{V_{CB}}{V_{SUPPLY(MAX)}} \quad (16)$$

If R6 is 27Ω, R4 is 38.3k. The peak circuit breaker power limit is:

$$POWER_{MAX} = \frac{\left(V_{SUPPLY(MIN)} + V_{SUPPLY(MAX)}\right)^2}{4 \bullet V_{SUPPLY(MIN)} \bullet V_{SUPPLY(MAX)}} \bullet POWER_{SUPPLY(MIN)} = 1.064 \bullet POWER_{SUPPLY(MIN)} \quad (17)$$

when

$V_{SUPPLY} = 0.5 \bullet (V_{SUPPLY(MIN)} + V_{SUPPLY(MAX)}) = 57V.$

The peak power at the fault current limit occurs at the supply overvoltage threshold. The fault current limited power is:

$$POWER_{FAULT} = \frac{V_{SUPPLY}}{R_S} \bullet \left(V_{ACL} - \left(V_{SUPPLY} - V_Z\right) \bullet \frac{R6}{R4} \right) \quad (18)$$

APPLICATIONS INFORMATION

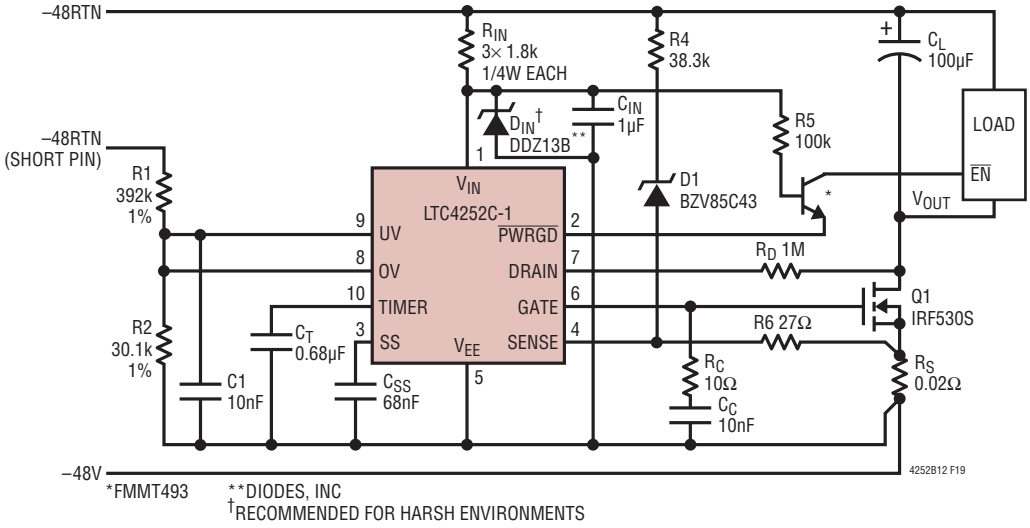


Figure 19. Power Limit Circuit Breaking Application

Circuit Breaker with Foldback Current Limit

Figure 20 shows the LTC4252C in a foldback current limit application. When V_{OUT} is shorted to the –48V RTN supply, current flows through resistors R4 and R5. This results in a voltage drop across R5 and a corresponding reduction in voltage drop across the sense resistor, R_S, as the ACL amplifier servos the sense voltage between the SENSE and V_{EE} pins to about 60mV. The short-circuit current through R_S reduces as the V_{OUT} voltage increases during an output short-circuit condition. Without foldback current limiting resistor R5, the current is limited to 3A during analog current limit. With R5, the short-circuit current is limited to 0.5A when V_{OUT} is shorted to 71V.

Inrush Control Without a Sense Resistor During Power-Up

Figure 21 shows the LTC4252C in an application where the inrush current is controlled without a sense resistor during power-up. This setup is suitable only for applications that don't require short-circuit protection from the LTC4252C. Resistor R4 and capacitor C2 act as a feedback network to accurately control the inrush current. The C2 capacitor can be calculated with the following equation:

$$C2 = \frac{I_{GATE} \bullet C_L}{I_{INRUSH}} \quad (19)$$

where I_{GATE} = 58µA and C_L is the total load capacitance.

Capacitor C3 and resistor R4 prevent Q1 from momentarily turning on when the power pins first make contact. Without C3 and R4, capacitor C2 pulls the gate of Q1 up to a voltage roughly equal to $V_{EE} \bullet C2/C_{GS(Q1)}$ before the LTC4252C powers up. By placing capacitor C3 in parallel with the gate capacitance of Q1 and isolating them from C2 using resistor R4, the problem is solved. The value of C3 is given by:

$$C3 = \frac{V_{SUPPLY(MAX)}}{V_{GS(TH),Q1}} \bullet \left(C2 + C_{GD(Q1)}\right) \quad (20)$$

$C3 \approx 35 \bullet C2$ for $V_{SUPPLY(MAX)}$ = 71V

where $V_{GS(TH),Q1}$ is the MOSFET's minimum gate threshold and $V_{SUPPLY(MAX)}$ is the maximum operating input voltage.

Diode-ORing

Figure 22 shows the LTC4252B used as diode-oring with Hot Swap capability in a dual –48V power supply application. The conventional diode-OR method uses two high power diodes and heat sinks to contain the large heat dissipation of the diodes. With the LTC4252B controlling the external FETs Q2 and Q3 in a diode-OR manner, the small turn-on voltage across the fully enhanced Q2 and Q3 reduces the power dissipation significantly.

APPLICATIONS INFORMATION

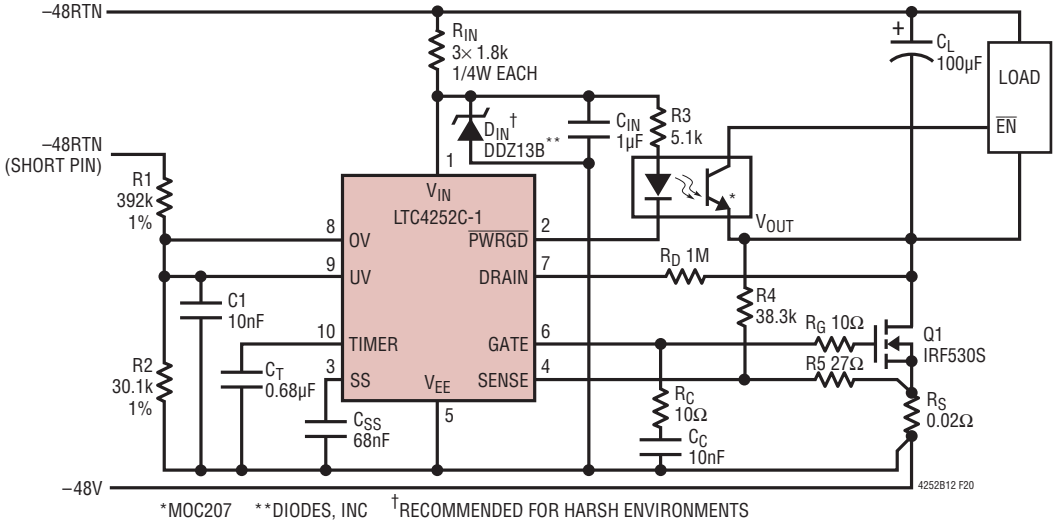


Figure 20. Circuit Breaker with Foldback Current Limit Application

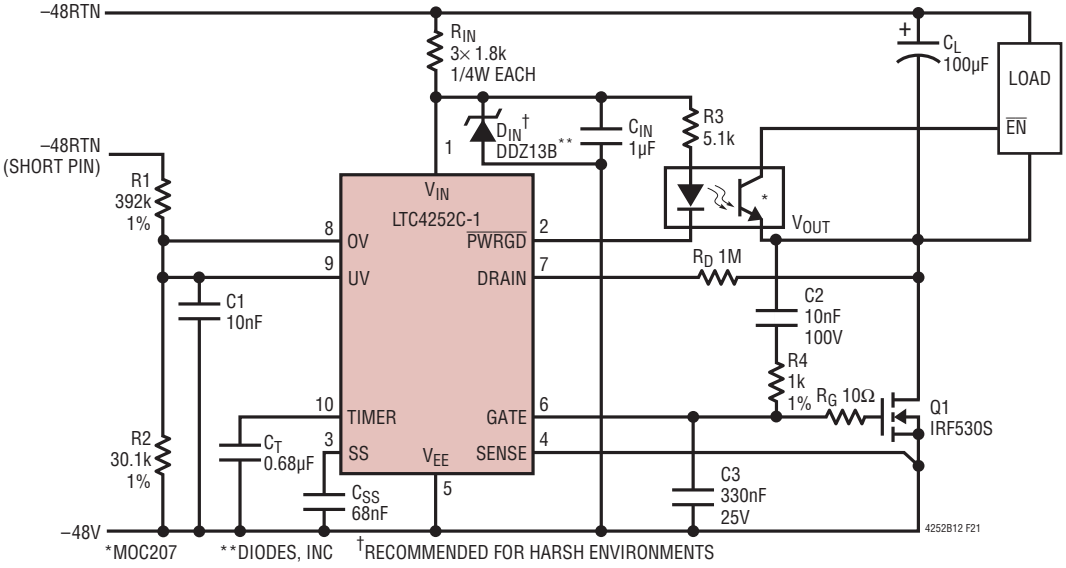


Figure 21. Inrush Control Without a Sense Resistor Application

At power-up, Q5 and Q8 are held off low by the SS pin of the LTC4252B; resistors R5 and R8 pull the SENSE pin closed to V_{EE}. V_{EE} is connected to the power supply with lower voltage through the body diodes Q2 or Q3 until Q2 or Q3 is turned on. This allows the LTC4252B to perform a start-up cycle and ramp up the SS and GATE voltage.

As the SS voltage ramps up to 2.2V, it turns on Q5 and Q8 and pulls TIMER low through Q6 and Q9. The sense voltage rises as current flows into R5 and R8 through resistors R3 and R6. The ACL amplifier of the LTC4252B servos the sense voltage to about 100mV as the GATE voltage regulates Q2 and Q3. Current flows into R4, Q4 and R7, Q7 as Q2 and Q3 turn on. The respective node voltages at the R3 and R4 connection and the R6 and R7 connection are always kept equal to their respective sense voltages by the Q4 and Q2 V_{DS} drop and the Q7 and Q3 V_{DS} drop assuming the Q5 and Q8 V_{DS} drop is negligible.

APPLICATIONS INFORMATION

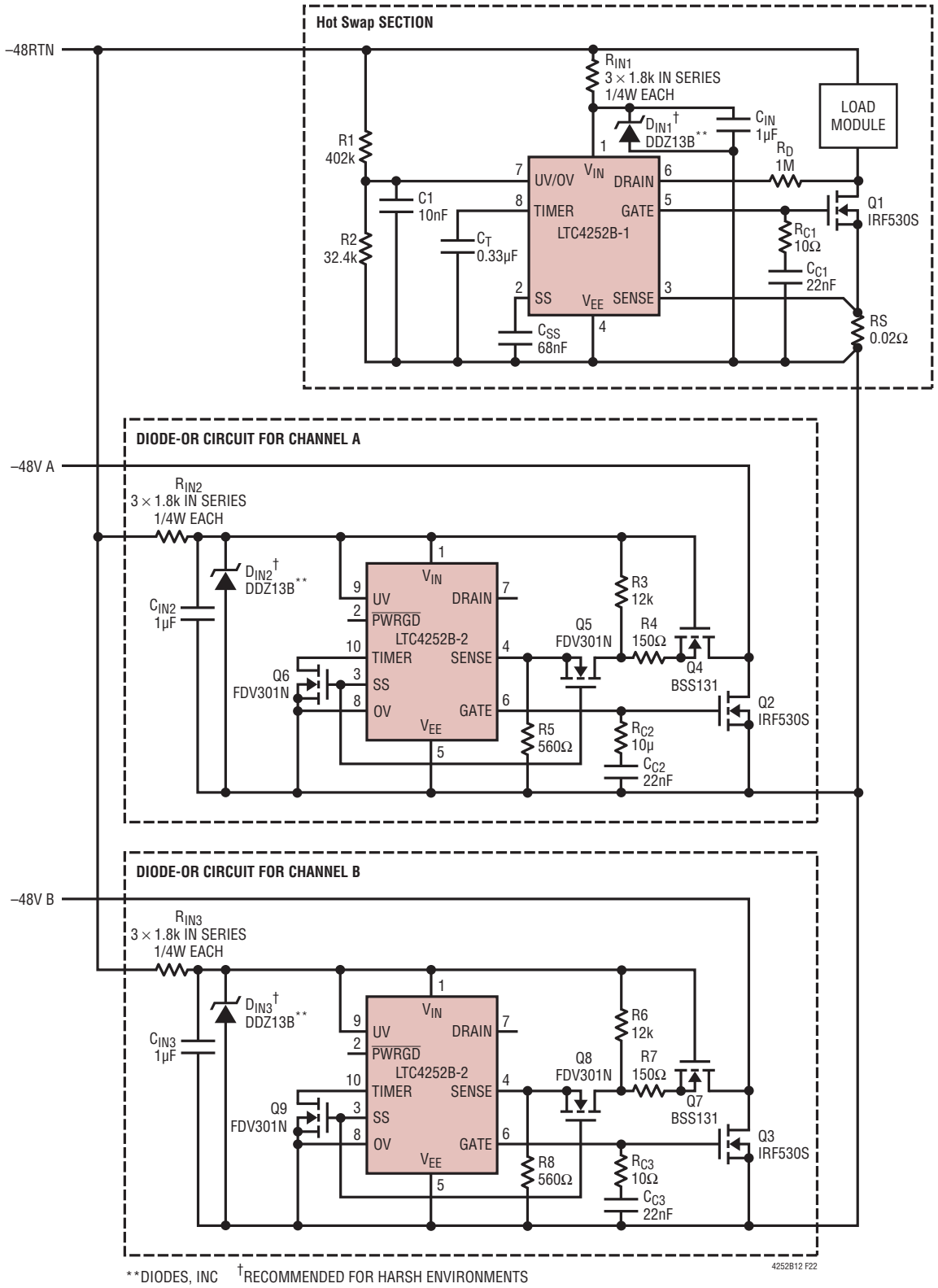


Figure 22. –48V/2.5A Diode-OR Application

APPLICATIONS INFORMATION

The internal fault latches of the LTC4252B are disabled as the TIMER pin is always held low by the SS voltage when Q2 and Q3 are in analog current limit.

If both power supplies from channel A and B are exactly equal, then equal load current will flow through Q2 and Q3 to the load module via the Hot Swap section.

If the channel A supply is greater than the channel B by more than 100mV, the sense voltage will rise above the fast comparator trip threshold of 200mV, the GATE will be pulled low and Q2 is turned off. The GATE ramps up and regulates Q2 when the channel A supply is equal to the channel B supply. Likewise, if the channel B supply is greater than channel A by more than 100mV, it trips the fast comparator and GATE is pulled low and Q3 is turned off. The GATE ramps up and regulates Q3 when the channel B supply is equal to the channel A supply.

Resistors R4, R7 and external FETs Q4 and Q7 limit the current flow into Q5 and Q8 during their respective supply source short. When the channel A supply is shorted to the –48V RTN (or GND), large current flows into Q4 momentarily and creates a voltage drop across R4, which in turn reduces the gate-to-source voltage of Q4, limiting the current flow. The sense voltage is lifted up and causes the fast comparator of LTC4252B to trip and pull the GATE low instantly. The channel A supply short will not cause Q3 of channel B diode-OR circuit to turn off.

Similarly, when the channel B supply is shorted to the –48V RTN (or GND), large current flows into Q7 momentarily and creates a voltage drop across R7, which in turn reduces the gate-to-source voltage of Q7, thus limiting the current flow. The increase in sense voltage will trip the fast comparator of LTC4252B and pull the GATE low instantly. The channel B supply short will not cause Q2 of channel A diode-OR circuit to turn off. The load short at the output of Q1 is protected by the Hot Swap section.

Using an EMI Filter Module

Many applications place an EMI filter module in the power path to prevent switching noise of the module from being injected back onto the power supply. A typical application using the Lucent FLTR100V10 filter module is shown in Figure 23. When using a filter, an opto-isolator is required to prevent common mode transients from destroying the $\overline{\text{PWRGD}}$ and $\overline{\text{ON}}$/OFF pins.

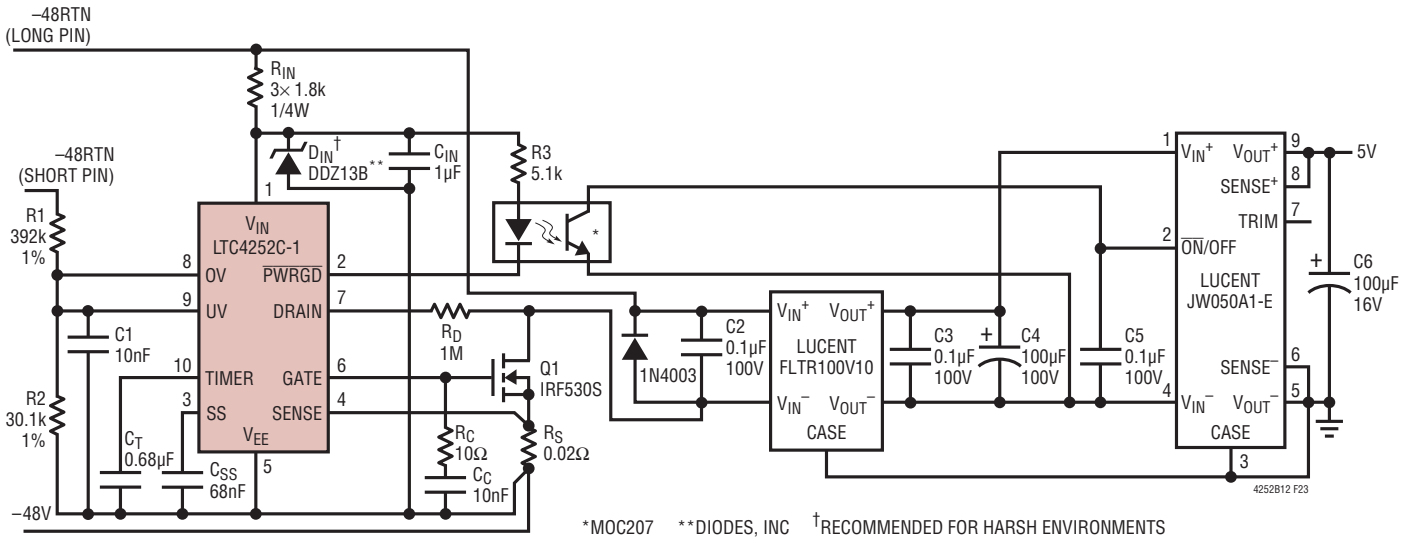
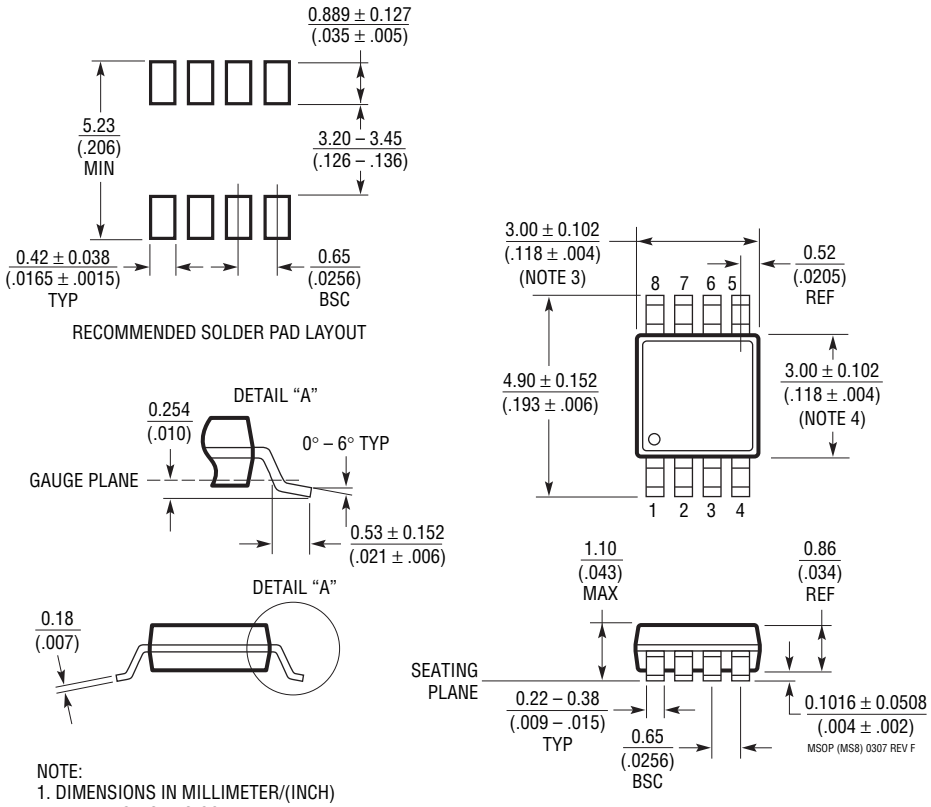


Figure 23. Typical Application Using a Filter Module

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev F)

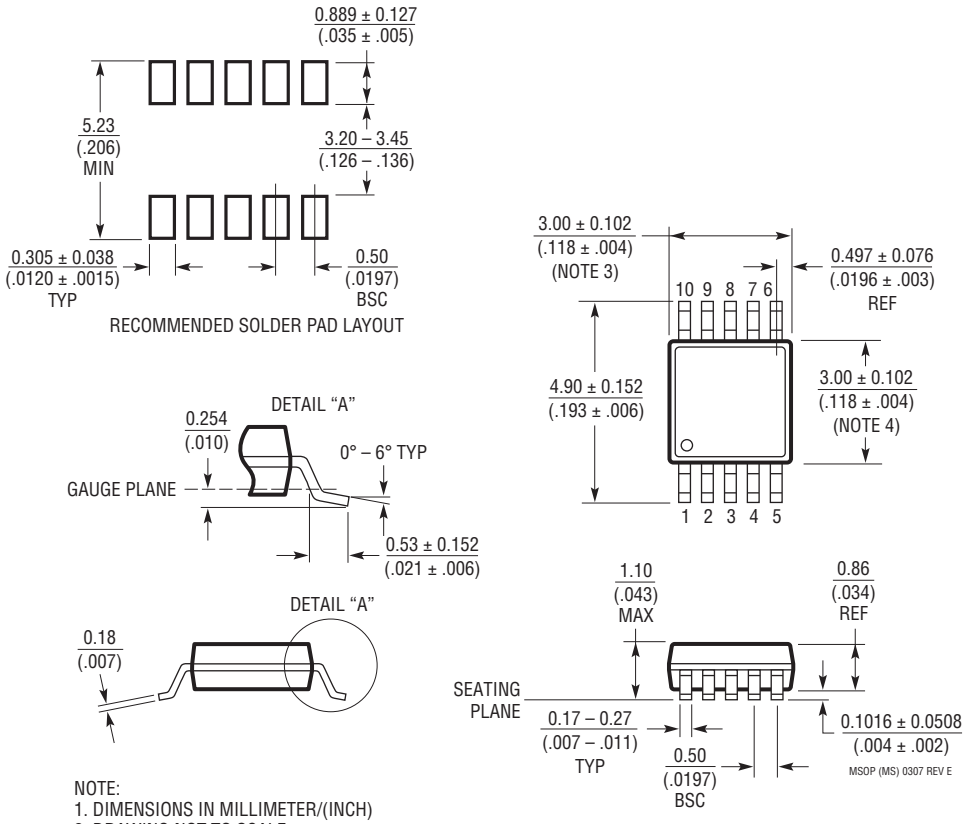


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661 Rev E)



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   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

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TYPICAL APPLICATION

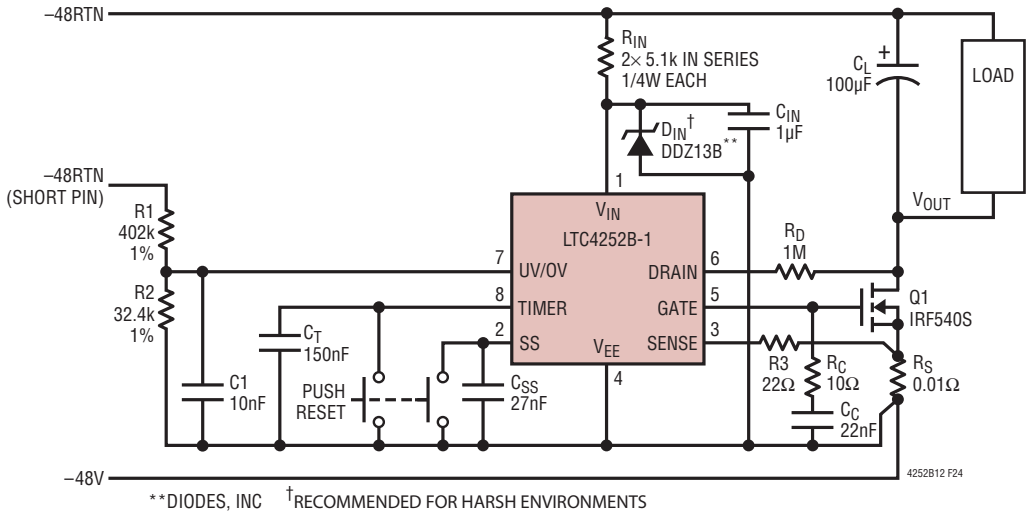

Figure 24. –48V/5A Application

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1640AH/LT1640AL	Negative High Voltage Hot Swap Controllers in SO-8	Negative High Voltage Supplies from –10V to –80V
LT1641-1/LT1641-2	Positive High Voltage Hot Swap Controllers in SO-8	Supplies from 9V to 80V, Latched Off/Autoretry
LTC1642	Fault Protected Hot Swap Controller	3V to 16.5V, Overvoltage Protection up to 33V
LTC4214	Negative Voltage Hot Swap Controller	Operates from –6V to –16V
LTC4220	Dual Supply Hot Swap Controller	±2.2V to ±16.5V Operation
LT4250	–48V Hot Swap Controller in SO-8	Active Current Limiting, Supplies from –20V to –80V
LTC4251B/ LTC4251B-1/ LTC4251B-2	–48V Hot Swap Controllers in SOT-23	Fast Active Current Limiting, Supplies from –15V
LTC4253B	–48V Hot Swap Controller with Sequencer	Fast Current Limiting with Three Sequenced Power Good Outputs, Supplies from –15V

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