

DS90LV804 4-Channel 800 Mbps LVDS Buffer/Repeater

Check for Samples: [DS90LV804](#)

FEATURES

- 800 Mbps Data Rate per Channel
- Low Output Skew and Jitter
- LVDS/CML/LVPECL Compatible Input, LVDS Output
- On-Chip 100Ω Input and Output Termination
- 12 kV ESD Protection on LVDS Outputs
- Single 3.3V Supply
- Very Low Power Consumption
- Industrial -40 to +85°C Temperature Range
- Small WQFN Package Footprint

DESCRIPTION

The DS90LV804 is a four channel 800 Mbps LVDS buffer/repeater. In many large systems, signals are distributed across cables and signal integrity is highly dependent on the data rate, cable type, length, and the termination scheme.

In order to maximize signal integrity, the DS90LV804 features both an internal input and output (source) termination to eliminate these extra components from the board, and to also place the terminations as close as possible to receiver inputs and driver output. This is especially significant when driving longer cables.

The DS90LV804, available in the WQFN (Leadless Leadframe Package) package, minimizes the footprint, and improves system performance.

An output enable pin is provided, which allows the user to place the LVDS outputs and internal biasing generators in a TRI-STATE®, low power mode.

The differential inputs interface to LVDS, and Bus LVDS signals such as those on TI's 10-, 16-, and 18-bit Bus LVDS SerDes, as well as CML and LVPECL. The differential inputs are internally terminated with a 100Ω resistor to improve performance and minimize board space. This function is especially useful for boosting signals over lossy cables or point-to-point backplane configurations.

Block and Connection Diagrams

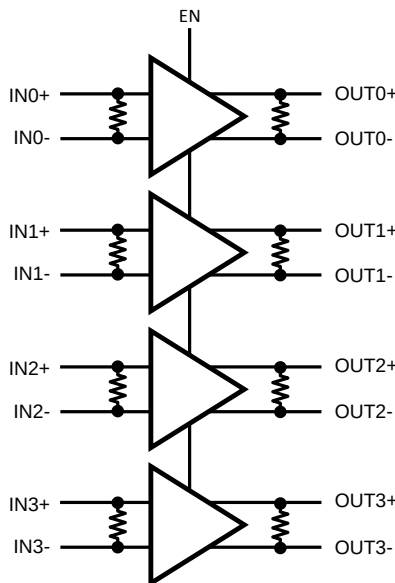
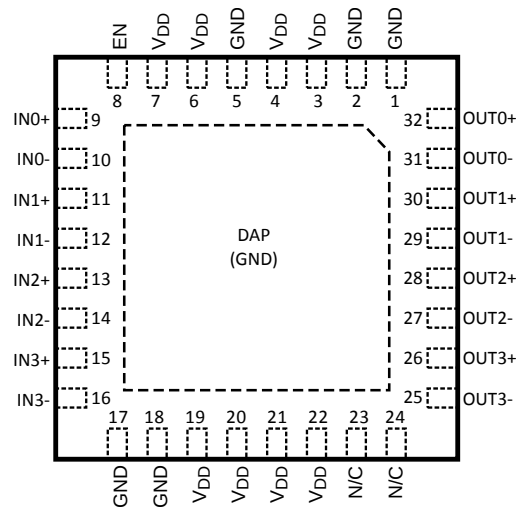


Figure 1. DS90LV804 Block Diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TRI-STATE is a registered trademark of National Semiconductor Corporation.
All other trademarks are the property of their respective owners.



**DS90LV804 WQFN Pinout
(Top View)**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾

Supply Voltage (V_{DD})		-0.3V to +4.0V
CMOS Input Voltage (EN)		-0.3V to ($V_{DD}+0.3V$)
LVDS Input Voltage ⁽²⁾		-0.3V to ($V_{DD}+0.3V$)
LVDS Output Voltage		-0.3V to ($V_{DD}+0.3V$)
LVDS Output Short Circuit Current		+90 mA
Junction Temperature		+150°C
Storage Temperature		-65°C to +150°C
Lead Temperature (Solder, 4sec)		260°C
Max Pkg Power Capacity @ 25°C		4.16W
Thermal Resistance	θ_{JA}	29.5°C/W
	θ_{JC}	3.5°C/W
Package Derating above +25°C		33.3mW/°C
ESD Last Passing Voltage (LVDS output pins)	HBM, 1.5k Ω , 100pF	12 kV
	EIAJ, 0 Ω , 200pF	250V
	Charged Device Model	1000V
ESD Last Passing Voltage (All other pins)	HBM, 1.5k Ω , 100pF	8 kV
	EIAJ, 0 Ω , 200pF	250V
	Charged Device Model	1000V

(1) Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. TI does not recommend operation of products outside of recommended operation conditions.

(2) V_{ID} max < 2.4V

Recommended Operating Conditions

Supply Voltage (V_{CC})	3.15V to 3.45V	
Input Voltage (V_I) ⁽¹⁾	0V to V_{DD}	
Output Voltage (V_O)	0V to V_{DD}	
Operating Temperature (T_A)	Industrial	-40°C to +85°C

(1) $V_{ID} \text{ max} < 2.4\text{V}$

Electrical Characteristics

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ ⁽¹⁾	Max	Units
LVTTTL DC SPECIFICATIONS (EN)						
V _{IH}	High Level Input Voltage		2.0		V _{DD}	V
V _{IL}	Low Level Input Voltage		GND		0.8	V
I _{IH}	High Level Input Current	V _{IN} = V _{DD} = V _{DDMAX}	−10		+10	μA
I _{IL}	Low Level Input Current	V _{IN} = V _{SS} , V _{DD} = V _{DDMAX}	−10		+10	μA
C _{IN1}	Input Capacitance	Any Digital Input Pin to V _{SS}		3.5		pF
V _{CL}	Input Clamp Voltage	I _{CL} = −18 mA	−1.5	−0.8		V
LVDS INPUT DC SPECIFICATIONS (INn±)						
V _{TH}	Differential Input High Threshold ⁽²⁾	V _{CM} = 0.8V to 3.4V, V _{DD} = 3.45V		0	100	mV
V _{TL}	Differential Input Low Threshold ⁽²⁾	V _{CM} = 0.8V to 3.4V, V _{DD} = 3.45V	−100	0		mV
V _{ID}	Differential Input Voltage	V _{CM} = 0.8V to 3.4V, V _{DD} = 3.45V	100		2400	mV
V _{CMR}	Common Mode Voltage Range	V _{ID} = 150 mV, V _{DD} = 3.45V	0.05		3.40	V
C _{IN2}	Input Capacitance	IN+ or IN− to V _{SS}		3.5		pF
I _{IN}	Input Current	V _{IN} = 3.45V, V _{DD} = V _{DDMAX}	−10		+10	μA
		V _{IN} = 0V, V _{DD} = V _{DDMAX}	−10		+10	μA
LVDS OUTPUT DC SPECIFICATIONS (OUTn±)						
V _{OD}	Differential Output Voltage ⁽²⁾	R _L = 100Ω external resistor between OUT+ and OUT−	250	500	600	mV
ΔV _{OD}	Change in V _{OD} between Complementary States		−35		35	mV
V _{OS}	Offset Voltage ⁽³⁾		1.05	1.18	1.475	V
ΔV _{OS}	Change in V _{OS} between Complementary States		−35		35	mV
I _{OS}	Output Short Circuit Current	OUT+ or OUT− Short to GND		−60	−90	mA
C _{OUT2}	Output Capacitance	OUT+ or OUT− to GND when TRI-STATE		5.5		pF
SUPPLY CURRENT (Static)						
I _{CC}	Total Supply Current	All inputs and outputs enabled and active, terminated with external differential load of 100Ω between OUT+ and OUT−.		117	140	mA
I _{CCZ}	TRI-STATE Supply Current	EN = 0V		2.7	6	mA

(1) Typical parameters are measured at $V_{DD} = 3.3\text{V}$, $T_A = 25^\circ\text{C}$. They are for reference purposes, and are not production-tested.

(2) Differential output voltage V_{OD} is defined as $\text{ABS}(\text{OUT+} - \text{OUT-})$. Differential input voltage V_{ID} is defined as $\text{ABS}(\text{IN+} - \text{IN-})$.

(3) Output offset voltage V_{OS} is defined as the average of the LVDS single-ended output voltages at logic high and logic low states.

Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ ⁽¹⁾	Max	Units
SWITCHING CHARACTERISTICS—LVDS OUTPUTS						
t_{LHT}	Differential Low to High Transition Time	Use an alternating 1 and 0 pattern at 200 Mbps, measure between 20% and 80% of V_{OD} ⁽⁴⁾		210	300	ps
t_{HLT}	Differential High to Low Transition Time			210	300	ps
t_{PLHD}	Differential Low to High Propagation Delay	Use an alternating 1 and 0 pattern at 200 Mbps, measure at 50% V_{OD} between input to output.		2.0	3.2	ns
t_{PHLD}	Differential High to Low Propagation Delay			2.0	3.2	ns
t_{SKD1}	Pulse Skew	$ t_{PLHD} - t_{PHLD} $ ⁽⁴⁾		25	80	ps
t_{SKCC}	Output Channel to Channel Skew	Difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels ⁽⁴⁾		50	125	ps
t_{SKP}	Part to Part Skew	Common edge, parts at same temp and V_{CC} ⁽⁴⁾			1.1	ns
t_{JIT}	Jitter ⁽⁵⁾	RJ - Alternating 1 and 0 at 400 MHz ⁽⁶⁾		1.1	1.5	psrms
		DJ - K28.5 Pattern, 800 Mbps ⁽⁷⁾		15	35	psp-p
		TJ - PRBS 2 ²³ -1 Pattern, 800 Mbps ⁽⁸⁾		30	55	psp-p
t_{ON}	LVDS Output Enable Time	Time from EN to OUT± change from TRI-STATE to active.			300	ns
t_{OFF}	LVDS Output Disable Time	Time from EN to OUT± change from active to TRI-STATE.			12	ns

(4) Not production tested. Ensured by statistical analysis on a sample basis at the time of characterization.

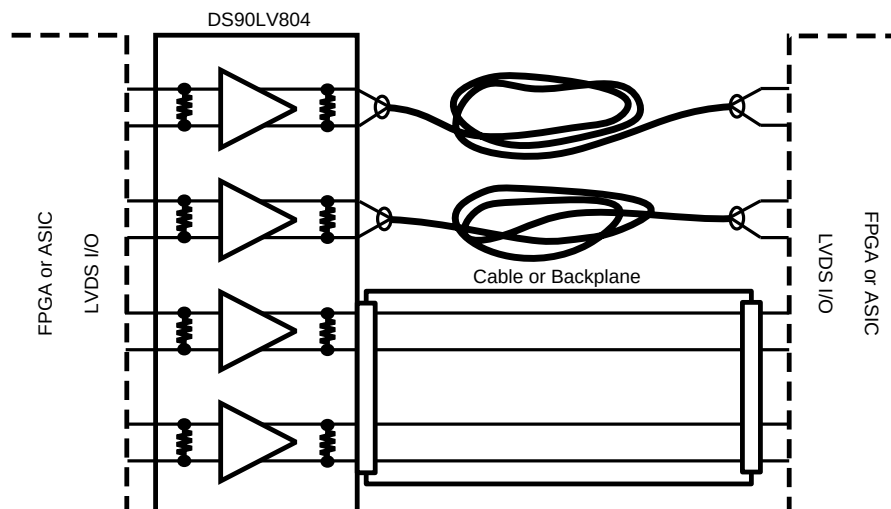
(5) Jitter is not production tested, but ensured through characterization on a sample basis.

(6) Random Jitter, or RJ, is measured RMS with a histogram including 1500 histogram window hits. The input voltage = $V_{ID} = 500\text{mV}$, 50% duty cycle at 400 MHz, $t_r = t_f = 50\text{ps}$ (20% to 80%).

(7) Deterministic Jitter, or DJ, is measured to a histogram mean with a sample size of 350 hits. The input voltage = $V_{ID} = 500\text{mV}$, K28.5 pattern at 800 Mbps, $t_r = t_f = 50\text{ps}$ (20% to 80%). The K28.5 pattern is repeating bit streams of (0011111010 1100000101).

(8) Total Jitter, or TJ, is measured peak to peak with a histogram including 3500 window hits. Stimulus and fixture jitter has been subtracted. The input voltage = $V_{ID} = 500\text{mV}$, 2²³-1 PRBS pattern at 800 Mbps, $t_r = t_f = 50\text{ps}$ (20% to 80%).

Typical Application



APPLICATION INFORMATION

INTERNAL TERMINATIONS

The DS90LV804 has integrated termination resistors on both the input and outputs. The inputs have a 100Ω resistor across the differential pair, placing the receiver termination as close as possible to the input stage of the device. The LVDS outputs also contain an integrated 100Ω ohm termination resistor, this resistor is used to reduce the effects of Near End Crosstalk (NEXT) and does not take the place of the 100 ohm termination at the inputs to the receiving device. The integrated terminations improve signal integrity and decrease the external component count resulting in space savings.

OUTPUT CHARACTERISTICS

The output characteristics of the DS90LV804 have been optimized for point-to-point backplane and cable applications, and are not intended for multipoint or multidrop signaling.

TRI-STATE MODE

The EN input activates a hardware TRI-STATE mode. When the TRI-STATE mode is active (EN=L), all input and output buffers and internal bias circuitry are powered off and disabled. Outputs are tri-stated in TRI-STATE mode. When exiting TRI-STATE mode, there is a delay associated with turning on bandgap references and input/output buffer circuits as indicated in the LVDS Output Switching Characteristics

INPUT FAILSAFE BIASING

External pull up and pull down resistors may be used to provide enough of an offset to enable an input failsafe under open-circuit conditions. This configuration ties the positive LVDS input pin to V_{DD} thru a pull up resistor and the negative LVDS input pin is tied to GND by a pull down resistor. The pull up and pull down resistors should be in the 5kΩ to 15kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point ideally should be set to approximately 1.2V (less than 1.75V) to be compatible with the internal circuitry. Please refer to application note [AN-1194](#) "Failsafe Biasing of LVDS Interfaces" for more information.

INPUT INTERFACING

The DS90LV804 accepts differential signals and allow simple AC or DC coupling. With a wide common mode range, the DS90LV804 can be DC-coupled with all common differential drivers (that is, LVPECL, LVDS, CML). [Figure 2](#), [Figure 3](#), and [Figure 4](#) illustrate typical DC-coupled interface to common differential drivers. Note that the DS90LV804 inputs are internally terminated with a 100Ω resistor.

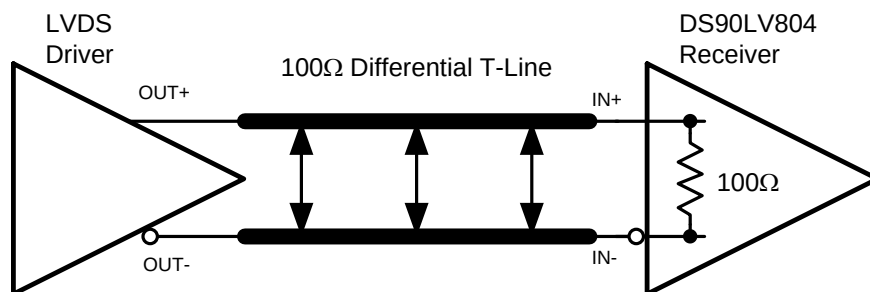


Figure 2. Typical LVDS Driver DC-Coupled Interface to DS90LV804 Input

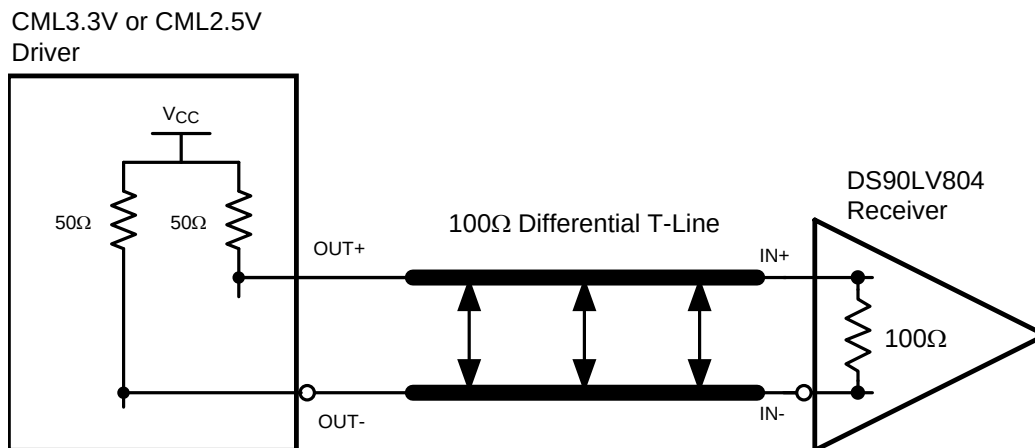


Figure 3. Typical CML Driver DC-Coupled Interface to DS90LV804 Input

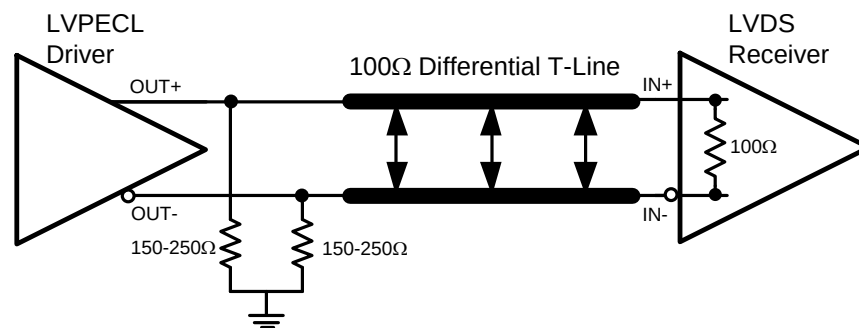


Figure 4. Typical LVPECL Driver DC-Coupled Interface to DS90LV804 Input

OUTPUT INTERFACING

The DS90LV804 outputs signals that are compliant to the LVDS standard. Their outputs can be DC-coupled to most common differential receivers. Figure 5 illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accommodate LVDS compliant signals, it is recommended to check respective receiver's data sheet prior to implementing the suggested interface implementation.

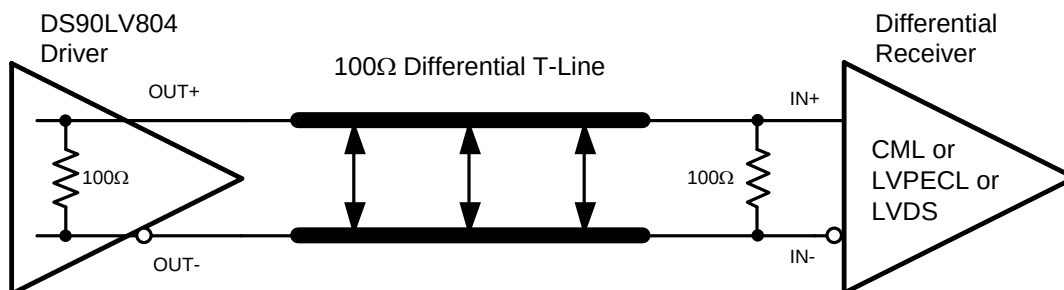


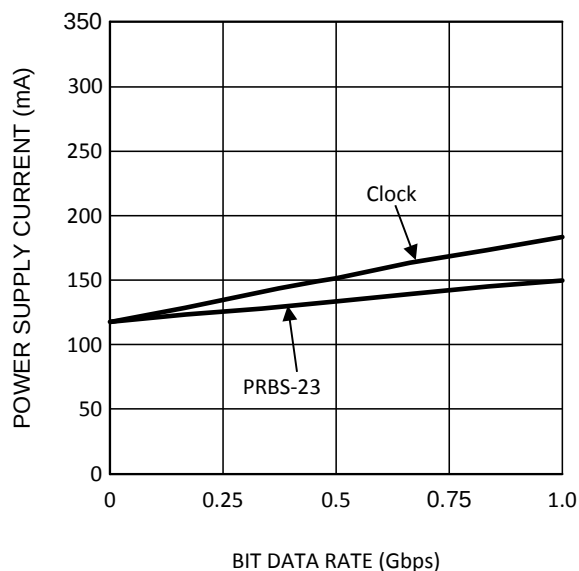
Figure 5. Typical DS90LV804 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

PIN DESCRIPTIONS

Pin Name	WQFN Pin Number	I/O, Type	Description
DIFFERENTIAL INPUTS			
IN0+ IN0–	9 10	I, LVDS	Channel 0 inverting and non-inverting differential inputs.
IN1+ IN1–	11 12	I, LVDS	Channel 1 inverting and non-inverting differential inputs.
IN2+ IN2–	13 14	I, LVDS	Channel 2 inverting and non-inverting differential inputs.
IN3+ IN3–	15 16	I, LVDS	Channel 3 inverting and non-inverting differential inputs.
DIFFERENTIAL OUTPUTS			
OUT0+ OUT0–	32 31	O, LVDS	Channel 0 inverting and non-inverting differential outputs ⁽¹⁾
OUT1+ OUT1–	30 29	O, LVDS	Channel 1 inverting and non-inverting differential outputs ⁽¹⁾
OUT2+ OUT2–	28 27	O, LVDS	Channel 2 inverting and non-inverting differential outputs ⁽¹⁾
OUT3+ OUT3–	26 25	O, LVDS	Channel 3 inverting and non-inverting differential outputs ⁽¹⁾
DIGITAL CONTROL INTERFACE			
EN	8	I, LVTTTL	Enable pin. When EN is LOW, the driver is disabled and the LVDS outputs are in TRI-STATE. When EN is HIGH, the driver is enabled. LVCMOS/LVTTTL level input.
POWER			
V _{DD}	3, 4, 6, 7, 19, 20, 21, 22	I, Power	V _{DD} = 3.3V, ±5%
GND	1, 2, 5, 17, 18 ⁽²⁾	I, Power	Ground reference for LVDS and CMOS circuitry. For the WQFN package, the DAP is used as the primary GND connection to the device. The DAP is the exposed metal contact at the bottom of the WQFN-32 package. It should be connected to the ground plane with at least 4 vias for optimal AC and thermal performance. The pin numbers listed should also be tied to ground for proper biasing.
N/C	23, 24		No Connect

- (1) The LVDS outputs do not support a multidrop (BLVDS) environment. The LVDS output characteristics of the DS90LV804 device have been optimized for point-to-point backplane and cable applications.
- (2) Note that for the WQFN package the GND is connected thru the DAP on the back side of the WQFN package in addition to grounding actual pins on the package as listed.

Typical Performance Characteristics



A. Dynamic power supply current was measured while running a clock or PRBS $2^{23}-1$ pattern with all 4 channels active. $V_{CC} = 3.3V$, $T_A = +25^{\circ}C$, $V_{ID} = 0.5V$, $V_{CM} = 1.2V$

Figure 6. Power Supply Current vs Bit Data Rate

PACKAGING INFORMATION

The Leadless Leadframe Package (WQFN) is a leadframe based chip scale package (CSP) that may enhance chip speed, reduce thermal impedance, and reduce the printed circuit board area required for mounting. The small size and very low profile make this package ideal for high density PCBs used in small-scale electronic applications such as cellular phones, pagers, and handheld PDAs. The WQFN package is offered in the no Pullback configuration. In the no Pullback configuration the standard solder pads extend and terminate at the edge of the package. This feature offers a visible solder fillet after board mounting.

The WQFN has the following advantages:

- Low thermal resistance
- Reduced electrical parasitics
- Improved board space efficiency
- Reduced package height
- Reduced package mass

For more details about WQFN packaging technology, refer to applications note [AN-1187](#), "Leadless Leadframe Package".

REVISION HISTORY

Changes from Revision K (April 2013) to Revision L

Page

- Changed layout of National Data Sheet to TI format [8](#)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS90LV804TSQ/NOPB	Active	Production	WQFN (RTV) 32	1000 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	804TSQ
DS90LV804TSQ/NOPB.A	Active	Production	WQFN (RTV) 32	1000 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	804TSQ
DS90LV804TSQX/NOPB	Active	Production	WQFN (RTV) 32	4500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	804TSQ
DS90LV804TSQX/NOPB.A	Active	Production	WQFN (RTV) 32	4500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	804TSQ

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

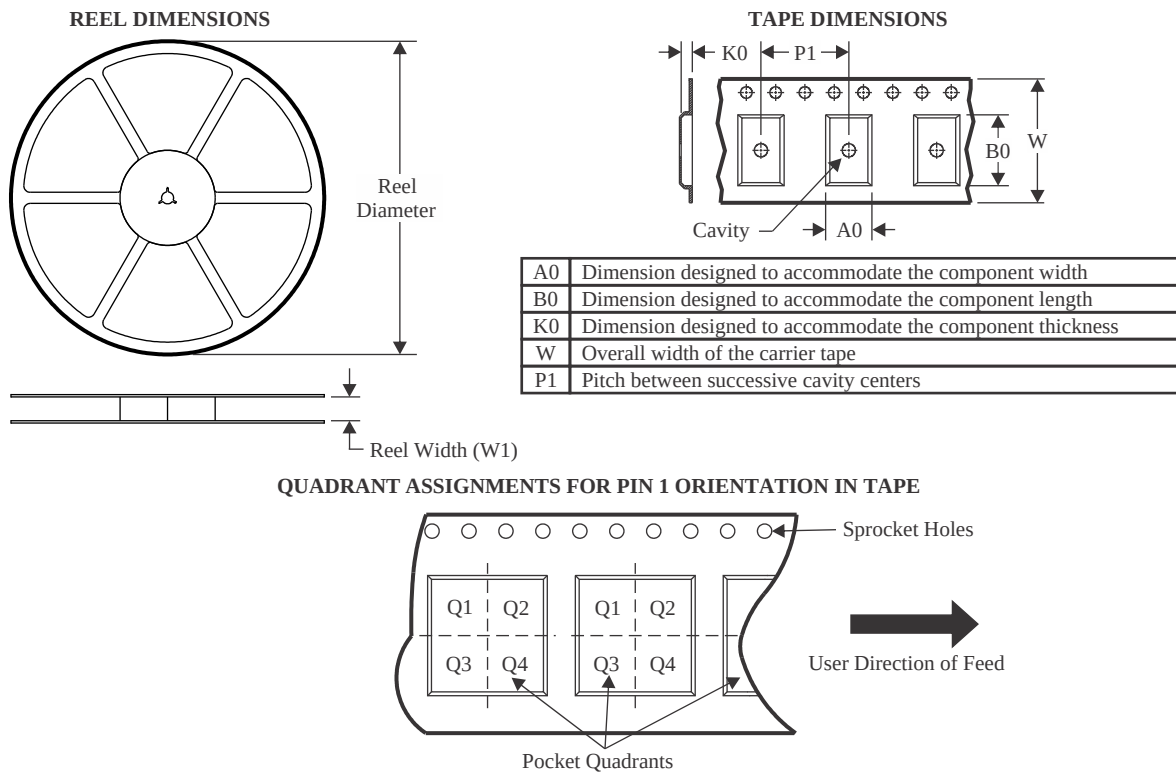
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

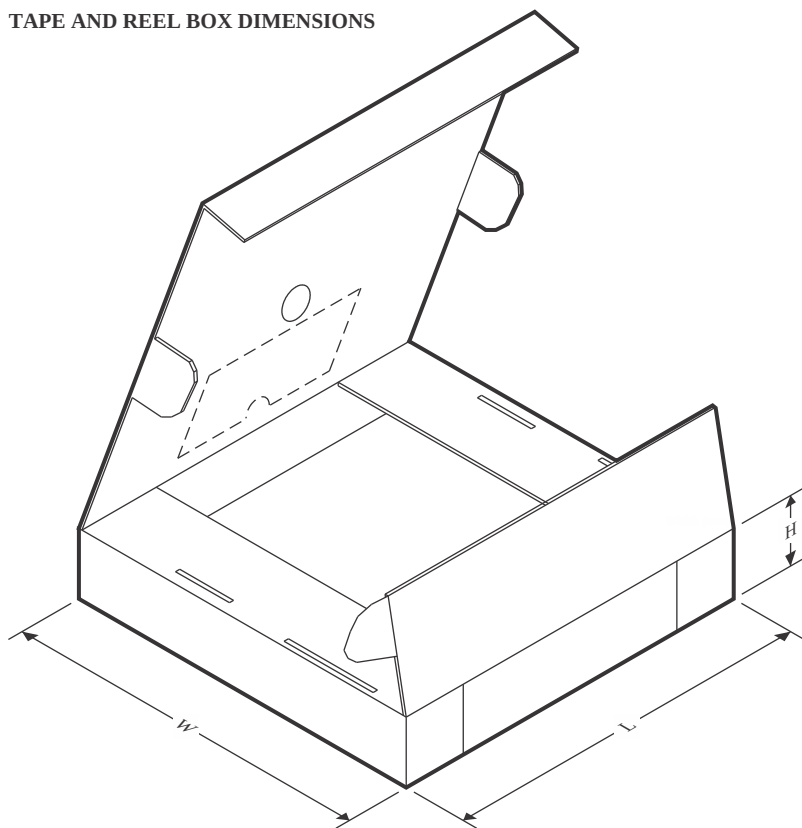
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90LV804TSQ/NOPB	WQFN	RTV	32	1000	177.8	12.4	5.3	5.3	1.3	8.0	12.0	Q1
DS90LV804TSQX/NOPB	WQFN	RTV	32	4500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

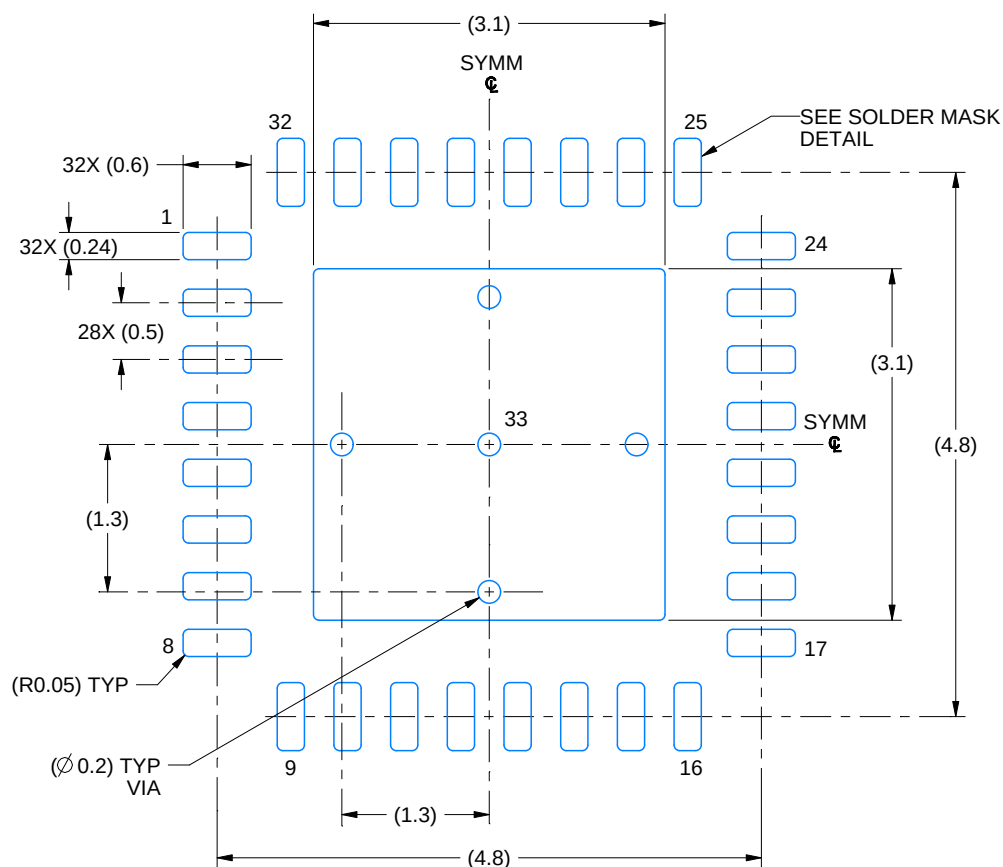
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90LV804TSQ/NOPB	WQFN	RTV	32	1000	208.0	191.0	35.0
DS90LV804TSQX/NOPB	WQFN	RTV	32	4500	356.0	356.0	36.0

EXAMPLE BOARD LAYOUT

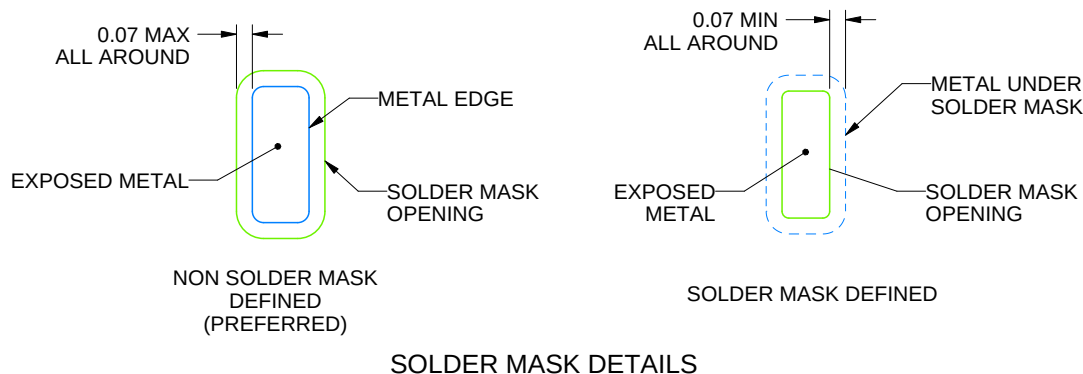
RTV0032A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



4224386/B 04/2019

NOTES: (continued)

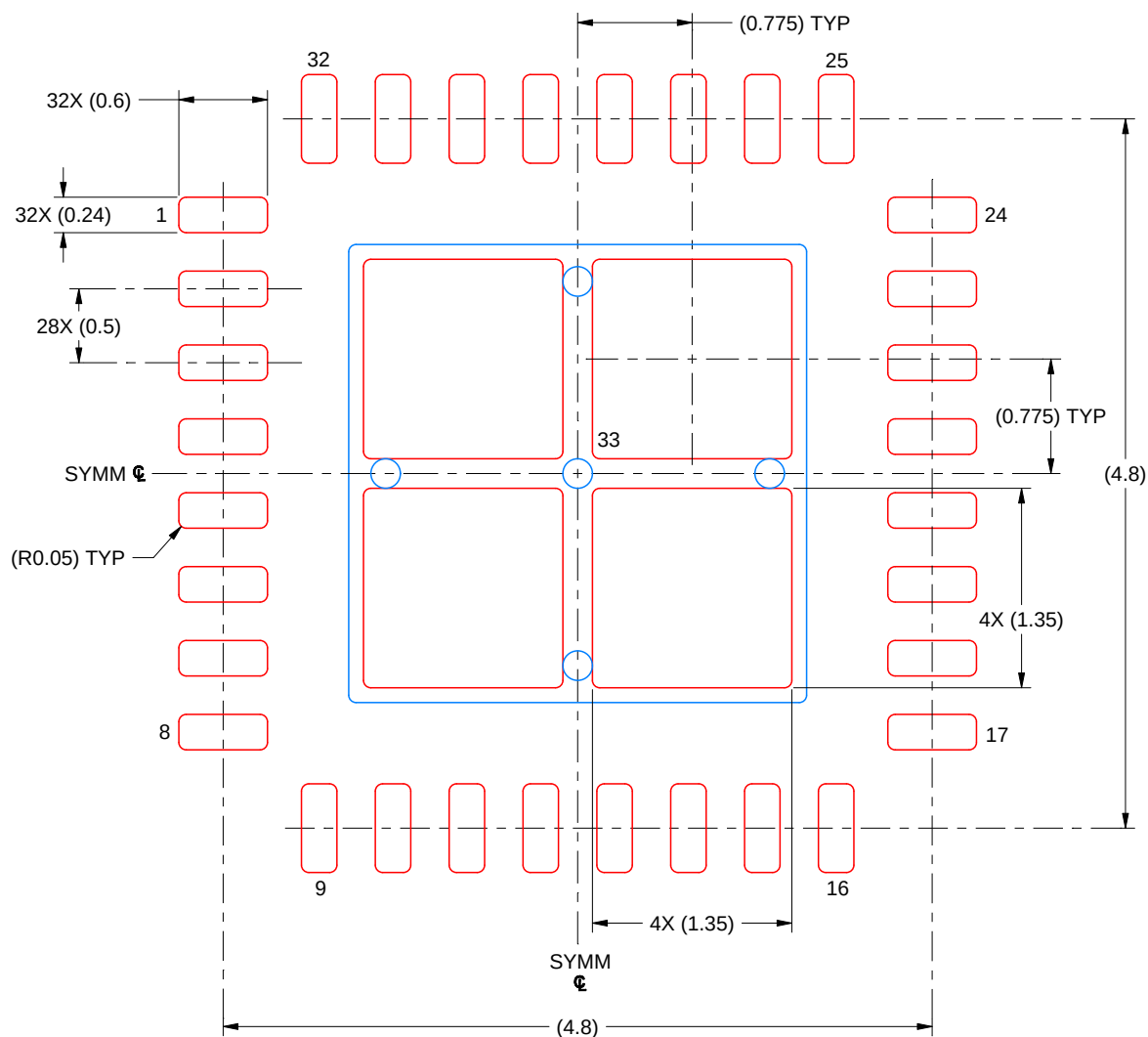
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTV0032A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 MM THICK STENCIL
 SCALE: 20X

EXPOSED PAD 33
 76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224386/B 04/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025