MAXIM

Calibrated 4-Channel 12-Bit ADC with T/H and Reference

MAX182

General Description

The MAX182 is a complete, calibrated 4-channel 12-bit A/D converter (ADC) which includes a precision voltage reference, track-and-hold, and conversion clock. Internal calibration circuitry maintains true 12-bit performance over the full operating temperature range without external adjustments. In addition, each 60µs conversion includes an auto-zero cycle which reduces zero errors to typically below 100µV.

$\overline{\text{CHIP SELECT}}$, $\overline{\text{READ}}$, and $\overline{\text{WRITE}}$ inputs are included for easy microprocessor interfacing without additional logic. 2-byte, 12-bit conversion data is provided over an 8-bit three-state output bus. Either byte may be read first. Two address bits control the 4-channel input multiplexer.

The MAX182's analog input range is 0V to +5V when using a +5V reference. All four high-impedance input channels have excellent matching (typically 0.05 LSB). The MAX182A's internal reference accuracy is ±0.3%, while the MAX182B is intended for use with an external reference.

Applications

Digital-Signal Processing

Audio and Telecom Processing

High-Speed Data Acquisition

High-Accuracy Process Control

Features

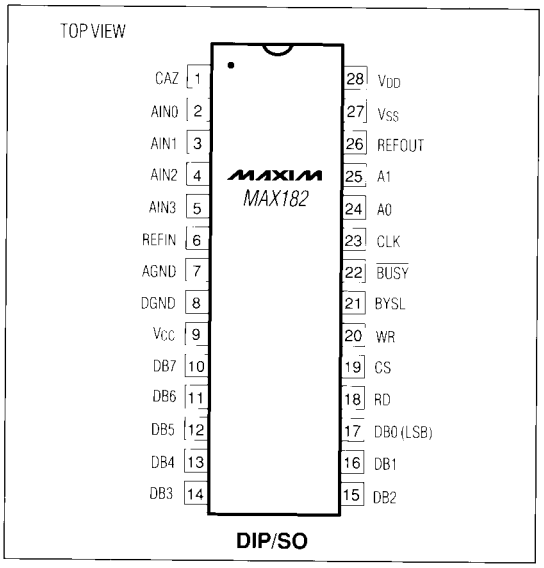
- ♦ **Continuous Transparent Calibration of Offset and Gain**
- ♦ **True 12-Bit Performance without Adjustments**
- ♦ **T/H Front End and Internal Reference**
- ♦ **Four High-Impedance Input Channels**
- ♦ **DC and Dynamically Specified**
- ♦ **Zero Error Typically < 100µV**
- ♦ **Standard Microprocessor Interface**
- ♦ **28-Pin DIP and Wide SO Packages**

Ordering Information

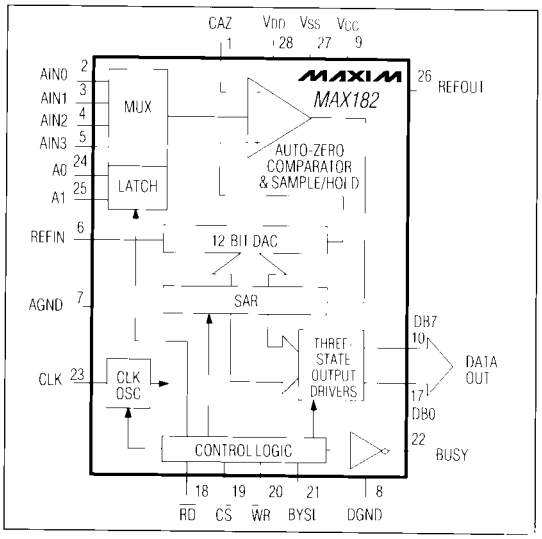
PART	TEMP. RANGE	PIN-PACKAGE
MAX182ACPI	0°C to +70°C	28 Plastic DIP
MAX182BCPI	0°C to +70°C	28 Plastic DIP
MAX182ACWI	0°C to +70°C	28 Wide SO*
MAX182BCWI	0°C to +70°C	28 Wide SO*
MAX182BC/D	0°C to +70°C	Dice**
MAX182AEPI	-40°C to +85°C	28 Plastic DIP
MAX182BEPI	-40°C to +85°C	28 Plastic DIP
MAX182AEWI	-40°C to +85°C	28 Wide SO*
MAX182BEWI	-40°C to +85°C	28 Wide SO*
MAX182AMJI	-55°C to +125°C	28 CERDIP*
MAX182BMJI	-55°C to +125°C	28 CERDIP*

* *Consult factory.*
** *Consult factory for dice specifications*

Pin Configuration



Functional Diagram



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Calibrated 4-Channel 12-Bit ADC with T/H and Reference

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V, +17V
V_{SS} to DGND ..... +0.3V, -7V
AGND to DGND ..... -0.3V, REFIN +0.3V
V_{CC} to DGND ..... -0.3V, +7V
REFIN to AGND ..... -0.3V, V_{DD} +0.3V
AIN to AGND ..... -0.3V, V_{DD} +0.3V
Digital Input Voltage to DGND ..... -0.3V, V_{DD} +0.3V
Digital Output Voltage to DGND ..... -0.3V, V_{DD} +0.3V

Power Dissipation (any Package)
To +75°C 1,000mW
Derate above +75°C by 10mW/C
Operating Temperature Ranges:
MAX182_C ..... 0°C to +70°C
MAX182_E ..... -40°C to +85°C
MAX182_M ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +15V, V_{CC} = +5V, V_{SS} = -5V, REFIN = +5.0V, all specifications T_A = T_{MIN} to T_{MAX}, f_{CLK} =266.67kHz external, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY						
Resolution			12			Bits
Total Unadjusted Error (Note 1)	TUE	AIN0-AIN3			±1	LSB
Differential Nonlinearity	DNL	No missing codes guaranteed			±1	LSB
Full-Scale Error (Gain Error)		AIN0-AIN3, T_A = +25°C			±1/2	LSB
Full-Scale Tempco				0.5		ppm/°C
Zero Error		AIN0-AIN3, T_A = +25°C			±1/2	LSB
Zero Tempco				0.5		ppm/°C
Channel-to-Channel Mismatch					±1/2	LSB
ANALOG INPUT						
Input Voltage Range		V_{REF} = +5V	0		+5	V
On-Channel Input Capacitance	C_{AIN}			8		pF
Input Leakage Current	I_{AIN}	AIN0-AIN3 = 0V to +5V: T_A = +25°C T_A = T_{MIN} to T_{MAX}			10 100	nA
DYNAMIC ACCURACY ($f_{\overline{WR}}$ = 14.81kHz, f_{AIN} = 2.011kHz, T_A = 25°C, Note 2)						
Signal-to-Noise + Distortion	S/(N + D)		70			dB
Total Harmonic Distortion	THD	2kHz Input Signal T_A = +25°C			-80	dB
Peak Harmonic or Spurious Noise					-80	dB
REFERENCE INPUT						
REFIN Range	V_{REFIN}	For specified performance		+5 ±5%		V
		Degraded transfer accuracy	+4		+6	
REFIN Input Current		REFIN = +5V			1.0	mA
REFERENCE OUTPUT						
MAX182A						
REFOUT Voltage		T_A = +25°C	+4.985	+5	+5.015	V
REFOUT Temp (C°)				±10	±40	ppm/°C
REFOUT Sink Current					1	mA
MAX182B Use External Reference Only						

ELECTRICAL CHARACTERISTIC (continued)

(V_{DD} = +15V, V_{CC} = +5V, V_{SS} = -5V, REFIN = +5.0V, all specifications T_A = T_{MIN} to T_{MAX}, f_{CLK} = 266.67kHz external, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS (RD, CS, WR, BYSL, A0, A1)						
Input High Voltage	V_{IH}	V_{CC} = +5V ±5%	+2.4			V
Input Low Voltage	V_{IL}	V_{CC} = +5V ±5%			+0.8	V
Input Current	I_{IN}	V_{IN} = 0 to V_{CC}: T_A = +25°C T_A = T_{MIN} to T_{MAX}			±1 ±10	µA
Input Capacitance	C_{IN}	(Note 3)			10	pF
CLOCK						
Input High Voltage	V_{IH}	V_{CC} = +5V ±5%	+3.0			V
Input Low Voltage	V_{IL}	V_{CC} = +5V ±5%			+0.8	V
Input High Current	I_{IH}	V_{CC} = +5V ±5%			1.5	mA
Input Low Current	I_{IL}	V_{CC} = +5V ±5%			1.2	mA
LOGIC OUTPUTS (DB0-DB7, BUSY)						
Output High Voltage	V_{OH}	V_{CC} = +5V ±5%, I_{SOURCE} = 200µA	+4.0			V
Output Low Voltage	V_{OL}	V_{CC} = +5V ±5%, I_{SINK} = 1.6mA			+0.4	V
Floating State Leakage Current (DB0-DB7)	I_{LKG}	V_{OUT} = 0V to V_{CC}			±1	µA
Floating State Output Capacitance (DB0-DB7)	C_{OUT}	(Note 3)			15	pF
CONVERSION TIME (Note 4)						
With External Clock		f_{CLK} = 266.67kHz	60			µs
With Internal Clock		T_A = +25°C	90		140	µs
POWER REQUIREMENTS (Note 5)						
Power-Supply Voltage	V_{DD}		+11.4		+15.75	V
	V_{SS}		-4.75		-5.25	
	V_{CC}		+4.75		+5.25	
V_{DD} Supply Rejection		V_{DD} = +14.25V to +15.75V, V_{SS} = -5V		±1/8		LSB
V_{SS} Supply Rejection		VSS = -4.75V to -5.25V, V_{DD} = +15V		±1/8		LSB
V_{DD} Supply Rejection		V_{DD} = +11.4V to +12.6V, V_{SS} = -5V		±1/8		LSB
V_{SS} Supply Rejection		V_{SS} = -4.75V to -5.25V, V_{DD} = +12V		±1/8		LSB
Power-Supply Current	I_{DD}	V_{IN} = V_{IL} or V_{IH}		6	10	mA
	I_{SS}				8	
	I_{CC}			0.1	1.0	

Note 1: Includes: Full-Scale Error, Offset Error, Relative Accuracy.
Note 2: Up to 5th Harmonic is measured.
Note 3: Guaranteed by design.
Note 4: Track/Hold aquisition time included in conversion time, using t_{13} condition (see Timing Characteristics).
Note 5: Power-supply current is measured when MAX182 is inactive ($\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = $\overline{BUSY}$ = High).

Calibrated 4-Channel 12-Bit ADC with T/H and Reference

TIMING CHARACTERISTICS (Note 6, Figures 1 and 2)

(V_{DD} = +15V, V_{CC} = +5V, V_{SS} = -5V, REFIN = +5.0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			T_A = -40°C to +85°C			T_A = -55°C to +125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_1		0			0			0			ns
$\overline{WR}$ Pulse Width	t_2		120			120			120			ns
CS to $\overline{WR}$ Hold Time	t_3		0			0			0			ns
$\overline{WR}$ to $\overline{BUSY}$ Propagation Delay	t_4			85	120		100	140		115	160	ns
A0, A1 Valid to $\overline{WR}$ Setup Time	t_5		0			0			0			ns
A0, A1 Valid to $\overline{WR}$ Hold Time	t_6		0			0			0			ns
$\overline{BUSY}$ to $\overline{CS}$ Setup Time	t_7	(Note 3)	0			0			0			ns
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_8		0			0			0			ns
$\overline{RD}$ Pulse Width	t_9		120			120			120			ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{10}		0			0			0			ns
BYSL to $\overline{RD}$ Setup Time	t_{11}		50			50			50			ns
BYSL to $\overline{RD}$ Hold Time	t_{12}		0			0			0			ns
$\overline{RD}$ to Valid Data (Note 7)	t_{13}	(Bus Access Time)		60	100		70	110		90	130	ns
$\overline{RD}$ to Three-State Output (Note 8)	t_{14}	(Bus Relinquish Time)	20		100	20		100	20		100	ns
WR to CLK for 16 Clock Conversions (Note 9)	t_{15}		20			20			20			ns
$\overline{WR}$ to CLK for 17 Clock Conversions (Note 9)	t_{16}		20			20			20			ns

Note 6: Data is timed from V_{OH}, V_{OL}; all input control signals are timed from a voltage level of +1.6V and specified with t_r = t_f = 20ns (10% to 90% of +5V).
Note 7: t_{11}, the time required for an output to cross 0.8V or 2.4V, is measured with the load circuits of Figure 3.
Note 8: t_{12}, the time required for the data lines to change 0.5V, is measured with the load circuits of Figure 4.
Note 9: See Figure 7.

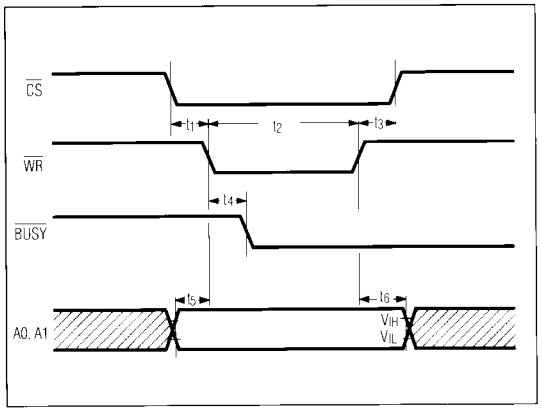

Figure 1: Start Cycle Timing

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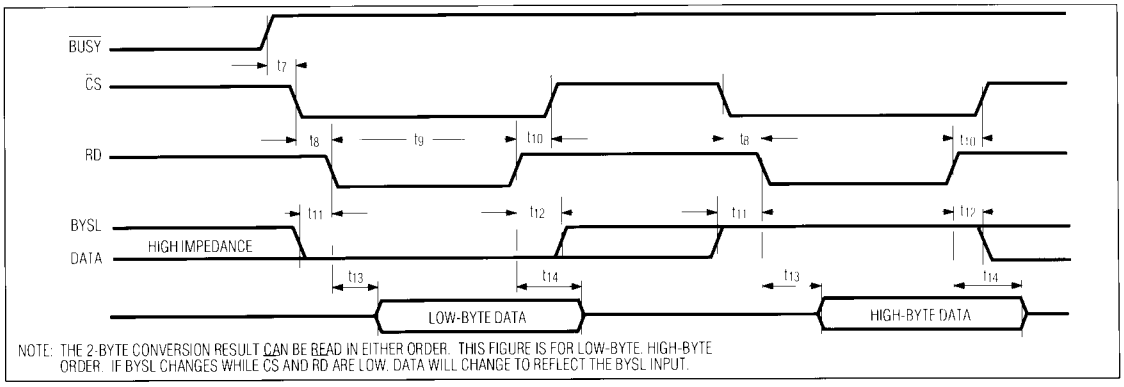
Pin Description

PIN	NAME	FUNCTION
1	CAZ	Auto-Zero Capicitor Input. Connect other end of capacitor to AGND.
2	AIN0	Analog Input for Channel 0
3	AIN1	Analog Input for Channel 1
4	AIN2	Analog Input for Channel 2
5	AIN3	Analog Input for Channel 3
6	REFIN	Voltage Reference Input. The MAX182 is specified with REFIN = +5V.
7	AGND	Analog Ground
8	DGND	Digital Ground
9	V_{CC}	Logic Supply. Digital inputs and outputs are TTL compatible for V_{CC} = +5V.
10-17	DB0-DB7	Three-State Data Outputs. Active when CS and $\overline{RD}$ are brought low. Individual pin functions depend upon BYTE SELECT (BYSL) input.

DATA BUS OUTPUT, $\overline{CS}$, $\overline{RD}$ = LOW		
PIN	BYSL = HIGH	BYSL = LOW
10	BUSY (Note 10)	DB7
11	LOW (Note 11)	DB6
12	LOW (Note 11)	DB5
13	LOW (Note 11)	DB4
14	DB11 (MSB)	DB3
15	DB10	DB2
16	DB9	DB1
17	DB8	DB0 (LSB)

PIN	NAME	FUNCTION
18	$\overline{RD}$	$\overline{READ}$ Input. Used with $\overline{CS}$ to enable the three-state data outputs. RD is active low.
19	$\overline{CS}$	CHIP SELECT Input. Used with either RD or WR for control. $\overline{CS}$ is active low.
20	$\overline{WR}$	$\overline{WRITE}$ Input. In combination with $\overline{CS}$, this active low signal starts a new conversion.
21	BYSL	BYTE SELECT. BYSL selects high- or low-byte output during a data READ operation. ($\overline{RD}$, $\overline{CS}$ = low.) See pins 10-17.
22	$\overline{BUSY}$	Converter Status. $\overline{BUSY}$ is only low during conversion.
23	CLK	CLOCK Input. Internal clock operation with this pin floating and unloaded, typically results in 120µs conversion time (Figure 8). This can be shortened by using an external 74HC clock source (Figure 9).
24	A0	Address input A0. See description of A1.
25	A1	Address Input A1. Address inputs A0 and A1 determine the input channel to be digitized. The address input latch is available when $\overline{CS}$ and $\overline{WR}$ are low. The address inputs are entered by $\overline{WR}$ returning high. A1 A0 Channel Selected 0 0 AIN0 0 1 AIN1 1 0 AIN2 1 1 AIN3
26	REFOUT	Reference Output
27	V_{SS}	Negative Supply Voltage, -5V
28	V_{DD}	Positive Supply Voltage, +15V

Note 10: High during a conversion. *BUSY* is a converter status flag.
Note 11: *When BYSL is high, pins 11-13 output a logic low. The 12-bit digital result is in DB0-DB11.* DB11 is the MSB.



NOTE: THE 2-BYTE CONVERSION RESULT CAN BE READ IN EITHER ORDER. THIS FIGURE IS FOR LOW-BYTE, HIGH-BYTE ORDER. IF BYSL CHANGES WHILE CS AND RD ARE LOW, DATA WILL CHANGE TO REFLECT THE BYSL INPUT.

Figure 2. Read Cycle Timing

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Detailed Operation

Operating Information

Figure 5 shows an operational diagram for the MAX182. The only required passive components are a hold capacitor (CAZ) and a reference bypass capacitor and resistor. Individual pin functions are listed in the Pin Description table.

On-Chip Clock Operation

The on-chip oscillator requires no external components. Therefore, the CLK pin can be left unconnected resulting in a typical 120µs conversion time. The conversion time can be increased by adding a capacitive load on the CLK pin. The timing diagrams in Figures 6 and 7 show the resulting tracking duration for relative positions of $\overline{WR}$ and CLK. Figure 8 is a schematic for on-chip clock operation.

A new conversion is initiated by bringing $\overline{WR}$ low, with $\overline{CS}$ low. This starts a track acquisition sequence. In this state, the T/H goes into track mode. Capacitor CAZ charges to the analog input voltage minus the input offset voltage of the comparator. Note: when $\overline{WR}$ is low (with $\overline{CS}$ low), the MAX182 is in track mode. When $\overline{WR}$ goes high, tracking time is extended by another 4 to 5 clock periods (4 clock periods beginning with the first falling clock edge following the rising edge of $\overline{WR}$). 16 to 17 clock periods are required for each conversion (Figure 7).

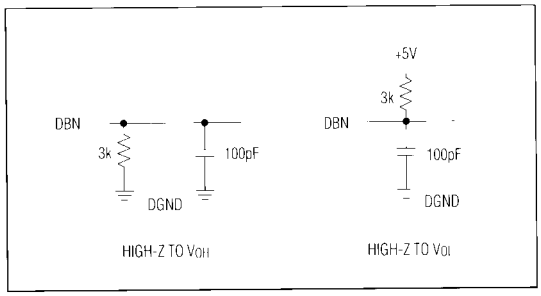

Figure 3. Load Circuits for Access Time Test (t_{13})

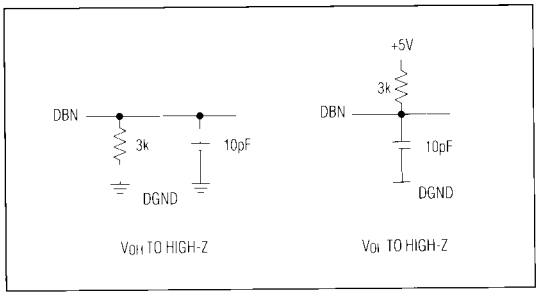

Figure 4. Load Circuits for Output Three-State Delay Test (t_{14})

The MAX182 is in track mode between conversions when $\overline{BUSY}$ is high. After the tracking sequence, the most significant bit (MSB) decision is made. Following this, the remaining 11 bits are digitized on successive clock cycles, as indicated in Figure 6. The $\overline{WR}$ pulse need not be synchronized with the internal clock.

External Clock Operation

For external clock operation, drive the CLK input with a 74HC compatible clock source (Figure 9).

The MAX182 automatically tracks for the appropriate time by means of an on-chip counter. Both $\overline{WR}$ and $\overline{CS}$ must be low to initiate a new conversion. Whenever $\overline{WR}$ and $\overline{CS}$ are low, the chip enters into track mode until WR or $\overline{CS}$ rises. After the rising edge of $\overline{WR}$, the next falling edge of the clock starts a counter, which extends the tracking time by 4 to 5 external clock periods.

The analog input acquisition is complete at the end of the tracking period, and the signal is stored in the internal track-and-hold. The external clock source need not be synchronized with the $\overline{WR}$ pulse.

Reading Data

The 12-bit result of a conversion plus the converter status flag are accessible over an 8-bit data bus. The data is available from the MAX182 in right-justified format (the least significant bit (LSB) is the right-most bit in a 16-bit word). Two byte sized read operations are needed. The Byte Select (BYSL) input determines which byte is to be read first, 8LSBs or 4MSBs plus status flag.

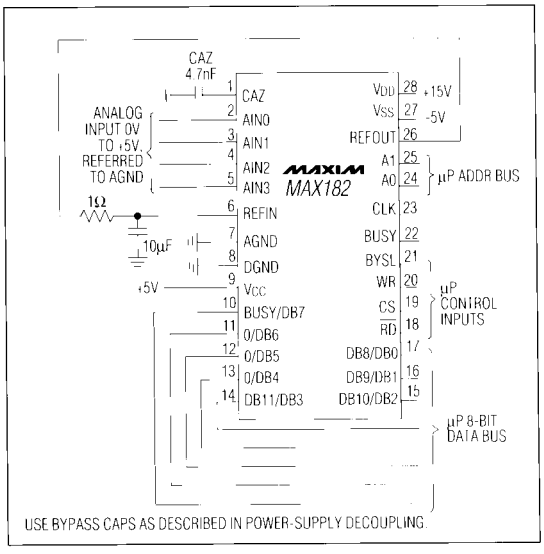

Figure 5. MAX182 Operational Diagram

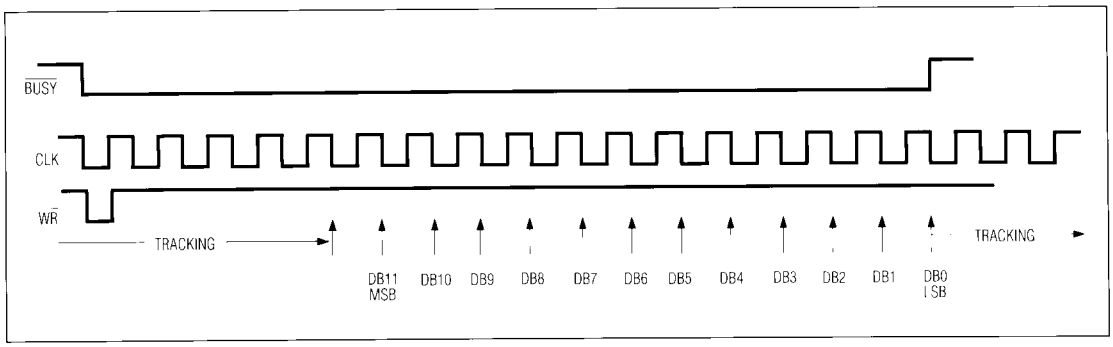

Figure 6. MAX182 Timing Diagram

It is necessary to wait for the end of a conversion to obtain valid 12-bit data from the MAX182's successive approximation register (SAR). If a read instruction is performed during a conversion, the MAX182 will dump the existing contents of the SAR onto the data bus. There are three methods to ensure correct operation:

1. Insert a software delay longer than the ADC conversion time between the conversion start and the data read operations.
2. The $\overline{BUSY}$ output is low during the conversion and high at the conversion end. Use this signal as an interrupt to the µP.
3. Poll the converter status flag, BUSY, at user-defined intervals after a conversion start. The status flag is available on DB7 during a high-byte $\overline{READ}$. The flag is the left-most bit and can be shifted directly into the µP's carry flag for testing. BUSY is high during a conversion.

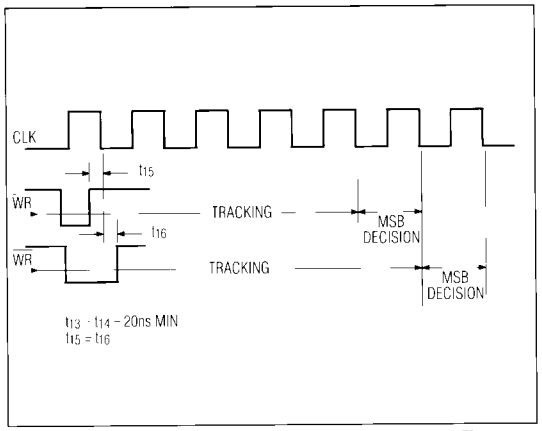

Figure 7. Width of Tracking Interval as a Function of $\overline{WR}$ Rising Edge Timing with Respect to CLK Falling Edge

A write operation to the MAX182 during a conversion restarts the conversion.

Application Hints

Auto-Zero Capacitor (CAZ)

CAZ (Figure 5) must be a low-leakage, low-dielectric absorption capacitor such as polypropylene, polystyrene, or teflon. Connect the outside foil of CAZ to AGND to minimize noise. CAZ should be 4,700pF.

Clock

Figure 10 shows typical conversion time versus temperature when using the MAX182's on-chip clock. Due to variations in manufacturing, the actual operating frequency can differ from chip-to-chip by up to 20%. For this reason, it is suggested that an external clock be used when fixed conversion times are required.

Analog Inputs

The high-impedance analog inputs, AIN0-AIN3, allow simple analog interfacing. Signal sources from 0V to +5V may be connected directly to AIN without extra buffering for source impedances up to 5kΩ (Figure 11). The input/output (I/O) transfer characteristic and transition

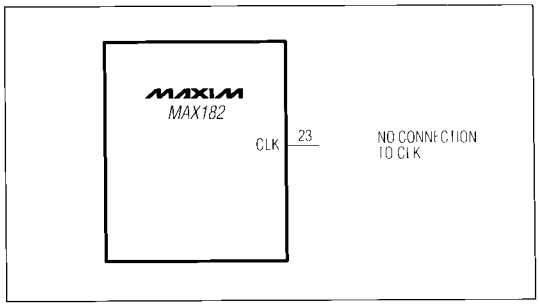

Figure 8. Internal Clock Operation

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points for this input signal range are demonstrated in Figure 12 and Table 1. The MAX182 transfer characteristic has transition points designed to occur on integer multiples of 1LSB. The output code is natural binary with:

1LSB = (Full Scale (FS))/4096
= (5/4096)V = 1.22mV.

For signal ranges other than 0V to +5V, use resistor divider networks to provide 0V to +5V signal ranges at the MAX182 input pins. The connection in Figure 13 shows a divider network on channel 0 for a 0V to +10V signal range. Resistors should be of the same type and manufacturer to ensure matched temperture coefficients. The source impedance must now be as low as possible since it adds to the resistor divider impedance.

Figure 14 shows how bipolar signals (-5V to +5V) on channel 0 are accommodated by referencing a resistor divider network to REFIN. The signal source must be capable of sinking 0.5mA with the resistor values shown. Refer to Figure 15 and Table 2 for the I/O transfer characteristic and transition points for this signal range. Output coding is offset binary with an LSB size of:

(FS)(1/4096) = (10/4096)V = 2.44mV.

To adjust bipolar zero error apply 1.22mx (+1/2LSB) to AIN0-AIN3 so that the ADC output switches between 1000 0000 0000 and 1000 0000 0001.

Power-Supply Decoupling

Power supplies to the MAX182 should be bypassed with either a 10µF electrolytic or tantulum capacitor in parallel with a 0.01µF disc ceramic capacitor for clean, high-frequency performance. Place all capacitors as close as possible to the MAX182 supply pins. Figure 16 shows preferred decoupling circuit.

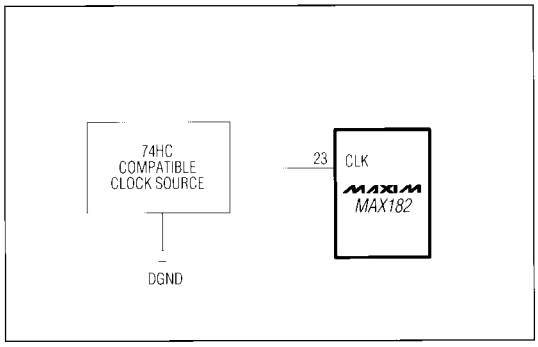


Figure 9. External Clock Operation

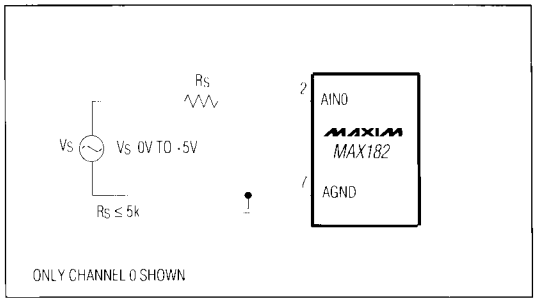


Figure 11. Unipolar 0V to +5V Operation

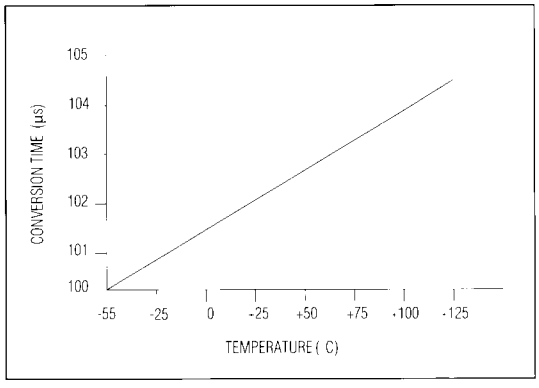


Figure 10. Typical Change in Conversion Time Variation vs. Temperature when Using Internal Clock

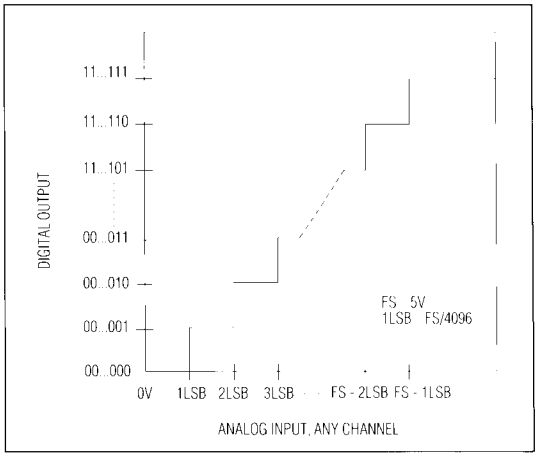


Figure 12. Ideal Input/Output Transfer Characteristic for Unipolar Circuit of Figure 11

Internal Reference

The internal reference (REFOUT) should be bypassed with a 1Ω resistor in series with a capacitor. The capacitor should be a 10µF electrolytic or tantalum in parallel with a 0.01µF disc ceramic (Figure 17). Figure 18 shows a circuit that allows input adjustment which is useful for trimming out initial (room temperature) error in the reference voltage.

Table 1. Transition Points for Unipolar 0V to +5V Operation

Analog Input (V)	Digital Output
0.00122	0000 0000 0001
0.00244	0000 0000 0010
. . .	. . .
2.49878	0111 1111 1111
2.50000	1000 0000 0000
2.50122	1000 0000 0001
. . .	. . .
4.99756	1111 1111 1110
4.99878	1111 1111 1111

Table 2. Transition Points for Bipolar -5V to +5V Operation

Analog Input (V)	Digital Output
-4.99878	0000 0000 0001
-4.99634	0000 0000 0010
. . .	. . .
-0.00122	1000 0000 0000
+0.00122	1000 0000 0001
. . .	. . .
+4.99389	1111 1111 1110
+4.99634	1111 1111 1111

External Reference Circuit

Figure 18 shows how to a MX584LH to generate a reference voltage of 5.00V. A typical adjustment range of 75mV is provided by R2. Over the commercial temperature range, the MX584LH contributes no more than ±1LSB of gain error.

During a conversion, transient currents flow at the REFIN input. To prevent dynamic errors, place either a 10µF electrolytic or tantalum smoothing capacitor in parallel with a 0.01µF disc ceramic from the REFIN pin to AGND.

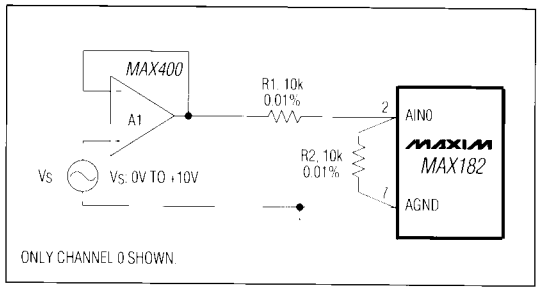


Figure 13. Unipolar 0V to +10V Operation

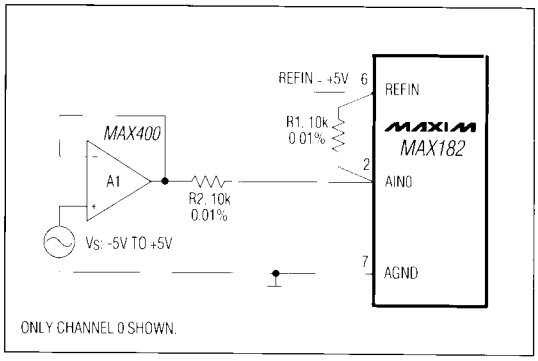


Figure 14. Bipolar -5V to +5V Operation

Calibrated 4-Channel 12-Bit ADC with T/H and Reference

Layout

When designing a layout for a printed circuit board, keep digital and analog signal lines separated whenever possible. It is critical that no digital line runs alongside an analog signal line or near the CAZ. Guard the analog inputs, the reference input and the CAZ input with AGND.

Establish a single-point analog ground (AGND) as close to the MAX182 as possible, isolated from the logic system. Connect the single-point analog ground to the digital system ground, which is attached to DGND at one point, as close as possible to the MAX182. The following should be returned to the analog ground point: input-signal common, input guards, the CAZ, and any bypass capacitors for the reference input and the analog supplies. Low-impedance analog and digital power-supply common returns with wide trace widths are essential for quiet operation of the MAX182.

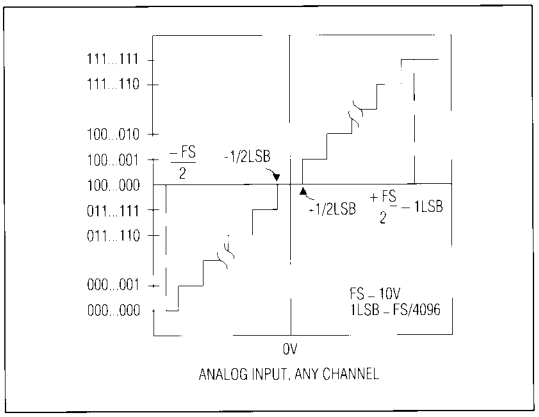


Figure 15. Ideal Input/Output Transfer Characteristic for Bipolar Circuit of Figure 14

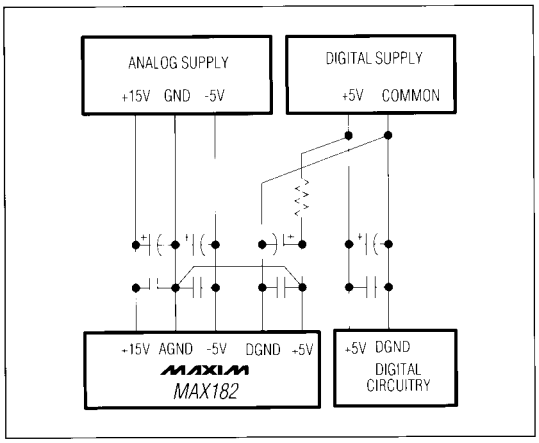


Figure 16. Power-Supply Grounding

Noise

To minimize input noise coupling, input signal leads to AIN and signal return leads from AGND should be kept as short as possible. A shielded cable between source and ADC is suggested in applications where longer leads are required. Also, care should be taken to reduce ground circuit impedances as much as possible since any potential difference in grounds between the signal source and ADC creates an error voltage in series with the input signal.

When interfacing to continuously busy and noisy µP buses, it is possible to get errors at the LSB level. These errors exist because of feedthrough from the bus to the integrated circuit through the package. The problem can be minimized in ceramic packaged chips by grounding the metal lid. Another solution is to isolate the MAX182 from the noisy µP bus using three-state buffers.

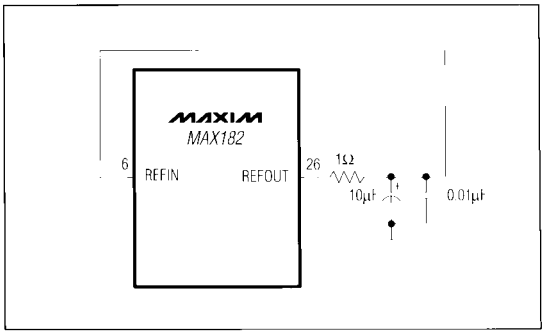


Figure 17. Internal Reference Hookup.

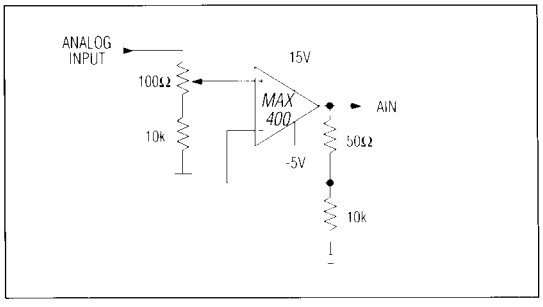


Figure 18. Adjusting Analog Input Gain to Trim Out Initial Reference Voltage Error

Dynamic Performance

High-speed sampling capability and 14kHz throughput make the MAX182 ideal for wideband signal processing. To support these and other related applications, fast fourier transform (FFT) test techniques are used to guarantee the ADC's dynamic frequency response, distortion, and noise at the rated throughput. Specifically, this involves applying a low-distortion sinewave to the ADC input and recording the digital conversion results for a specified time. The data is then analyzed using an FFT algorithm which determines its spectral content. Conversion errors are then seen as spectral elements outside of the fundamental input frequency.

ADCs have traditionally been evaluated by specifications such as zero and full-scale error, integral nonlinearity and differential non-linearity. Such parameters are widely accepted for specifying performance with DC and slowly varing signals but are less useful in signal-processing appications where the ADCs impact on the system transfer function is the main concern. The significance of various DC errors does not translate well to the dynamic case, so different tests are required.

Signal-to-Noise Ratio and Effective Number of Bits

The ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other A/D output signals is the signal-to-noise ratio (SNR). The output band is limited to frequencies above DC and below one half the A/D sample (conversion) rate. This usually (but not always) includes distortion as well as noise components. For this reason, the ratio is sometimes referred to as "signal-to-noise + distortion".

The theoretical minimum A/D noise is caused by quantization error and is a direct result of the ADC's resolution: SNR = (6.02N + 1.76)dB, where N is the number of bits of resolution. A perfect 12-bit ADC can do no better than 74dB. Figure 20 shows the result of sampling a pure 10kHz sinusoid at a 100kHz rate with the MAX182. An FFT plot of the output shows the output level in various spectral bands.

By transposing the equation that converts resolution to SNR, we can, from the measured SNR, determine the effective resolution or the "effective number of bits" that the A/D provides: N = (SNR -1.76)/6.02.

Total Harmonic Distortion

The ratio of the RMS sum of all harmonics of the input signal (in the frequency band above DC and below one half the sample rate) to the fundamental itself is total harmonic distortion (THD). This is expressed as:

$$THD = 20Log[\sqrt{(V_2^2 + V_3^3 + V_4^2 + V_4^2 + \ldots + V_N^2)}/V_1]$$

where V_1 is the fundamental RMS amplitude and V_2 to V_N are the amplitudes of the 2nd through Nth harmonics.

Peak Harmonic or Spurious Noise

The ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one half the sample rate) is referred to as the peak harmonic or spurious noise. Usually this peak occurs at some harmonic of the input frequency. But if the ADC is exceptionally linear, it may occur only at a random peak in the ADC's noise floor.

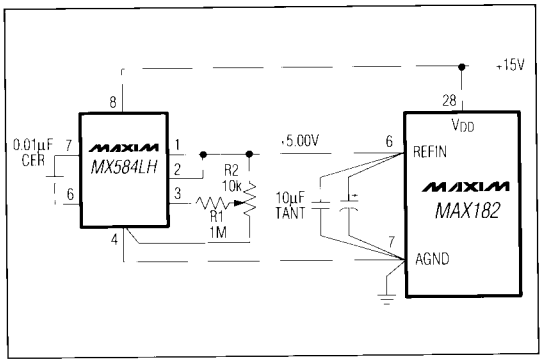


Figure 19. MX584LH as Reference Generator

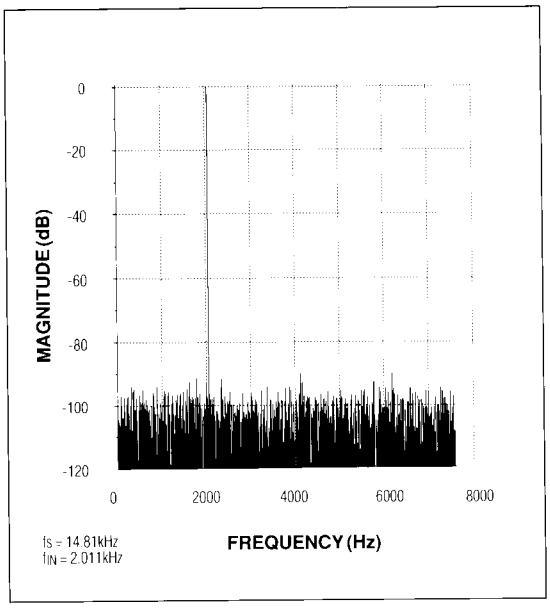
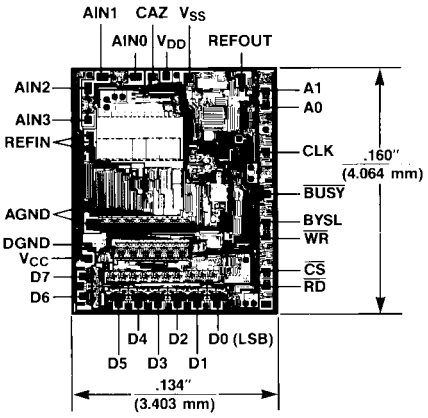


Figure 20. FFT Plot for the MAX182

Calibrated 4-Channel 12-Bit ADC with T/H and Reference

Chip Topography



MAX182

* Substrate internally connected to V_{DD}.

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