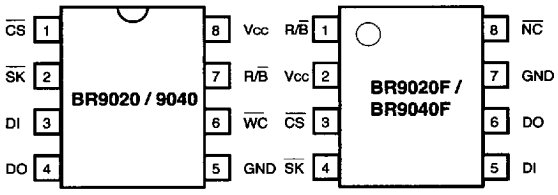
2,048/4,096-Bit Serial Electrically Erasable PROM

BR9020/BR9020F
BR9040/BR9040F

●Features

- Low power CMOS technology
- 128 x 16 bits configuration (BR9020/F)
  256 x 16 bits configuration (BR9040/F)
- 2.7V to 5.5V operation
- 4-wire Bus Interface
- 1MHz Clock Rate
- Low power consumption
  – 1.5mA (max.) active current : 3V
  – 2 μA (max.) stanby current : 3V
- Automatic erase-before-write
- Hardware and Software write Protection
  – Default to write-disable state at power up
  – Software instructions for write-enable/disable
  – Vcc lockout inadvertent write protection
- 8-pin SOP/8-pin DIP pockages
- Device status signal during write cycle (R/$\overline{B}$ pin & DO pin)
- 100,000 Erase/write cycles
- 10 years Data Retention

●Pin configuration



●Pin name

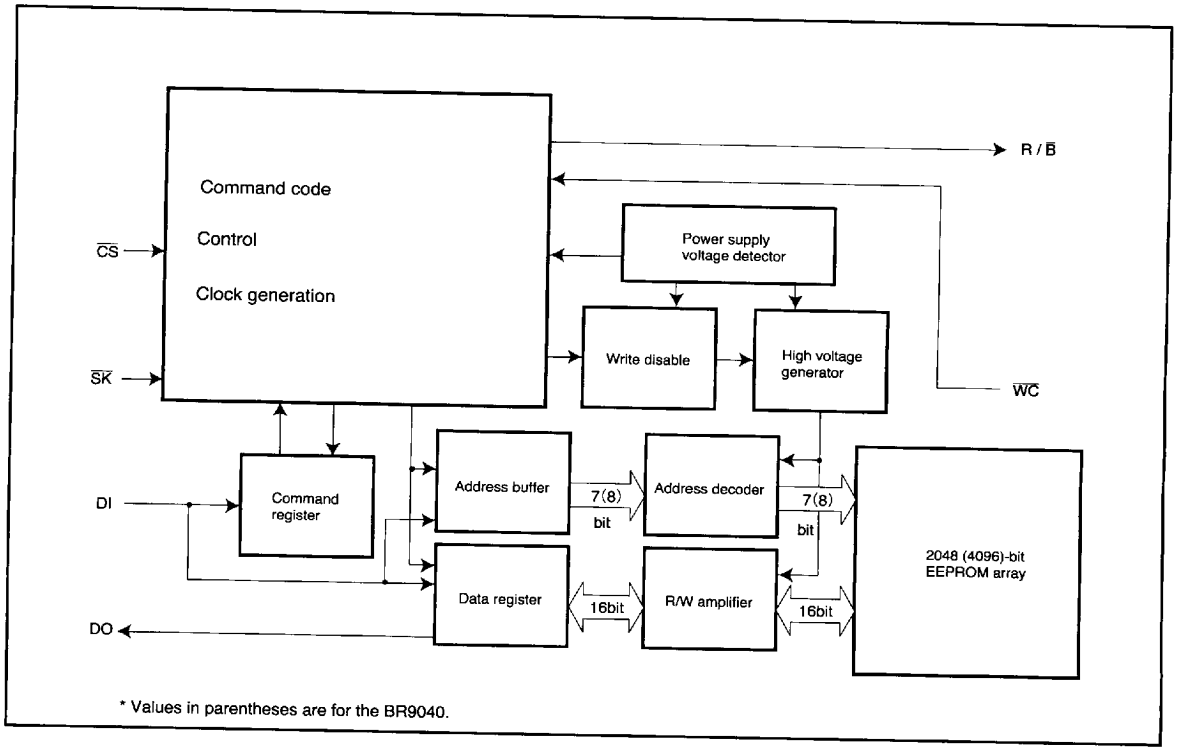
Pin Name	Function
$\overline{CS}$	Chip select input
$\overline{SK}$	Serial data clock input
DI	Operating code, address, and serial data input
DO	Serial data output
GND	Reference voltage for all I/O, 0 V
$\overline{WC}$	Write control input
R/$\overline{B}$	READY, $\overline{BUSY}$ status signal output
Vcc	Power supply connection

●Overview

The BR9020, BR9020F, BR9040, and BR9040F are serial EEPROMs that can be connected directed to a serial port and can be erased and written to electrically. The BR9020/F is configured of 128 words × 16 bits, and the BR9040/F of 256 words × 16 bits.

Writing is performed in word units, using four types of operation commands. The commands are synchronized to the $\overline{SK}$ pin (serial clock input), and data is read through the DI pin and output from the DO pin. $\overline{WC}$ pin control is used to initiate a write disabled state, enabling these EEPROMs to be used as one-time ROMs. During writing, operation can be checked from the R/$\overline{B}$ pin and the DO pin.

●Block diagram



* Values in parentheses are for the BR9040.

●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Limits		Unit
Applied voltage	Vcc	−0.3~7.0		V
Power dissipation	Pd	DIP8	500*1	mW
		SOP8	350*2	
Storage temperature	Tstg	−65~125		℃
Operating temperature	Topr	−40~85		℃
Terminal voltage	—	−0.3~Vcc+0.3		V

*1 Reduced by 5.0mW for each increase in Ta of 1°C over 25°C.
*2 Reduced by 3.5mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions

Parameter	Symbol	Limits	Unit
Power supply voltage	Vcc	2.7~5.5 (WRITE)	V
		2.0~5.5 (READ)	V
Input voltage	VIN	0~Vcc	V

●Electrical characteristics

BR9020/F : At 5V (Unless otherwise noted, Ta=-40 to 85℃, V_{CC}=5V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
"L" input voltage 1	V_{IL1}	—	—	0.3×V_{CC}	V	DI pin
"H" input voltage 1	V_{IH1}	0.7×V_{CC}	—	—	V	DI pin
"L" input voltage 2	V_{IL2}	—	—	0.2×V_{CC}	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ pin
"H" input voltage 2	V_{IH2}	0.8×V_{CC}	—	—	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ pin
"L" output voltage	V_{OL}	0	—	0.4	V	I_{OL}=2.1mA
"H" output voltage	V_{OH}	V_{CC}−0.4	—	V_{CC}	V	I_{OH}=−0.4mA
Input leakage current	I_{LI}	−1	—	1	μA	V_{IN}=0V~V_{CC} $\overline{CS}$=V_{CC}
Output leakage current	I_{LO}	−1	—	1	μA	V_{OUT}=0V~V_{CC} $\overline{CS}$=V_{CC}
Operating current consumption	I_{CC1}	—	—	2	mA	f_{SK}=1MHz tE / W=10mS (WRITE)
	I_{CC2}	—	—	1	mA	f_{SK}=1MHz (READ)
Standby current	I_{SB}	—	—	3	μA	$\overline{CS}$,$\overline{SK}$,DI,$\overline{WC}$,=V_{CC} DO,R / $\overline{B}$=OPEN
$\overline{SK}$ frequency	f_{SK}	—	—	1	MHz	—

BR9020/F : At 3V (Unless otherwise noted, Ta=-40 to 85℃, V_{CC}=3V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
"L" input voltage 1	V_{IL1}	—	—	0.3×V_{CC}	V	DI pin
"H" input voltage 1	V_{IH1}	0.7×V_{CC}	—	—	V	DI pin
"L" input voltage 2	V_{IL2}	—	—	0.2×V_{CC}	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ pin
"H" input voltage 2	V_{IH2}	0.8×V_{CC}	—	—	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ pin
"L" output voltage	V_{OL}	0	—	0.4	V	I_{OL}=100 μA
"H" output voltage	V_{OH}	V_{CC}−0.4	—	V_{CC}	V	I_{OH}=−100 μA
Input leakage current	I_{LI}	−1	—	1	μA	V_{IN}=0V~V_{CC}
Output leakage current	I_{LO}	−1	—	1	μA	V_{OUT}=0V~V_{CC} $\overline{CS}$=V_{CC}
Operating current consumption	I_{CC1}	—	—	1.5	mA	f_{SK}=1MHz tE / W=15mS (WRITE)
	I_{CC2}	—	—	500	μA	f_{SK}=1MHz (READ)
Standby current	I_{SB}	—	—	2	μA	$\overline{CS}$,$\overline{SK}$,DI,$\overline{WC}$,=V_{CC} DO,R / $\overline{B}$=OPEN
$\overline{SK}$ frequency	f_{SK}	—	—	1	MHz	—

BR9040/F : At 5V (Unless otherwise noted, Ta=-40 to 85℃, V_{CC}=5V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
"L" input voltage 1	V_{IL1}	—	—	0.3×V_{CC}	V	DI pin
"H" input voltage 1	V_{IH1}	0.7×V_{CC}	—	—	V	DI pin
"L" input voltage 2	V_{IL2}	—	—	0.2×V_{CC}	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ pin
"H" input voltage 2	V_{IH2}	0.8×V_{CC}	—	—	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ pin
"L" output voltage	V_{OL}	0	—	0.4	V	I_{OL}=2.1mA
"H" output voltage	V_{OH}	V_{CC}−0.4	—	V_{CC}	V	I_{OH}=−0.4mA
Input leakage current	I_{LI}	−1	—	1	μA	V_{IN}=0V~V_{CC} $\overline{CS}$=V_{CC}
Output leakage current	I_{LO}	−1	—	1	μA	V_{OUT}=0V~V_{CC} $\overline{CS}$=V_{CC}
Operating current consumption	I_{CC1}	—	—	2	mA	$f_{\overline{SK}}$=1MHz tE / W=10mS (WRITE)
	I_{CC2}	—	—	1	mA	$f_{\overline{SK}}$=1MHz (READ)
Standby current	I_{SB}	—	—	3	μA	$\overline{CS}$,$\overline{SK}$,DI,$\overline{WC}$,=V_{CC} DO,R / $\overline{B}$=OPEN
$\overline{SK}$ frequency	f_{SK}	—	—	1	MHz	—

BR9040/F : At 3V (Unless otherwise noted, Ta=-40 to 85℃, V_{CC}=3V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
"L" input voltage 1	V_{IL1}	—	—	0.3×V_{CC}	V	DI pin
"H" input voltage 1	V_{IH1}	0.7×V_{CC}	—	—	V	DI pin
"L" input voltage 2	V_{IL2}	—	—	0.2×V_{CC}	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ pin
"H" input voltage 2	V_{IH2}	0.8×V_{CC}	—	—	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ pin
"L" output voltage	V_{OL}	0	—	0.4	V	I_{OL}=100 μA
"H" output voltage	V_{OH}	V_{CC}−0.4	—	V_{CC}	V	I_{OH}=−100 μA
Input leakage current	I_{LI}	−1	—	1	μA	V_{IN}=0V~V_{CC}
Output leakage current	I_{LO}	−1	—	1	μA	V_{OUT}=0V~V_{CC} $\overline{CS}$=V_{CC}
Operating current consumption	I_{CC1}	—	—	1.5	mA	$f_{\overline{SK}}$=1MHz tE / W=15mS (WRITE)
	I_{CC2}	—	—	500	μA	$f_{\overline{SK}}$=1MHz (READ)
Standby current	I_{SB}	—	—	2	μA	$\overline{CS}$,$\overline{SK}$,DI,$\overline{WC}$,=V_{CC} DO,R / $\overline{B}$=OPEN
$\overline{SK}$ frequency	f_{SK}	—	—	1	MHz	V_{CC}=3.0~3.3V
		—	—	750	kHz	V_{CC}=2.7~3.0V

●Operation timing characteristics

BR9020/F : At 5V (Unless otherwise noted, Ta=-40 to 85℃, Vcc=5V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit
$\overline{CS}$ setup time	tCSS	200	—	—	nS
$\overline{CS}$ hold time	tCSH	0	—	—	nS
Data setup time	tDIS	150	—	—	nS
Data hold time	tDIH	150	—	—	nS
DO rise delay time	tPD1	—	—	350	nS
DO fall delay time	tPD0	—	—	350	nS
Self-timing programming cycle	tE / W	—	—	10	mS
$\overline{CS}$ minimum "H" time	tCS	1	—	—	μS
READY/$\overline{BUSY}$ display valid time	tSV	—	—	1	μS
Time at which DO goes High-Z (from $\overline{CS}$)	tOH	0	—	400	nS
Data clock "H" time	tWH	450	—	—	nS
Data clock "L" time	tWL	450	—	—	nS
Write control setup time	tWCS	0	—	—	nS
Write control hold time	tWCH	0	—	—	nS

BR9020/F : At 3V (Unless otherwise noted, Ta=-40 to 85℃, Vcc=3V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit
$\overline{CS}$ setup time	tCSS	200	—	—	nS
$\overline{CS}$ hold time	tCSH	0	—	—	nS
Data setup time	tDIS	150	—	—	nS
Data hold time	tDIH	150	—	—	nS
DO rise delay time	tPD1	—	—	350	nS
DO fall delay time	tPD0	—	—	350	nS
Self-timing programming cycle	tE / W	—	—	15	mS
$\overline{CS}$ minimum "H" time	tCS	1	—	—	μS
READY/$\overline{BUSY}$ display valid time	tSV	—	—	1	μS
Time at which DO goes High-Z (from $\overline{CS}$)	tOH	0	—	400	nS
Data clock "H" time	tWH	450	—	—	nS
Data clock "L" time	tWL	450	—	—	nS
Write control setup time	tWCS	0	—	—	nS
Write control hold time	tWCH	0	—	—	nS

BR9040/F : At 5V (Unless otherwise noted, Ta=-40 to 85℃, Vcc=5V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit
$\overline{CS}$ setup time	tCSS	200	—	—	nS
$\overline{CS}$ hold time	tCSH	0	—	—	nS
Data setup time	tDIS	150	—	—	nS
Data hold time	tDIH	150	—	—	nS
DO rise delay time	tPD1	—	—	350	nS
DO fall delay time	tPD0	—	—	350	nS
Self-timing programming cycle	tE / W	—	—	10	mS
$\overline{CS}$ minimum "H" time	tCS	1	—	—	μS
READY/$\overline{BUSY}$ display valid time	tSV	—	—	1	μS
Time at which DO goes High-Z (from $\overline{CS}$)	tOH	0	—	400	nS
Data clock "H" time	tWH	500	—	—	nS
Data clock "L" time	tWL	500	—	—	nS
Write control setup time	tWCS	0	—	—	nS
Write control hold time	tWCH	0	—	—	nS

BR9040/F : At 3V (Unless otherwise noted, Ta=-40 to 85℃, Vcc=3V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit
$\overline{CS}$ setup time	tCSS	200	—	—	nS
$\overline{CS}$ hold time	tCSH	0	—	—	nS
Data setup time	tDIS	150	—	—	nS
Data hold time	tDIH	150	—	—	nS
DO rise delay time Vcc = 3.0 to 3.3 V	tPD1	—	—	350	nS
DO fall delay time Vcc = 3.0 to 3.3 V	tPD0	—	—	350	nS
DO rise delay time Vcc = 2.7 to 3.0 V	tPD1	—	—	500	nS
DO fall delay time Vcc = 2.7 to 3.0 V	tPD0	—	—	500	nS
Self-timing programming cycle	tE / W	—	—	15	mS
$\overline{CS}$ minimum "H" time	tCS	1	—	—	μS
READY/$\overline{BUSY}$ display valid time	tSV	—	—	1	μS
Time at which DO goes High-Z (from $\overline{CS}$)	tOH	0	—	400	nS
Data clock "H" time Vcc =3.0 to 3.3 V	tWH	500	—	—	nS
Data clock "L" time Vcc = 3.0 to 3.3 V	tWL	500	—	—	nS
Data clock "H" time Vcc = 2.7 to 3.0 V	tWH	650	—	—	nS
Data clock "L" time Vcc = 2.7 to 3.0 V	tWL	650	—	—	nS
Write control setup time	tWCS	0	—	—	nS
Write control hold time	tWCH	0	—	—	nS

●Synchronized data input/output timing

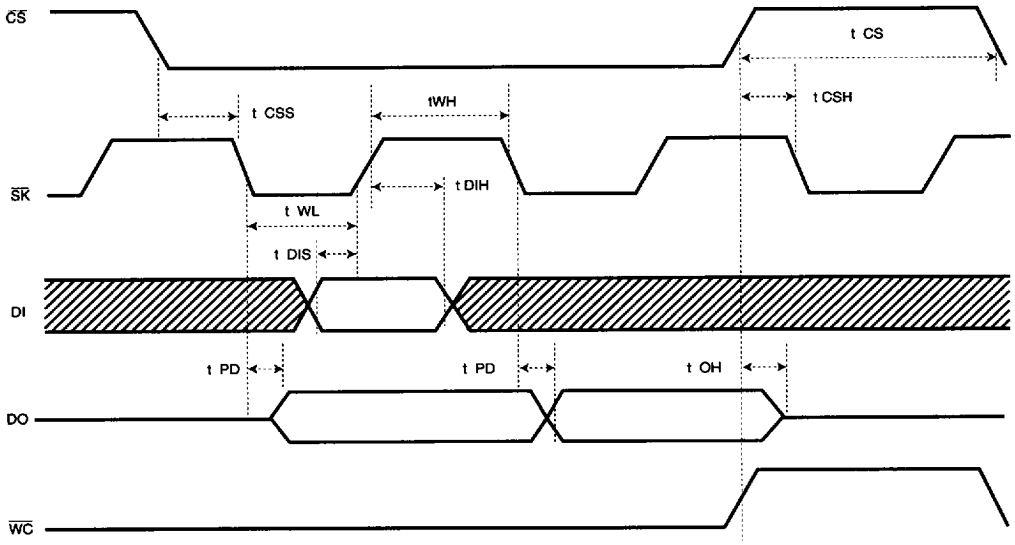


Fig.1

- Input data is read at rising edge of SK.
- Data is output from DO in synchronization with the SK falling edge.
- WC is related only to the write commands, and reading and writing can be enabled and disabled regardless of the status of WC.
- CS should be set to HIGH for at least the tCS timing between commands. If CS is LOW, the next command cannot be received.

●Circuit operation

1. Command mode

Command	Start bit	Operating code	Address	Data
Read (READ)	1010	1000	A0 A1 A2 A3 A4 A5 A6 (A7) ※	
Write (WRITE)	1010	0100	A0 A1 A2 A3 A4 A5 A6 (A7) ※	D0 D1—D14 D15
Erase/Write enabled (EWEN)	1010	0011	* * * * * * * *	
Erase/Write disabled (EWDS)	1010	0000	* * * * * * * *	

* Either V_{IH} or V_{IL}

※ (0) for BR9020/F

2. Writing enabled/disabled

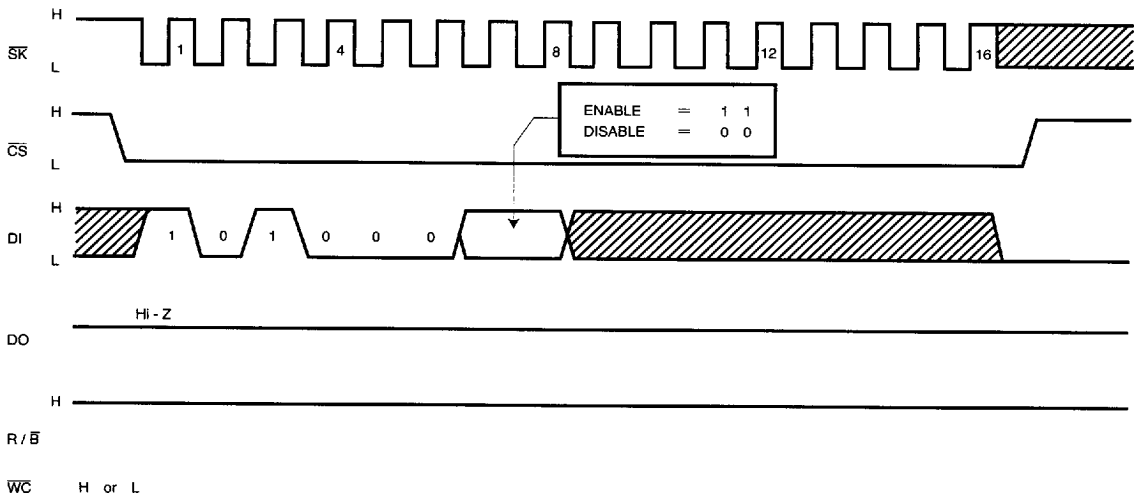


Fig.2

- When the power supply is turned on, the latch used to acknowledge writing is reset in the same way as when the write disable command is executed. Before entering the write mode, the write enabled mode must first be entered. Once the write enabled mode has been recognized, it remains valid until the write disabled mode is entered, or the power supply is turned off.
- The clock is no longer necessary after the first 16 clock pulses have been received. Any subsequent input will be ignored.
- $\overline{WC}$ does not exist for either the write enabled or write disabled command, so $\overline{WC}$ may be either HIGH or LOW when the command is being input.
- Commands are received in these modes by means of 8-bit operating codes. Please be aware that, after an operating code has been entered, commands will not be cancelled even if $\overline{CS}$ is set to HIGH. (To cancel a command, either turn off the power supply, or input the command once again.)

3. Read cycle

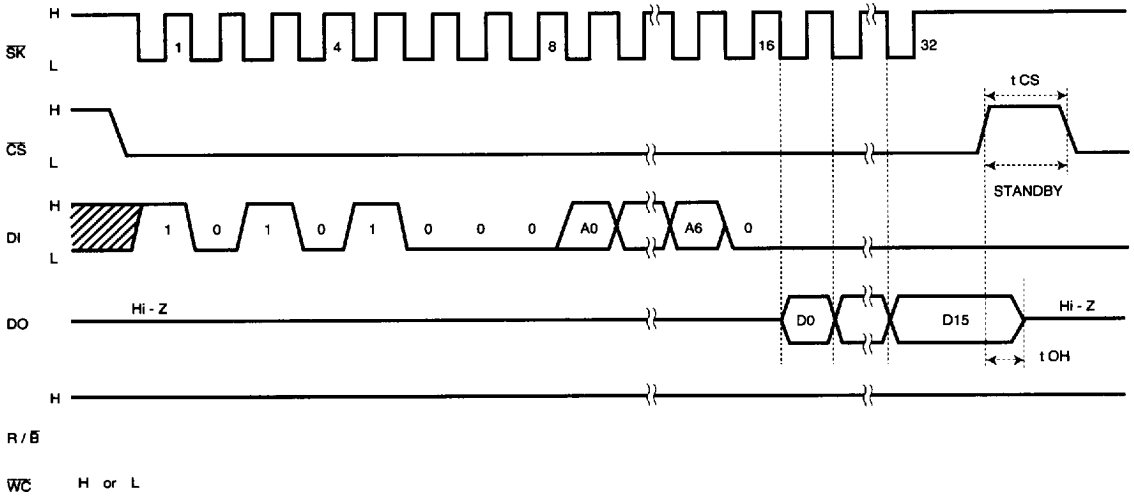


Fig.3 (BR9020 / F)

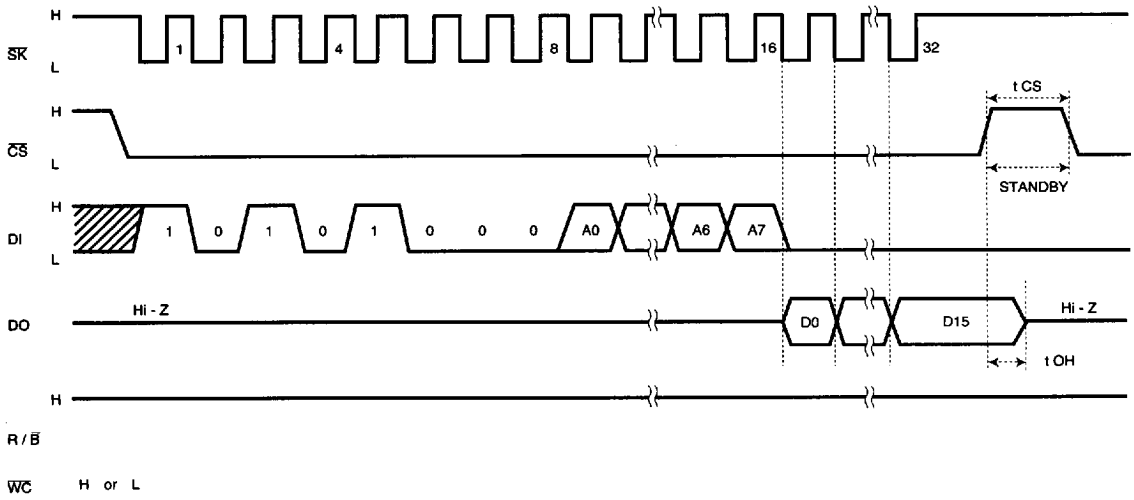


Fig.4 (BR9040 / F)

- After the fall of the 16th clock pulse, 16-bit data is output from the DO pin in synchronization with the falling edge of the $\overline{SK}$ signal. (DO output changes at a time lag of tPD0, tPD1 because of internal circuit delay following the falling edge of the $\overline{SK}$ signal. During the tPD0 and tPD1 timing, the tPD time should be assured before data is read, to avoid the previous data being lost. See the synchronized data input/output timing chart in Figure 1.)

●Circuit operation

4. Reading cycle

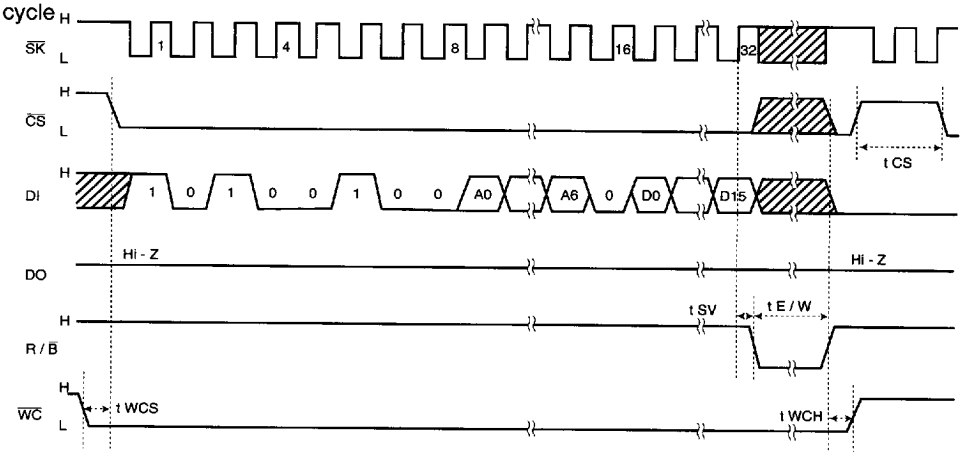


Fig.5 (BR9020 / F)

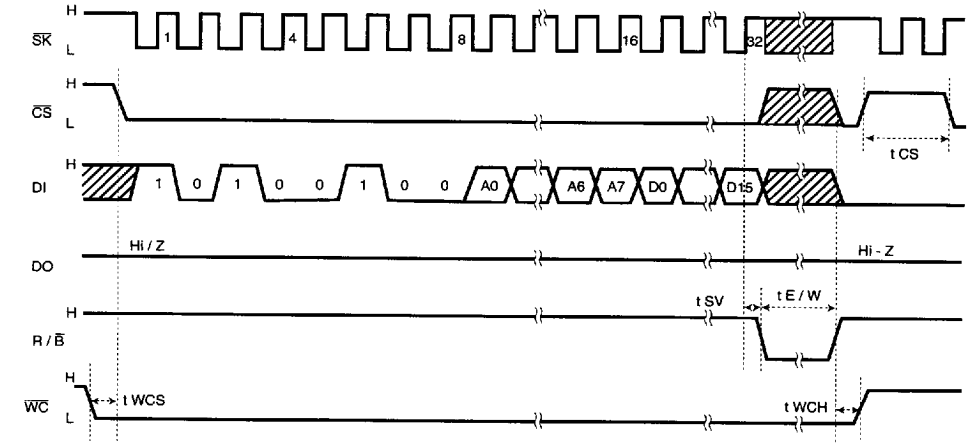


Fig.6 (BR9040 / F)

- During input in the write mode, $\overline{CS}$ must be LOW, but once writing starts, $\overline{CS}$ may be either HIGH or LOW. However, if $\overline{CS}$ and $\overline{WC}$ share the same connection, both $\overline{CS}$ and $\overline{WC}$ should be set to LOW during writing operations. (If the $\overline{WC}$ pin is set to HIGH during a writing operation, writing will be forcibly interrupted at that point. If this happens, the data for that address may be lost, in which case it should be rewritten to that address.)
- Following input of a write command, $\overline{CS}$ goes HIGH. If $\overline{CS}$ is then set to LOW, data will be received from $\overline{SK}$ and DI, because the command reception status has been entered.
  If $\overline{CS}$ remains LOW following command input, however, without first going HIGH, command input will be cancelled until $\overline{CS}$ is set to HIGH.
- Starting from the rising edge of the 32nd clock, the R/$\overline{B}$ pin goes LOW after tSV has elapsed.
- The R/$\overline{B}$ pin is LOW during writing operations. (Following the rising edge of $\overline{SK}$ after the last data D15 has been read, the internal timer circuit is activated, and writing of data in the memory cell is automatically completed during tE/W.) At this point, $\overline{SK}$ input may be either HIGH or LOW during tE/W.
- Following input of a write command, if $\overline{CS}$ falls while $\overline{SK}$ is LOW, the R/$\overline{B}$ status can be displayed from the DO pin. (See the section on READY/$\overline{BUSY}$ states.)

5. READY/$\overline{\text{BUSY}}$ display (R/$\overline{\text{B}}$ pin and DO pin)

- This display outputs the internal status signal; the R/$\overline{\text{B}}$ pin outputs the HIGH or LOW status at all times. The display can also be output from the DO pin. Following completion of the writing command, if $\overline{\text{CS}}$ falls while $\overline{\text{SK}}$ is LOW, either HIGH or LOW is output. (The display can also be output without using the R/B pin, leaving it open.)
- When writing data to a memory cell, the READY/$\overline{\text{BUSY}}$ display is output from the rise of the 32nd clock pulse of the $\overline{\text{SK}}$ signal after tSV, from the R/$\overline{\text{B}}$ pin.

R/$\overline{\text{B}}$ display = LOW : writing in progress

(The internal timer circuit is activated, and after the tE/W timing has been created, the timer circuit stops automatically. Writing of data to the memory cell is done during the tE/W timing, during which time other commands cannot be received.)

R/$\overline{\text{B}}$ display = HIGH : command standby state

(Writing of data to the memory cell has been completed and the next command can be received.)

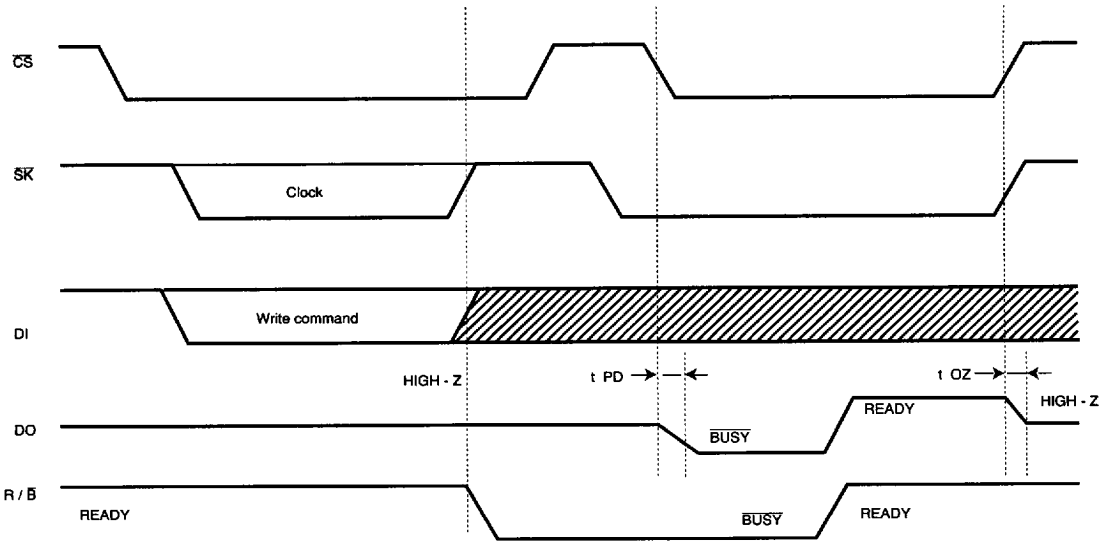


Fig.7 R / $\overline{\text{B}}$ Status output timing diagram

●Operation notes

1. Turning the power supply on and off

- When the power supply is turned on and off, $\overline{CS}$ should be set to HIGH (= Vcc).
- When $\overline{CS}$ is LOW, the command input reception state (active) is entered. If the power supply is turned on in this state, erroneous operations and erroneous writing can occur because of noise and other factors. To avoid this, make sure $\overline{CS}$ is set to HIGH (= Vcc) before turning on the power supply.

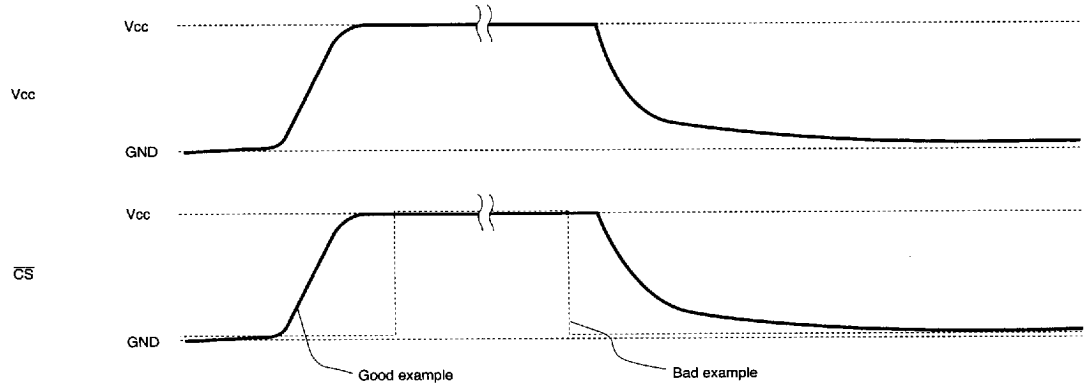
(Good example) Here, the $\overline{CS}$ pin is pulled up to Vcc.

When turning off the power supply, wait at least 10 msec before turning it on again. Failing to observe this condition can result in the internal circuit failing to be reset when the power supply is turned on.

(Bad example) $\overline{CS}$ is LOW when the power supply is turned on or off

In this case, because $\overline{CS}$ remains LOW, the EEPROM may perform erroneous operations or write erroneous data because of noise or other factors.

Note: Please be aware that the case shown in this example can also occur if $\overline{CS}$ input is HIGH-Z.



2. Noise countermeasures

2-1. $\overline{SK}$ noise

If noise occurs at the rise of the $\overline{SK}$ clock input, the clock is assumed to be excessive, and this can cause malfunction because the bits are out of alignment.

2-2. $\overline{WC}$ noise

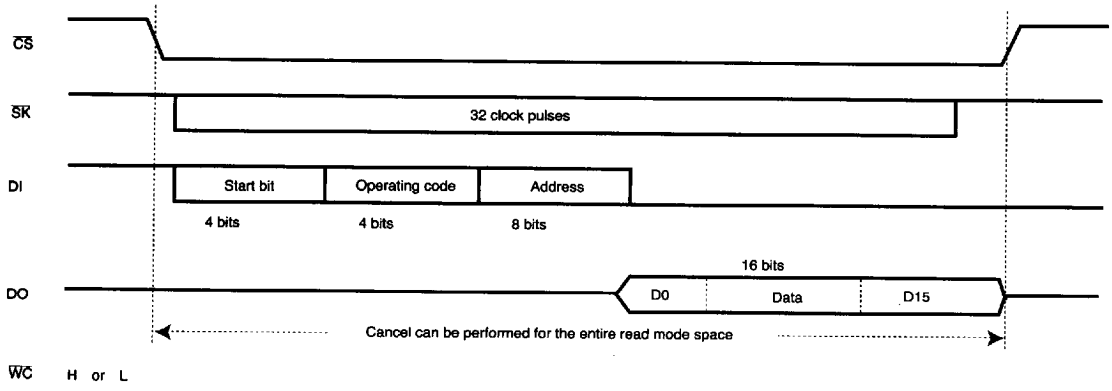
During a writing operation, noise at the $\overline{WC}$ pin can be erroneously judged to be data, and this can cause writing to be forcibly interrupted.

2-3. Vcc noise

Noise and surges on the power supply line can cause malfunction. We recommend installing a bypass capacitor between the power supply and ground to eliminate this problem.

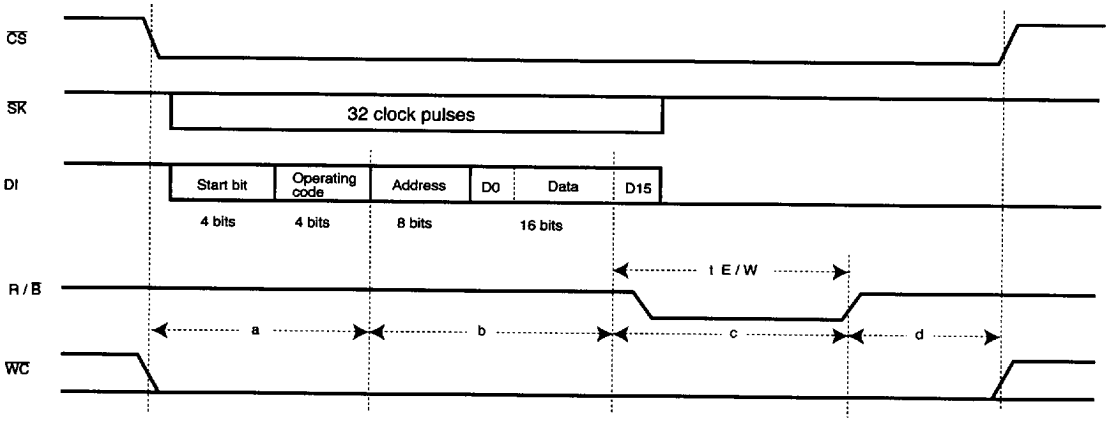
3. Cancelling modes

3-1. Read commands



Cancellation method : $\overline{CS}$ HIGH

3-2. Write commands



Cancelling methods

a : Canceled by setting $\overline{CS}$ HIGH. The WC pin is not involved.

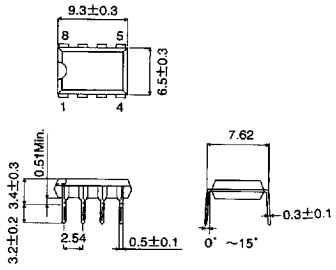
b : If the $\overline{WC}$ pin goes HIGH for even a second, writing is forcibly interrupted. Cancellation occurs even if the $\overline{CS}$ pin is HIGH. At this point, data has not been written to the memory, so the data in the designated address has not yet been changed.

c : The operation is forcibly cancelled by setting the $\overline{WC}$ pin to HIGH or turning off the power supply (although we do not recommend using this method). The data in the designated address is not guaranteed and should be written once again.

d : If $\overline{CS}$ is set to HIGH while the R/$\overline{B}$ signal is HIGH (following the tE/W timing), the IC is reset internally, and waits for the next command to be input.

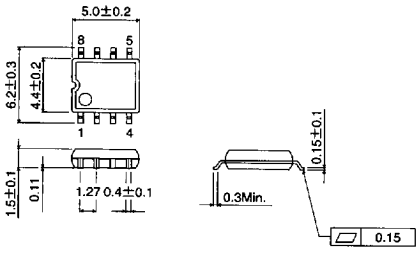
●External dimensions (Units: mm)

BR9020/BR9040



DIP8

BR9020F/BR9040F



SOP8