

SN54AHC573, SN74AHC573 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS242I – OCTOBER 1995 – REVISED JANUARY 2000

- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Operating Range 2-V to 5.5-V V_{CC}
- 3-State Outputs Directly Drive Bus Lines
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

description

The 'AHC573 devices are octal transparent D-type latches designed for 2-V to 5.5-V V_{CC} operation.

When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

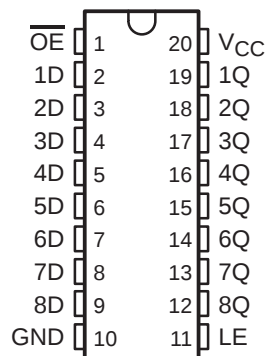
A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

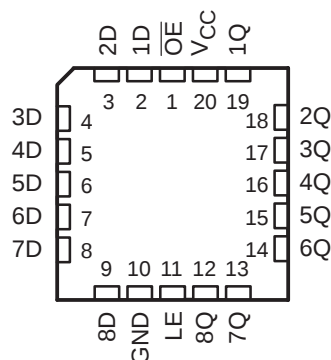
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54AHC573 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AHC573 is characterized for operation from -40°C to 85°C .

SN54AHC573 . . . J OR W PACKAGE
SN74AHC573 . . . DB, DGV, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC573 . . . FK PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2000, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

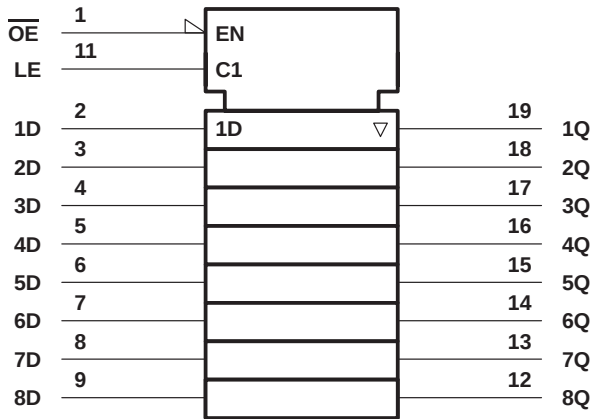
SN54AHC573, SN74AHC573
OCTAL TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

SCLS242I – OCTOBER 1995 – REVISED JANUARY 2000

FUNCTION TABLE
(each latch)

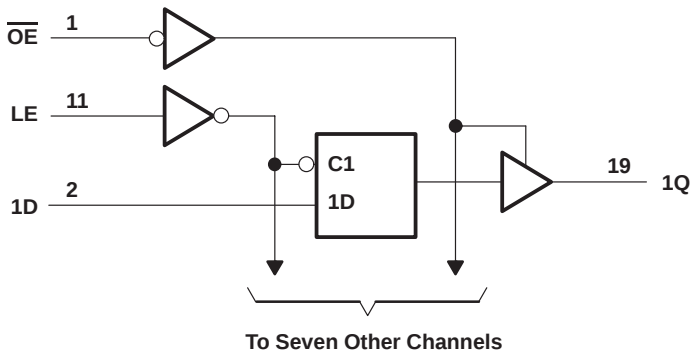
INPUTS			OUTPUT Q
$\overline{\text{OE}}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SCLS242I – OCTOBER 1995 – REVISED JANUARY 2000

Supply voltage range, V_{CC}		-0.5 V to 7 V
Input voltage range, V_I (see Note 1)		-0.5 V to 7 V
Output voltage range, V_O (see Note 1)		-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)		-20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)		± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})		± 25 mA
Continuous current through V_{CC} or GND		± 75 mA
Package thermal impedance, θ_{JA} (see Note 2):		
DB package		70°C/W
DGV package		92°C/W
DW package		58°C/W
N package		69°C/W
PW package		83°C/W
Storage temperature range, T_{sta}		-65°C to 150°C

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JEDEC 51.

			SN54AHC573		SN74AHC573		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 3 V	2.1		2.1		
		V _{CC} = 5.5 V	3.85		3.85		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5		0.5	V
		V _{CC} = 3 V		0.9		0.9	
		V _{CC} = 5.5 V		1.65		1.65	
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		−50		−50	μA
		V _{CC} = 3.3 V ± 0.3 V		−4		−4	mA
		V _{CC} = 5 V ± 0.5 V		−8		−8	
I _{OL}	Low-level output current	V _{CC} = 2 V		50		50	μA
		V _{CC} = 3.3 V ± 0.3 V		4		4	mA
		V _{CC} = 5 V ± 0.5 V		8		8	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V _{CC} = 5 V ± 0.5 V		20		20	
T _A	Operating free-air temperature		−55	125	−40	85	°C



SN54AHC573, SN74AHC573

OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SCLS242I – OCTOBER 1995 – REVISED JANUARY 2000

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHC573		SN74AHC573		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = –50 µA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I _{OH} = –4 mA	3 V	2.58			2.48		2.48		
	I _{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 µA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I _{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I _{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I _I	V _I = V _{CC} or GND	0 V to 5.5 V			±0.1		±1*		±1	µA
I _{OZ}	V _I = V _{IL} or V _{IH} , V _O = V _{CC} or GND	5.5 V			±0.25		±2.5		±2.5	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		40		40	µA
C _i	V _I = V _{CC} or GND	5 V		2.5	10				10	pF
C _o	V _O = V _{CC} or GND	5 V		3.5						pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

**timing requirements over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

		T _A = 25°C		SN54AHC573		SN74AHC573		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE high	5		5		5		ns
t _{su}	Setup time, data before LE↓	3.5		3.5		3.5		ns
t _h	Hold time, data after LE↓	1.5		1.5		1.5		ns

**timing requirements over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

		T _A = 25°C		SN54AHC573		SN74AHC573		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE high	5		5		5		ns
t _{su}	Setup time, data before LE↓	3.5		3.5		3.5		ns
t _h	Hold time, data after LE↓	1.5		1.5		1.5		ns



SN54AHC573, SN74AHC573 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS242I – OCTOBER 1995 – REVISED JANUARY 2000

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54AHC573		SN74AHC573		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	Q	C _L = 15 pF		7*	11*	1*	13*	1	13	ns
t _{PHL}					7*	11*	1*	13*	1	13	
t _{PLH}	LE	Q	C _L = 15 pF		7.6*	11.9*	1*	14*	1	14	ns
t _{PHL}					7.6*	11.9*	1*	14*	1	14	
t _{PZH}	$\overline{OE}$	Q	C _L = 15 pF		7.3*	11.5*	1*	13.5*	1	13.5	ns
t _{PZL}					7.3*	11.5*	1*	13.5*	1	13.5	
t _{PHZ}	$\overline{OE}$	Q	C _L = 15 pF		8.3*	11*	1*	13*	1	13	ns
t _{PLZ}					8.3*	11*	1*	13*	1	13	
t _{PLH}	D	Q	C _L = 50 pF		9.5	14.5	1	16.5	1	16.5	ns
t _{PHL}					9.5	14.5	1	16.5	1	16.5	
t _{PLH}	LE	Q	C _L = 50 pF		10.1	15.4	1	17.5	1	17.5	ns
t _{PHL}					10.1	15.4	1	17.5	1	17.5	
t _{PZH}	$\overline{OE}$	Q	C _L = 50 pF		9.8	15	1	17	1	17	ns
t _{PZL}					9.8	15	1	17	1	17	
t _{PHZ}	$\overline{OE}$	Q	C _L = 50 pF		10.7	14.5	1	16.5	1	16.5	ns
t _{PLZ}					10.7	14.5	1	16.5	1	16.5	
t _{sk(o)}			C _L = 50 pF			1.5**				1.5	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54AHC573		SN74AHC573		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	Q	C _L = 15 pF		4.5*	6.8*	1	8*	1	8	ns
t _{PHL}					4.5*	6.8*	1	8*	1	8	
t _{PLH}	LE	Q	C _L = 15 pF		5*	7.7*	1	9*	1	9	ns
t _{PHL}					5*	7.7*	1	9*	1	9	
t _{PZH}	$\overline{OE}$	Q	C _L = 15 pF		5.2*	7.7*	1	9*	1	9	ns
t _{PZL}					5.2*	7.7*	1	9*	1	9	
t _{PHZ}	$\overline{OE}$	Q	C _L = 15 pF		5.2*	7.7*	1	9*	1	9	ns
t _{PLZ}					5.2*	7.7*	1	9*	1	9	
t _{PLH}	D	Q	C _L = 50 pF		6	8.8	1	10	1	10	ns
t _{PHL}					6	8.8	1	10	1	10	
t _{PLH}	LE	Q	C _L = 50 pF		6.5	9.7	1	11	1	11	ns
t _{PHL}					6.5	9.7	1	11	1	11	
t _{PZH}	$\overline{OE}$	Q	C _L = 50 pF		6.7	9.7	1	11	1	11	ns
t _{PZL}					6.7	9.7	1	11	1	11	
t _{PHZ}	$\overline{OE}$	Q	C _L = 50 pF		6.7	9.7	1	11	1	11	ns
t _{PLZ}					6.7	9.7	1	11	1	11	
t _{sk(o)}			C _L = 50 pF			1**				1	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.



SN54AHC573, SN74AHC573

OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SCLS242I – OCTOBER 1995 – REVISED JANUARY 2000

noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER	SN74AHC573		UNIT
	MIN	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}		1	V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}		-0.8	V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}	4		V
$V_{IH(D)}$ High-level dynamic input voltage	3.5		V
$V_{IL(D)}$ Low-level dynamic input voltage		1.5	V

NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	16	pF

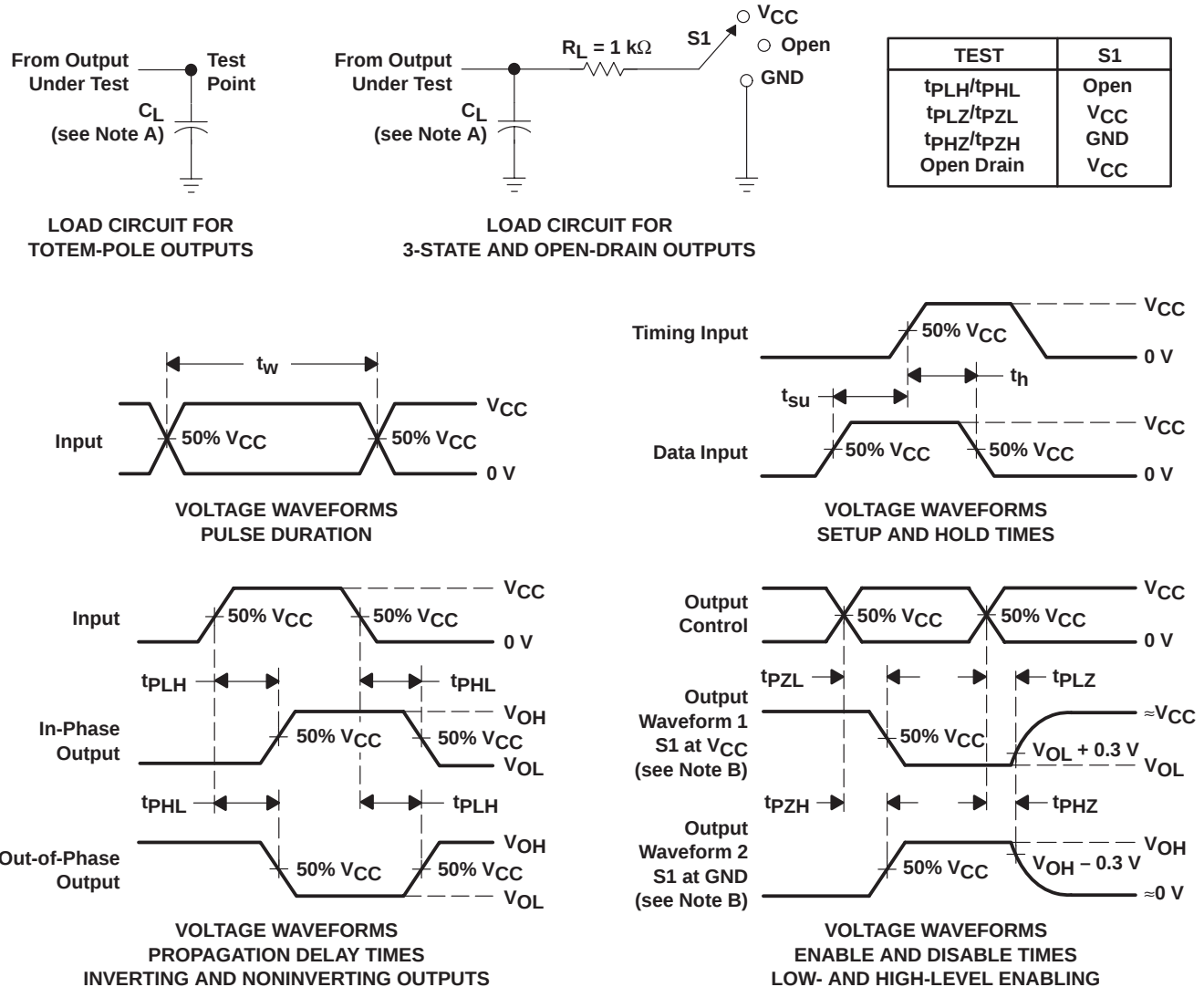


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54AHC573, SN74AHC573 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS242I – OCTOBER 1995 – REVISED JANUARY 2000

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.