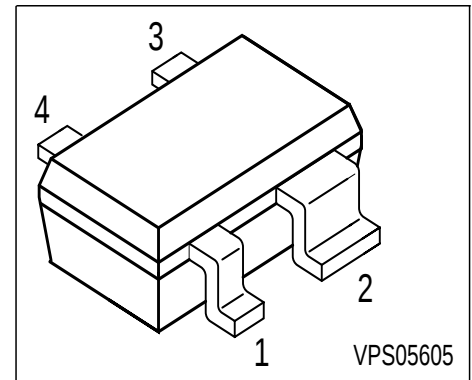


Silicon N-Channel MOSFET Tetrode

- Short-channel transistor with high S/C quality factor
- For low-noise, gain-controlled input stages up to 1 GHz



ESD: Electrostatic discharge sensitive device, observe handling precaution!

Type	Marking	Pin Configuration				Package
BF998W	MRs	1=D	2=S	3=G1	4=G2	SOT343

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	12	V
Continuous drain current	I_D	30	mA
Gate 1/gate 2 peak source current	$\pm I_{G1/2SM}$	10	
Total power dissipation, $T_S = 94\text{ °C}$	P_{tot}	200	mW
Storage temperature	T_{stg}	55 ... 150	°C
Channel temperature	T_{ch}	150	

Thermal Resistance

Channel - soldering point ¹⁾	R_{thchs}	≤ 280	K/W
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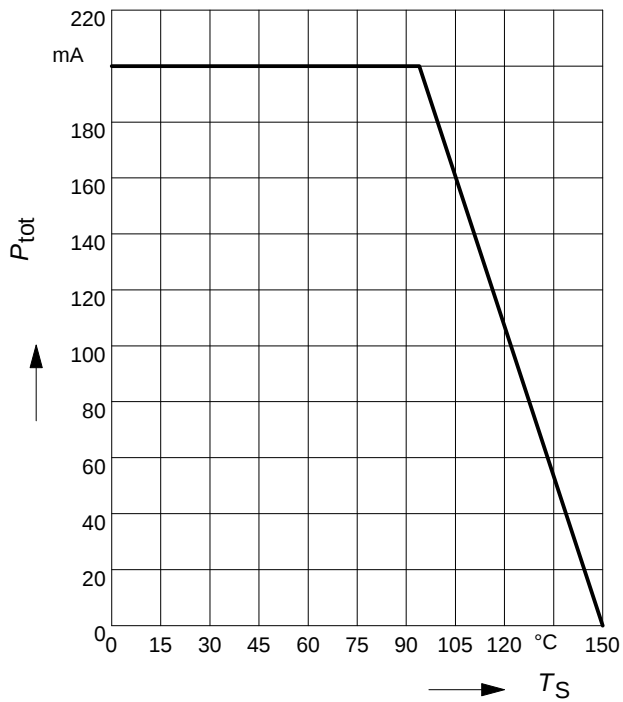
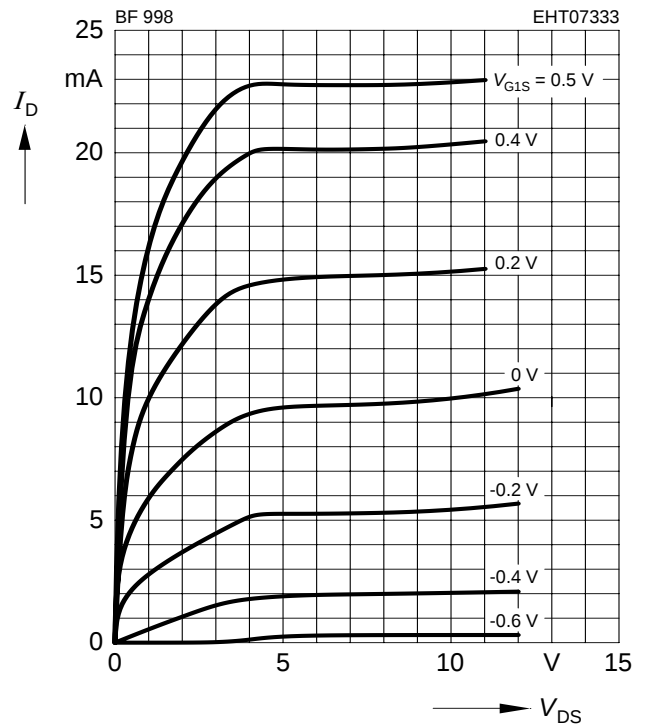
¹⁾For calculation of R_{thJA} please refer to Application Note Thermal Resistance

Electrical Characteristics at $T_A = 25\text{ °C}$; unless otherwise specified.

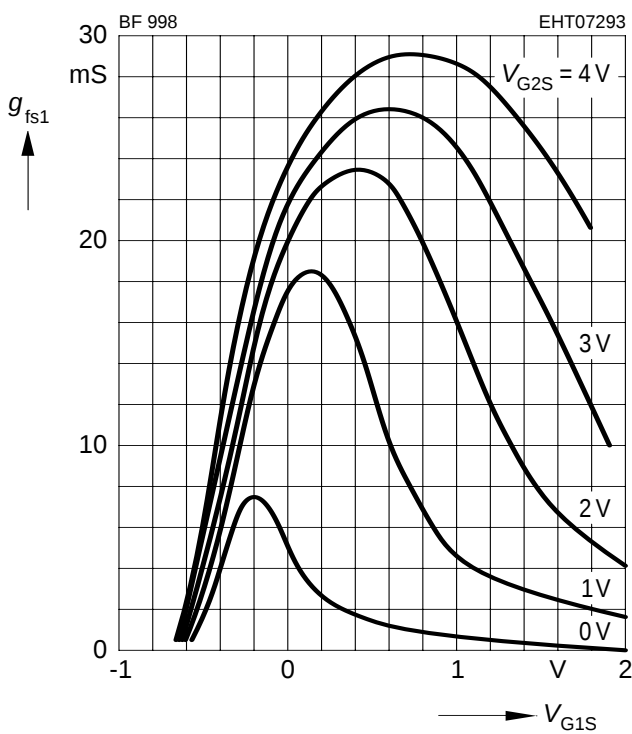
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC characteristics					
Drain-source breakdown voltage $I_D = 10\text{ }\mu\text{A}$, $V_{G1S} = -4\text{ V}$, $V_{G2S} = -4\text{ V}$	$V_{(BR)DS}$	12	-	-	V
Gate 1 source breakdown voltage $\pm I_{G1S} = 10\text{ mA}$, $V_{G2S} = V_{DS} = 0$	$\pm V_{(BR)G1SS}$	8	-	12	
Gate 2 source breakdown voltage $\pm I_{G2S} = 10\text{ mA}$, $V_{G1S} = 0\text{ V}$, $V_{DS} = 0\text{ V}$	$\pm V_{(BR)G2SS}$	8	-	12	
Gate 1 source leakage current $\pm V_{G1S} = 8\text{ V}$, $V_{G2S} = V_{DS} = 0$	$\pm I_{G1SS}$	-	-	50	nA
Gate 2 source leakage current $\pm V_{G2S} = 8\text{ V}$, $V_{G1S} = 0\text{ V}$, $V_{DS} = 0\text{ V}$	$\pm I_{G2SS}$	-	-	50	
Drain current $V_{DS} = 8\text{ V}$, $V_{G1S} = 0$, $V_{G2S} = 4\text{ V}$	I_{DSS}	2	-	18	mA
Gate 1 source pinch-off voltage $V_{DS} = 8\text{ V}$, $V_{G2S} = 0$, $I_D = 20\text{ }\mu\text{A}$	$-V_{G1S(p)}$	-	-	2.5	V
Gate 2 source pinch-off voltage $V_{DS} = 8\text{ V}$, $V_{G1S} = 0$, $I_D = 20\text{ }\mu\text{A}$	$-V_{G2S(p)}$	-	-	2	

Electrical Characteristics

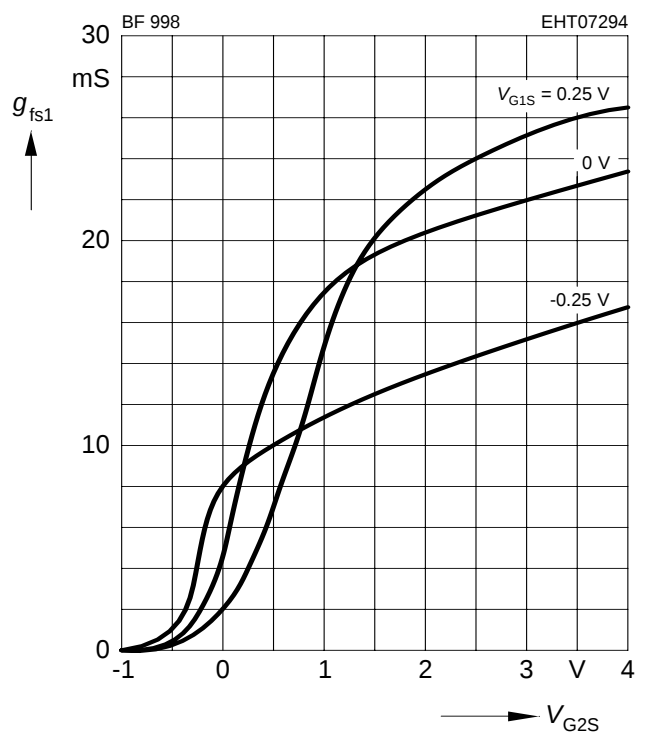
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
AC characteristics					
Forward transconductance $V_{DS} = 8\text{ V}$, $I_D = 10\text{ mA}$, $V_{G2S} = 4\text{ V}$	g_{fs}	-	24	-	mS
Gate 1 input capacitance $V_{DS} = 8\text{ V}$, $I_D = 10\text{ mA}$, $V_{G2S} = 4\text{ V}$, $f = 1\text{ MHz}$	C_{g1ss}	-	2.1	2.5	pF
Gate 2 input capacitance $V_{DS} = 8\text{ V}$, $I_D = 10\text{ mA}$, $V_{G2S} = 4\text{ V}$, $f = 1\text{ MHz}$	C_{g2ss}	-	1.2	-	
Feedback capacitance $V_{DS} = 8\text{ V}$, $I_D = 10\text{ mA}$, $V_{G2S} = 4\text{ V}$, $f = 1\text{ MHz}$	C_{dg1}	-	25	-	fF
Output capacitance $V_{DS} = 8\text{ V}$, $I_D = 10\text{ mA}$, $V_{G2S} = 4\text{ V}$, $f = 1\text{ MHz}$	C_{dss}	-	1.1	-	pF
Power gain $V_{DS} = 8\text{ V}$, $I_D = 10\text{ mA}$, $V_{G2S} = 4\text{ V}$, $f = 200\text{ MHz}$	G_{ps}	-	28	-	dB
Power gain $V_{DS} = 8\text{ V}$, $I_D = 10\text{ mA}$, $V_{G2S} = 4\text{ V}$, $f = 800\text{ MHz}$	G_{ps}	-	20	-	
Noise figure $V_{DS} = 8\text{ V}$, $I_D = 10\text{ mA}$, $V_{G2S} = 4\text{ V}$, $f = 200\text{ MHz}$	F	-	0.6	-	
Noise figure $V_{DS} = 8\text{ V}$, $I_D = 10\text{ mA}$, $V_{G2S} = 4\text{ V}$, $f = 800\text{ MHz}$	F	-	1	-	
Gain control range $V_{DS} = 8\text{ V}$, $V_{G2S} = 4 \dots -2\text{V}$, $f = 800\text{ MHz}$	ΔG_{ps}	40	-	-	

Total power dissipation $P_{\text{tot}} = f(T_S)$

Output characteristics $I_D = f(V_{DS})$

Gate 1 forward transconductance

$$g_{fs1} = f(V_{G1S})$$

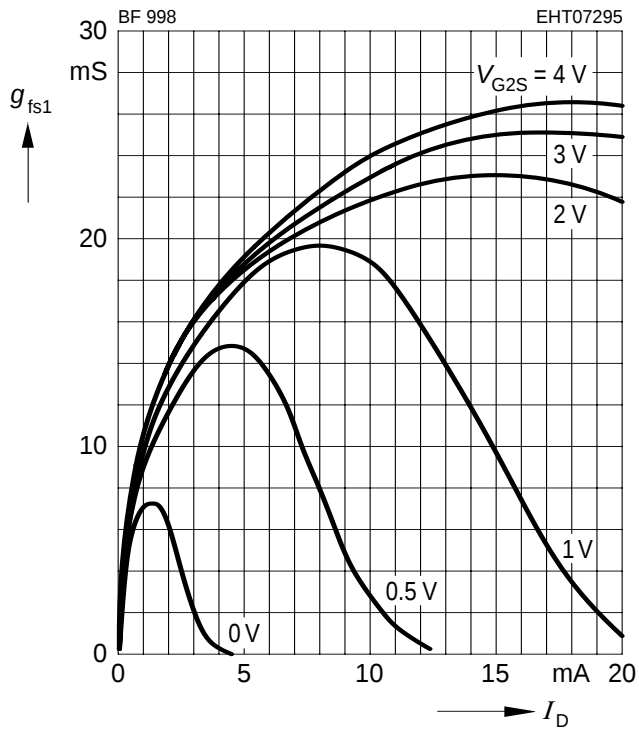
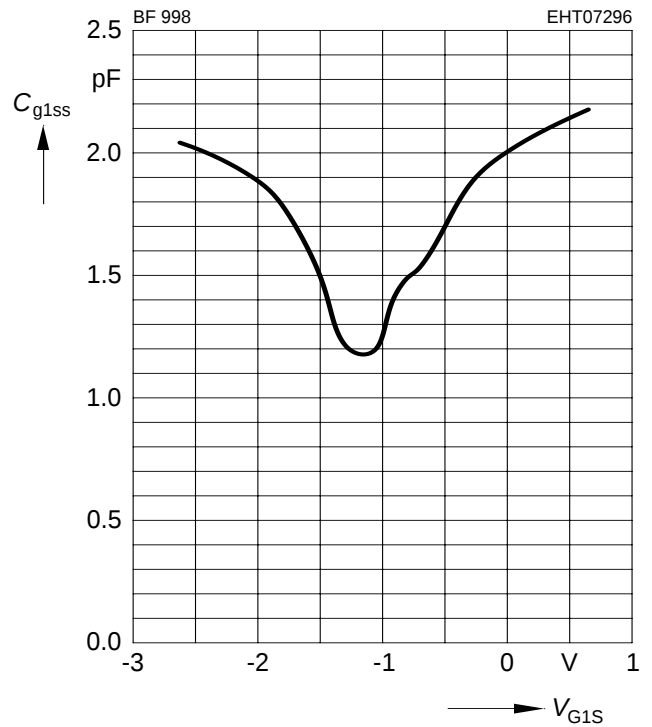
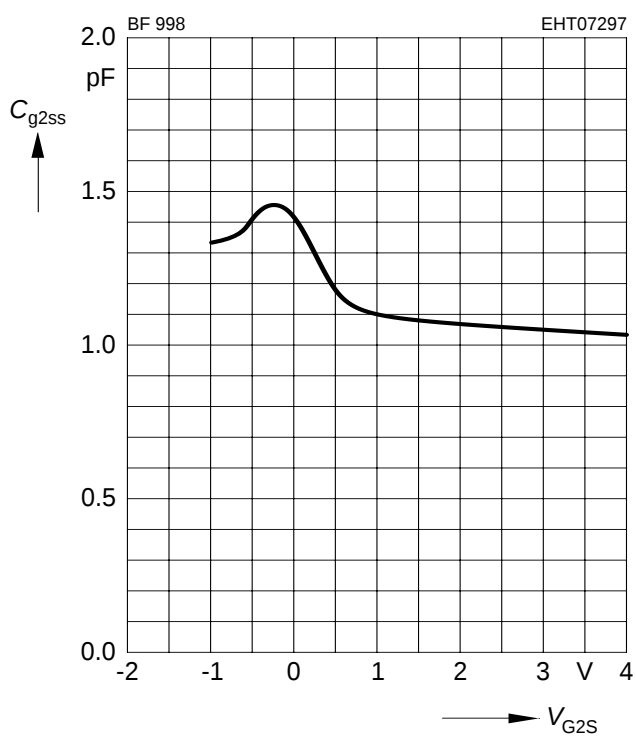
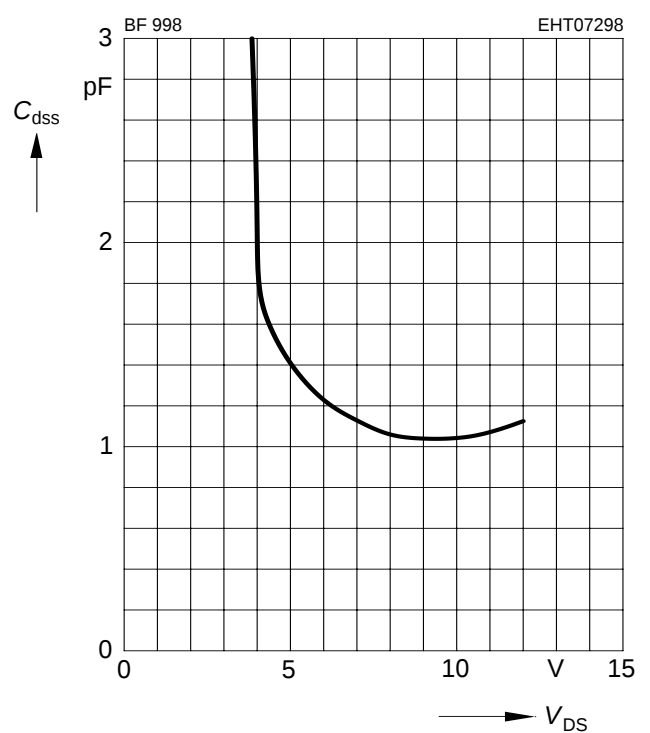

Gate 1 forward transconductance

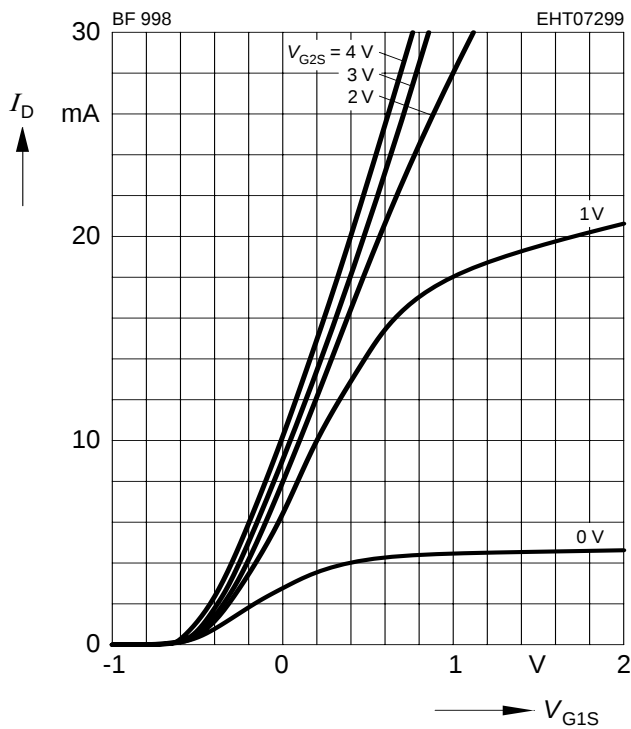
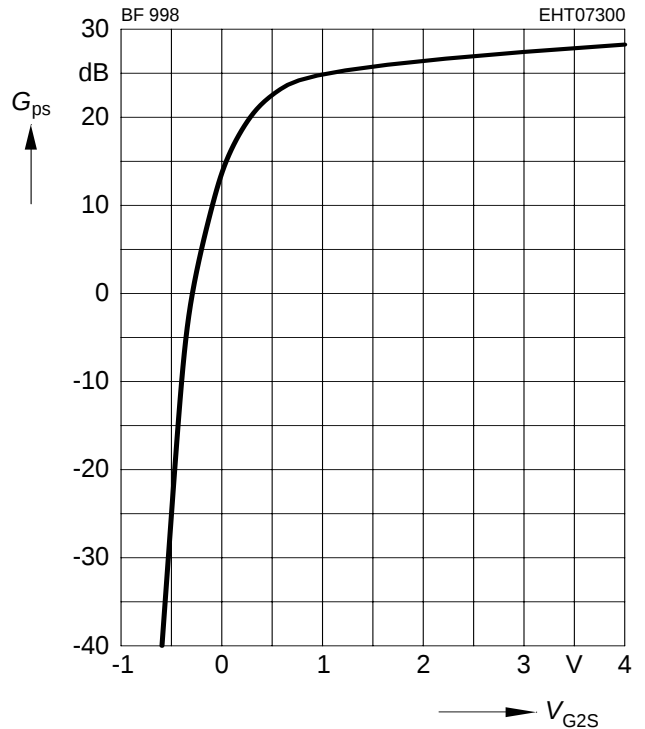
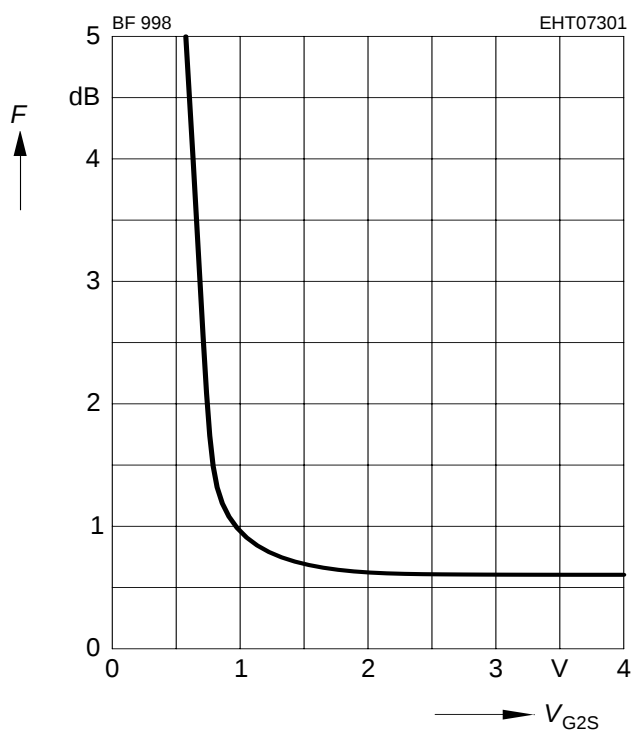
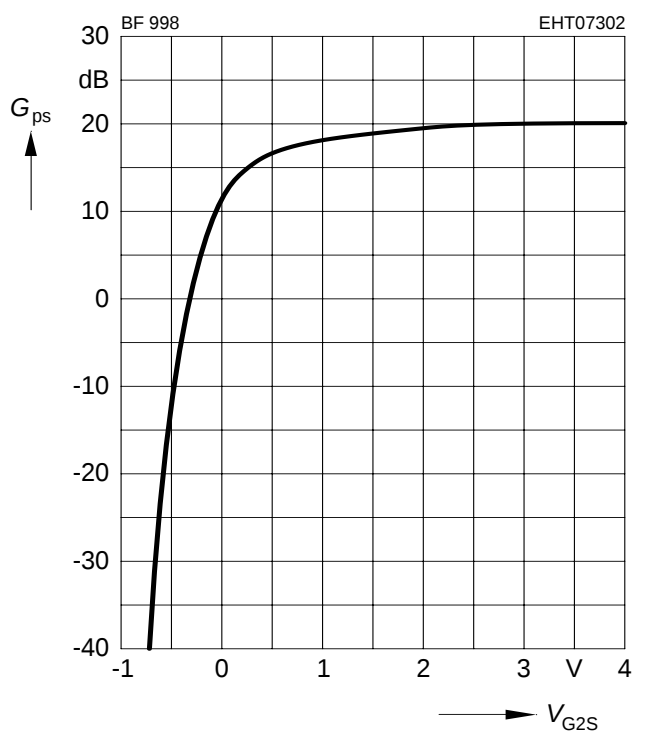
$$g_{fs1} = f(V_{G2S})$$



Gate 1 forward transconductance

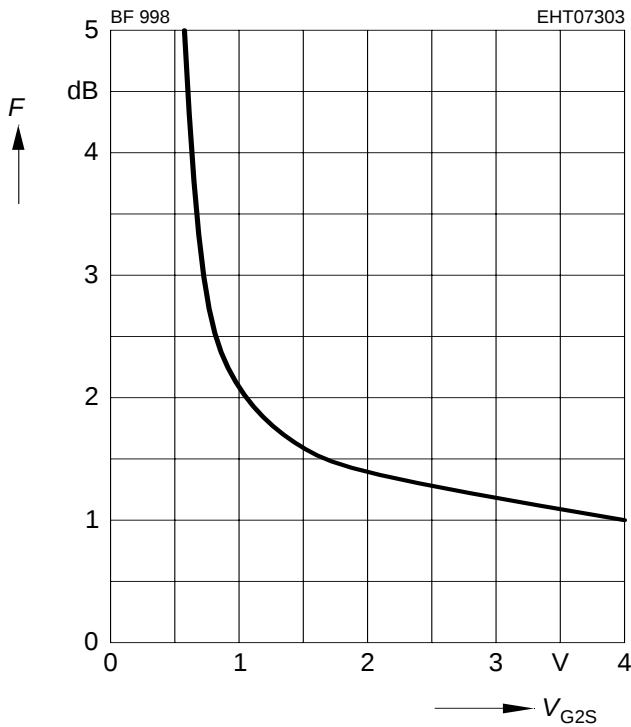
$$g_{fs1} = f(I_D)$$


Gate 1 input capacitance $C_{g1ss} = f(V_{G1S})$

Gate 2 input capacitance $C_{g2ss} = f(V_{G2S})$

Output capacitance $C_{dss} = f(V_{DS})$


Drain current $I_D = f(V_{G1S})$

Power gain $G_{ps} = f(V_{G2S})$
 $f = 200 \text{ MHz}$

Noise figure $F = f(V_{G2S})$
 $f = 200 \text{ MHz}$

Power gain $G_{ps} = f(V_{G2S})$
 $f = 800 \text{ MHz}$


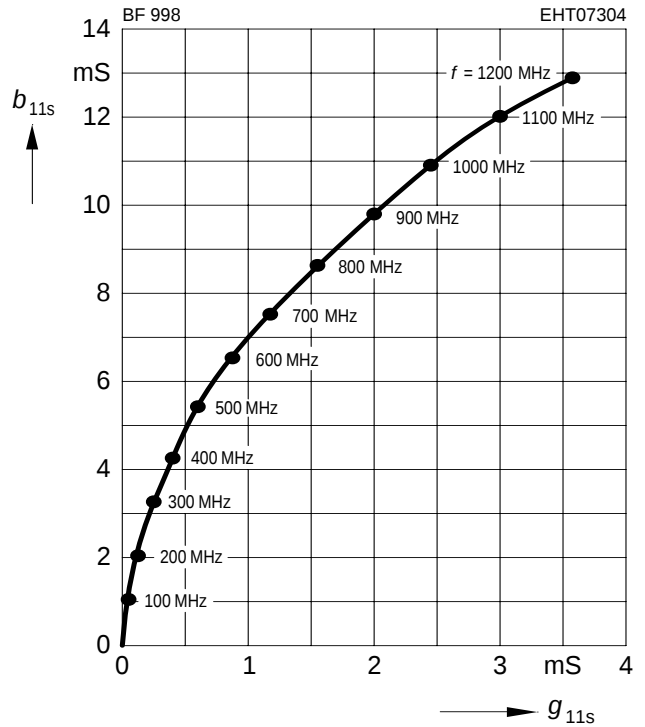
Noise figure $F = f(V_{G2S})$

$f = 800 \text{ MHz}$



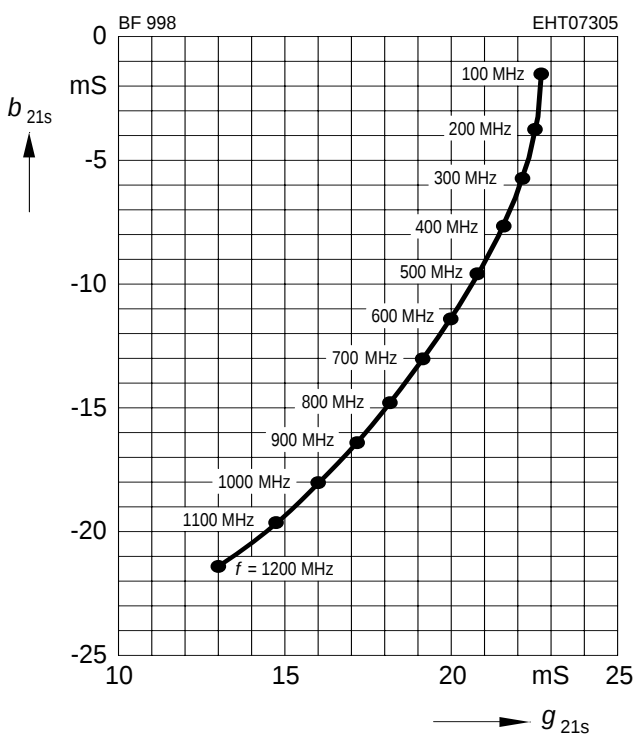
Gate 1 input admittance y_{11s}

(common source)



Gate 1 forward transfer admittance y_{21s}

(common source)



Output admittance y_{22s}

(common-source)

