



## MIC47053

### 500mA Micropower ULDO™ Linear Regulator

## General Description

The MIC47053 is a high-speed, adjustable output ultra-low dropout, dual NMOS ULDO™ designed to power point-of-load applications that require a low-voltage, high-current power supply. The MIC47053 can source 500mA of output current while only requiring a 1μF ceramic output capacitor for stability. The MIC47053 offers 2% output voltage accuracy over temperature, low dropout voltage (49mV @ 500mA), and low ground current which makes this device ideally suited for mobile and point-of-load applications.

The MIC47053 has an NMOS output stage offering very low output impedance. The NMOS output stage makes for a unique ability to respond very quickly to sudden load changes such as that required by a microprocessor, DSP or FPGA. The MIC47053 consumes little quiescent current and therefore can be used for driving the core voltages of mobile processors and post regulating a core DC/DC converter in any processor.

The MIC47053 is available in the tiny 2mm x 2mm Thin DFN packages with an operating junction temperature range of -40°C to +125°C.

Data sheets and support documentation can be found on Micrel's web site at: [www.micrel.com](http://www.micrel.com).

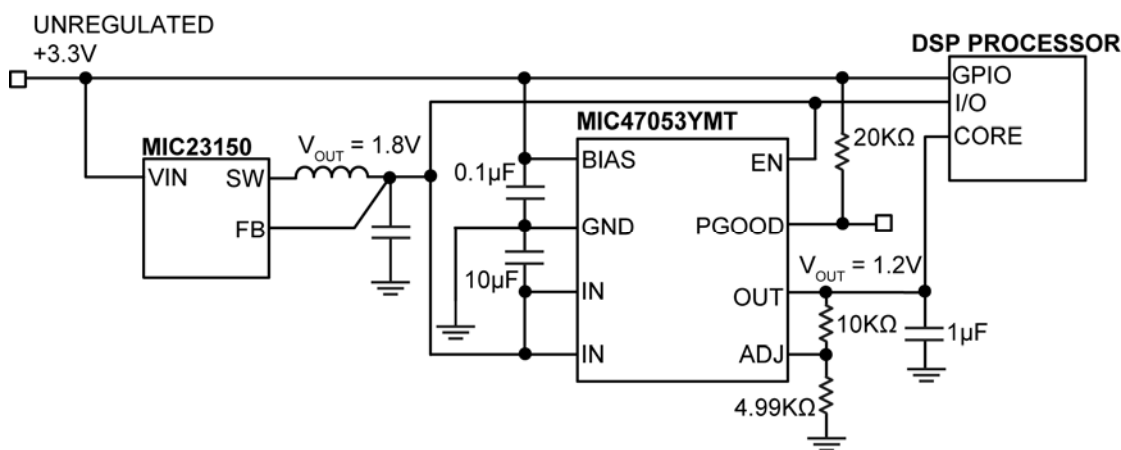
## Features

- Wide input voltage range
  - Input voltage: 1.0V to 3.6V
  - Bias voltage: 2.3V to 5.5V
- Adjustable output voltage range down to 0.4V
- Low dropout voltage of 49mV at 500mA
- Low shutdown current: 0.1μA typical
- ±2% initial output voltage accuracy over temperature
- High bandwidth – very fast transient response
- Stable with a 1μF ceramic output capacitor
- Logic level enable input
- UVLO on both supply voltages
- Available in thermally-enhanced 2mm x 2mm Thin DFN package
- Junction temperature range of -40°C to +125°C

## Applications

- Point-of-load applications
- PDAs, Notebooks, and Desktops
- DSP, PLD, and FPGA power supply
- Low-voltage post regulation

## Typical Application



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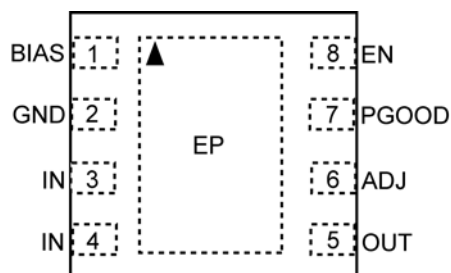
## Ordering Information

Part Number	Marking Code <sup>(1)</sup>	Output Voltage	Package <sup>(2,3)</sup>	Lead Finish
MIC47053YMT	Z53	ADJ	8 pin 2mm x 2mm Thin DFN	Pb-Free

### Notes:

1. Over bar symbol ( ¯ ) may not be to scale.
2. Thin DFN is a GREEN RoHS-compliant package. Lead finish is NiPdAu. Mold compound is Halogen Free.
3. Thin DFN package Pin 1 identifier = ▲.

## Pin Configuration



8-Pin 2mm x 2mm Thin DFN (MT)  
Top View

## Pin Description

Pin Number	Pin Name	Pin Function
1	BIAS	Bias Supply. The bias supply is the power supply for the internal circuitry of the regulator.
2	GND	Ground. Ground pins and exposed pad must be connected externally.
3, 4	IN	Input Supply. Drain of NMOS pass transistor which is the power input voltage for regulator. The NMOS pass transistor steps down this input voltage to create the output voltage.
5	OUT	Output. Output Voltage of Regulator.
6	ADJ	Adjust Input. Connect external resistor divider to program the output voltage.
7	PGOOD	Power Good Output. Open-drain output. Output is driven low when the output voltage is less than the power good threshold of its programmed nominal output voltage. When the output goes above the power good threshold, the open-drain output goes high-impedance, allowing it to be pulled up to a fixed voltage.
8	EN	Enable: TTL/CMOS compatible input. Logic high = enable, logic low = shutdown.
EP	ePad	Exposed thermal pad. Connect to the ground plane to maximize thermal performance.

**Absolute Maximum Ratings<sup>(1)</sup>**

Bias Supply Voltage ( $V_{BIAS}$ )	–0.3V to +6V
IN Supply Voltage ( $V_{IN}$ )	–0.3V to +4V
OUT Pin Voltage ( $V_{OUT}$ )	–0.3V to $V_{IN}$
ADJ Pin Voltage ( $V_{ADJ}$ )	–0.3V to +6V
Power Good (PGOOD) Voltage ( $V_{PGOOD}$ )	–0.3V to +6V
Enable Voltage ( $V_{EN}$ )	–0.3V to +6V
Lead Temperature (soldering, 10s)	260°C
Storage Temperature ( $T_S$ )	–65°C to +150°C
ESD Rating <sup>(3)</sup>	ESD Sensitive
Power Dissipation <sup>(4)</sup>	Internally Limited

**Operating Ratings<sup>(2)</sup>**

IN Supply Voltage ( $V_{IN}$ )	+1.0V to +3.6V ( $V_{IN} < V_{BIAS}$ )
Bias Voltage ( $V_{BIAS}$ )	+2.3V to +5.5V
Enable Voltage ( $V_{EN}$ )	0V to $V_{BIAS}$
Power Good Voltage ( $V_{PGOOD}$ )	0V to $V_{BIAS}$
Output Voltage Range	0.4V to 3.4V
Junction Temperature ( $T_J$ )	–40°C to +125°C
Ambient Temperature ( $T_A$ )	–40°C to +125°C
Junction Thermal Resistance	
2mm x 2mm Thin DFN-8L ( $\theta_{JA}$ )	90°C/W

**Electrical Characteristics<sup>(5)</sup>**

$V_{IN} = V_{OUT} + 0.5V$ ;  $V_{BIAS} = V_{OUT} + 2.1V$ ;  $C_{OUT} = 1\mu F$ ;  $I_{OUT} = 100\mu A$ ;  $T_J = 25^\circ C$ , **bold** values indicate  $-40^\circ C \leq T_J \leq +125^\circ C$ , unless noted.

Parameter	Condition	Min.	Typ.	Max.	Units
<b>Input Supply</b>					
Input Voltage Range ( $V_{IN}$ )		<b>1.0</b>		<b>3.6</b>	V
$V_{IN}$ UVLO Threshold <sup>(6)</sup>	$V_{IN}$ Rising	<b>0.7</b>	0.81	<b>1.0</b>	V
$V_{IN}$ UVLO Hysteresis			25		mV
Ground Current in Shutdown ( $I_{GND}$ )	$V_{EN} = 0V$ (Regulator Shutdown)		0.1	1.0	$\mu A$
Ground Current ( $I_{GND}$ )	$I_{OUT} = 500mA$ ; $V_{IN} = V_{OUT} + 0.5V$		6	<b>15</b>	$\mu A$
<b>Bias Supply</b>					
BIAS Input Voltage ( $V_{BIAS}$ )		<b>2.3</b>		<b>5.5</b>	V
$V_{BIAS}$ UVLO Threshold <sup>(6)</sup>	$V_{BIAS}$ Rising	<b>1.7</b>	2.0	<b>2.3</b>	V
$V_{BIAS}$ UVLO Hysteresis			70		mV
Dropout Voltage ( $V_{BIAS} - V_{OUT}$ )	$I_{OUT} = 100mA$ $I_{OUT} = 500mA$		1.3 1.4	<b>2.1</b>	V
$V_{BIAS}$ Supply Current ( $I_{BIAS}$ )	$I_{OUT} = 500mA$ ; $V_{BIAS} = V_{OUT} + 2.1V$		330	<b>500</b>	$\mu A$
$V_{BIAS}$ Supply Current in Shutdown ( $I_{BIAS}$ )	$V_{EN} = 0V$ (Regulator Shutdown)		0.1	<b>1.0</b>	$\mu A$
<b>Output Voltage</b>					
Dropout Voltage ( $V_{IN} - V_{OUT}$ )	$I_{OUT} = 100mA$ $I_{OUT} = 500mA$		12 49	<b>50</b> <b>120</b>	mV
Output Voltage Accuracy	$I_{OUT} = 100\mu A$	<b>–2.0</b>		<b>+2.0</b>	%
$V_{BIAS}$ Line Regulation	$V_{BIAS} = V_{OUT} + 2.1V$ to 5.5V	–0.1		0.1	%/V

## Electrical Characteristics <sup>(5)</sup> (Continued)

$V_{IN} = V_{OUT} + 0.5V$ ;  $V_{BIAS} = V_{OUT} + 2.1V$ ;  $C_{OUT} = 1\mu F$ ;  $I_{OUT} = 100\mu A$ ;  $T_J = 25^\circ C$ , **bold** values indicate  $-40^\circ C \leq T_J \leq 125^\circ C$ , unless noted.

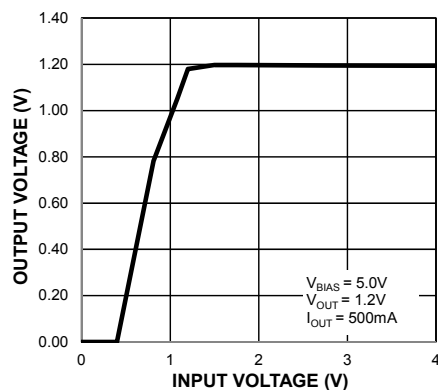
Parameter	Condition	Min.	Typ.	Max.	Units
$V_{IN}$ Line Regulation	$V_{IN} = V_{OUT} + 0.5V$ to $3.6V$	-0.05		0.05	%/V
Load Regulation	$I_{OUT} = 10mA$ to $500mA$	-0.5	0.2	0.5	%
<b>Current Limit</b>					
Short-Circuit Current Limit	$V_{IN} = 2.7V$ ; $V_{OUT} = 0V$	0.6	1.6	2.5	A
<b>Enable Input</b>					
EN Logic Level High		<b>1.0</b>			V
EN Logic Level Low				<b>0.2</b>	V
Enable Bias Current	$V_{EN} = 0V$ (Regulator Shutdown) $V_{EN} = 1.0V$ (Regulator Enabled)		0 6	<b>2</b> <b>10</b>	$\mu A$
Turn-On Time	$C_{OUT} = 1\mu F$ ; 90% of typical $V_{OUT}$		25	<b>500</b>	$\mu s$
<b>Thermal Protection</b>					
Over-Temperature Shutdown	$T_J$ Rising		160		$^\circ C$
Over-Temperature Shutdown Hysteresis			20		$^\circ C$
<b>Power Good (PGOOD)</b>					
PGOOD Threshold Voltage	$V_{OUT}$ Rising $V_{OUT}$ Falling	85	90.5 89.5	95	%
PGOOD Hysteresis			1		%
PGOOD Output Low Voltage	$I_{PG} = 250\mu A$		0.02	0.1	V
PGOOD Leakage Current	$V_{PG} = 5.0V$	-1	0.01	+1	$\mu A$
<b>Reference Voltage</b>					
Feedback Reference Voltage	$I_{OUT} = 100\mu A$	<b>0.392</b>	0.4	<b>0.408</b>	V
FB Bias Current	$V_{FB} = 0.8V$		20		nA
<b>Output Voltage Noise and Ripple Rejection</b>					
Output Voltage Noise	$f = 10Hz$ to $100kHz$ ; $I_{OUT} = 500mA$ ; $C_{OUT} = 1\mu F$		111		$\mu V_{RMS}$
Ripple Rejection	$f = 10kHz$ ; $C_{OUT} = 1\mu F$ , $I_{OUT} = 100mA$		47		dB
	$f = 100kHz$ ; $C_{OUT} = 1\mu F$ , $I_{OUT} = 100mA$		35		

### Notes:

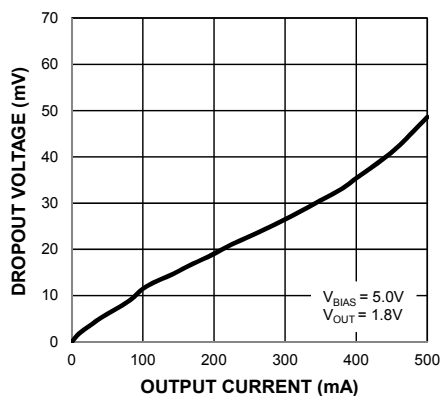
- Exceeding the absolute maximum rating may damage the device.
- The device is not guaranteed to function outside its operating rating.
- Devices are ESD sensitive. Handling precautions recommended. Human body model,  $1.5k\Omega$  in series with  $100pF$ .
- The maximum allowable power dissipation of any  $T_A$  (ambient temperature) is  $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$ .
- Specification for packaged product only.
- Both  $V_{IN}$  and  $V_{BIAS}$  UVLO thresholds must be met for the output voltage to turn-on. If either of the two input voltages is below the UVLO thresholds, the output is disabled.

## Typical Characteristics

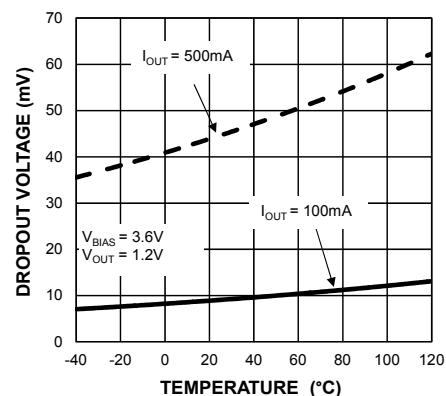
Output Voltage vs.  
Input Voltage



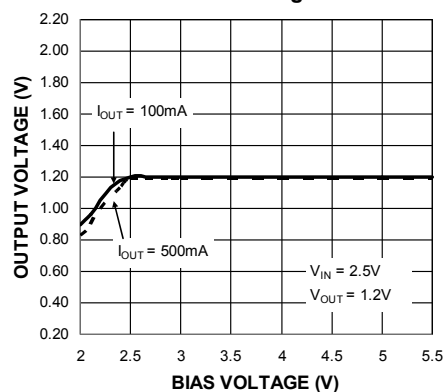
Input Dropout Voltage vs.  
Output Current



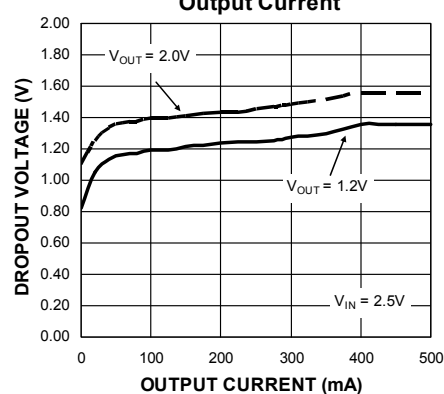
Input Dropout Voltage  
vs. Temperature



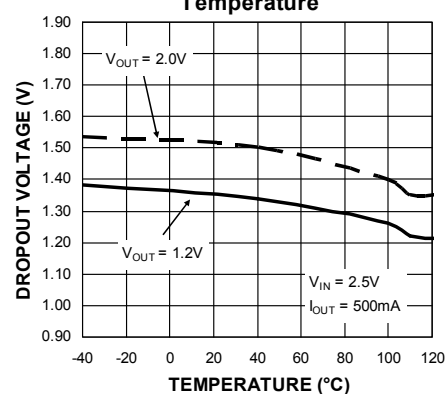
Output Voltage vs.  
Bias Voltage



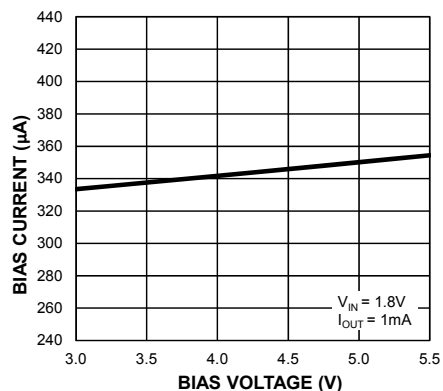
Bias Dropout Voltage vs.  
Output Current



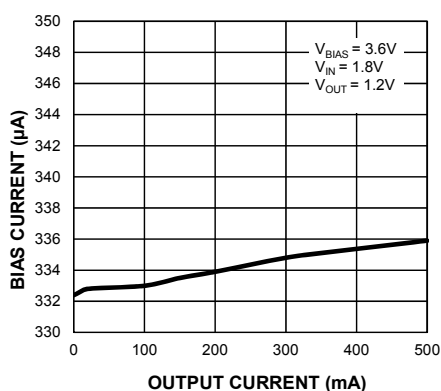
Bias Dropout Voltage vs.  
Temperature



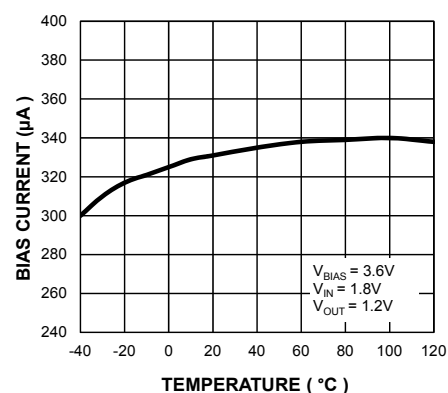
Bias Current vs.  
Bias Voltage



Bias Current vs.  
Output Current

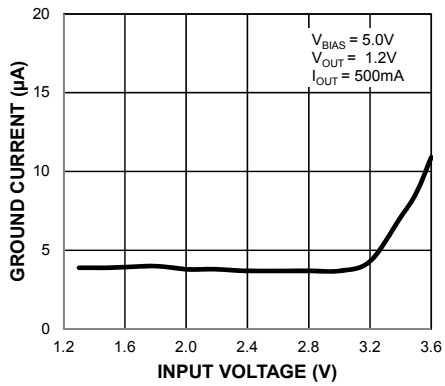


Bias Current vs.  
Temperature

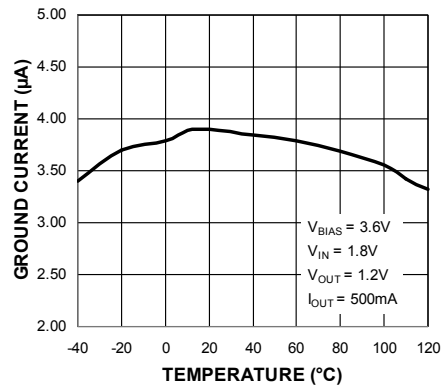


## Typical Characteristics (Continued)

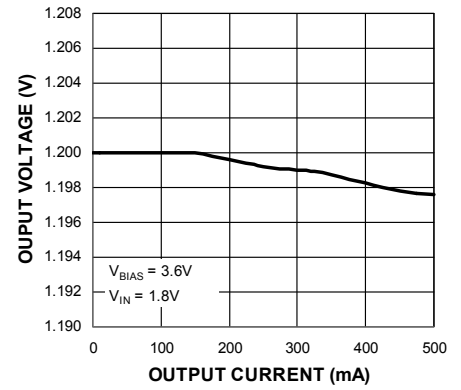
Ground Current vs.  
Input Voltage



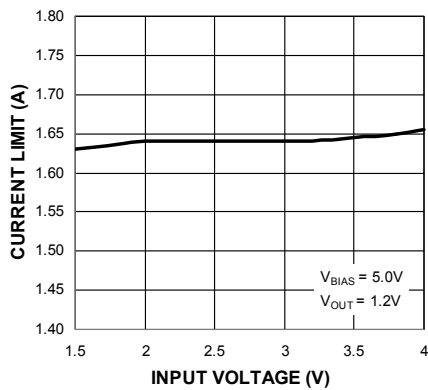
Ground Current vs.  
Temperature



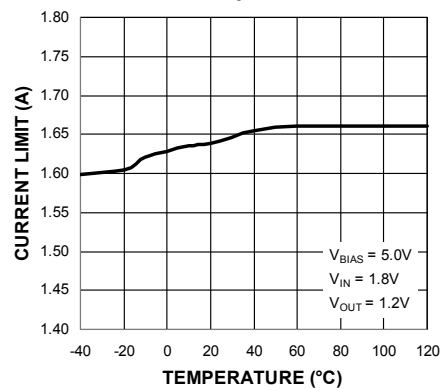
Output Voltage vs.  
Output Current



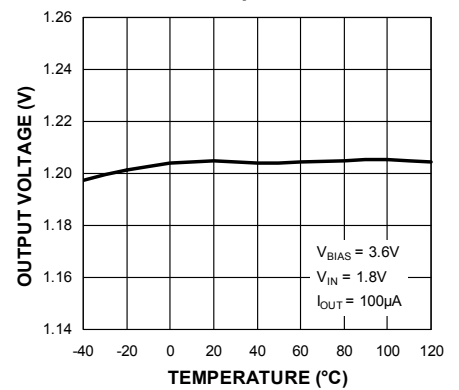
Current Limit vs.  
Input Voltage



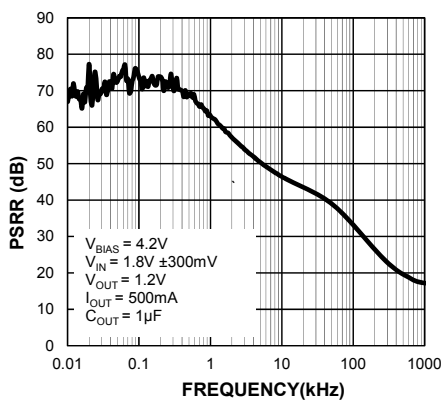
Current Limit vs.  
Temperature



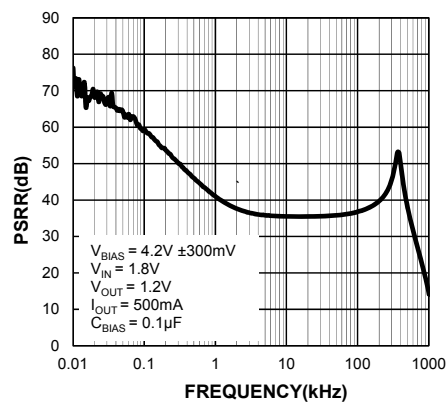
Output Voltage vs.  
Temperature



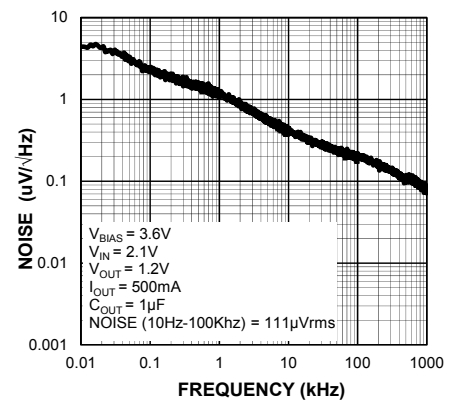
Power Supply Ripple Rejection  
(Input Voltage)



Power Supply Rejection Ratio  
(Bias Voltage)

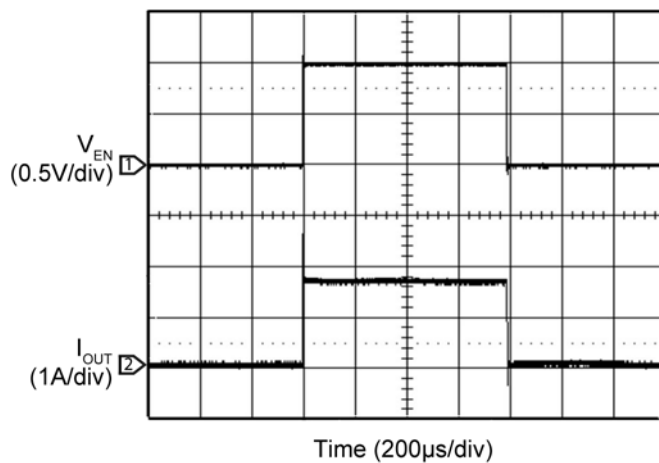


Output Noise

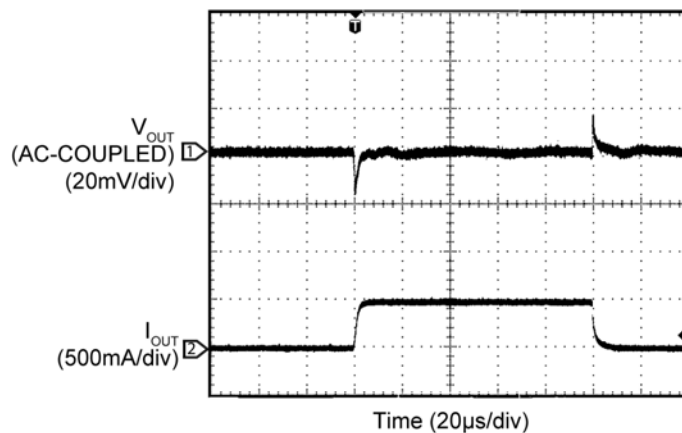


## Functional Characteristics

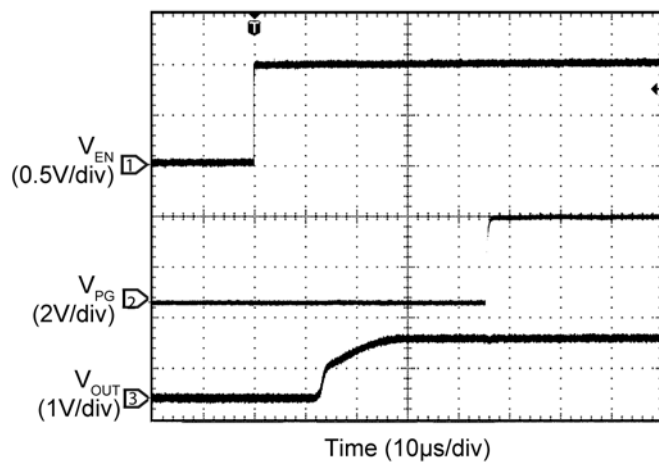
Enable Into Short Circuit



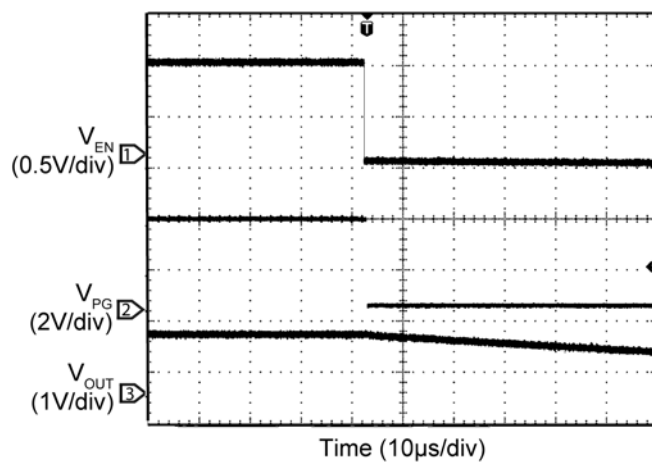
Load Transient Response



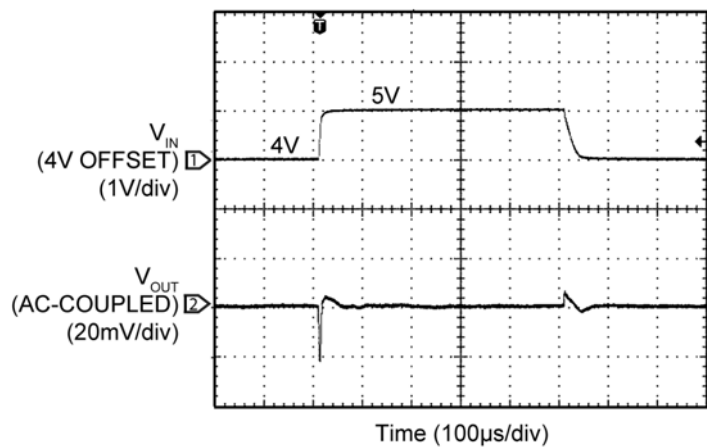
Enable Turn-On Time



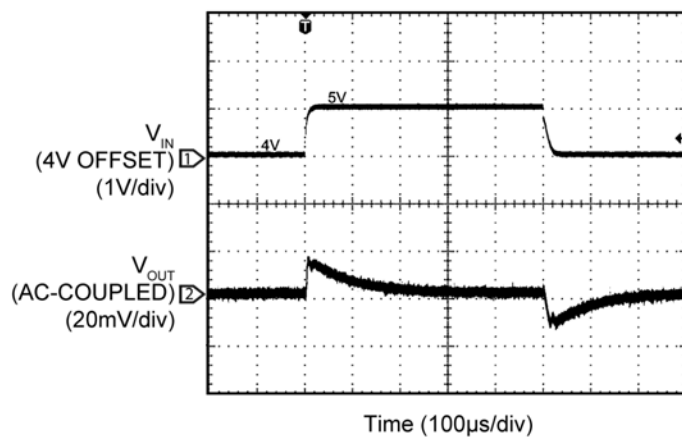
Enable Turn-Off Time



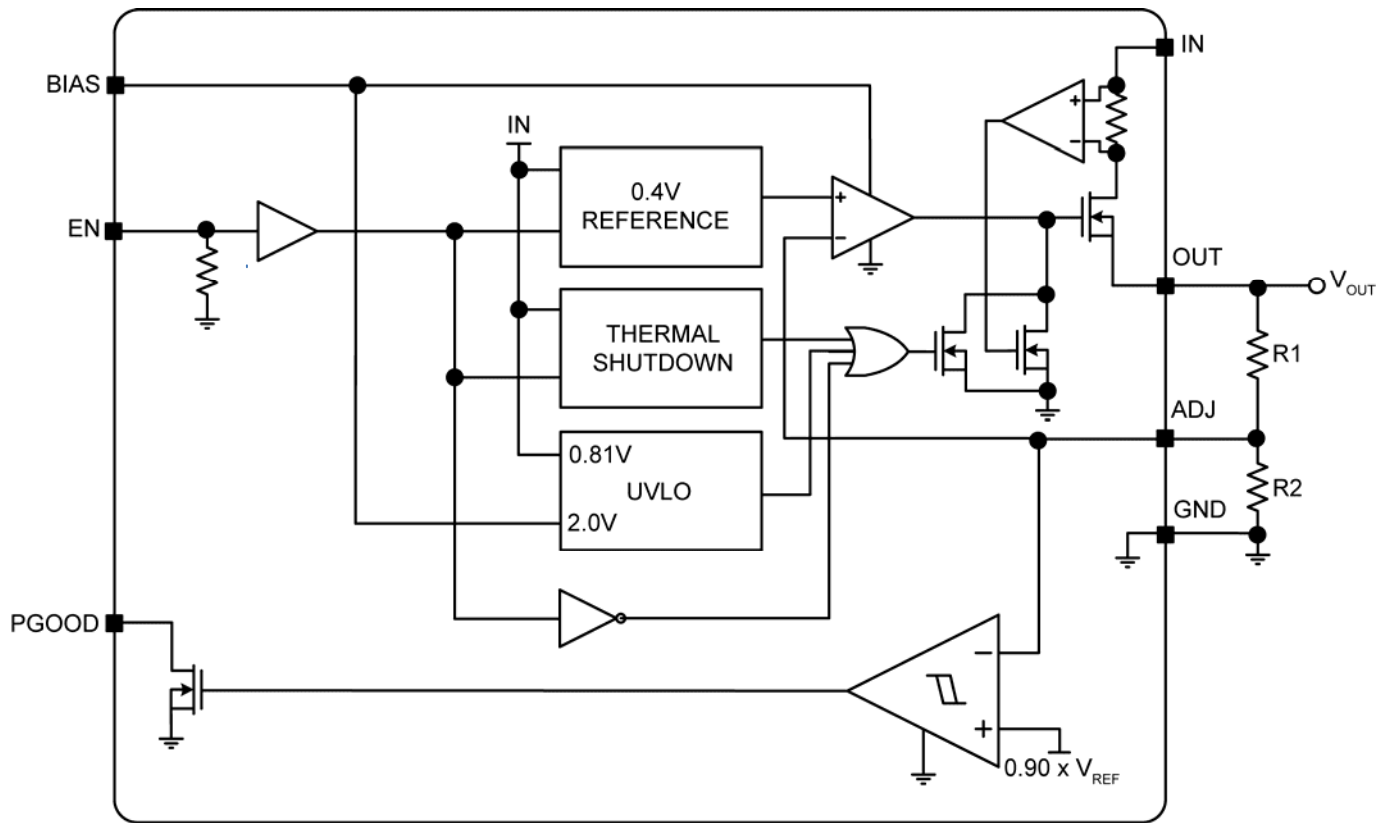
Input Line Transient



Bias Line Transient



## Functional Diagram



MIC47053 Adjustable Output Block Diagram



## Functional Description

The MIC47053 is a high-speed, ultra-low dropout, NMOS ULDO designed to take advantage of point-of-load applications that use supply rails to generate a low-voltage, high-current power supply. The MIC47053 can source 0.5A of output current while only requiring a 1μF ceramic output capacitor for stability. The MIC47053 regulator is fully protected from damage due to fault conditions, offering linear current limiting and thermal shutdown.

### Bias Supply Voltage

V<sub>BIAS</sub>, requiring relatively light current, provides power to the control portion of the MIC47053. Bypassing on the bias pin is recommended to improve performance of the regulator during line and load transients. Small 0.1μF ceramic capacitors from V<sub>BIAS</sub>-to-ground help reduce high frequency noise from being injected into the control circuitry from the bias rail and are good design practice.

### Input Supply Voltage

V<sub>IN</sub> provides the supply to power the LDO. The minimum input voltage is 1.0V. This allows conversion from low voltage supplies to reduce the power dissipation in the pass element.

### Input Capacitor

The MIC47053 is a high-performance, high bandwidth device. Therefore, it requires a well-bypassed input supply for optimal performance. A 1μF capacitor is the minimum required for stability. A 10μF ceramic capacitor is recommended for most applications, especially if the LDO's headroom (V<sub>IN</sub> - V<sub>OUT</sub>) is small and/or large load transients are present. Fast load transient and low headroom requires a larger input filter capacitor to ensure that the regulator does not drop out of regulation. A 10μF will better attenuate any voltage glitches from exceeding the maximum voltage rating of the part.

Additional high-frequency capacitors, such as small-valued NPO dielectric-type capacitors, help filter out high-frequency noise and are good practice in any RF-based circuit.

X7R and X5R dielectric ceramic capacitors are recommended because of their temperature performance. X7R-type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors are not recommended since they change value by as much as 50% and 60% respectively over their operating temperature ranges. To use a ceramic-chip capacitor with Y5V dielectric, the value must be much higher than an X7R ceramic or a tantalum capacitor to ensure the same capacitance value over the operating temperature range.

Tantalum capacitors have a very stable dielectric (10% over their operating temperature range) and can also be used with this device.

### Output Capacitor

The MIC47053 requires an output capacitor of 1μF or greater to maintain stability. The design is optimized for use with low-ESR ceramic chip capacitors. High-ESR capacitors may cause high-frequency oscillation. The output capacitor can be increased, but performance has been optimized for a 1μF ceramic output capacitor and does not improve significantly with larger capacitance. (See the *Typical Characteristic* section for examples of load transient response).

The output capacitor type and placement criteria are the same as the input capacitor. See the "Input Capacitor" subsection for a detailed description.

### Minimum Load Current

The MIC47053, unlike most other regulators, does not require a minimum load to maintain output voltage regulation.

### Adjustable Regulator Design

The MIC47053 allows programming of the output voltage with external resistors. The R2 resistor connected between the ADJ pin and ground should not exceed 10kΩ, as larger values can cause instability. R1 connects between the ADJ pin and the OUT pin. The resistor values are calculated as follows:

$$R1 = R2 \times \left( \frac{V_{OUT}}{0.4V} - 1 \right)$$

Where V<sub>OUT</sub> is the desired output voltage and 0.4V is the internal reference voltage.

### Enable/Shutdown

The MIC47053 comes with a single active-high enable pin that allows the regulator to be disabled. Forcing the enable pin low disables the regulator and sends it into a "zero" off-mode-current state. In this state, current consumed by the regulator goes nearly to zero. Forcing the enable pin high enables the output voltage.

### Power Good (PGOOD)

The Power Good (PGOOD) pin is an open drain output that goes low when the output voltage (fixed version) drops below the PGOOD threshold voltage.

The pull-up resistor value should be large enough to guarantee a proper “low” voltage when the PGOOD pin pulls low. The PGOOD low voltage is typically 0.1V at 250uA current. A 10k resistor or greater is recommended when pulling up to 3.3V bias.

If the PGOOD function is not required, the PGOOD pin may be left unconnected.

### Thermal Shutdown

The MIC47053 has an internal over-temperature protection feature. This feature is for protection only. The device should never be intentionally operated near this temperature as this may reduce long term reliability. The device will turn off when the over-temperature threshold is exceeded. A 20°C hysteresis is built in to allow the device to cool before turning back on.

### Thermal Considerations

The MIC47053 is designed to provide 0.5A of continuous current in a very small package. Maximum ambient operating temperature can be calculated based upon the output current and the voltage drop across the part. Given that the input voltage is 1.8V, the output voltage is 1.2V and the output current is 0.5A. The actual power dissipation of the regulator circuit can be determined using the equation:

$$P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT} + V_{IN} \cdot I_{GND} + V_{BIAS} \cdot I_{BIAS}$$

Because this device is CMOS, the ground current is insignificant for power dissipation and can be ignored for this calculation.

$$P_D = (1.8V - 1.2V) \cdot 0.5A = 0.3W$$

To determine the maximum ambient operating temperature of the package, use the junction-to-ambient thermal resistance of the device and the following basic equation:

$$P_{D(MAX)} = \left[ \frac{T_{J(MAX)} - T_A}{\Theta_{JA}} \right]$$

$T_{J(MAX)} = 125^\circ\text{C}$ , the maximum junction temperature of the die.

$\Theta_{JA}$  thermal resistance =  $90^\circ\text{C/W}$ .

Table 1 shows junction-to-ambient and junction to case thermal resistance for the MIC47053 in the thin DFN.

Package	$\Theta_{JA}$ Recommended Minimum Footprint	$\Theta_{JC}$
8-pin 2mm x 2mm Thin DFN	$90^\circ\text{C/W}$	$45^\circ\text{C/W}$

**Table 1. Thermal Resistance**

Substituting  $P_D$  for  $P_{D(max)}$  and solving for the ambient operating temperature will give the maximum operating conditions for the regulator circuit. The junction-to-ambient thermal resistance for the minimum footprint is  $90^\circ\text{C/W}$ . The maximum power dissipation must not be exceeded for proper operation. For example, when operating the MIC47053-1.2YMT at an input voltage of 1.8V and a 0.5A load with a minimum footprint layout, the maximum ambient operating temperature  $T_A$  can be determined as follows:

$$T_A = T_{J(MAX)} - \Theta_{JA} \times P_{D(MAX)}$$

$$T_A = 125^\circ\text{C} - 90^\circ\text{C/W} \times 0.3W$$

$$T_A = 98^\circ\text{C}$$

Therefore, a 1.2V application with 0.5A of output current can accept an ambient operating temperature of  $98^\circ\text{C}$  in a 2mm x 2mm thin DFN.

## Thermal Measurements

Measuring the IC's case temperature is recommended to ensure it is within its operating limits. Although this might seem like a very elementary task, it is easy to get erroneous results. The most common mistake is to use the standard thermal couple that comes with a thermal meter. This thermal couple wire gauge is large, typically 22 gauge, and behaves like a heatsink, resulting in a lower case measurement.

Two methods of temperature measurement are using a smaller thermal couple wire or an infrared thermometer. If a thermal couple wire is used, it must be constructed of 36 gauge wire or higher (smaller wire size) to minimize the wire heat-sinking effect.

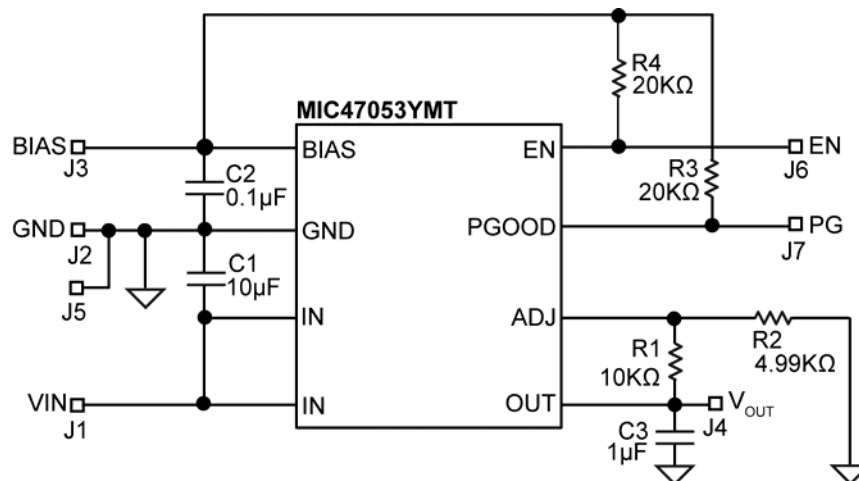
In addition, the thermal couple tip must be covered in either thermal grease or thermal glue to make sure that the thermal couple junction is making good contact with the case of the IC. Omega brand thermal couple (5SC-TT-K-36-36) is adequate for most applications.

Wherever possible, an infrared thermometer is recommended. The measurement spot size of most infrared thermometers is too large for an accurate reading on a small form factor ICs. However, a IR thermometer from Optris has a 1mm spot size, which makes it a good choice for the 2mm x 2mm Thin DFN package. An optional stand makes it easy to hold the beam on the IC for long periods of time.

For a full discussion of heat sinking and thermal effects of voltage regulators, refer to the "Regulator Thermals" section of Micrel's *Designing with Low-Dropout Voltage Regulators* handbook. This information can be found on Micrel's website at:

[http://www.micrel.com/PDF/other/LDOBk\\_ds.pdf](http://www.micrel.com/PDF/other/LDOBk_ds.pdf)

## Typical Application Schematic



MIC47053 Adjustable Output

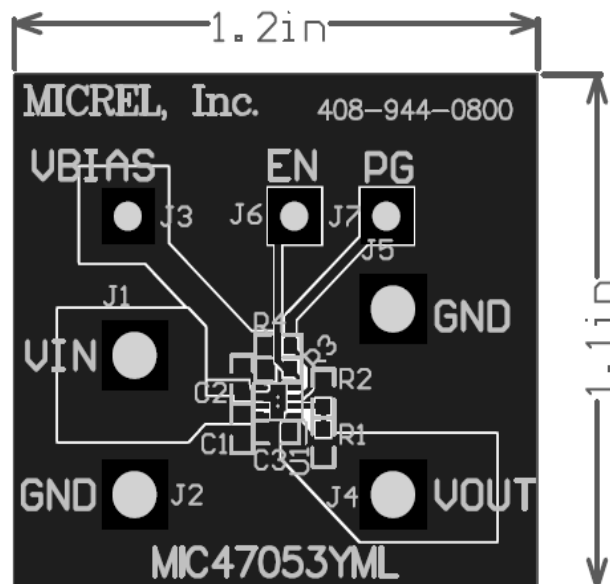
## MIC47053 Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1	GRM21BR60J106ME19	Murata <sup>(1)</sup>	Ceramic Capacitor, 10µF, 6.3V, X5R, Size 0603	1
	C1608X5R0J106MT	TDK <sup>(2)</sup>	Ceramic Capacitor, 10µF, 6.3V, X5R, Size 0603	
C2	06035D104MAT2A	AVX <sup>(3)</sup>	Ceramic Capacitor, 0.1µF, 50V, X5R, Size 0603	1
C3	GRM155R61A105KE15D	Murata <sup>(1)</sup>	Ceramic Capacitor, 1µF, 10V, X5R, Size 0603	1
	C1005X5R0J105KT	TDK <sup>(2)</sup>	Ceramic Capacitor, 1µF, 10V, X5R, Size 0603	
R1	CRCW060310K0FKEYE3	Vishay Dale <sup>(4)</sup>	Resistor, 10kΩ, 1/16W, 1%, Size 0603	1
R2	CRCW06034K99FKEYE3	Vishay Dale <sup>(4)</sup>	Resistor, 4.99kΩ, 1/16W, 1%, Size 0603	1
R3, R4	CRCW060320K0FKEYE3	Vishay Dale <sup>(4)</sup>	Resistor, 20kΩ, 1/16W, 1%, Size 0603	2
U1	MIC47053YMT	Micrel, Inc. <sup>(5)</sup>	Low Input and Output 500mA ULDO™ – Adjustable Output	1

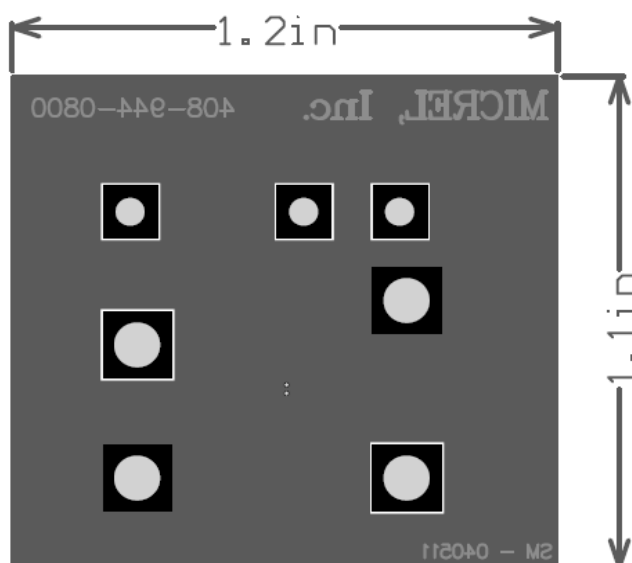
### Notes:

1. Murata: [www.murata.com](http://www.murata.com)
2. TDK: [www.tdk.com](http://www.tdk.com)
3. AVX: [www.avx.com](http://www.avx.com)
4. Vishay: [www.vishay.com](http://www.vishay.com)
5. Micrel, Inc.: [www.micrel.com](http://www.micrel.com)

## PCB Layout Recommendations



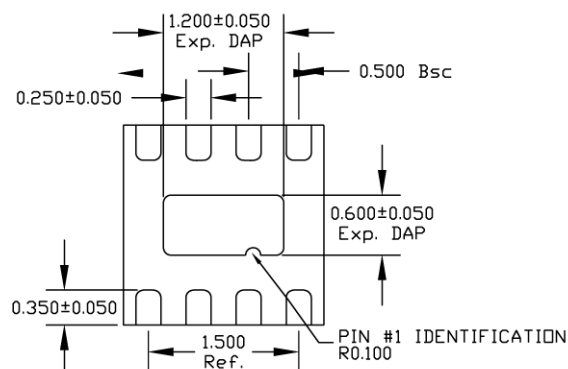
Top Layer



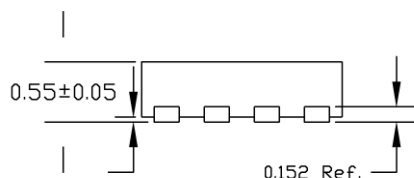
Bottom Layer

Figure 6-10 illustrates dimensioning a square feature. The width is dimensioned as  $2.000 \pm 0.050$ . The height is dimensioned as  $8$ . A callout indicates "PIN 1 ID BY MARKING".

TOP VIEW



BOTTOM VIEW



SIDE VIEW

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.08 mm.
3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID WILL BE LASER MARKED.

### 8-Pin 2mm x 2mm Thin DFN (MT)

**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**  
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB <http://www.micrel.com>

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