CY62256N

256K (32K x 8) Static RAM

Features

- Temperature Ranges
  - Commercial: 0°C to 70°C
  - Industrial: –40°C to 85°C
  - Automotive-A: –40°C to 85°C
  - Automotive-E: –40°C to 125°C
- High Speed: 55 ns
- Voltage Range: 4.5V to 5.5V Operation
- Low Active Power
  - 275 mW (max)
- Low Standby Power (LL version)
  - 82.5 µW (max)
- Easy Memory Expansion with $\overline{CE}$ and $\overline{OE}$ Features
- TTL-Compatible Inputs and Outputs
- Automatic Power Down when Deselected
- CMOS for Optimum Speed and Power
- Available in Pb-free and Non Pb-free 28-Pin (600-mil) PDIP, 28-Pin (300-mil) Narrow SOIC, 28-Pin TSOP-I, and 28-Pin Reverse TSOP-I Packages

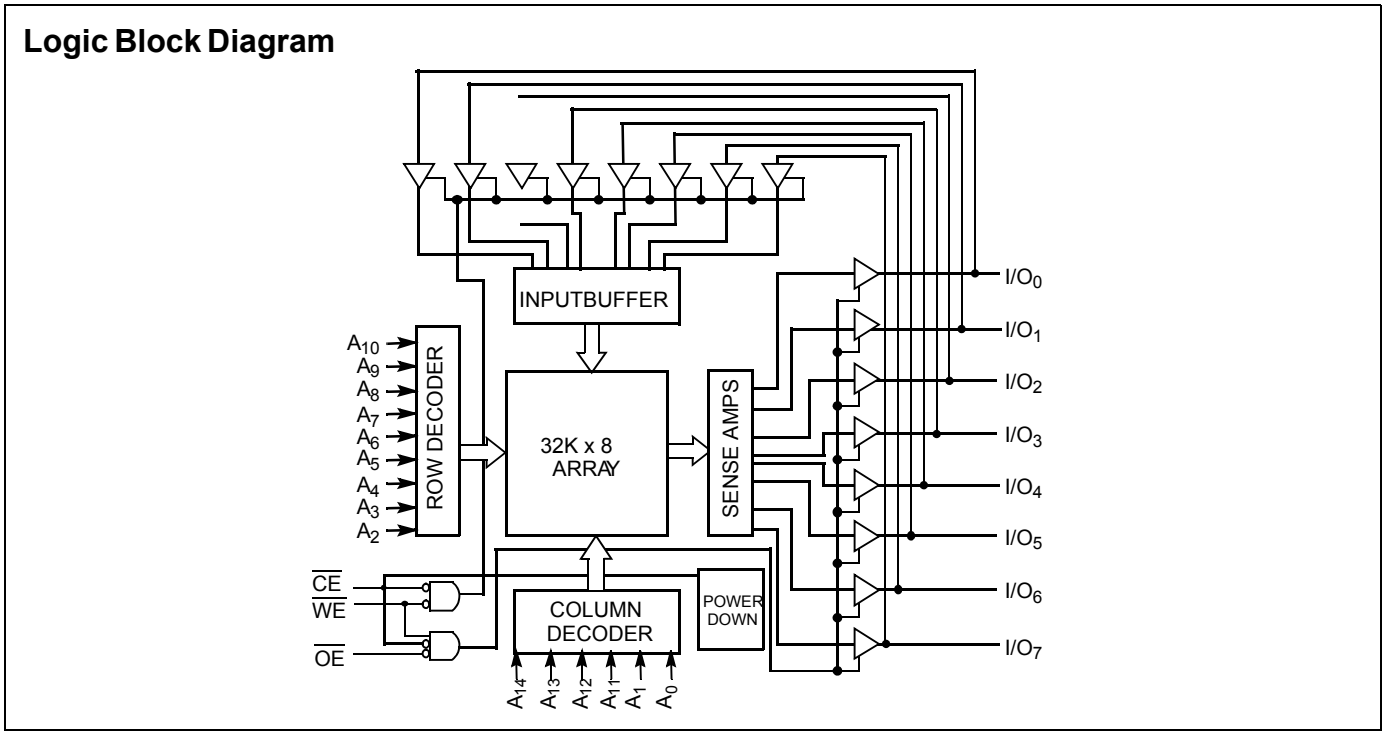
Functional Description

The CY62256N[1] is a high performance CMOS static RAM organized as 32K words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and active LOW output enable ($\overline{OE}$) and tristate drivers. This device has an automatic power down feature, reducing the power consumption by 99.9 percent when deselected.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



Note
1. For best practice recommendations, do refer to the Cypress application note “System Design Guidelines” on http://www.cypress.com

Product Portfolio

Product		V_{CC} Range (V)			Speed (ns)	Power Dissipation			
						Operating, I_{CC} (mA)		Standby, I_{SB2} (µA)	
		Min	Typ[2]	Max		Typ[2]	Max	Typ[2]	Max
CY62256NL	Commercial / Industrial	4.5	5.0	5.5	70	25	50	2	50
CY62256NLL	Commercial				70	25	50	0.1	5
CY62256NLL	Industrial				55/70	25	50	0.1	10
CY62256NLL	Automotive-A				55/70	25	50	0.1	10
CY62256NLL	Automotive-E				55	25	50	0.1	15

Pin Configurations

Figure 1. 28-Pin DIP and Narrow SOIC

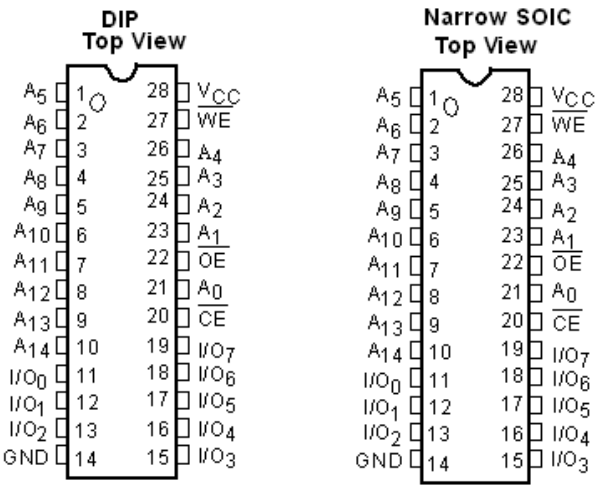


Figure 2. 28-Pin TSOP I and Reverse TSOP I

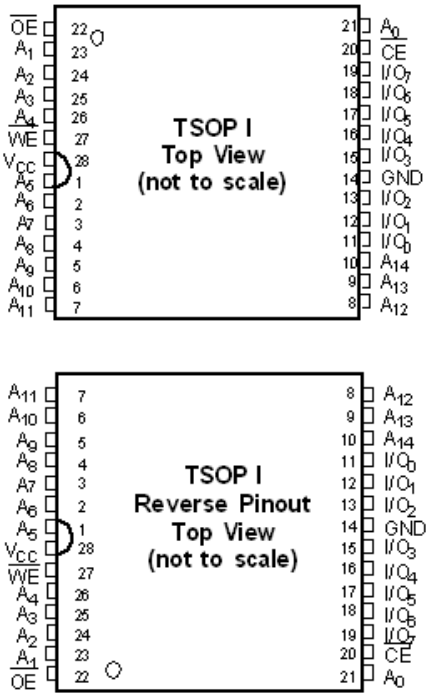


Table 1. Pin Definitions

Pin Number	Type	Description
1–10, 21, 23–26	Input	**A_0–A_{14}**. Address Inputs
11–13, 15–19,	Input/Output	**I/O_0–I/O_7**. Data lines. Used as input or output lines depending on operation
27	Input/Control	**WE**. When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted
20	Input/Control	**CE**. When LOW, selects the chip. When HIGH, deselects the chip
22	Input/Control	**OE**. Output Enable. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins
14	Ground	**GND**. Ground for the device
28	Power Supply	**V_{CC}**. Power supply for the device

Note
2. Typical specifications are the mean values measured over a large sample size across normal production process variations and are taken at nominal conditions (T_A = 25°C, V_{CC}). Parameters are guaranteed by design and characterization, and not 100% tested.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14)..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High-Z State[3]..... –0.5V to V_{CC} + 0.5V

DC Input Voltage[3] ..... –0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch up Current..... > 200 mA

Operating Range

Range	Ambient Temperature (T_A)[4]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%
Automotive-A	–40°C to +85°C	5V ± 10%
Automotive-E	–40°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		-55			-70			Unit
				Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1.0 mA		2.4			2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA				0.4			0.4	V
V_{IH}	Input HIGH Voltage			2.2		V_{CC} +0.5V	2.2		V_{CC} +0.5V	V
V_{IL}	Input LOW Voltage			–0.5		0.8	–0.5		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–0.5		+0.5	–0.5		+0.5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–0.5		+0.5	–0.5		+0.5	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	L-Commercial/ Industrial					25	50	mA
			LL-Commercial					25	50	mA
			LL - Industrial		25	50		25	50	mA
			LL - Auto-A		25	50		25	50	mA
			LL - Auto-E		25	50				mA
I_{SB1}	Automatic CE Power down Current—TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	L					0.4	0.6	mA
			LL-Commercial					0.3	0.5	mA
			LL - Industrial		0.3	0.5		0.3	0.5	mA
			LL - Auto-A		0.3	0.5		0.3	0.5	mA
			LL - Auto-E		0.3	0.5				mA
I_{SB2}	Automatic CE Power down Current—CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0	L					2	50	µA
			LL-Commercial					0.1	5	µA
			LL - Industrial		0.1	10		0.1	10	µA
			LL - Auto-A		0.1	10		0.1	10	µA
			LL - Auto-E		0.1	15				µA

Capacitance

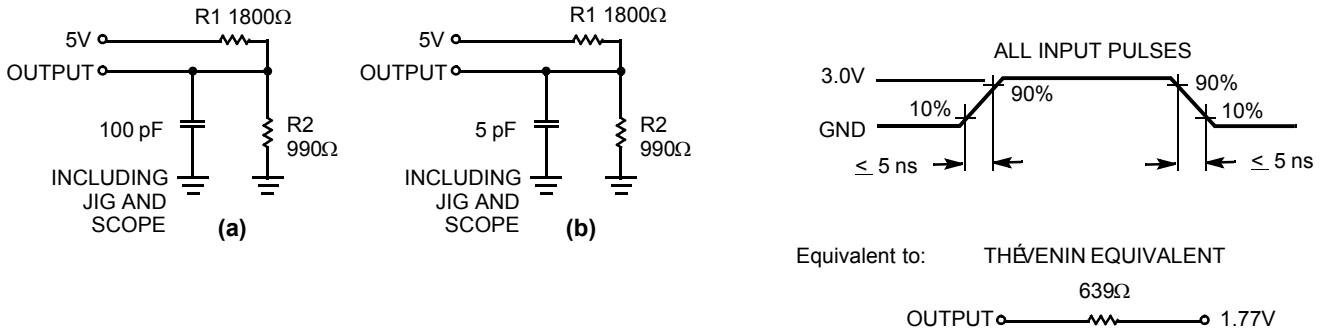
Parameter	Description	Test Conditions[5]	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	6	pF
C_{OUT}	Output Capacitance		8	pF

Notes
3. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
4. T_A is the "Instant-On" case temperature.
5. Tested initially and after any design or process changes that may affect these parameters.

Thermal Resistance

Parameter	Description[5]	Test Conditions	DIP	SOIC	TSOP	RTSOP	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	75.61	76.56	93.89	93.89	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		43.12	36.07	24.64	24.64	°C/W

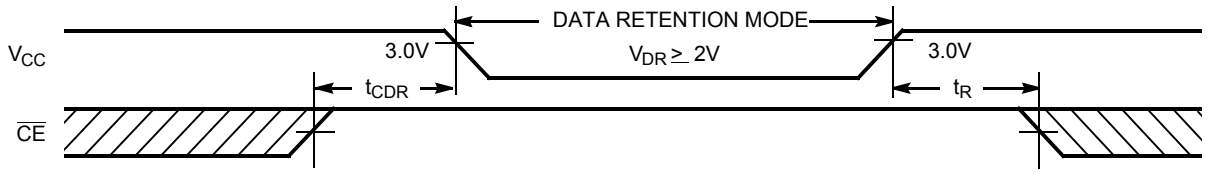
Figure 3. AC Test Loads and Waveforms



Data Retention Characteristics

Parameter	Description		Conditions[6]	Min	Typ[2]	Max	Unit
V_{DR}	V_{CC} for Data Retention			2.0			V
I_{CCDR}	Data Retention Current	L	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$, or $V_{IN} \leq 0.3V$		2	50	µA
		LL-Commercial			0.1	5	µA
		LL - Industrial/Auto-A			0.1	10	µA
		LL - Auto-E			0.1	10	µA
t_{CDR}[8]	Chip Deselect to Data Retention Time			0			ns
t_R[8]	Operation Recovery Time			t_{RC}			ns

Figure 4. Data Retention Waveform



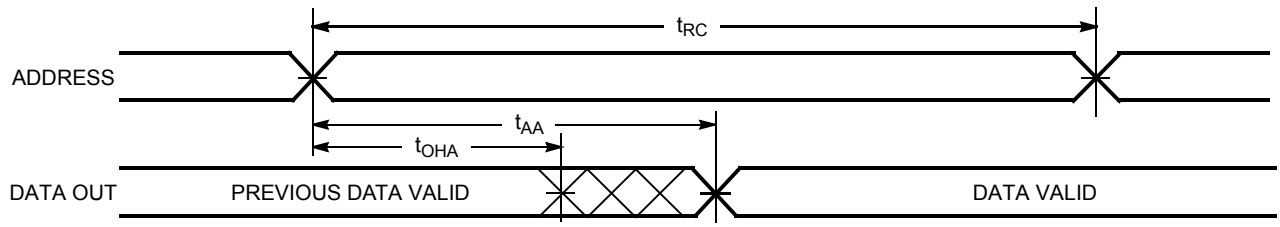
Note
6. No input may exceed V_{CC} + 0.5V.

Switching Characteristics Over the Operating Range[7]

Parameter	Description	CY62256N-55		CY62256N-70		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address to Data Valid		55		70	ns
t_{OHA}	Data Hold from Address Change	5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z[8]	5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[8, 9]		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z[8]	5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z[8, 9]		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power down		55		70	ns
Write Cycle[10, 11]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	45		60		ns
t_{AW}	Address Setup to Write End	45		60		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Setup to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	40		50		ns
t_{SD}	Data Setup to Write End	25		30		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[8, 9]		20		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[8]	5		5		ns

Switching Waveforms

Figure 5. Read Cycle No. 1[12, 13]



Notes
7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
8. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
9. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
10. The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a Write and either signal can terminate a Write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the Write.
11. The minimum Write cycle time for Write Cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.
12. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
13. $\overline{WE}$ is HIGH for Read cycle.

Switching Waveforms (continued)

Figure 6. Read Cycle No. 2[13, 14]

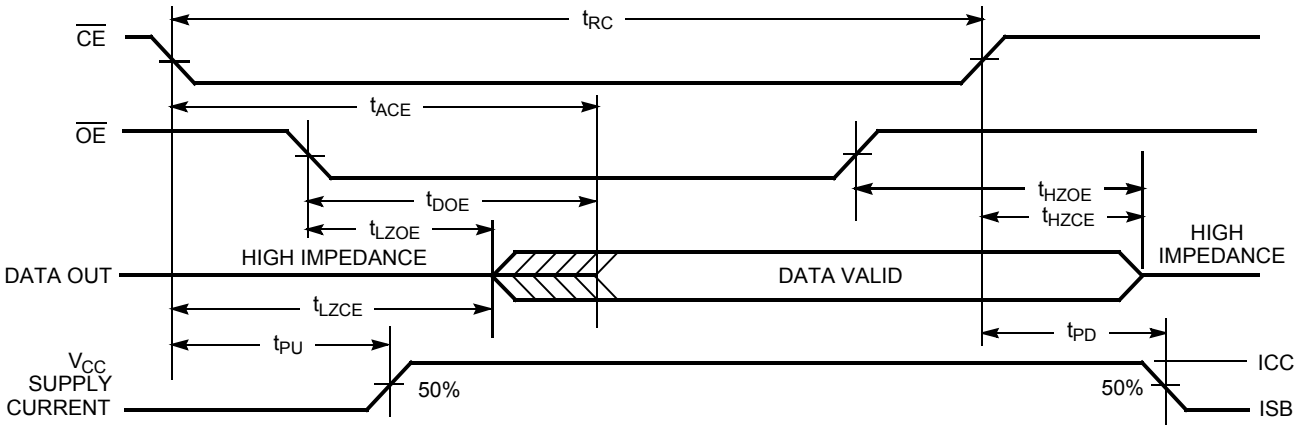


Figure 7. Write Cycle No. 1 ($\overline{WE}$ Controlled)[10, 15, 16]

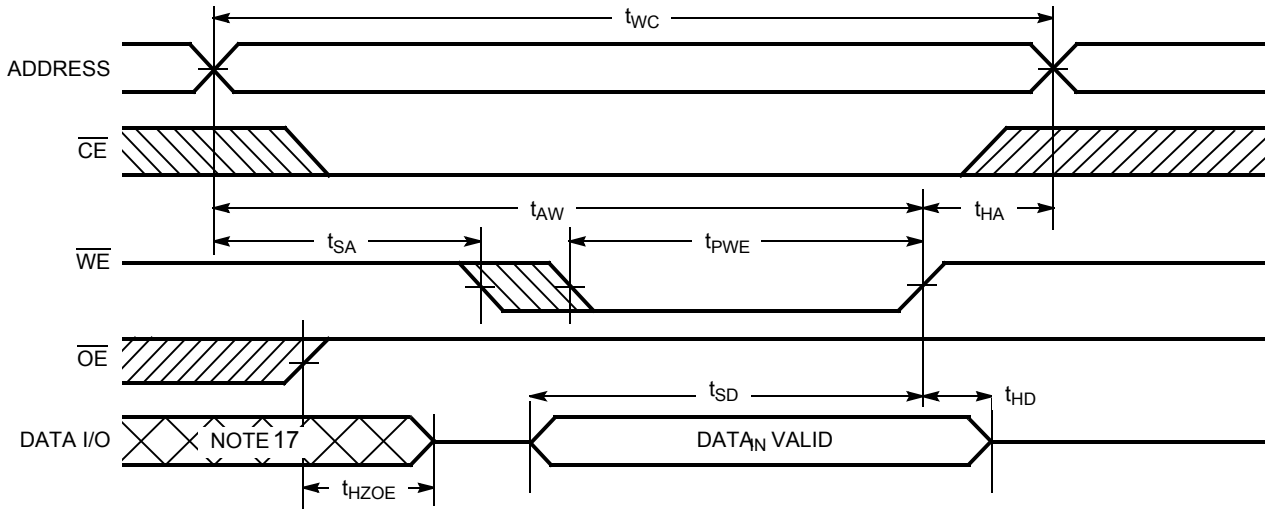
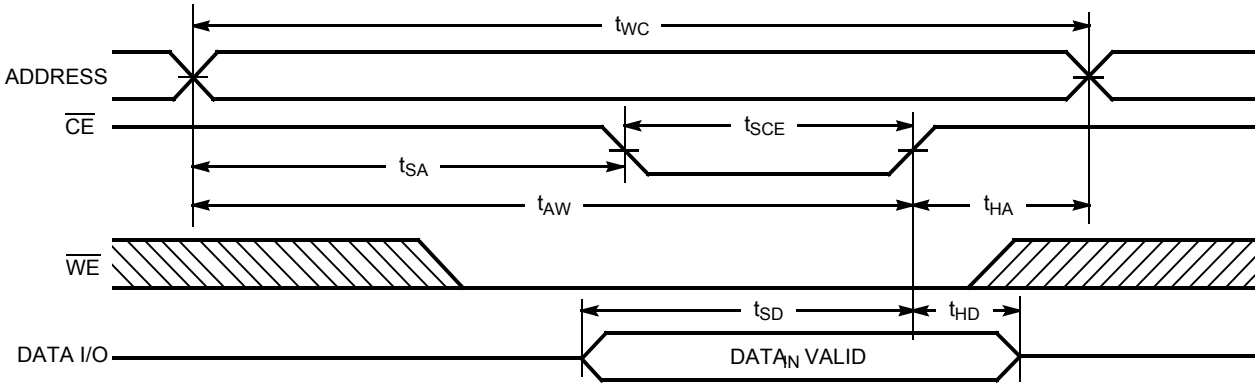


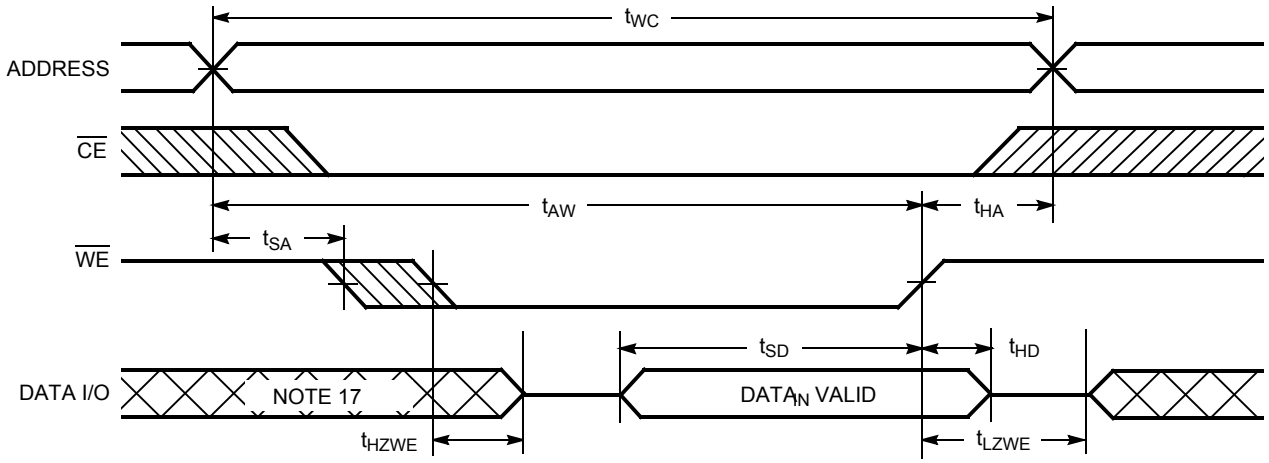
Figure 8. Write Cycle No. 2 ($\overline{CE}$ Controlled)[10, 15, 16]



Notes
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
15. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
17. During this period, the I/Os are in output state and input signals should not be applied.

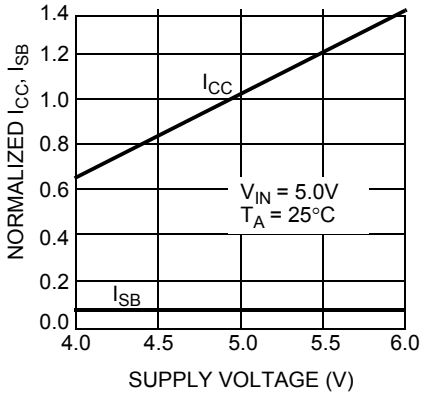
Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[11, 16]

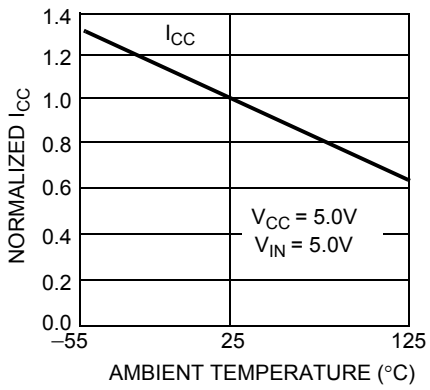


Typical DC and AC Characteristics

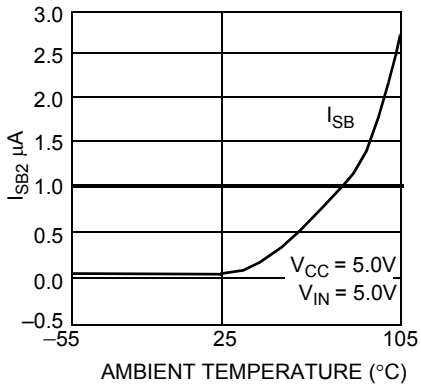
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



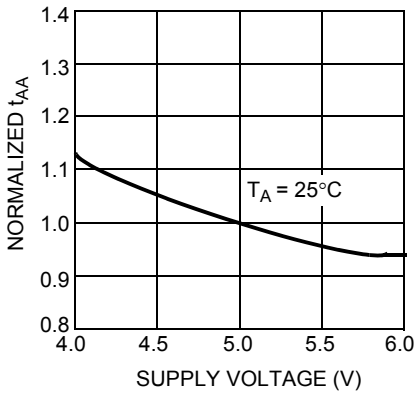
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



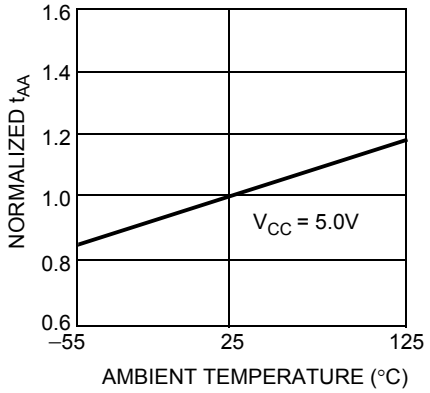
STANDBY CURRENT vs. AMBIENT TEMPERATURE



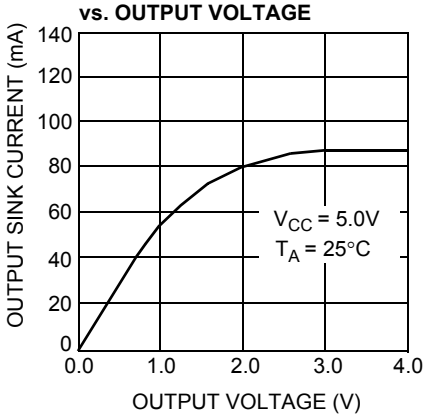
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



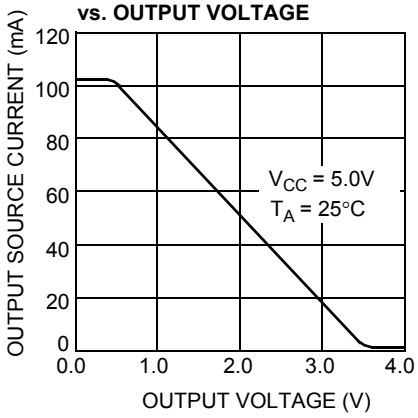
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

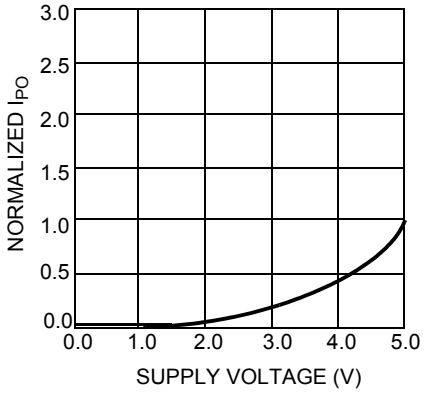


OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE

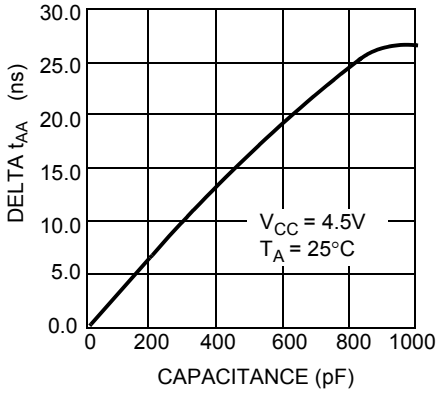


Typical DC and AC Characteristics (continued)

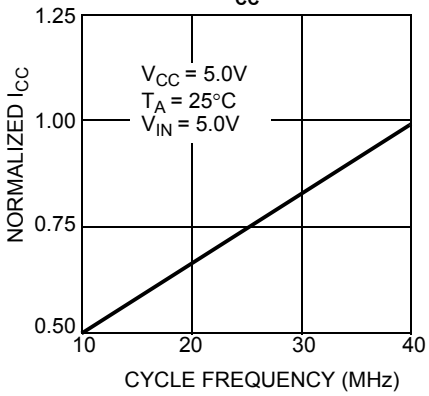
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High-Z	Deselect/Power down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High-Z	Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62256NLL–55SNI	51-85092	28-Pin (300-Mil) Narrow SOIC	Industrial
	CY62256NLL–55SNXI		28-Pin (300-Mil) Narrow SOIC (Pb-Free)	
	CY62256NLL–55ZI	51-85071	28-Pin TSOP I	
	CY62256NLL–55ZXI		28-Pin TSOP I (Pb-Free)	
	CY62256NLL–55ZXA	51-85071	28-Pin TSOP I (Pb-Free)	Automotive-A
	CY62256NLL–55SNXE	51-85092	28-Pin (300-Mil) Narrow SOIC (Pb-Free)	Automotive-E
	CY62256NLL–55ZXE	51-85071	28-Pin TSOP I (Pb-Free)	
	CY62256NLL–55ZRXE	51-85074	28-Pin Reverse TSOP I (Pb-Free)	
70	CY62256NL–70PC	51-85017	28-Pin (600-Mil) Molded DIP	Commercial
	CY62256NL–70PXC		28-Pin (600-Mil) Molded DIP (Pb-Free)	
	CY62256NLL–70PC		28-Pin (600-Mil) Molded DIP	
	CY62256NLL–70PXC		28-Pin (600-Mil) Molded DIP (Pb-Free)	
	CY62256NL–70SNC	51-85092	28-Pin (300-Mil) Narrow SOIC	
	CY62256NL–70SNXC		28-Pin (300-Mil) Narrow SOIC (Pb-Free)	
	CY62256NLL–70SNC		28-Pin (300-Mil) Narrow SOIC	
	CY62256NLL–70SNXC		28-Pin (300-Mil) Narrow SOIC (Pb-Free)	
	CY62256NLL–70ZC	51-85071	28-Pin TSOP I	
	CY62256NLL–70ZXC		28-Pin TSOP I (Pb-Free)	
	CY62256NL–70SNI	51-85092	28-Pin (300-Mil) Narrow SOIC	Industrial
	CY62256NL–70SNXI		28-Pin (300-Mil) Narrow SOIC (Pb-Free)	
	CY62256NLL–70SNI		28-Pin (300-Mil) Narrow SOIC	
	CY62256NLL–70SNXI		28-Pin (300-Mil) Narrow SOIC (Pb-Free)	
	CY62256NLL–70ZI	51-85071	28-Pin TSOP I	
	CY62256NLL–70ZXI		28-Pin TSOP I (Pb-Free)	
	CY62256NLL–70ZRI	51-85074	28-Pin Reverse TSOP I	
	CY62256NLL–70ZRXI		28-Pin Reverse TSOP I (Pb-Free)	
	CY62256NLL–70SNXA	51-85092	28-Pin (300-Mil) Narrow SOIC (Pb-Free)	Automotive-A

Do contact your local Cypress sales representative for availability of these parts

Package Diagrams

Figure 10. 28-Pin (600-Mil) Molded DIP (51-85017)

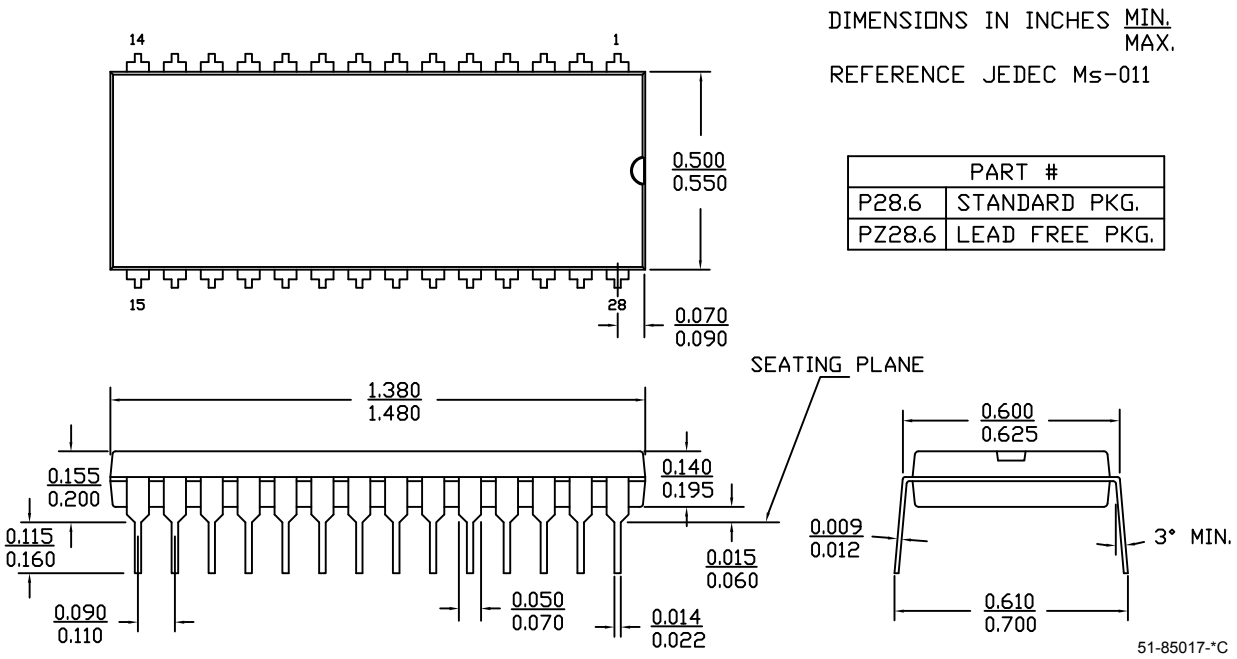


Figure 11. 28-Pin (300-mil) SNC (Narrow Body) (51-85092)

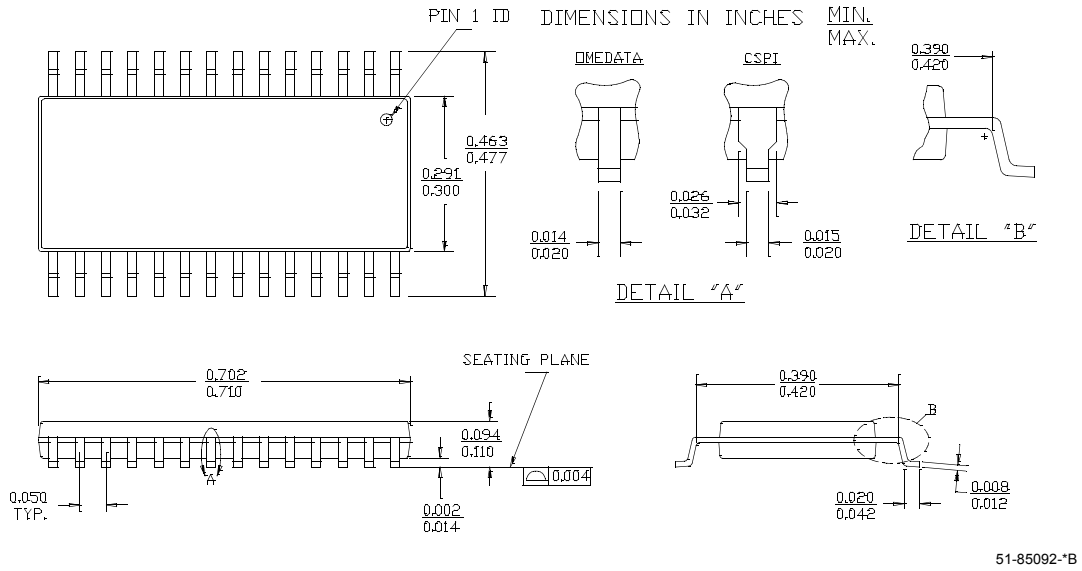


Figure 12. 28-Pin TSOP I (8 x 13.4 mm) (51-85071)

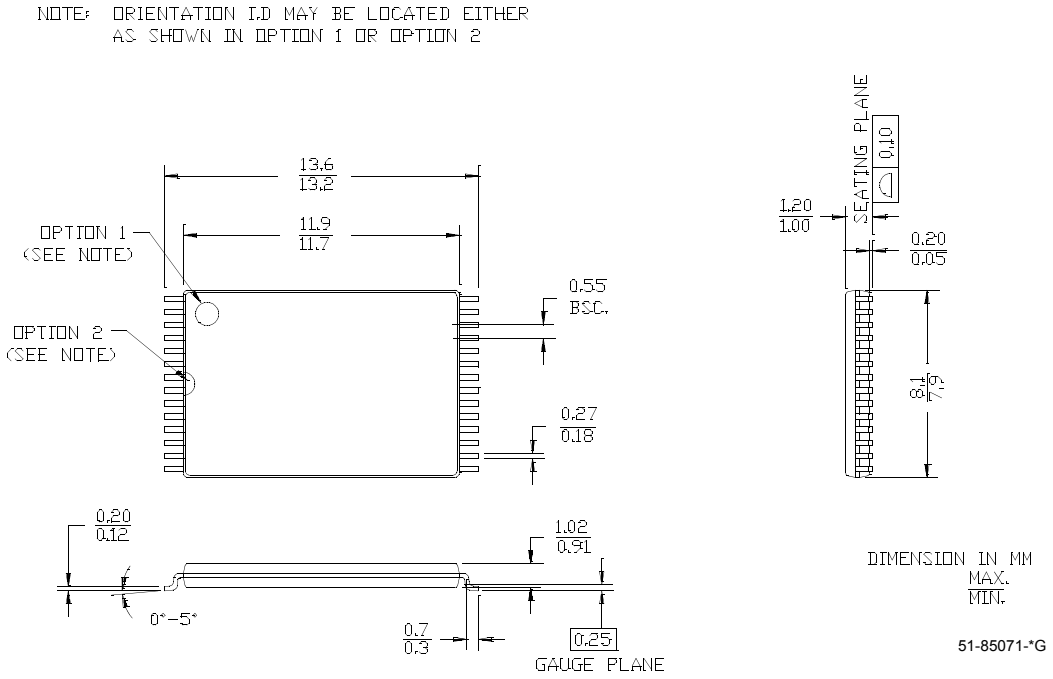
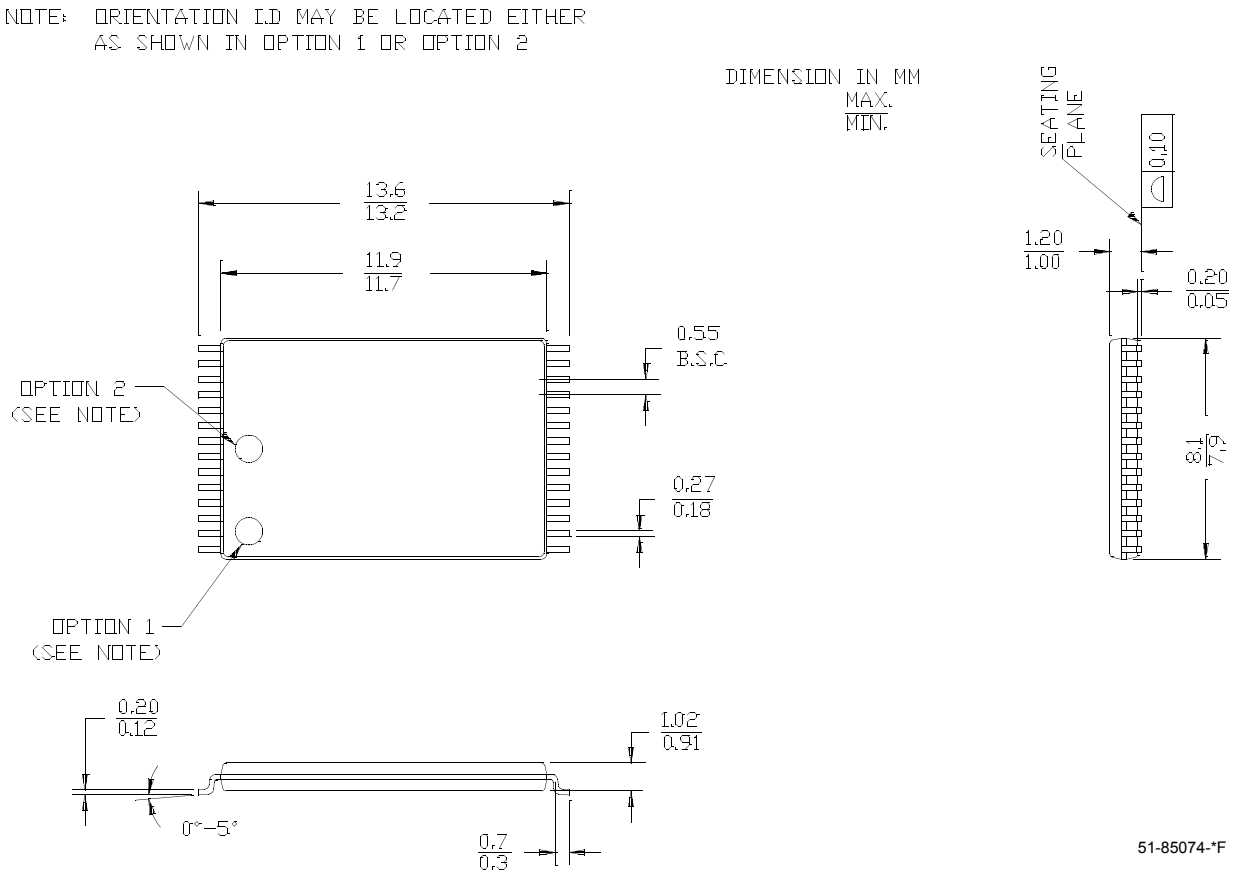


Figure 13. 28-Pin TSOP I (8 x 13.4 mm) (51-85074)



Document History Page

Document Title: CY62256N 256K (32K x 8) Static RAM Document Number: 001- 06511				
REV.	**ECN NO.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	426504	See ECN	NXR	New Data Sheet
*A	488954	See ECN	NXR	Added Automotive product Updated ordering Information table
*B	2715270	06/05/2009	VKN/AESA	Updated POD of 28-Pin (600-Mil) Molded DIP package (Spec# 51-85017)

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

Products

PSoC	psoc.cypress.com
Clocks & Buffers	clocks.cypress.com
Wireless	wireless.cypress.com
Memories	memory.cypress.com
Image Sensors	image.cypress.com