

SN54ALS323, SN74ALS323
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS
WITH SYNCHRONOUS CLEAR AND 3-STATE OUTPUTS

SDAS267A – DECEMBER 1982 – REVISED DECEMBER 1994

- Multiplexed I/O Ports Provide Improved Bit Density
- Four Modes of Operation:
 - Hold (Store)
 - Shift Right
 - Shift Left
 - Load Data
- Operate With Outputs Enabled or at High Impedance
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for n-Bit Word Lengths
- Synchronous Clear
- Applications:
 - Stacked or Push-Down Registers
 - Buffer Storage
 - Accumulator Registers
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

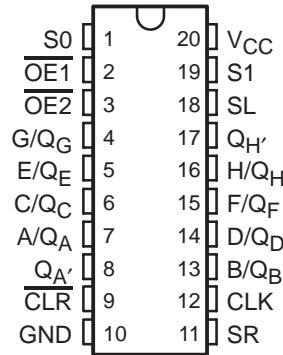
description

These 8-bit universal shift/storage registers feature multiplexed input/output (I/O) ports to achieve full 8-bit data handling in a 20-pin package. Two function-select (S0, S1) inputs and two output-enable (\overline{OE}_1 , \overline{OE}_2) inputs can be used to choose the modes of operation listed in the function table.

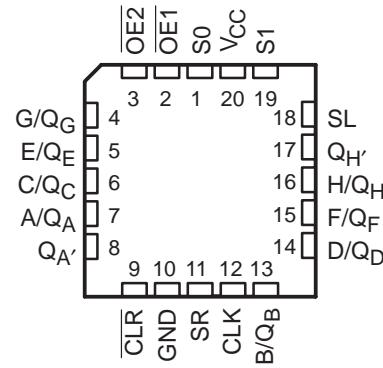
Synchronous parallel loading is accomplished by taking both S0 and S1 high. This places the 3-state outputs in the high-impedance state and permits data applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs synchronously when the clear (CLR) input is low. Taking either \overline{OE}_1 or \overline{OE}_2 high disables the outputs but has no effect on clearing, shifting, or storing data.

The SN54ALS323 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS323 is characterized for operation from 0°C to 70°C .

SN54ALS323 . . . J PACKAGE
SN74ALS323 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS323 . . . FK PACKAGE
(TOP VIEW)



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1994, Texas Instruments Incorporated



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

SN54ALS323, SN74ALS323
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS
WITH SYNCHRONOUS CLEAR AND 3-STATE OUTPUTS

SDAS267A - DECEMBER 1982 - REVISED DECEMBER 1994

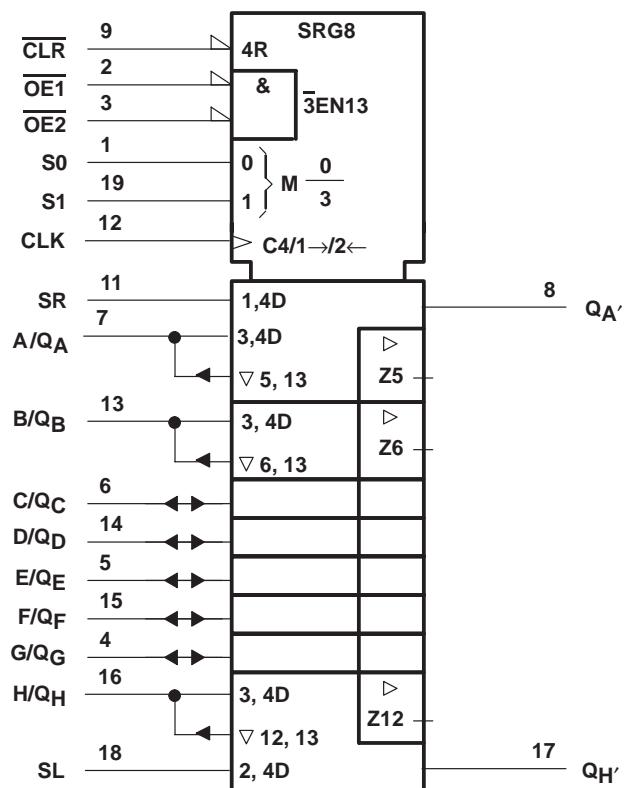
FUNCTION TABLE

MODE	INPUTS							I/O PORTS								OUTPUTS		
	CLR	S1	S0	OE1†	OE2†	CLK	SL	SR	A/Q _A	B/Q _B	C/Q _C	D/Q _D	E/Q _E	F/Q _F	G/Q _G	H/Q _H	Q _{A'}	Q _{H'}
Clear	L	X	L	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	↑	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0
	H	X	X	L	L	L	X	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0
Shift Right	H	L	H	L	L	↑	X	H	H	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	H	Q _{Gn}
	H	L	H	L	L	↑	X	L	L	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	L	Q _{Gn}
Shift Left	H	H	L	L	L	↑	H	X	QBn	QCn	QDn	QEn	QFn	QGn	QHn	H	QBn	H
	H	H	L	L	L	↑	L	X	QBn	QCn	QDn	QEn	QFn	QGn	QHn	L	QBn	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

NOTE: a . . . h = the level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputs are isolated from the I/O terminals.

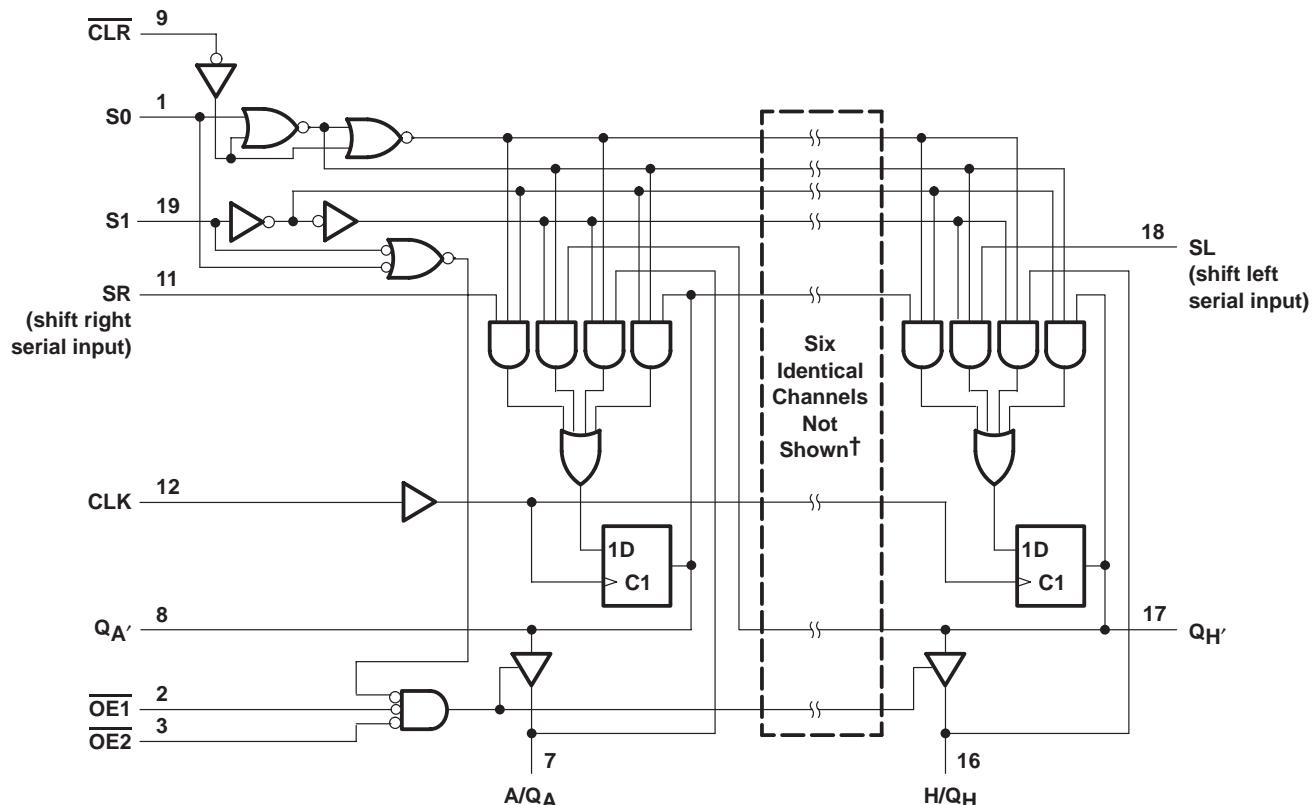
† When one or both output-enable inputs are high, the eight I/O terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



† I/O ports not shown: B/Q_B (13), C/Q_C (6), D/Q_D (14), E/Q_E (5), F/Q_F (15), and G/Q_G (4).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V _{CC}	7 V
Input voltage, V _I : All inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range, T _A : SN54ALS323	-55°C to 125°C
SN74ALS323	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN54ALS323, SN74ALS323
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS
WITH SYNCHRONOUS CLEAR AND 3-STATE OUTPUTS

SDAS267A - DECEMBER 1982 - REVISED DECEMBER 1994

recommended operating conditions

				SN54ALS323			SN74ALS323			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage			2			2			V
V _{IL}	Low-level input voltage				0.7			0.8		V
I _{OH}	High-level output current	Q _{A'} or Q _{H'}			-0.4			-0.4		mA
		Q _A thru Q _H			-1			-2.6		
I _{OL}	Low-level output current	Q _{A'} or Q _{H'}			4			8		mA
		Q _A thru Q _H			12			24		
T _A	Operating free-air temperature			-55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS323			SN74ALS323			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}		V _{CC} = 4.5 V,	I _I = -18 mA			-1.5			-1.5	V
V _{OH}	Any output	V _{CC} = 4.5 V to 5.5 V,	I _{OH} = -0.4 mA	V _{CC} - 2			V _{CC} - 2			V
	Q _A thru Q _H	V _{CC} = 4.5 V	I _{OH} = -1 mA	2.4	3.3					
			I _{OH} = -2.6 mA				2.4	3.2		
V _{OL}	Q _{A'} or Q _{H'}	V _{CC} = 4.5 V	I _{OL} = 4 mA	0.25	0.4	0.25	0.4			V
	I _{OL} = 8 mA					0.35	0.5			
	Q _A thru Q _H	V _{CC} = 4.5 V	I _{OL} = 12 mA	0.25	0.4	0.25	0.4			
			I _{OL} = 24 mA				0.35	0.5		
I _I	A thru H	V _{CC} = 5.5 V	V _I = 5.5 V		0.1		0.1			mA
	Any others		V _I = 7 V		0.1		0.1			
I _{IH} ‡		V _{CC} = 5.5 V,	V _I = 2.7 V		20		20			µA
I _{IL} ‡	S0, S1, SR, SL	V _{CC} = 5.5 V,	V _I = 0.4 V		-0.2		-0.2			mA
	Any others				-0.1		-0.1			
I _{OS} §	Q _{A'} or Q _{H'}	V _{CC} = 5.5 V,	V _O = 2.25 V	-15	-70	-15	-70			mA
	Q _A thru Q _H			-20	-112	-30	-112			
I _{CC}		V _{CC} = 5.5 V	Outputs high	15	28	15	28			mA
			Outputs low	22	38	22	38			
			Outputs disabled	23	40	23	40			

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ For I/O ports (Q_A thru Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.



SN54ALS323, SN74ALS323
**8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS
 WITH SYNCHRONOUS CLEAR AND 3-STATE OUTPUTS**

SDAS267A - DECEMBER 1982 - REVISED DECEMBER 1994

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				SN54ALS323	SN74ALS323	UNIT
		MIN	MAX	MIN	MAX	
f_{clock}		Clock frequency (at 50% duty cycle)		0	17	MHz
t_w		Pulse duration		22	16.5	ns
t_{su}	Setup time before CLK^\uparrow	S0 or S1		25	20	ns
		Serial or parallel data	High	18	16	
			Low	15	6	
		CLR active		25	20	
t_h		Inactive-state setup time before $CLK^{\uparrow\ddagger}$		CLR	18	16
t_h	Hold time after CLK^\uparrow	S0 or S1		0	0	ns
		Serial or parallel data		0	0	

[†] Inactive-state setup time is also referred to as recovery time.

switching characteristics (see Figure 1)

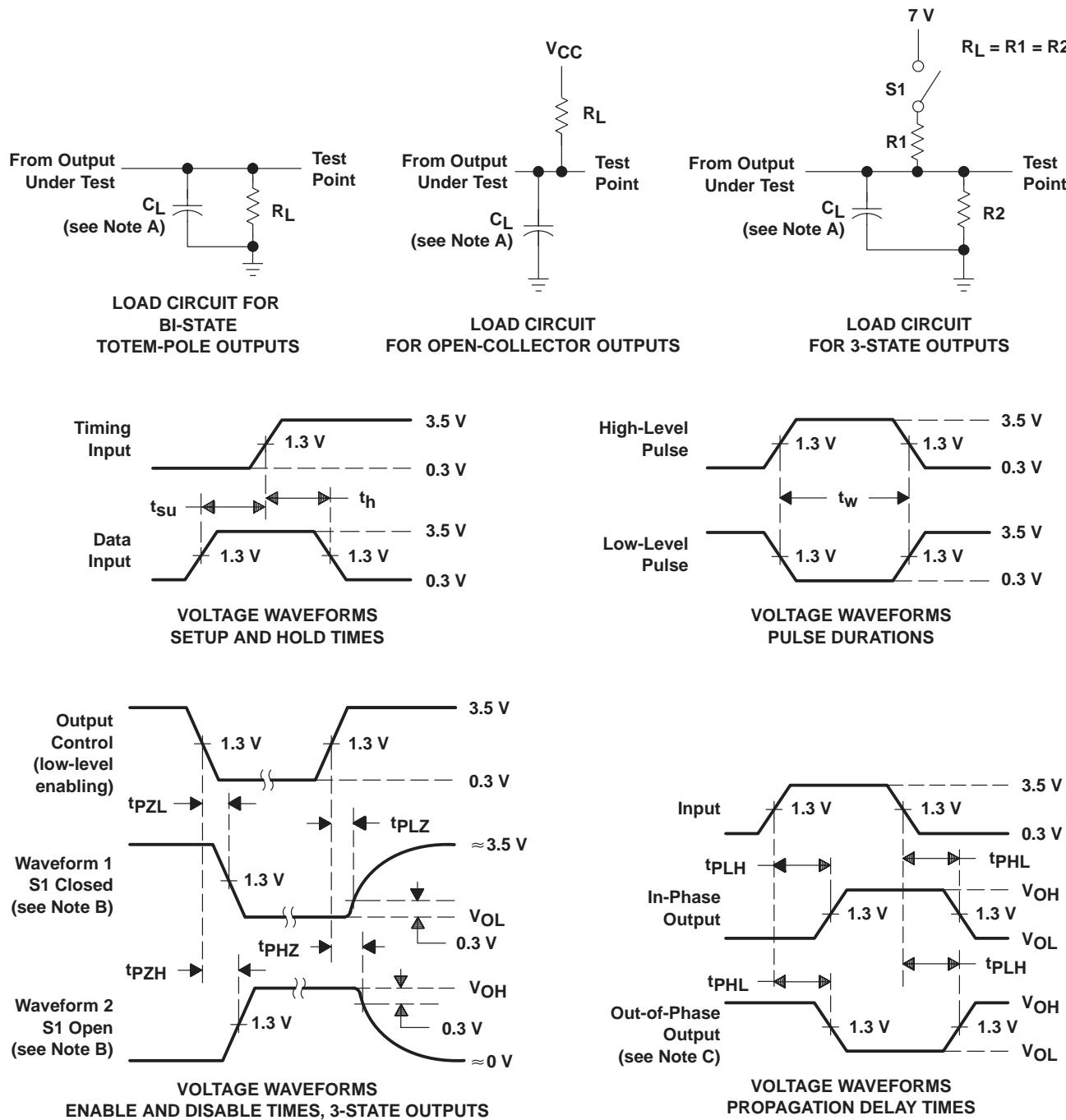
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R1 = 500 \Omega$, $R2 = 500 \Omega$, $T_A = \text{MIN to MAX}^{\ddagger}$		UNIT
			SN54ALS323	SN74ALS323	
			MIN	MAX	
f_{max}			17	17	MHz
t_{PLH}	CLK	Q _A thru Q _H	2	19	ns
			4	25	
t_{PHL}	CLK	Q _{A'} or Q _{H'}	2	21	ns
			4	25	
t_{PZH}	$\overline{OE1}, \overline{OE2}$	Q _A thru Q _H	5	22	ns
			6	27	
t_{PZL}	$\overline{OE1}, \overline{OE2}$	Q _A thru Q _H	5	27	ns
			6	27	
t_{PLZ}	S ₀ , S ₁	Q _A thru Q _H	1	15	ns
			4	38	
t_{PHZ}	$\overline{OE1}, \overline{OE2}$	Q _A thru Q _H	1	16	ns
			4	34	
t_{PLZ}	S ₀ , S ₁	Q _A thru Q _H	1	12	ns
			4	25	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**SN54ALS323, SN74ALS323
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS
WITH SYNCHRONOUS CLEAR AND 3-STATE OUTPUTS**

SDAS267A - DECEMBER 1982 - REVISED DECEMBER 1994

**PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1 \text{ MHz}$, $t_r = t_f = 2 \text{ ns}$, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
83021022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	83021022A SNJ54ALS 323FK	Samples
8302102RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8302102RA SNJ54ALS323J	Samples
8302102SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	8302102SA SNJ54ALS323W	Samples
SN74ALS323N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS323N	Samples
SN74ALS323N3	OBsolete	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74ALS323NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS323N	Samples
SNJ54ALS323FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	83021022A SNJ54ALS 323FK	Samples
SNJ54ALS323J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8302102RA SNJ54ALS323J	Samples
SNJ54ALS323W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	8302102SA SNJ54ALS323W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ALS323, SN74ALS323 :

- Catalog: [SN74ALS323](#)
- Military: [SN54ALS323](#)

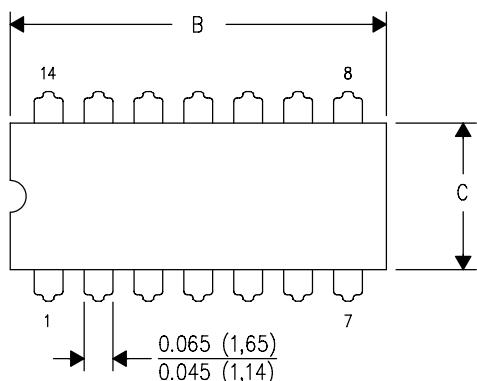
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

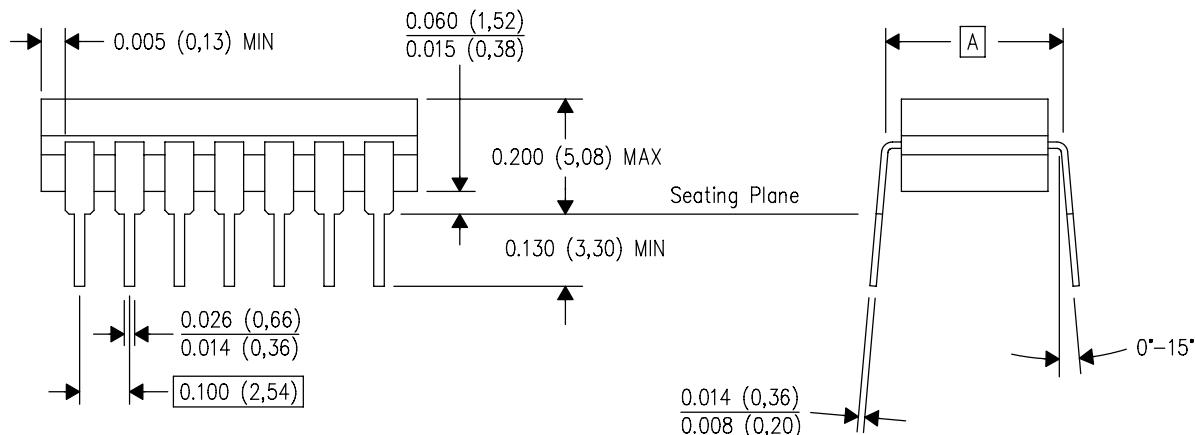
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

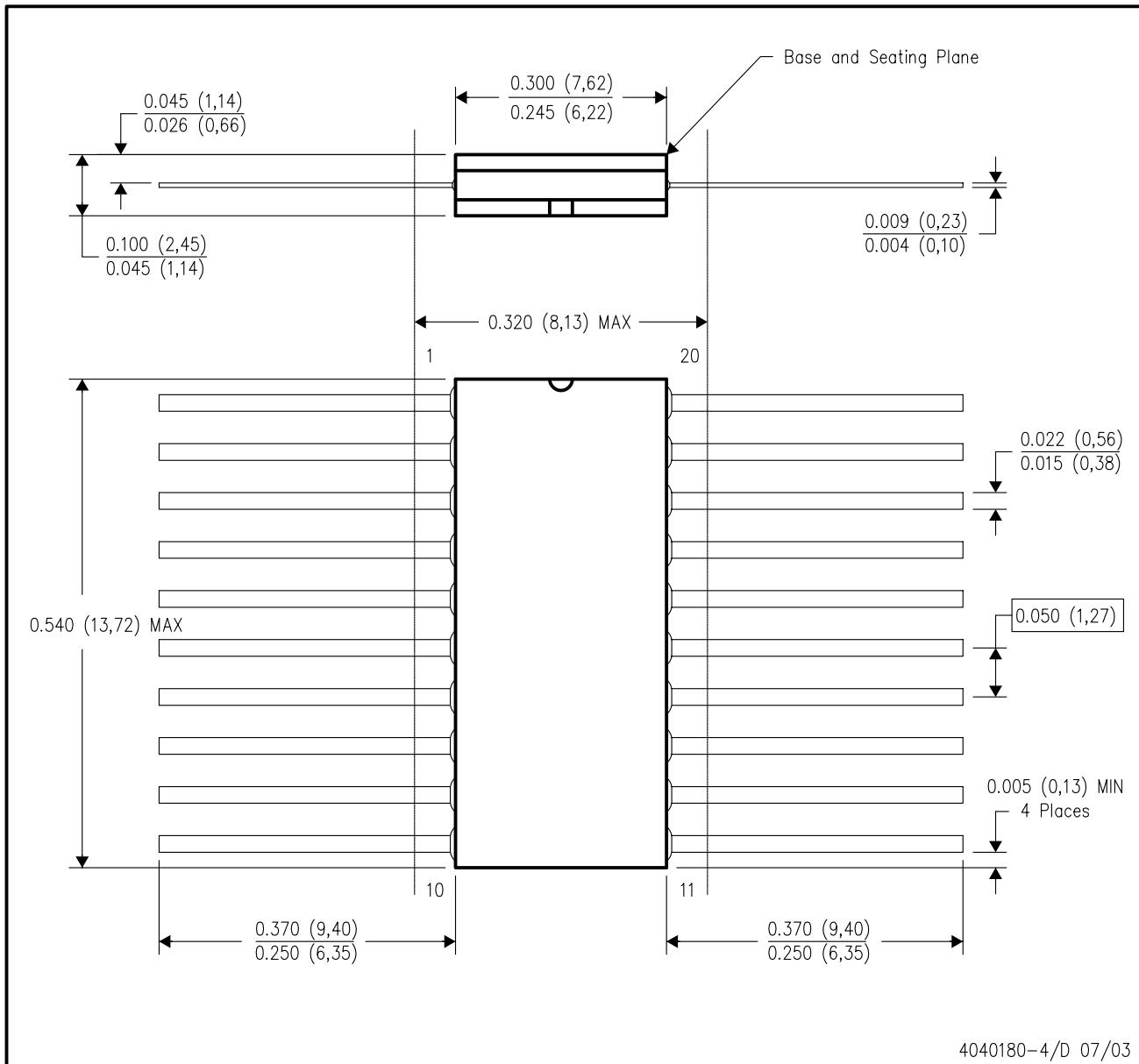


4040083/F 03/03

- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK

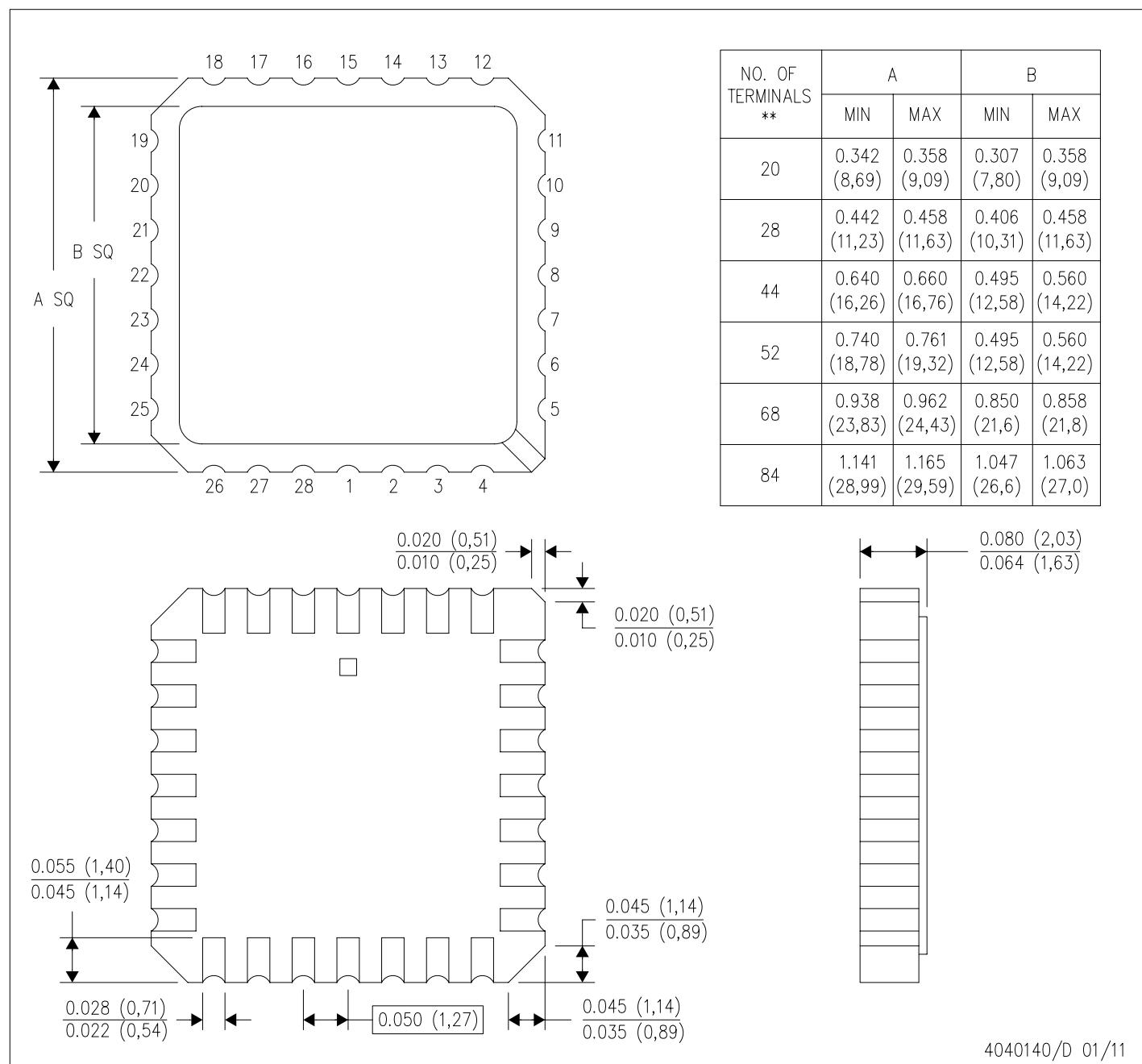


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



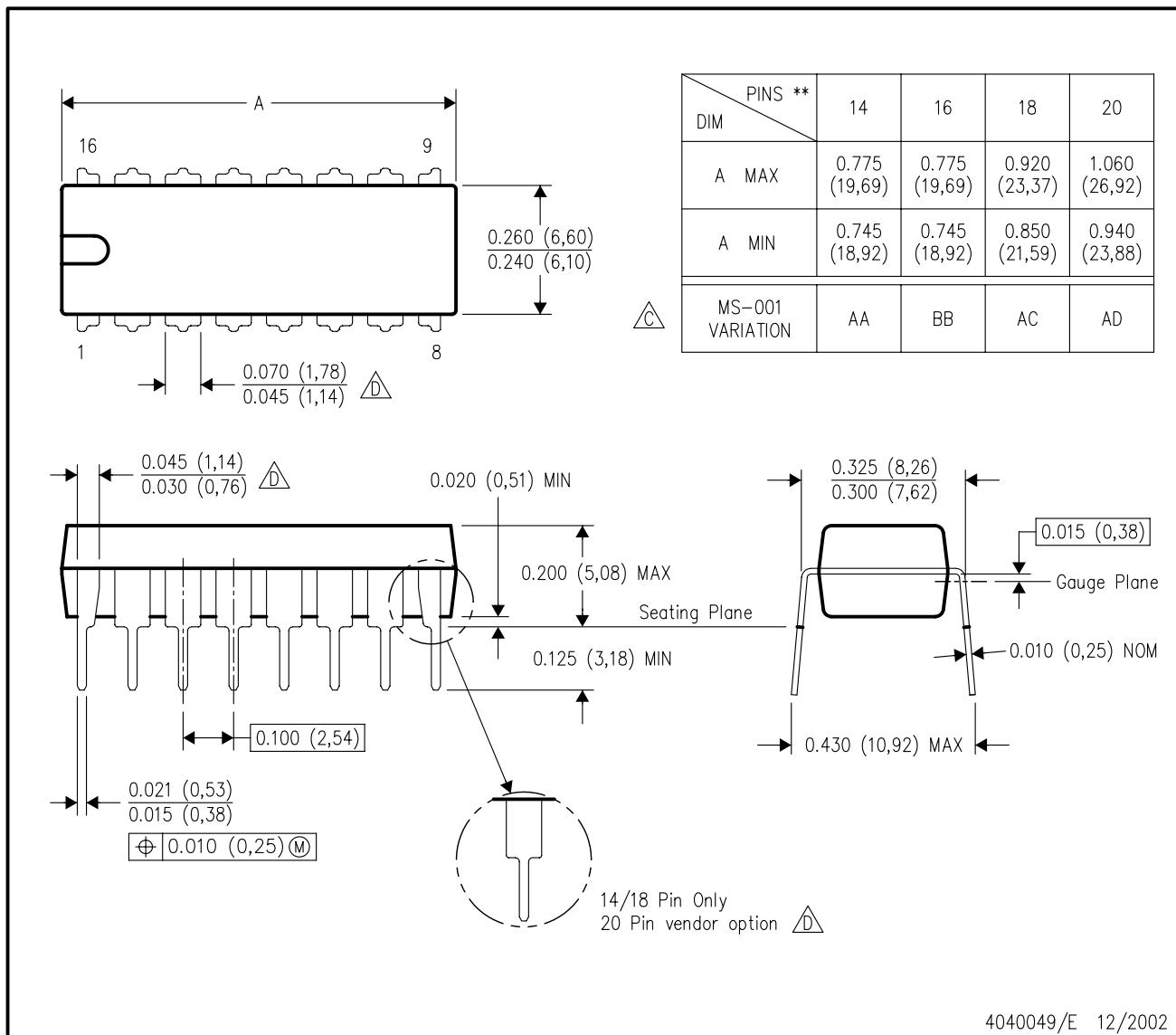
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a metal lid.
 D. Falls within JEDEC MS-004

4040140/D 01/11

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products	Applications
Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity
	TI E2E Community
	e2e.ti.com