

# CYIS1SM0250-AA STAR250 250K Pixel Radiation Hard CMOS Image Sensor

## Overview

The STAR250 sensor is a CMOS Active Pixel Sensor, designed for application in Optical Inter-Satellite Link beam trackers. The STAR250 is part of broader range of applications including space-borne systems such as sun sensing and star tracking. It features 512 by 512 pixels on a 25  $\mu\text{m}$  pitch, on chip Fixed Pattern Noise (FPN) correction, a programmable gain amplifier, and a 10-bit ADC. Flexible operating (multiple windowing, subsampling) is possible by direct addressable X and Y registers.

The sensor has an outstanding radiation tolerance that is observed using proprietary technology modifications and design techniques. Two versions of the sensors are available, STAR250 and STAR250BK7. STAR250 has a quartz glass lid and air in the cavity. The STAR250BK7 has a BK7G18 glass lid with anti reflective coating. The cavity is filled with  $\text{N}_2$  increasing the temperature operating range.

## Features

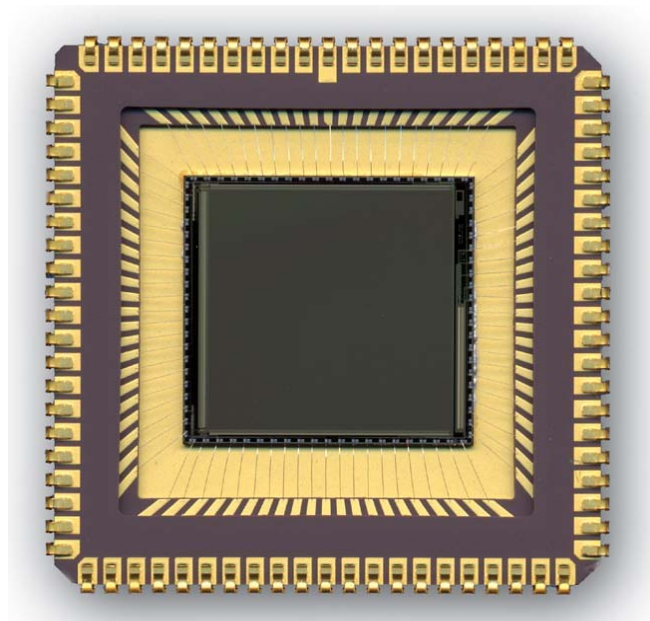
Parameter	Typical Value
Optical Format	1 Inch
Active Pixels	512 x 512
Pixel Size	25 $\mu\text{m}$
Shutter Type	Electronic
Maximum Data Rate/ Master Clock	8 MHz
Frame Rate	Up to 30 full frames/s
ADC Resolution	10 bit
Sensitivity	3340 $\text{V.m}^2/\text{W.s}$
Dynamic Range	74dB (5000:1)
kTC Noise	76 $\text{e}^-$
Dark Current	4750 $\text{e}^-/\text{s}$ at RT
Supply Voltage	5V
Operating Temperature	0°C - +65°C (STAR250) -40°C - +85°C (STAR250BK7)

## Features (continued)

Parameter	Typical Value
Gamma Total Dose Radiation tolerance	Increase in average dark current < 1 $\text{nA/cm}^2$ after 3 MRad Image operation with dark signal < 1V/s after 10 Mrad demon- strated (Co60)
Proton Radiation Tolerance	1% of pixels has an increase in dark current > 1 $\text{nA/cm}^2$ after $3 \times 10^{10}$ protons at 11.7 MeV
SEL Threshold	> 80 MeV $\text{cm}^3 \text{mg}^{-1}$
Color Filter Array	Mono
Packaging	84 pin JLCC
Power Consumption	< 350 mW

## Applications

- Satellites
- Spacecraft Monitoring
- Nuclear Inspection



Marketing Part Number	Description	Package
CYIS1SM0250AA-HHC	Mono with BK7G18 Glass	84-pin JLCC
CYIS1SM0250AA-HHCS	Mono with BK7G18 Glass, Space Qualified	
CYIS1SM0250AA-HQC	Mono with Quartz fused silica Glass	
CYIS1SM0250AA-HWC	Mono without Glass	
CYIS1SM0250-EVAL	Mono demo kit	Demo kit

## Specifications

**Table 1. General Specifications**

Parameter	Specification	Remarks
Pixel Architecture	3-transistor active pixel 4 diodes per pixel	Radiation-tolerant pixel design 4 photodiodes for improved MTF
Pixel Size	25 x 25 $\mu\text{m}^2$	
Resolution	512 by 512 pixels	
Pixel Rate	8 Mps	
Shutter Type	Electronic	Integration time is variable in time, steps equal to the row readout time
Frame Rate	29 full frames/second	
Extended dynamic range	Double slope	
Programmable gain	Programmable between x1, x2, x4, x8	Selectable through pins G0 and G1
Supply voltage VDD	5V	
Operational temperature range	0°C - +65°C	STAR250 (Quartz glass lid, air in cavity)
	-40°C - +85°C	STAR250BK7 (BK7G18 glass lid, N <sub>2</sub> in cavity)
Package	84 pins JLCC	

**Table 2. Electro-optical Specifications**

Parameter	Specification (Typical)	Comment
Detector Technology	CMOS Active Pixel Sensor	
Pixel Structure	3-transistor active pixel 4 diodes per pixel	Radiation-tolerant pixel design 4 Photodiodes for improved MTF
Photodiode	High fill factor photodiode	
Sensitive Area Format	512 by 512 pixels	
Pixel Size	25 x 25 $\mu\text{m}^2$	
Spectral Range	200 - 1000 nm	See <a href="#">Figure 1</a> and <a href="#">Figure 2</a>
Quantum Efficiency x Fill Factor	Max. 35%	Above 20% between 450 and 750 nm (Note: Metal FillFactor (MFF) is 63%)
Full Well Capacity	311K electrons	When output amplifier gain = 1
Linear Range within + 1%	128K electrons	When output amplifier gain = 1
Output Signal Swing	1.68 V	When output amplifier gain = 1
Conversion Gain	5.7 $\mu\text{V}/\text{e}^-$	When output amplifier gain = 1 near dark
Temporal Noise	76 $\text{e}^-$	Dominated by kTC
Dynamic Range	74 dB (5000:1)	At the analog output
FPN (Fixed Pattern Noise)	1 < 0.1% of full well (typical)	Measured local, on central image area 50% of pixels, in the dark
PRNU (Photo Response Non-uniformity)	Local: 1 = 0.39% of response Global: 1 = 1.3% of response	Measured in central image area 50% of pixels, at Qsat/2
Average Dark Current Signal	4750 $\text{e}^-/\text{s}$	At RT
DSNU (Dark Signal Non Uniformity)	3805 $\text{e}^-/\text{s}$ RMS	At RT, scale linearly with integration time
MTF	Horizontal: 0.36 Vertical: 0.39	at 600 nm.
Optical Cross Talk	5% (TBC) to nearest neighbor if central pixel is homogeneously illuminated	

**Table 2. Electro-optical Specifications** (continued)

Parameter	Specification (Typical)	Comment
Anti-blooming Capacity	x 1000 to x 100 000	
Output Amplifier Gain	1, 2, 4 or 8	Controlled by two bits
Windowing	X and Y 9-bit programmable shift registers	Indicate upper left pixel of each window
Electronic Shutter Range	1: 512	Integration time is variable in time steps equal to the row readout time
ADC	10 bit	
ADC Linearity	$\pm 3.5$ counts	INL
Missing Codes	none	
ADC Setup Time	310 ns	To reach 99% of final value
ADC Delay Time	125 ns	
Power Dissipation	< 350 mW	Average at 8 MHz pixel rate

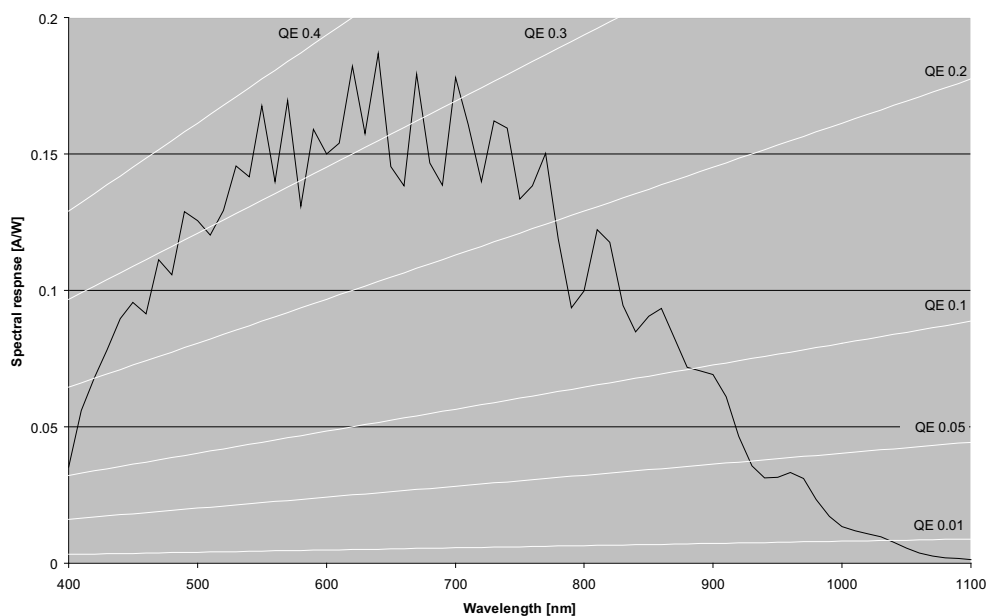
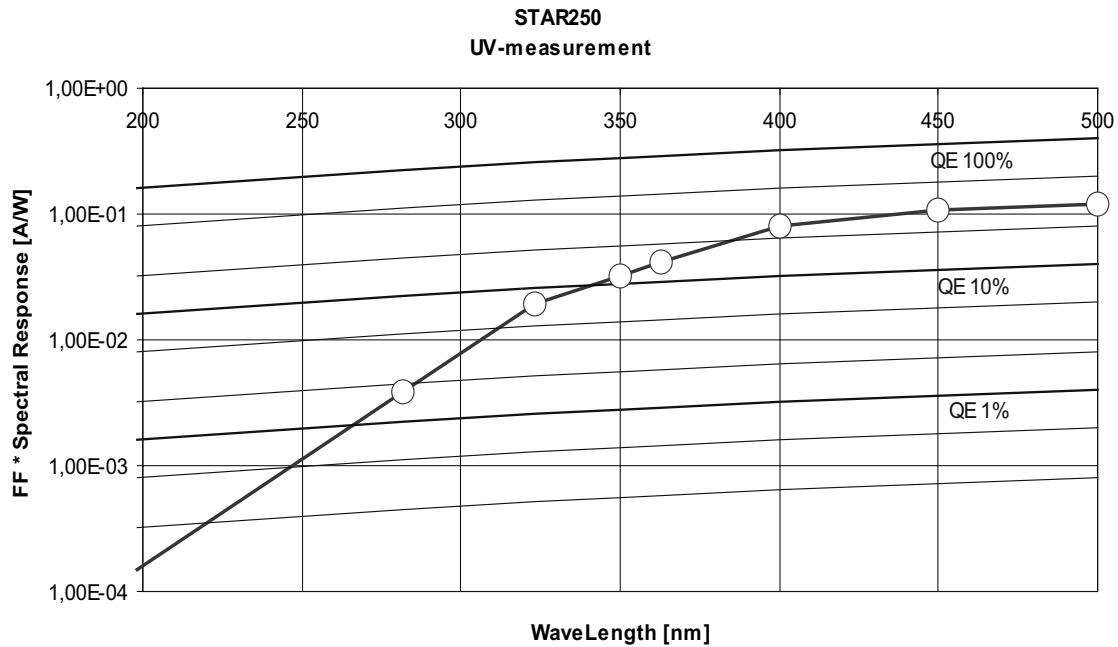
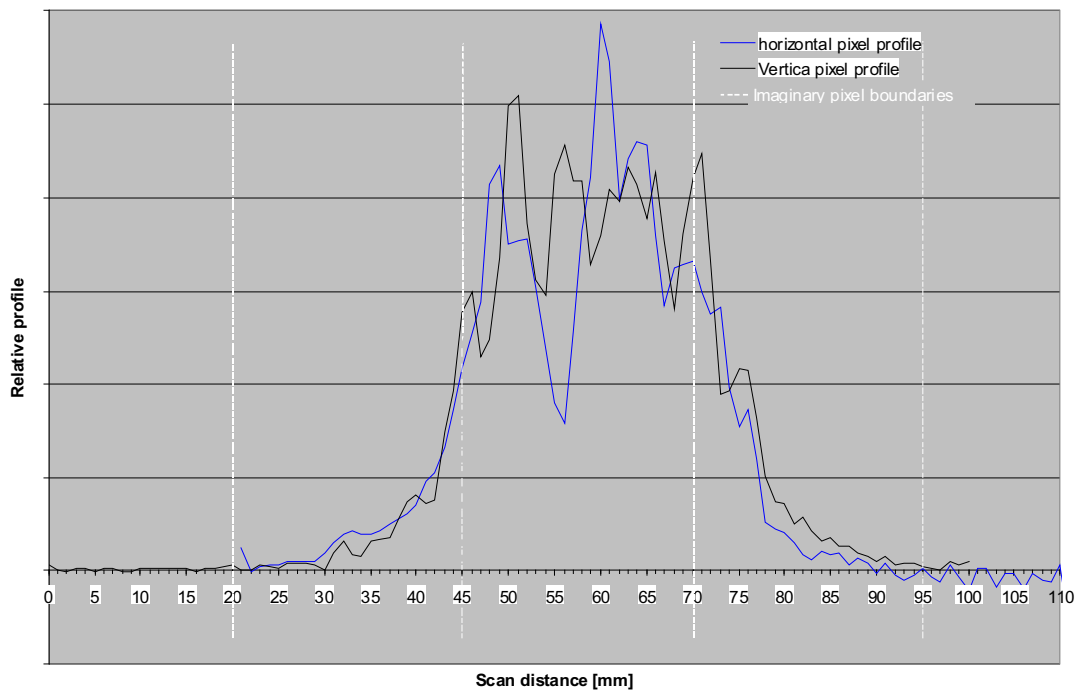
*Spectral Response Curve*
**Figure 1. Spectral Response Curve**


Figure 2. UV Region Spectral Response Curve



#### Pixel Profile

Figure 3. Pixel Profile



The pixel profile is measured using the 'knife edge' method: the image of a target containing a black to white transition is scanned over a certain pixel with subpixel resolution steps. The image

sensors settings and the illumination conditions are adjusted such that the transition covers 50% of the output range. The scan is performed both horizontal and vertical.

## Electrical Specifications

### Absolute Maximum Ratings

Absolute Ratings are those values beyond that damage to the device may occur.

**Table 3. Absolute Maximum Ratings STAR250**

Characteristics	Limits		Units	Remarks
	Min	Max		
Any Supply Voltage	-0.5	+7	V	
Voltage on any Input Terminal	-0.5	Vdd + 0.5	V	
Operating Temperature	0	+60	°C	
Storage Temperature	-10	+60	°C	
Sensor soldering Temperature	NA	125	°C	Hand soldering only. The sensor's temperature during soldering should not exceed this limit.

**Table 4. Absolute Maximum Ratings STAR250BK7**

Characteristics	Limits		Units	Remarks
	Min	Max		
Any Supply Voltage	-0.5	+7	V	
Voltage on any Input Terminal	-0.5	Vdd + 0.5	V	
Operating Temperature	-40	+85	°C	
Storage Temperature	-40	+85	°C	
	-40	+120	°C	Maximum 1 hour
Sensor Soldering Temperature	NA	125	°C	Hand soldering only. The sensor's temperature during soldering should not exceed this limit.

**Table 5. Radiation Tolerance**

Parameter	Criterion	Qualification level
Gamma Total Dose Radiation tolerance	Increase in average dark current < 1 nA/cm <sup>2</sup> after 3 MRad	See <a href="#">Figure 4</a>
	Image operation with dark signal < 1V/s	10 Mrad demonstrated (Co60)
	Single (test) pixel operation with dark signal < 1V/s	24 Mrad demonstrated (Co60)
Proton Radiation Tolerance	1% of pixels has an increase in dark current > 1 nA/cm <sup>2</sup> after 3*10 <sup>10</sup> protons at 11.7 MeV	See <a href="#">Figure 4</a>
SEL Threshold	> 80 MeV cm <sup>3</sup> mg <sup>-1</sup>	To be confirmed

Figure 4 shows the increase in dark current under total dose irradiation. This curve is measured when the radiation is at high dose rate. Annealing results in a significant dark current decrease.

Figure 4. Dark Current Increase

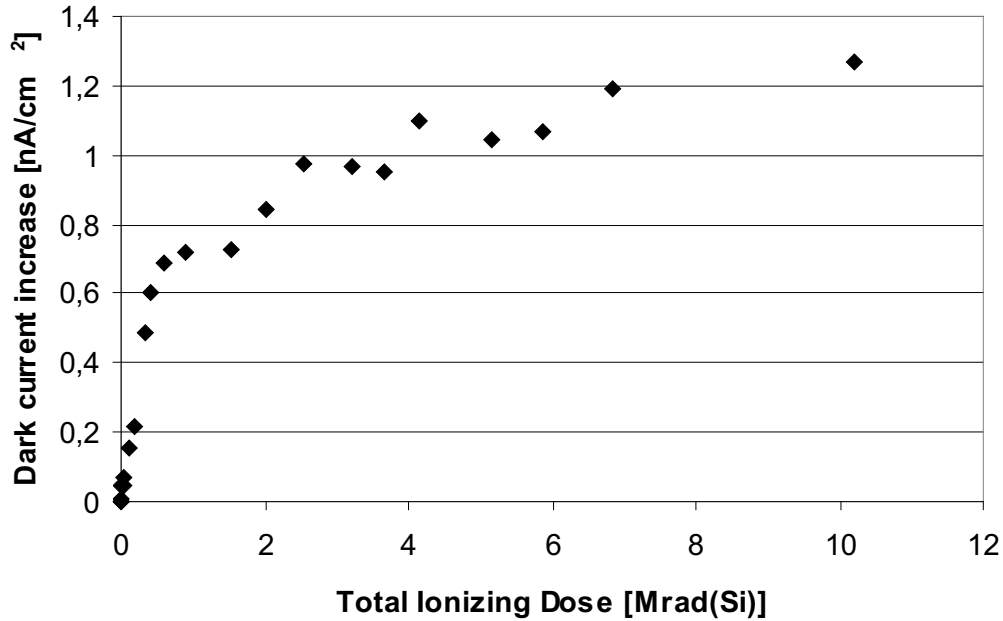
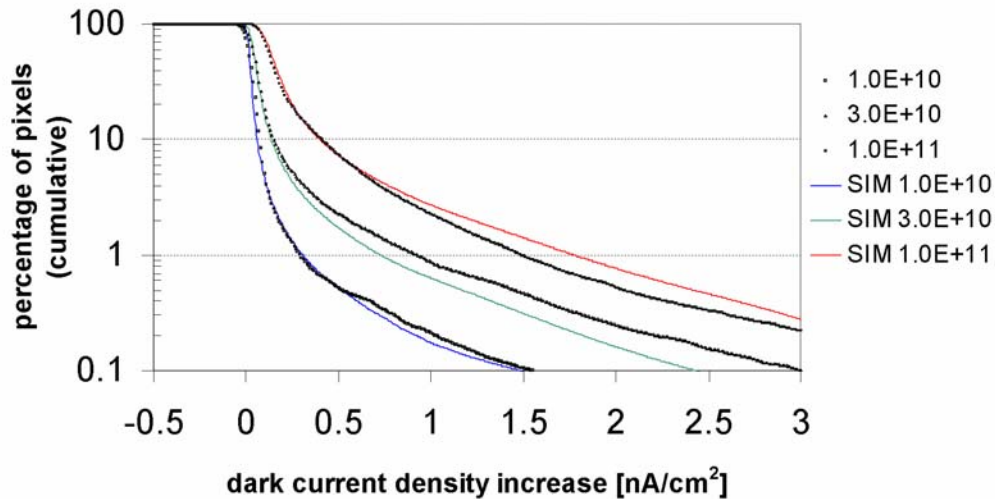


Figure 5 shows the percentage of pixels with a dark current increase under 11.7 MeV radiation with protons.

Figure 5. Percentage of Pixels with Dark Current Increase



# DC Operating Conditions

**Table 6. DC operating conditions**

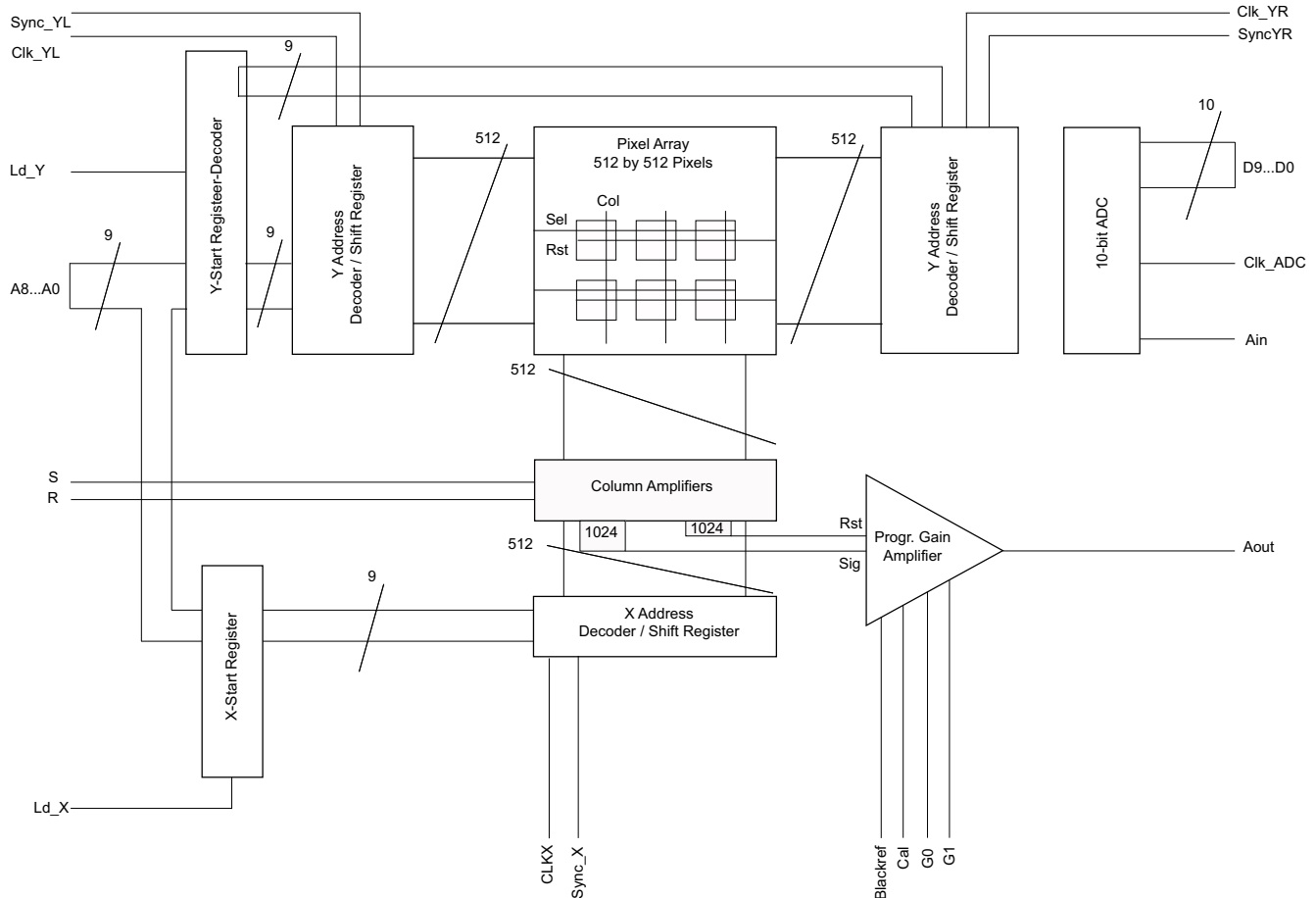
Symbol	Parameter <sup>[1,2,3]</sup>	Min	Typ	Max	Units
VDD_ANA	Analog supply voltage to imager part		5		V
VDD_DIG	Digital supply voltage to imager part		5		V
VDD_ADC_ANA	Analog supply voltage to ADC		5		V
VDD_ADC_DIG	Digital supply voltage to ADC		5		V
VDD_ADC_DIG_3.3/5	Supply voltage of ADC output stage		3.3 to 5		V
VIH	Logical '1' input voltage	2.3		Vdd	V
VIL	Logical '0' input voltage	0		1	V
VOH	Logical '1' output voltage	4.25	4.5		V
VOL	Logical '0' output voltage		0.1	1	V
VDD_PIX	Pixel array power supply (default 5V, the device is then in "soft reset". In order to avoid the image lag associated with soft reset, reduce this voltage to 3...3.5V "hard reset")		5		V
VDD_RESL	Reset power supply		5		V

## Notes

1. All parameters are characterized for DC conditions after establishing thermal equilibrium.
2. Unused inputs must always be tied to an appropriate logic level, for example, either VDD or GND.
3. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. Take normal precautions to avoid applying any voltages higher than the maximum rated voltages to this high impedance circuit.

## Sensor Architecture

Figure 6. STAR250 Schematic



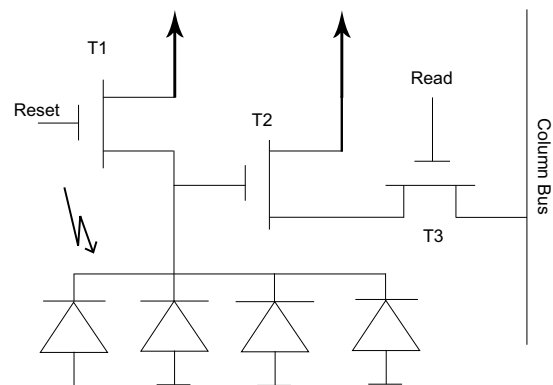
The base line of the STAR250 sensor design consists of an imager with a 512 by 512 array of active pixels at 25  $\mu\text{m}$  pitch. The detector contains on-chip correction for Fixed Pattern Noise (FPN) in the column amplifiers, a programmable gain output amplifier, and a 10-bit Analog-to-Digital Converter (ADC). Through additional preset registers the start position of a window can be programmed to enable fast read out of only part of the detector array.

### Pixel Structure

The image sensor consists of several building blocks as outlined in Figure 6. The central element is a 512 by 512 pixel array with square pixels at 25  $\mu\text{m}$  pitch. Unlike classical designs, the pixels of this sensor contain four photodiodes. This configuration enhances the MTF and reduces the PRNU. Figure 7 shows an electrical diagram of the pixel structure. The four photodiodes are connected in parallel to the reset transistor (T1). Transistor T2 converts the charge, collected on the photo diode node, to a voltage signal that is connected to the column bus by T3. The

Reset and the Read entrance of the pixel are connected to one of the Y shift registers.

Figure 7. STAR250 Pixel Structure





## Shift Registers

The shift registers are located next to the pixel array and contain as many outputs as the number of rows in the pixel array. They are designed as "1-hot" registers, (YL and YR shift register) each allowing selection of one row of pixels at a time. A clock pulse moves the pointer one position down the register resulting in the selection of every individual row for either reset or for readout. The spatial offset between the two selected rows determines the integration time. A synchronization pulse to the shift registers loads the value from a preset register into the shift register forcing the pointer to a predetermined position. Windowing in the vertical (Y) direction is achieved by presetting the registers to a row that is not the first row and by clocking out only the required number of rows.

## Column Amplifiers

All outputs from the pixels in a column are connected in parallel to a column amplifier. This amplifier samples the output voltage and the reset level of the pixel whose row is selected at that moment and presents these voltage levels to the output amplifier. As a result, the pixels are always reset immediately after readout as part of the sample procedure and the maximum integration time of a pixel is the time between two read cycles.

## Electronic Shutter

In a linescan integrating imager with electronic shutter, there are two continuous processes of image gathering.

The first process resets lines in a progressive scan. At line reset, all the pixels in a line are drained from any photo charges collected since their last reset or readout. After reset, a new exposure cycle starts for that particular line.

The second process is the actual readout, which also happens in an equally fast linewise progressive scan.

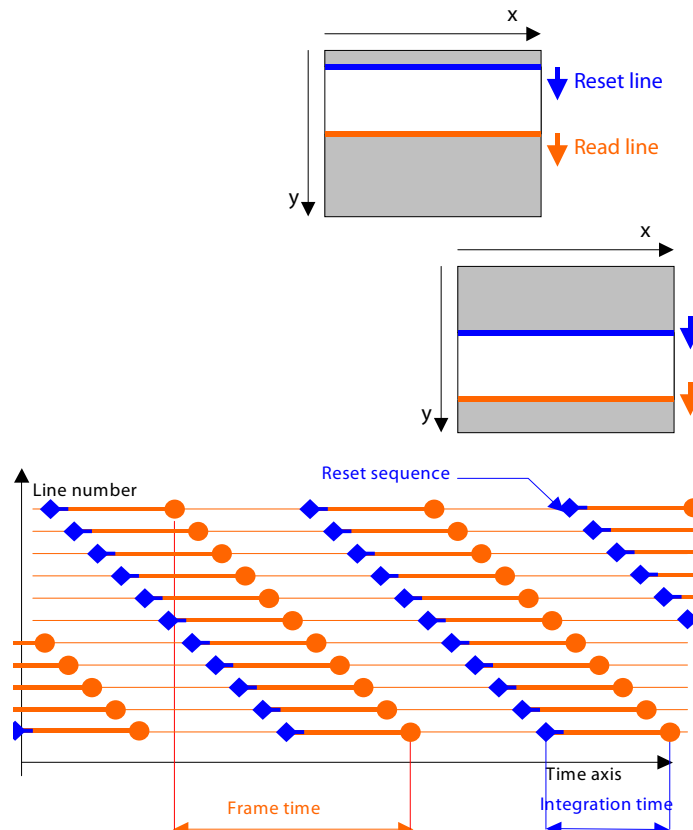
During readout, the photo charges collected since the previous reset are converted into an output voltage. This is then passed on pixel by pixel to the imager's pixel serial output and ADC. Readout is destructive, meaning the accumulation of charges from successive exposure phases is not possible in the present architecture.

The STAR250 has two Y- shift registers; YL and YR. One is used for readout of a line (YL) and the other is used to reset a line (YR). The integration time is equal to the time between the last reset and the readout of that line, see [Figure 8](#) The integration time is thus equal to:

Integration time = (Nr. Lines \* (RBT + pixel period \* Nr. Pixels)) with:

- Nr. Lines: Number of Lines between readout and reset (Y).
- Nr. Pixels: Number of pixels read out each line (X).
- RBT: Row Blanking Time = 3.2  $\mu$ s (typical).
- Pixel period: 1/8 MHz = 125 ns (typical).

Figure 8. Electronic Shutter



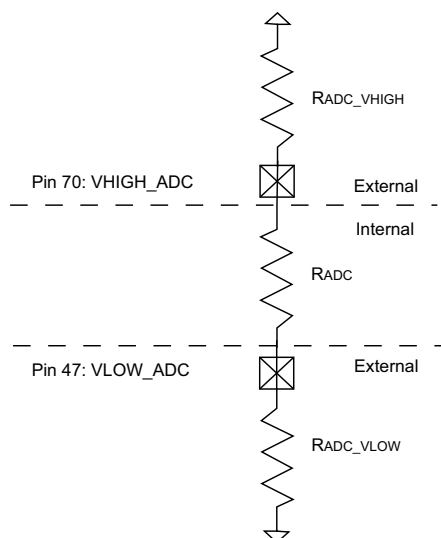
## Programmable Gain Amplifier

The signal from the column amplifiers is fed to an output amplifier with four presettable gains (adjustable with pins G0 and G1). The offset correction of this amplifier is done through a black reference procedure. The signal from the output amplifier is externally available on the analog output terminator of the device.

## Analog-to-Digital Converter

The on-chip 10-bit ADC is electrically separated from the other circuits of the device. The ADC conversion range is set by the voltages on VLOW\_ADC (pin 47) and VHIGHS\_ADC (pin 70). Make voltages on these pins equal to about 2V on VLOW\_ADC and 4V on VHIGHS\_ADC. The voltages are set by connecting VLOW with 1.2 k $\Omega$  to GND and VHIGHS\_ADC with 560 $\Omega$  to VDD. This way, a resistor ladder is created as shown in Figure 9

Figure 9. ADC Resistor Ladder



The internal ADC resistance varies according to temperature. The resistance value increases approximately 4.4 $\Omega$ /°C with increasing temperature. If the ADC range is set externally with resistors, the conversion range may vary with temperature. This effect is cancelled out by not making use of resistors but directly applying voltages on VLOW\_ADC and VHIGHS\_ADC.

## Timing and Readout of the Image Sensor

### Image Readout Procedure

A preamble or initialization phase is irrelevant. The sensor is read out continuously. The first frame is generally saturated and useless because there is no preceding reset of each pixel.

#### Image Readout

In an infinite uninterrupted loop, follow these steps line-by-line:

1. Synchronize the read (YL) and/or reset (YR) registers, in this cases:
  - SYNC\_YL - to re-initiate the readout sequence to row position Y1
  - SYNC\_YR - to re-initiate the reset pointer to row position Y1

For all other lines do not pulse one of these SYNC\_Y signals.

2. Operate the double sampling column amplifiers with two RESETs. Apply one to reset the line that is currently selected to produce the reset reference level for the double sampling column amplifiers. Apply the other reset to another line depending on the required integration time reduction.
3. Perform a Line Readout:

Reset the X read address shift register to the value in its shadow register (X1).

Perform a pixel readout operation, operating the track/hold and the ADC.

Shift the X read address shift register one position further.

Shift the Y read and reset address shift registers one position further. If either of Y read or reset address shift register comes to the end of the pixel array (or the ROI), wrap it around to the start position by pulsing SYNC\_YL.

#### Readout Timing

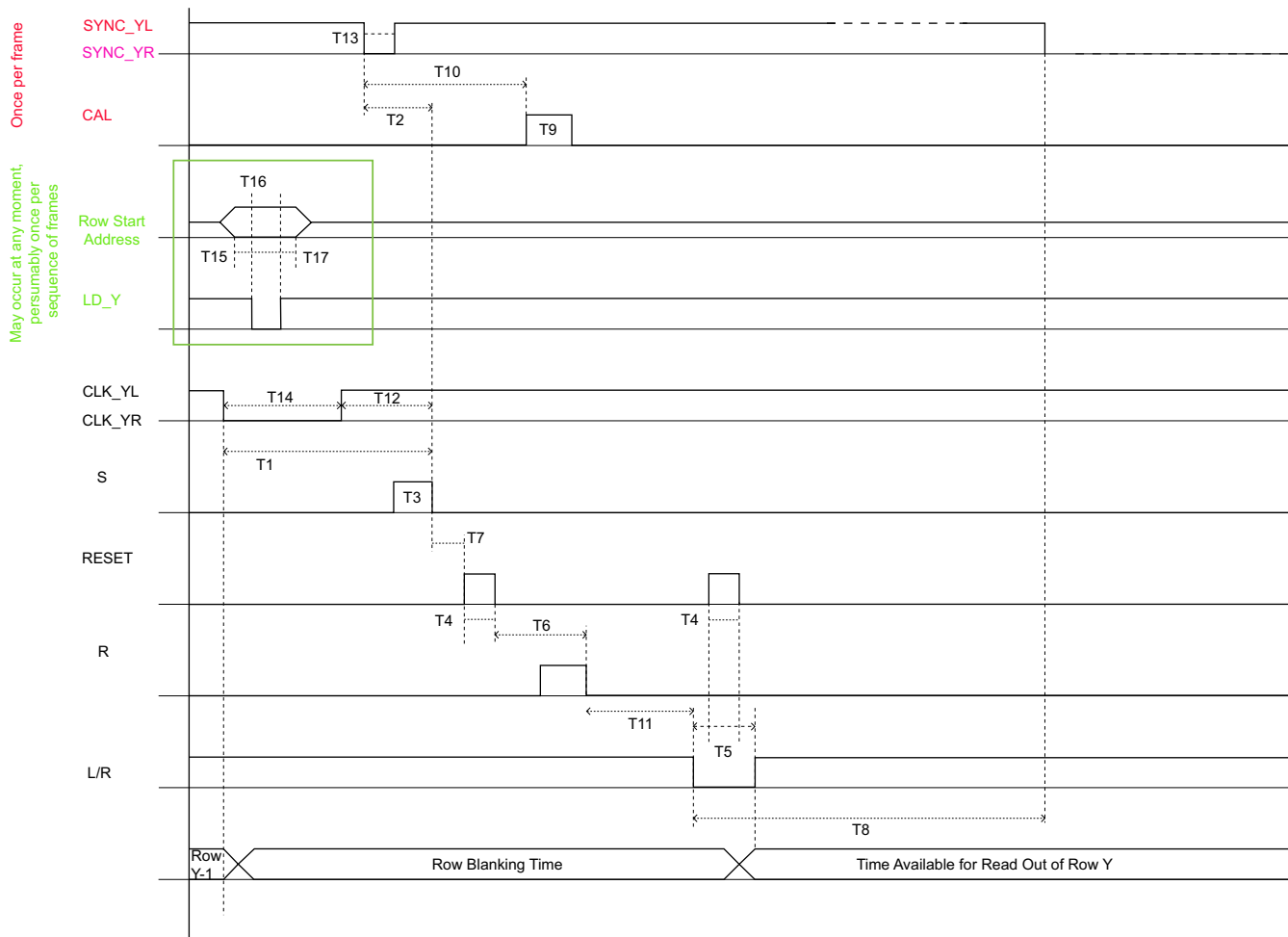
The actual line readout process starts with addressing the line to read. This is done either by initializing the YL pointer with a new value, or by shifting it one position beyond its previous value. (Addressing the line has reset, YR is done in an analogous fashion). During the "blanking time", after the new line is addressed on the sensor, the built-in column-parallel double sampling amplifiers are operated. This renders offset-corrected values of the line under readout.

After the blanking time the pixels of the row addressed by YL are read by multiplexing all the pixels one by one to the serial output chain. The pixel is selected by the X pointer, and that pointer is either initialized with a new value or an increment of the previous position.

The time between row resets and their corresponding row readouts is the effective exposure time (or integration time). This time is proportional to the number of lines (DelayLines) between the line currently under reset and the line currently under readout: DelayLines = (YR - YL+1). This time is also equal to the delay between the SYNC\_YR pulse and the subsequent SYNC\_YL.

The effective integration time tint is calculated as delaylines \* line time. The line time itself is a function of four terms: the time to output the desired number of pixels in the line (Wframe), and the overhead ("blanking") time that is needed to select a new line and perform the double sampling and reset operations.

Figure 10. Basic Readout Timing



SYNC\_YR is not identical to SYNC\_YL. SYNC\_YR is used in electronic shutter operation. The CLK\_YR is driven identical to CLK\_YL, but the SYNC\_YR pulse leads the SYNC\_YL pulse by a certain number of rows. This lead time is the effective integration (electronic shutter ~) time. Relative to the row timing, both SYNC pulses are given at the same time position, once for each frame, but during different rows.

SYNC\_YL is pulsed when the first row is read out and SYNC\_YR is pulsed for the electronic shutter to start for this first row. CAL is pulsed on the first row too, 2  $\mu$ s later than SYNC\_YL.

The minimal idle time is 1.4  $\mu$ s (before starting reading pixels). However, do not read out pixels during the complete row initialization process (in between the rising edge on S and the falling edge on L/R). In this case, the total idle time is minimal. This timing assumes that the Y start register was loaded in advance, which can occur at any time but before the pulse on SYNC\_YL or SYNC\_YR.

**Table 7. Readout Timing Specifications**

Symbol	Min	Typ	Description
T1	1.8 $\mu$ s		Delay between selection of new row by falling edge on CLK_YL and falling edge on S. Minimal value. Normally, CLK_YR is low already at the end of the previous sequence.
T2	1.8 $\mu$ s		Delay between selection of new a row by SYNC_YL and falling edge on S.
T3	0.4 $\mu$ s		Duration of S and R pulse.
T4	0.1 $\mu$ s		Duration of RESET pulse.
T5	T4 + 40 ns	0.3 $\mu$ s	L/R pulse must overlap second RESET pulse at both sides.
T6	0.8 $\mu$ s		Delay between falling edge on RESET and falling edge on R.
T7	20 ns	0.1 $\mu$ s	Delay between falling edge on S and rising edge on RESET.
T8	0	1 $\mu$ s	Delay between falling edge on L/R and falling edge on CLK_Y.
T9	100 ns	1 $\mu$ s	Duration of cal pulse. The CAL pulse is given once each frame.
T10	0	2 $\mu$ s	Delay between falling edge of SYNC_YL and rising edge of CAL pulse.
T11	40 ns	0.1 $\mu$ s	Delay between falling edge on R and rising edge on L/R.
T12	0.1 $\mu$ s	1 $\mu$ s	Delay between rising edge of CLK_Y and falling edge on S.
T13		0.5 $\mu$ s	Pulse width SYNC_YL/YR.
T14		0.5 $\mu$ s	Pulse width CLK_YL/YR.
T15	10 ns		Address setup time.
T16	20 ns		Load X/Y start register value.
T17	10 ns		Address stable after load.
T18	10 ns		
T19	20 ns		SYNC_X pulse width. SYNC_X while CLK_X is high.
T20	10 ns		
T21		40 ns	Analog output is stable during CLK_X low.
T22		40 ns	CLK_X pulse width: During this clock phase the analog output ramps to the next pixel level.
T23		125 ns	ADC digital output stable after falling edge of CLK_ADC.

### Loading the X- and Y- Start Positions

The start positions (start addresses) for "ROI" (Region Of Interest) are preloaded in the X or Y start register. They become effective by the application of the SYNC\_X, SYNC\_YL and/or SYNC\_YR. The start X or Y address must be applied to their common address bus, and the corresponding LD\_X or LD\_Y pin must be pulsed.

On each falling edge of CLK\_X, a new pixel of the same row (line) is accessed. The output stage is in hold when CLK\_X is low and starts generating a new output after a rising edge on CLK\_X.

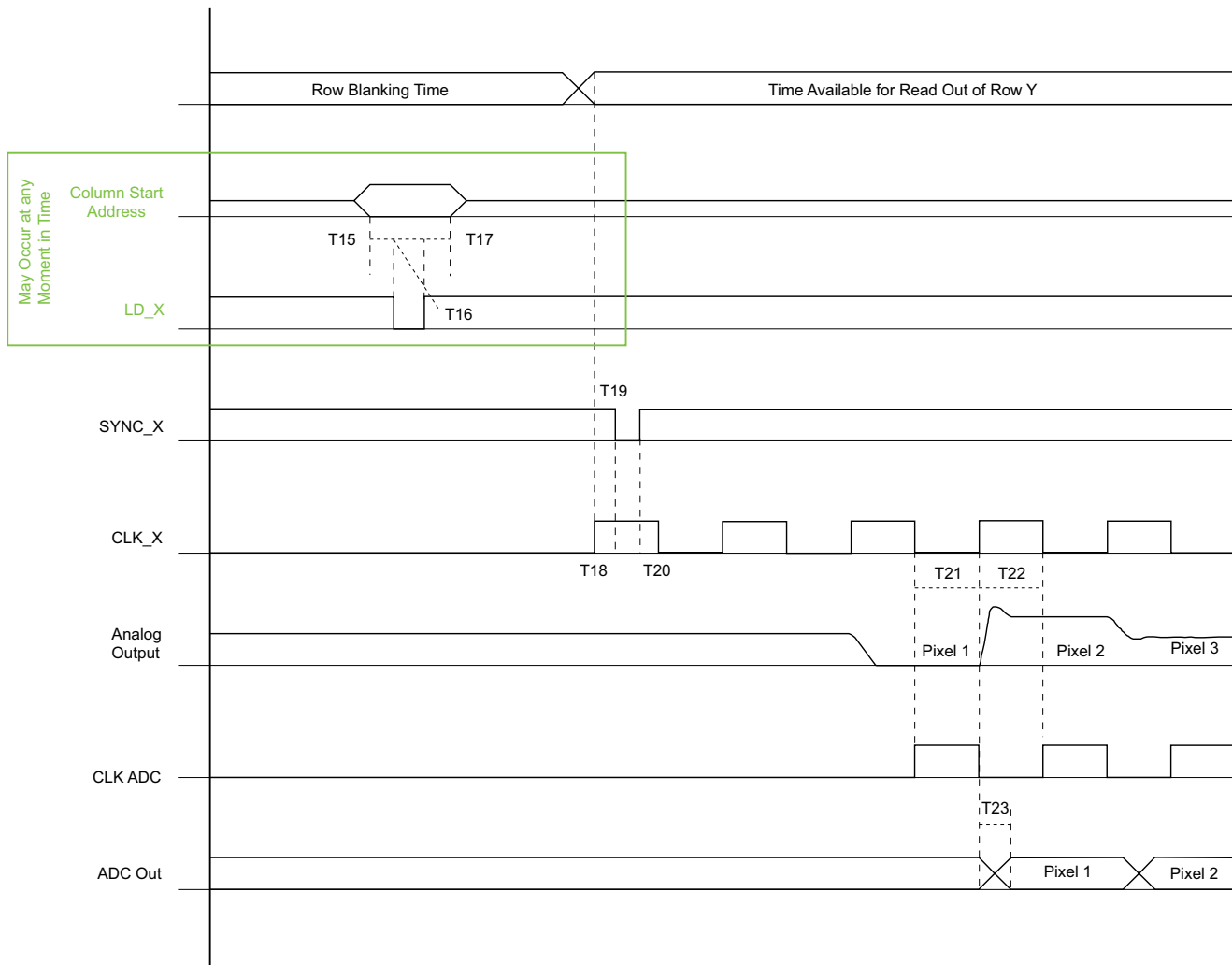
The following timing constraints apply:

Load the X or Y start addresses in advance, before the X or Y shift registers are preset by a SYNC pulse. However, if necessary, they can be load just before the SYNC\_X or SYNC\_Y pulse as shown in [Figure 11](#).

For example, the X start register can be loaded during the row idle time. The Y start register can be loaded during readout of the last row of the previous frame.

If the X or Y start address does not change for later frames, it does not need to be reloaded in the register.

Figure 11. Timing for Loading X and Y Registers



## Other Signals

Tie SELECT signal to VDD for normal operation. This signal is added for diagnostic reasons and inhibits the pixel array operation when held low.

The CAL signal sets the output amplifier DC offset level. When this signal is active (high) the pixel array is internally disconnected from the output amplifier, its gain is set to unity and its input signal is connected to the BLACK\_REF input. Perform this action at least once for each frame.

EOS\_X, EOS\_YL and EOS\_YR produce a pulse when the respective shift register comes at its end. These outputs are used mainly during testing to verify proper operation of the shift registers.

TEST DIODE and TESTPIXEL ARRAY are connections to optical test structures that are used for electro optical evaluation. TESTDIODE is a plain photodiode with an area of 14x5 pixels. TESTPIXEL\_ARRAY is an array (14x5) of pixels where the photodiodes are connected in parallel. These structures measure the photocurrent of the diodes directly.

TESTPIXEL\_RESET and TESTPIXEL-OUT are connections to a single pixel that are used for testing.

## Pinlist

**Table 8. Power Supply Connections**

Pin	Pin Name	Pin Description
10	VDD_ANA	Analog power supply 5V.
11	VDD_DIG	Digital power supply 5V.
31	VDD_AMP	Power supply of output amplifier 5V.
33	VDD_DIG	Digital power supply 5V.
34	VDD_ANA	Analog power supply 5V.
49	VDD_RESR	Reset power supply 5V.
50	VDD_DIG	Digital power supply 5V.
53	VDD_ADC_ANA	ADC analog power supply 5V.
66	VDD_ADC_ANA	ADC analog power supply 5V.
67	VDD_ADC_DIG	ADC digital power supply 5V.
69	VDD_ADC_DIG_3.3/5	ADC 3.3V power supply for digital output of ADC. For interface with 5V external system: connect to VDD_ADC_DIG. For interface with 3.3V external system: connect to 3.3V power supply.
52 76	VDD_PIX	Pixel array power supply [default: 5V, the device is then in "soft reset". To avoid the image lag associated with soft reset, reduce this voltage to 3...3.5V "hard reset"].
78	VDD_DIG	Digital power supply 5V.
79	VDD_RESL	Reset power supply 5V.

**Table 9. Ground Connections**

Pin	Pin Name	Pin Description
9	GND_ANA	Analog ground.
12	GND_DIG	Digital ground.
30	GND_AMP	Ground of output amplifier.
32	GND_DIG	Digital ground.
35	GND_ANA	Analog ground.
51	GND_DIG	Digital ground.
54	GND_ADC_ANA	ADC analog ground.
65	GND_ADC_ANA	ADC analog ground.
68	GND_ADC_DIG	ADC digital ground.
77	GND_DIG	Digital ground.

**Table 10. Digital Input Signals**

Pin	Pin Name	Pin Description
1	S	Control signal for column amplifier. Apply pulse pattern - see <a href="#">Figure 10</a> .
2	R	Control signal for column amplifier. Apply pulse pattern - see <a href="#">Figure 10</a> .
3	RESET	Resets row indicated by left/right shift register. high active (1= reset row). Apply pulse pattern - see <a href="#">Figure 10</a> .
4	SELECT	Selects row indicated by left/right shift register. high active (1=select row). Apply 5V DC for normal operation.
5	L/R	Use left or right shift register for SELECT and RESET. 1 = left/0 = right - see <a href="#">Figure 10</a> .

**Table 10. Digital Input Signals** (continued)

Pin	Pin Name	Pin Description
6	A0	Start address for X- and Y- pointers (LSB).
7	A1	Start address for X- and Y- pointers.
8	A2	Start address for X- and Y- pointers.
13	A3	Start address for X- and Y- pointers.
14	A4	Start address for X- and Y- pointers.
15	A5	Start address for X- and Y- pointers.
16	A6	Start address for X- and Y- pointers.
17	A7	Start address for X- and Y- pointers.
18	A8	Start address for X- and Y- pointers (MSB).
19	LD_Y	Latch address (A0...A8) to Y start register (0 = track, 1 = hold).
20	LD_X	Latch address (A0...A8) to X start register(0 = track, 1 = hold).
21	CLK_YL	Clock YL shift register (shifts on falling edge).
22	SYNC_YL	Sets YL shift register to location preloaded in Y start register. Low active (0=sync). Apply SYNC_YL when CLK_YL is high.
24	CLK_X	Clock X shift register (output valid and s when CLK_X is low).
25	SYNC_X	Sets X shift register to location preloaded in X start register. Low active (0=sync). Apply SYNC_X when CLK_X is high. After SYNC_X, apply falling edge on CLK_X, and rising edge on CLK_X.
27	CLK_YR	Clock YR shift register (shifts on falling edge).
28	SYNC_YR	Sets YR shift register to location preloaded in Y start register. Low active (0=sync). Apply SYNC_YR when CLK_YR is high.
36	CAL	Initialize output amplifier. Output amplifier will output BLACKREF in unity gain mode when CAL is high (1). Apply pulse pattern (one pulse per frame) - see <a href="#">Figure 10</a> .
37	G0	Select output amplifier gain value: G0 = LSB; G1 = MSB. 00 = unity gain; 01 = x2; 10 = x4; 11= x8.
38	G1	idem.
71	CLK_ADC	ADC clock. ADC converts on falling edge.
75	BITINVERT	1 = invert output bits. 0 = no inversion of output bits.
80	TRI_ADC	Tri-state control of digital ADC outputs 1 = tri-state; 0 = output

**Table 11. Digital Output Signals**

Pin	Pin Name	Pin Description
23	EOS_YL	End-of-scan of YL shift register. Low first clock period after last row (low active).
26	EOS_X	End-of-scan of X shift register. Low first clock period after last active column (low active).
29	EOS_YR	End-of-scan of YR shift register. Low first clock period after last row (low active).
55	D0	ADC output bit (LSB).
56	D1	ADC output bit.
57	D2	ADC output bit.

**Table 11. Digital Output Signals**

Pin	Pin Name	Pin Description
58	D3	ADC output bit.
59	D4	ADC output bit.
60	D5	ADC output bit.
61	D6	ADC output bit.
62	D7	ADC output bit.
63	D8	ADC output bit.
64	D9	ADC output bit (MSB).

**Table 12. Analog Input Signals**

Pin	Pin Name	Pin Description
39	NBIASARR	Connect with 470k to Vdd and decouple to ground with a 100 nF capacitor.
40	PBIAS	Connect with 39k to ground and decouple to Vdd with a 100 nF capacitor for 8 MHz pixel rate. (Lower resistor values yield higher maximal pixel rates at the cost of extra power dissipation).
41	NBIAS_AMP	Output amplifier speed/power control. Connect with 51 k $\Omega$ to VDD and decouple with 100 nF to GND for 8 MHz output rate (Lower resistor values yield higher maximal pixel rates at the cost of extra power dissipation).
42	BLACKREF	Control voltage for output signal offset level. Buffered on-chip, the reference level can be generated by a 100k $\Omega$ resistive divider. Connect to $\pm 2$ V DC for use with on-chip ADC.
44	IN_ADC	Input, connect to sensor's output. Input range is between 2 and 4V (VLOW_ADC and VHIGH_ADC).
45	NBIASANA2	Connect with 100k to VDD and decouple to GND.
46	NBIASANA	Connect with 100k to VDD and decouple to GND.
47 70	VLOW_ADC VHIGH_ADC	Low reference and high reference voltages of ADC should be about 2 and 4V. The required voltage settings on VLOW_ADC and VHIGH_ADC can be approximated by tying VLOW_ADC with 1.2k $\Omega$ to GND and VHIGH_ADC with 560 $\Omega$ to VDD.
48	G_AB	Anti-blooming drain control voltage: Default: connect to ground. The anti-blooming is operational but not maximal. Apply 1V DC for improved anti-blooming.
72	PBIASDIG2	Connect with 100K to GND and decouple to VDD.
73	PBIASENCLOAD	Connect with 100K to GND and decouple to VDD.
74	PBIASDIG1	Connect with 47K to GND and decouple to VDD.

**Table 13. Analog Output Signals**

Pin	Pin Name	Pin Description
43	OUT	Analog output signal are connected to the analog input of the ADC.

**Table 14. Test Structures**

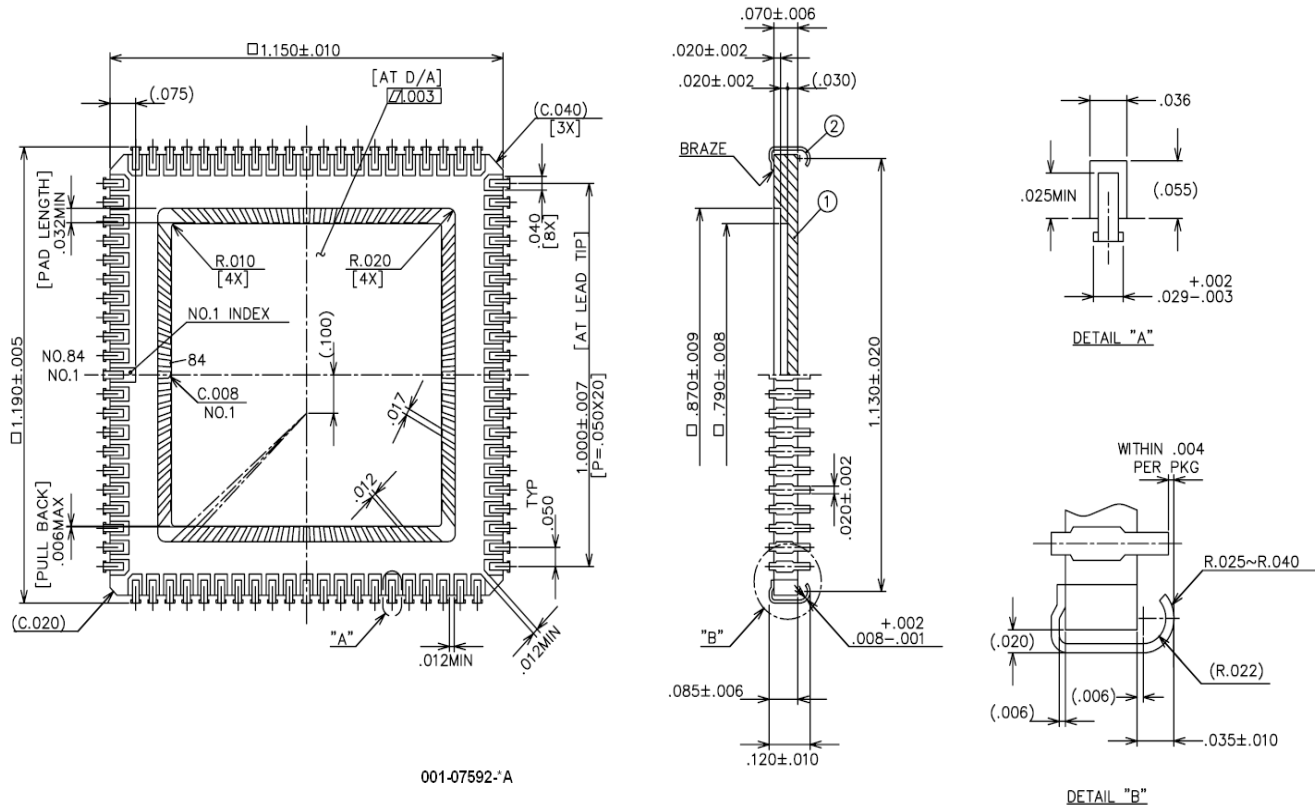
Pin	Pin Name	Pin Description
81	TESTDIODE	Plain photo diode, size: 14 x 25 pixels. Must be left open for normal operation.
82	TESTPIX ARRAY	Array of test pixels, connected in parallel (14 x 25 pixels). Must be left open for normal operation.
83	TESTPIXEL_RESET	Reset input of single test pixel. Must be tied to GND for normal operation.
84	TESTPIXEL_OUT	Output of single test pixel. Must be left open for normal operation.



## Package

### Package with Glass

Figure 12. STAR250 Package Dimensions



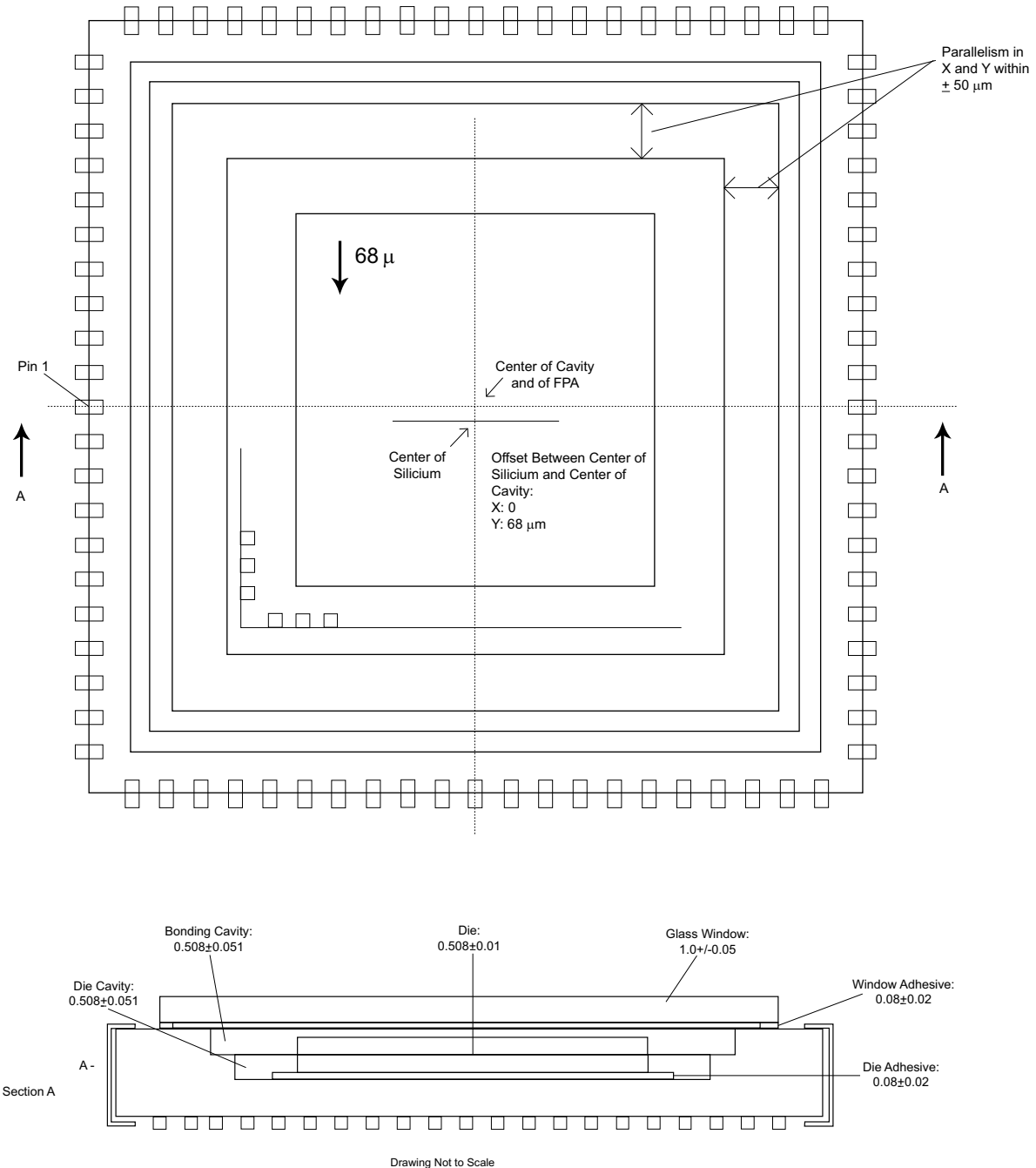
**Note** All dimensions in Figure 12 are measured in inches.

Table 15. Package Specifications:

Type	JLCC-84
Material	Black Alumina BA-914
Thermal expansion coefficient	$7.6 \times 10^{-6} /K$

## Die Alignment

Figure 13. Die Alignment



The die is aligned manually in the package to a tolerance of  $\pm 50 \mu\text{m}$  and the alignment is verified after hardening the die adhesive. All dimensions in Figure 13 are in mm.

## Window Specifications

STAR250

Table 16. STAR250 Glass Cover Specifications:

Material	Fused Silica
Dimensions	25 x 25 mm $\pm$ 0.2 mm
Thickness	1 mm $\pm$ 0.05 mm
Anti reflective coating	No
Cavity fill	Air

STAR250BK7

Table 17. STAR250BK7 Glass Cover Specifications

Material	BK7G18
Dimensions	25 x 25 mm $\pm$ 0.2 mm
Thickness	1 mm $\pm$ 0.05 mm
Anti reflective coating	Yes
Cavity fill	N <sub>2</sub>

## Soldering and Handling

### Soldering and Handling Conditions

Take special care when soldering image sensors onto a circuit board. Prolonged heating at elevated temperatures may result in deterioration of the performance of the sensor. The following recommendations are made to ensure that sensor performance is not compromised during end users' assembly processes.

#### Board Assembly

The STAR250 is very sensitive to ESD. Device placement onto boards should be done in accordance with strict ESD controls for Class 0, JESD22 Human Body Model, and Class A, JESD22 Machine Model devices. Assembly operators need to always wear all designated and approved grounding equipment; grounded wrist straps at ESD protected workstations are recommended including the use of ionized blowers. All tools should be ESD protected.

### RoHS (lead free) Compliance

This section reports the use of Hazardous chemical substances as required by the RoHS Directive (excluding packing material).

**Table 18. Chemical Substances in STAR250 Sensor**

Chemical Substance	Any Intentional Content	If there is any intentional content, in which portion is it contained?
Lead	NO	-
Cadmium	NO	-
Mercury	NO	-
Hexavalent chromium	NO	-
PBB (Polybrominated biphenyls)	NO	-
PBDE (Polybrominated diphenyl ethers)	NO	-

#### Information on Lead Free Soldering

The product cannot withstand a lead free soldering process. Reflow or wave soldering is not allowed; hand soldering only. Solder 1 pin on each side of the sensor and let it cool down for at least 1 minute before continuing

**Note** "Intentional content" is defined as any material demanding special attention that is contained into the inquired product by these cases:

1. A case that the above material is added as a chemical composition into the inquired product intentionally to produce and maintain the required performance and function of the intended product
2. A case that the above material, which is used intentionally in the manufacturing process, is contained in or adhered to the inquired product.

#### Manual Soldering

When a soldering iron is used the following conditions should be observed:

- Use a soldering iron with temperature control at the tip. The soldering iron tip temperature should not exceed 350°C.
- The soldering period for each pin should be less than five seconds.

#### Reflow Soldering

Reflow soldering is not allowed.

#### Precautions and Cleaning

Avoid spilling solder flux on the cover glass; bare glass and particularly glass with antireflection filters may be harmed by the flux. Avoid mechanical or particulate damage to the cover glass.

Use isopropyl alcohol (IPA) as a solvent for cleaning the image sensor glass lid. When using other solvents, it should be confirm whether the solvent will dissolve the package and/or the glass lid.

The following case is not treated as "intentional content":

A case that the above material is contained as an impurity into raw materials or parts of the intended product. The impurity is defined as a substance that cannot be removed industrially, or it is produced at a process such as chemical composing or reaction and it cannot be removed technically.

#### Evaluation kit

For evaluating purposes, an STAR250 evaluation kit is available. The STAR250 evaluation kit consists of a multifunctional digital board (memory, sequencer and IEEE 1394 Fire Wire interface) and an analog image sensor board. Visual Basic software (under Win 2000 or XP) allows the grabbing and display of images from the sensor. All acquired images can be stored in different file formats (8 or 16-bit). All setting can be adjusted on the fly to evaluate the sensors specs. Default register values can be loaded to start the software in a desired state. Please contact us for more information.

## Document History Page

Document Title: CYIS1SM0250-AA STAR250 250K Pixel Radiation Hard CMOS Image Sensor Document Number: 38-05713				
Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
**	310213	See ECN	SIL	Origination
*A	603159	See ECN	QGS	Converted to Framemaker Format
*B	649360	See ECN	FPW	Title update + package spec label
*C	2766198	09/19/09	NVEA	Updated Ordering Information table

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

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Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. For more information on Image sensors, contact [imagesensors@cypress.com](mailto:imagesensors@cypress.com).

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