WildPass

ADM8668

Communications

Never stop thinking.

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Trademarks

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1 Product Overview

1.1 Overview

WildPass is a highly integrated SOC chip which includes an 802.11a/b/g MAC/Baseband, two 802.3 MACs and one 10/100BASE-TX 802.3u compliant Auto-MDIX transceiver. Hardware NAT is supported for wired speed bridging for high speed broadband applications. A USB2.0 host controller, PCI 2.2 bridge, IDE controller, SPI and PCM interfaces are all provided.

WildPass has a 32-bit 200MHZ MIPS4KC CPU with 8K byte I cache and 8K byte D cache. An MMU (Memory Management Unit) is provided for RTOS applications. The internal AHB bus can run up to 100MHZ to provide increased performance.

WildPass implements the IEEE 802.11a/b/g MAC/Baseband for wireless applications in either the 2.4GHz or 5GHz bands. WildPass is interfaced with Infineon's 802.11a/b/g dual band RF chip set (PEF8820) to provide world class radio performance. It also integrates the wireless security function which is specified in 802.11i and is fully compliant to WPA and WPA2 certifications. Encryption/decryption hardware engines like AES/CCMP, TKIP/MIC and WEP are built into the data path which alleviates pressure on the CPU and internal AHB bus traffic. WildPass also supports 802.11e to fulfill the wireless QOS standard requirements. 802.11h is also supported for radar detection in the 5GHz band especially suited for areas with radar interference.

WildPass provides port1 (802.3 MAC + PHY), and port2 (802.3 MAC + reversed MII interface) for LAN, WAN applications. Wire speed hardware NAT for bi-directional 64-byte packet bridging (concurrently from LAN to WAN, and from WAN to LAN) with minimum IFG is achievable. The bridging function from wireless to LAN, and wireless to WAN is performed by the CPU. The reverse-MII interface is capable of connecting to a switch for multiple LAN port applications.

A USB 2.0 host, IDE and PCI interface are all provided for different system products. Programmable SPI and PCM interfaces provide support for VoIP applications.

WildPass is a high performance network processor and can cooperate with external devices via it’s SRAM interface and GPIO. NAND FLASH (with ECC support), NOR FLASH, SDRAM and SRAM memory types are fully supported.

1.2 Features

The following describes the WildPass’s features:

1.2.1 Main Features

- CPU: 200MHZ MIPS4KC + MMU with 8KB I-cache, 8KB D-cache
- CPU: AHB: SDRAM = 200MHZ: 100MHZ: 100MHZ
- 6 DMA engines for direct memory access
  - Port1 (one wired 10/100 MAC + 10/100 PHY with Hardware NAT)
  - Port2 (one wired 10/100 MAC + reverse-MII interface with Hardware NAT)
  - WLAN (one 802.11a/b/g MAC + Baseband)
  - USB 2.0 Host with PHY
  - PCI bridge with support for three devices
  - IDE

- High speed UART up to 920K baud rate for software debugging, a modem interface or other high speed serial interface applications
- Flexible external memory support:
  – NOR FLASH up to 20M bytes
  – NAND FLASH up to 128M bytes
  – SDRAM up to 256M bytes
  – SRAM up to 20M bytes
- Standards compliant:
  – IEEE 802.11a/b/g
  – IEEE 803.11e, WMM
  – IEEE 802.11i, WPA, WPA2
  – IEEE 802.11h
  – IEEE 802.11d
  – IEEE 802.3u
- AHB devices: MIPS4KC, MC, port1, port2, WLAN, USB2.0 host, PCI, IDE
- APB devices: UART, SPI, PCM
- LEDs:
  – led_bootack on: power on / flash: flash booting
  – wled_LinkAck on: associated / flash: radio traffic
  – led_linkact on: link / flash: activity for LAN1
  – led_speed on: 100M / off: 10M for LAN1
  – led_fdcol on: full duplex / flash traffic detected for LAN1
- Debugging interface: JTAG for MIPS-multiICE, trace32
- Package: 352BGA (sales code: ADM8668F), 289BGA (excludes PCI and IDE interface, sales code: ADM8668T)
- Power: On-chip 1.8 V voltage regulator is supported to reduce component cost

1.2.2 Applications

- Wireless AP (Access Point)
- Home Router
- Wireless NAS
- Wireless Storage Router
- Printer Server
- Embedded Applications
- VoIP Applications

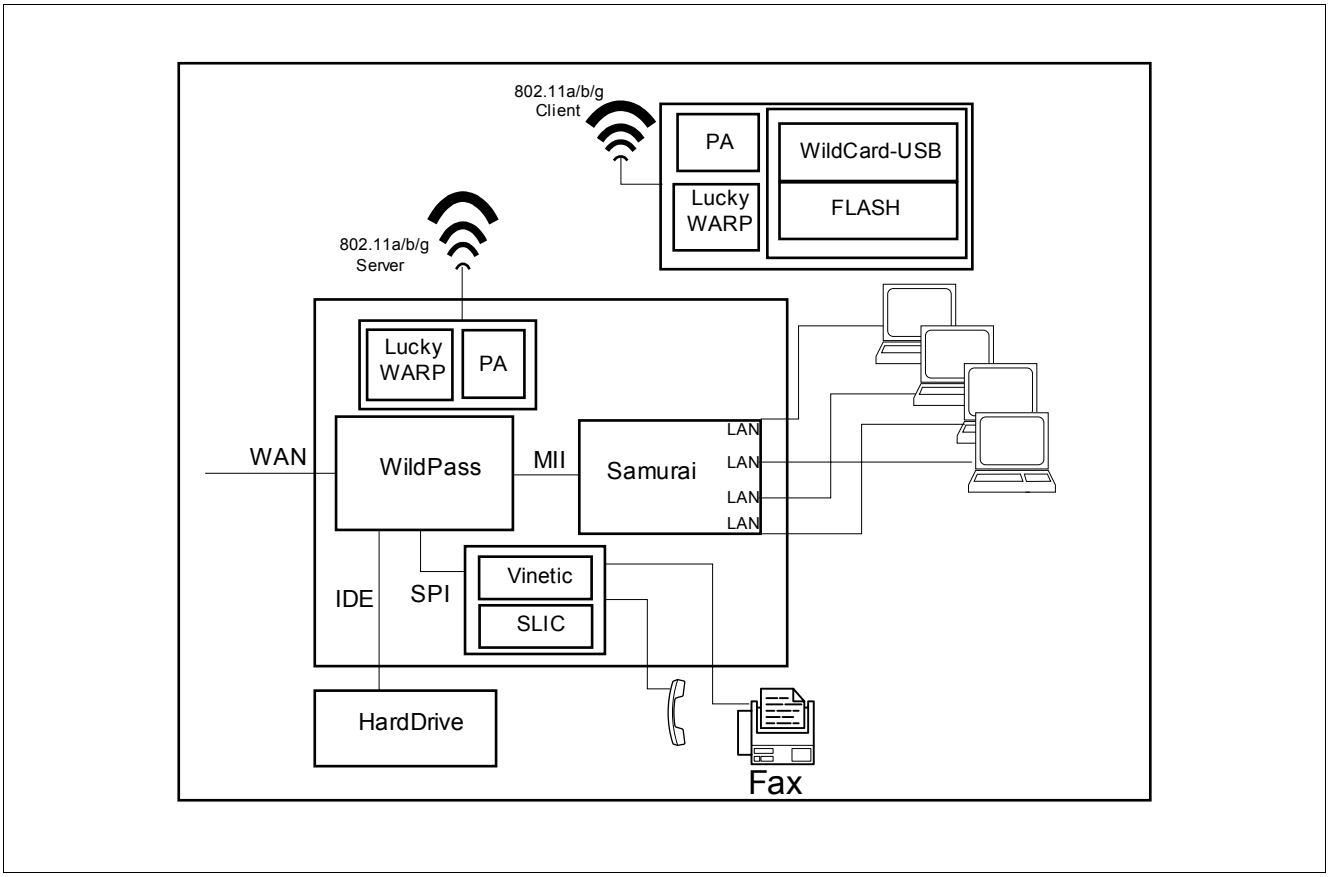

Figure 1 WildPass Application Example

1.3 WildPass (ADM8668) Chip Architecture

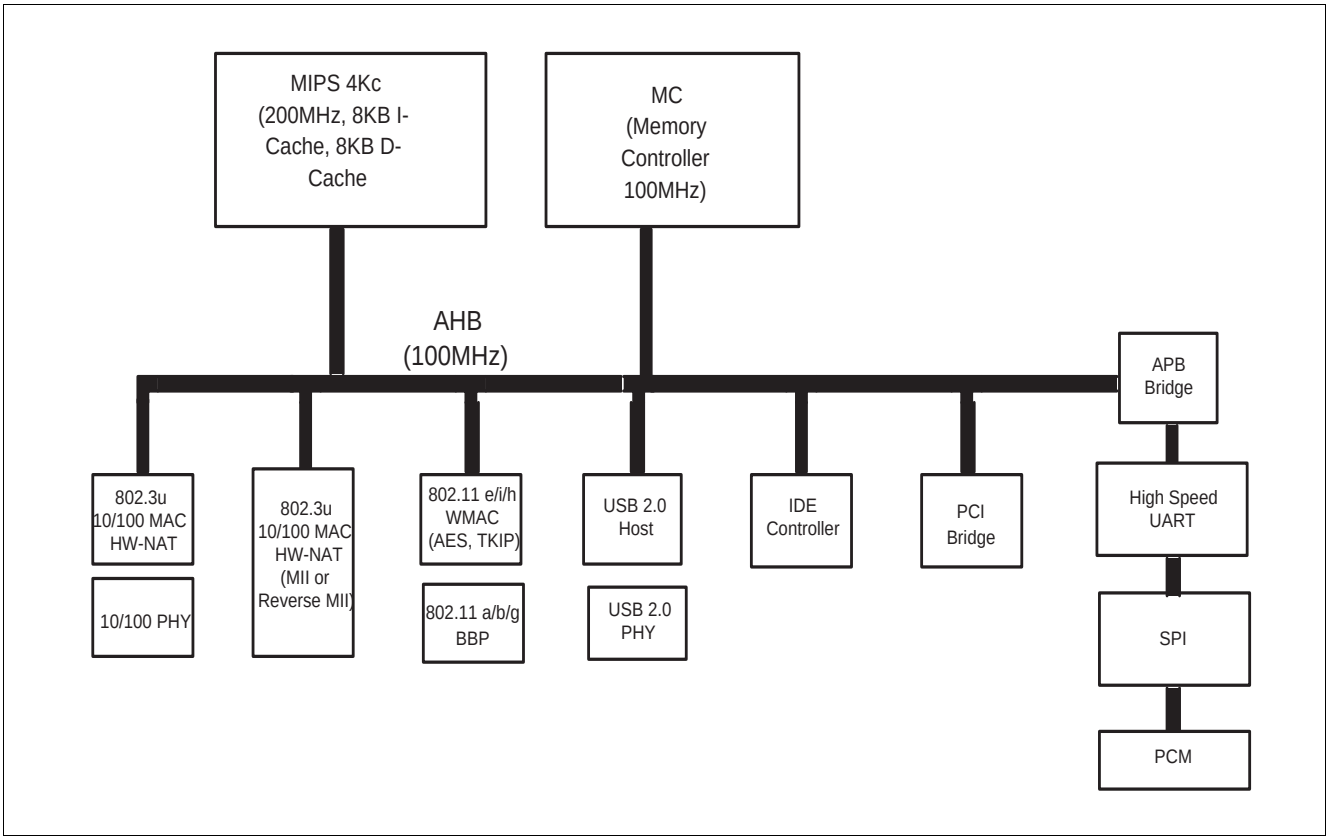

Figure 2 Hardware Block Diagram

1.4 WildPass Software Architecture

The software architecture of WildPass is based on the Linux system with several concurrent processes performing different tasks. Each process requests for various resources like system resources, computing power, memory, and network connectivity. The kernel is responsible for handling requests. The components of the kernel are shown in **Figure 3**

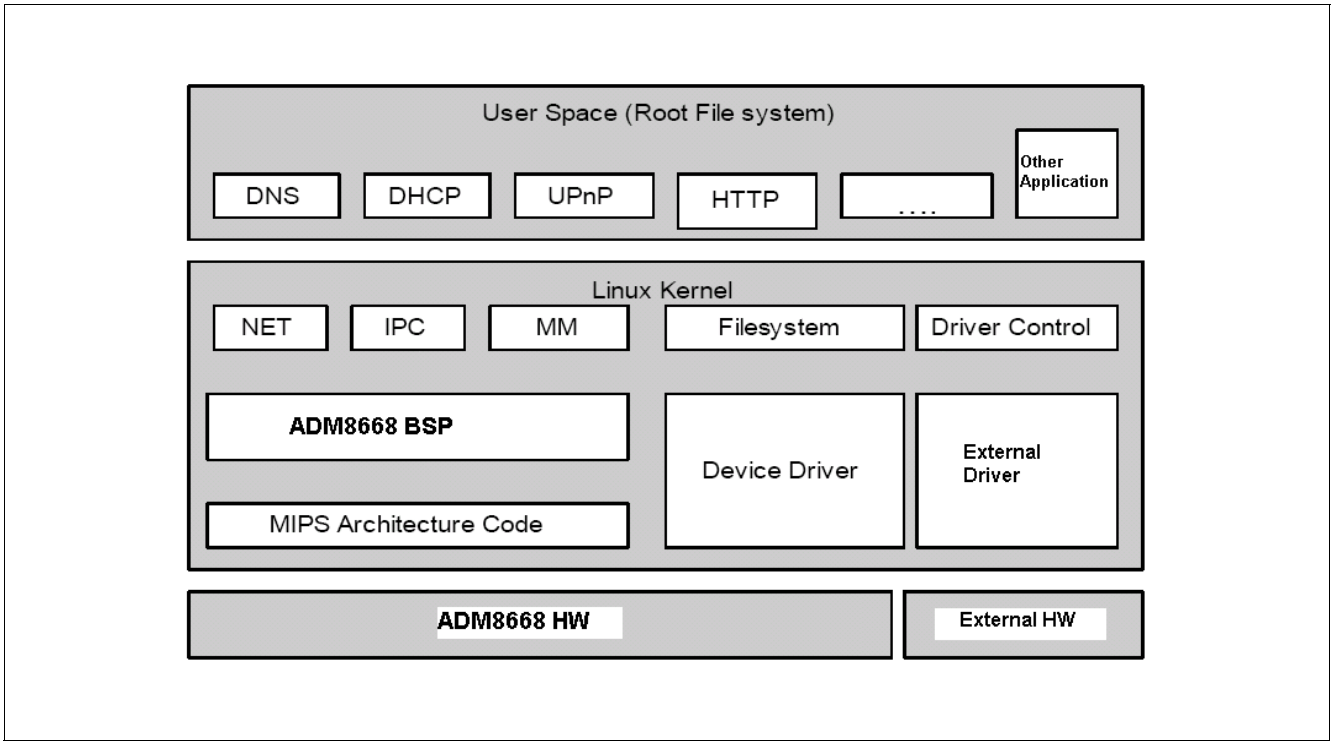

Figure 3 System Architecture

In the Linux kernel, the basic capabilities include networking protocols, inter-process communication functions, memory management functions, file system, and device control mechanisms. To enable an access point function, the wireless driver is also embedded in the Linux Kernel.

In the user space, you can find various applications for networking. For example: DNS, DHCP and HTTP. The WildPass application is a demonstration application for access point and router. Users can also run other applications (like storage, etc.) via the built-in variety of peripheral interfaces.

1.4.1 Software Features

The followings are the main software features of the WildPass:

- BSP
  - Linux kernel 2.4.20
  - Drivers (LAN/WAN, WLAN, PCI, IDE, USB 2.0, etc.)
- Link layer protocols
  - PPP, CCP, IPCP, PAP, CHAP, MSCHAP, PPPoE, PPTP
- Bridging
  - 802.1D transparent bridging
- Network layer protocols
  - ARP, IP, UDP, TCP, ICMP, RARP
- Routing and network core functions
  - Static routing
  - RIP1, RIP2
- Firewall
  - Packet filtering
  - DoS protection
  - DMZ
- NAT/NAPT
  - NAT pass-through

  - ALG
  - Virtual server
  - Port mapping
- Networking applications
  - DHCP client/server
  - NTP
  - DNS relay
  - DDNS
  - UPnP
- Management
  - WEB server
  - Syslog
  - E-mail alert
  - Firmware upgrade
  - CLI
- WLAN
  - AP/Client/Repeater mode
  - WPA, WPA2
  - 802.1X/EAP-TLS
  - WMM

2 Interface Description

The following chapter describes the interface for the WildPass packages - ADM8668T (289BGA) and ADM8668F (352BGA). For details on the mechanical specifications please refer to the package chapter.

2.1 Interface Description - ADM8668T

2.1.1 WildPass Ball Diagram

2.1.1.1 289 BGA

Below the ball diagram for the 289-BGA version is displayed.

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U
1	XA[20]	XD[1]	XD[14]	XD[12]	P_W2UE_PD	SDCKDQM[1]	NSDCWEOUT	NSDCXCS[0]	XA[14]	XA[11]	XA[9]	XA[6]	XD[31]	SDCKDQM[2]	XD[29]	XD[25]	XD[18]
2	JTAG_NTRST	NSMCXCS[0]	XD[5]	XD[6]	XD[15]	XD[11]	XD[8]	NSDCRASOUT	XA[13]	SCLK	XA[8]	XA[4]	XA[1]	SDCKDQM[3]	XD[28]	XD[16]	XD[20]
3	JTAG_TCK	XA[17]	NSMCXCS[1]	XD[3]	XD[4]	XD[7]	XD[10]	SDCKDQM[0]	NSDCXCS[1]	XA[12]	XA[7]	XA[5]	XA[3]	XD[30]	XD[27]	XD[17]	XD[22]
4	NUART_CTS	XA[16]	XD[0]	XA[19]	XD[2]	XD[13]	XD[9]	NSDCCASOUT	VDD	VSS/DVSS	XA[10]	XA[0]	XA[2]	XD[19]	XD[26]	XD[21]	XA[22]
5	NUART_DSR	JTAG_TDI	NSMCXOEN	XA[15]	DVDD	DVDD	VDD	DVDD	DVDD	VDD	DVDD	VDD	DVDD	CRGPIO[0]	XD[24]	XD[23]	XTLP_USB
6	NUART_DCD	JTAG_TDO	XA[18]	VDD	DVDD	VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS	VDD	FXS_DX	XA[21]	NSMCXCS[2]	XTLN_USB
7	PWR_SENSE2	UART_TXD	JTAG_TMS	PWR_REF2	DVDD	VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS	DVDD	VSS/DVSS	CRGPIO[1]	XTLP	XTLN
8	PWR_SENSE	XNRESET_IN	UART_RXD	VSS/DVSS	DVDD	VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS	VDD	VSS/DVSS	CRGPIO[2]	FXS_DR	FXS_PCLK
9	XCRYSTAL	XCRYSTAL_OUT	WLED_LINKACK	VDDAH_AFE	DVDD	VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS	VDD	VSS/DVSS	FXS_FSC	FXS_RESETZ	RPU
10	REF_RES	TXQ_P	PWR_REF	VDDAH_AFE	VDD	VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS	VDD	AVDD3_A	VDDC_A	GNDC_A	GNDBG_A
11	VDDAL_AFE	TXQ_M	TXI_M	RSSI	GNDA_AFE	GNDA_AFE	VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS	VDD	AVDD_A	AGND_A	DP	RREF
12	VCTRL	RXQ_P	TXI_P	RXVGC	GNDA_AFE	GNDA_AFE	VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS	VDD	REG_BASE	AGND_W2UE	DM	VDDBG_A
13	VDDAL_CKGEN	RXQ_M	RXI_M	RXI_P	B[1]	LED_SPEED	DVDD	DVDD	NNF_WP	VDD	VDD	W20MHZ_SEL	FXS_SDI	VREF	GNDPLL	AVDD_W2UE	VCCPLL
14	TXPE	GNDA_CKGEN	VDDAH_CKGEN	VDDAL_AFE	PAPE	B[2]	GPIO[0]	LED_LKACT	NF_RY_BY	L2_PHY_RSTZ	RMII_TXD0	FXS_INTZ	RMII_RXD2	VCCA20	TXP	GNDBSRG	CONTROL
15	PA_ON_A	ANTSEL	RXPE	CKREF	B[0]	B[7]	LEIFZ	NNF_RE	NNF_WE	RMII_TXD3	RMII_TXEN	FXS_SDO	FXS_SCLK	RXP	TXN	VCCBSRG	RTX
16	B[3]	B[4]	B[5]	B[6]	NF_CLE	SYNCLK	GPIO[1]	LED_BOOTACT	TESTCLK	RMII_TXD1	VOIPCLKIN	RMII_TXCLK	RMII_RXDV	RXN	RMII_RXD1	RMII_RXD3	GNDTR
17	TRSW	PWDN	NNF_CE	LED_FDCOL	NF_ALE	SYNDATA	GPIO[2]	TEST_IN	TESTRESET_IN	RMII_TXD2	FXO_INTZ	FXO_CSZ	FXS_CSZ	RMII_RXCLK	RMII_RXD0	RELAY_CONTROLZ	VCCAD

Figure 4 289 BGA Diagram

2.1.2 Ball Description by Function

WildPass balls are categorized into one of the following groups:

- **Chapter 2.1.2.1** UART Interface
- **Chapter 2.1.2.2** Memory Bus
- **Chapter 2.1.2.3** SDRAM control signals
- **Chapter 2.1.2.4** FLASH/SDRAM control signals
- **Chapter 2.1.2.5** JTAG signals

- **Chapter 2.1.2.6** WLAN signals
- **Chapter 2.1.2.7** LAN 1
- **Chapter 2.1.2.8** LAN 2
- **Chapter 2.1.2.9** USB
- **Chapter 2.1.2.10** VoIP (PCM and SPI)
- **Chapter 2.1.2.11** NAND Flash
- **Chapter 2.1.2.12**Power/Ground
- **Chapter 2.1.2.13**Miscellaneous

2.1.2.1 UART Interface

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 1 P-BGA-289 Package UART Interface

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
A4	nUART_CTS	I	-	**Clear to send, active low**
A6	nUART_DCD	I		**Data carrier detect, active low**
A5	nUART_DSR	I		**Data send ready, active low**
C8	UART_RXD	I		**Receive serial data input**
B7	UART_TXD	O		**Tx Serial Data Output**
A9	XCRYSTAL	I		**UART Crystal** UART X'tal in 3.6864MHZ ~ 73MHZ
B9	XCRYSTAL_OUT	O		**UART X'tal output**

2.1.2.2 Memory Bus

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 2 P-BGA-289 Package Memory Bus

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
N1	XD31	IO	-	**Data Bus** Data bus[31] for SDRAM, FLASH
P3	XD30	IO		**Data Bus** Data bus[30] for SDRAM, FLASH
R1	XD29	IO		**Data Bus** Data bus[29] for SDRAM, FLASH
R2	XD28	IO		**Data Bus** Data bus[28] for SDRAM, FLASH

Table 2 P-BGA-289 Package Memory Bus (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
R3	XD27	IO	-	**Data Bus** Data bus[27] for SDRAM, FLASH
R4	XD26	IO		**Data Bus** Data bus[26] for SDRAM, FLASH
T1	XD25	IO		**Data Bus** Data bus[25] for SDRAM, FLASH
R5	XD24	IO		**Data Bus** Data bus[24] for SDRAM, FLASH
T5	XD23	IO		**Data Bus** Data bus[23] for SDRAM, FLASH
U3	XD22	IO		**Data Bus** Data bus[22] for SDRAM, FLASH
T4	XD21	IO		**Data Bus** Data bus[21] for SDRAM, FLASH
U2	XD20	IO		**Data Bus** Data bus[20] for SDRAM, FLASH
P4	XD19	IO		**Data Bus** Data bus[19] for SDRAM, FLASH
U1	XD18	IO		**Data Bus** Data bus[18] for SDRAM, FLASH
T3	XD17	IO		**Data Bus** Data bus[17] for SDRAM, FLASH
T2	XD16	IO		**Data Bus** Data bus[16] for SDRAM, FLASH
E2	XD15	IO		**Data Bus** Data bus[15] for SDRAM, FLASH
C1	XD14	IO		**Data Bus** Data bus[14] for SDRAM, FLASH
F4	XD13	IO		**Data Bus** Data bus[13] for SDRAM, FLASH
D1	XD12	IO		**Data Bus** Data bus[12] for SDRAM, FLASH
F2	XD11	IO		**Data Bus** Data bus[11] for SDRAM, FLASH
G3	XD10	IO		**Data Bus** Data bus[10] for SDRAM, FLASH
G4	XD9	IO		**Data Bus** Data bus[9] for SDRAM, FLASH
G2	XD8	IO		**Data Bus** Data bus[8] for SDRAM, FLASH
F3	XD7	IO		**Data Bus** Data bus[7] for SDRAM, FLASH
D2	XD6	IO		**Data Bus** Data bus[6] for SDRAM, FLASH

Table 2 P-BGA-289 Package Memory Bus (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
C2	XD5	IO	-	**Data Bus** Data bus[5] for SDRAM, FLASH
E3	XD4	IO		**Data Bus** Data bus[4] for SDRAM, FLASH
D3	XD3	IO		**Data Bus** Data bus[3] for SDRAM, FLASH
E4	XD2	IO		**Data Bus** Data bus[2] for SDRAM, FLASH
B1	XD1	IO		**Data Bus** Data bus[1] for SDRAM, FLASH
C4	XD0	IO		**Data Bus** Data bus[0] for SDRAM, FLASH
U4	XA22	IO		**Data Bus for SDRAM and Flash** SDRAM address is XA[14:0].FLASH, SRAM address is XA[22:0]Please reference the Appendix for Reset information. *Note: WildPass has an internal address shifting function, i.e. the XA0 is byte addressing when FLASH is byte width, the XA0 is word addressing (16-bit) when FLASH is word width, the XA0 is double word addressing when FLASH is 32 bits.GPIO[2] will be configured as nSIROUT (output), and GPIO[1] will be SIRIN (input) by pull-up reset latched pin XA[20]*
R6	XA21	IO		
A1	XA20	IO		
D4	XA19	IO		
C6	XA18	IO		
B3	XA17	IO		
B4	XA16	IO		
D5	XA15	IO		
J1	XA14	IO		
J2	XA13	IO		
K3	XA12	IO		
K1	XA11	IO		
L4	XA10	IO		
L1	XA9	IO		
L2	XA8	IO		
L3	XA7	IO		
M1	XA6	IO		
M3	XA5	IO		
M2	XA4	IO		
N3	XA3	IO		
N4	XA2	IO		
N2	XA1	IO		
M4	XA0	IO		

2.1.2.3 SDRAM Control Signals

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 3 P-BGA-289 SDRAM control signals

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
K2	SCLK	O	-	**SDRAM clock**
H1	nSDCxCS0	O		**Bank Size** Minimum bank0 size = 64MB.Maximum bank0 size = 128MB.
J3	nSDCxCS1	O		**Address Rage** Address range continues from bank0
H2	nSDCRASout	O		**Address Strobe** SDRAM raw address strobe, active low
H4	nSDCCASout	O		**Col Address Strobe** SDRAM, column address strobe, active low
P2	SDCxDQM3	O		**SDRAM, byte data mask** Data bus width [8 :0] SDRAM_DQMData bus width [16 :1:0] SDRAM_DQM Data bus width 32: [3:0] SDRAM_DQM
P1	SDCxDQM2			
F1	SDCxDQM1			
H3	SDCxDQM0			
G1	nSDCWEout	O		**Write Enable Active Low** SDRAM, write enable, active low

2.1.2.4 FLASH/SRAM Control Signals

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 4 P-BGA-289 FLASH/SRAM control signals

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
T6	nSMCxCS2	O	-	**Chip Select Active Low 1** Chip select for external FLASH/SRAM, active low. Address range is from 1080_0000 to 10ff_ffff when XA[12] reset latch = 0. Address range starts from 0000_0000 when XA[12] reset latch =1
C3	nSMCxCS1	O		**Chip Select Active Low 2** Chip select for external FLASH/SRAM, active low. Address range is from1000_0000 to 107f_ffff
B2	nSMCxCS0	O		**Chip Select External Flash** Chip select for external FLASH, active low.Address range starts from $1FC0_H$_0000
C5	nSMCxOEN	O		**Output Enable** Output enable, active low.
G1	SMC_WEZ	O		**Write enable, active low. (multiplexed with nSDCWEout), dedicated for 16/32-bit FLASH**
P2	SMC_BLS3	O		**Bank Select3 Active Low 3** Bank select3, active low (multiplexed with SDCxDQM [3]) for 8-bit FLASH.
P1	SMC_BLS2	O		**Bank Select3 Active Low 2** Bank select3, active low (multiplexed with SDCxDQM [2]) for 8-bit FLASH.
F1	SMC_BLS1	O		**Bank Select3 Active Low 1** Bank select3, active low (multiplexed with SDCxDQM [1]) for 8-bit FLASH.
H3	SMC_BLS0	O		**Bank Select3 Active Low 0** Bank select3, active low (multiplexed with SDCxDQM [0]) for 8-bit FLASH.

2.1.2.5 JTAG Signals

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 5 P-BGA-289 Package JTAG Signals

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
A3	JTAG_TCK	I	-	**JTAG test clock**
C7	JTAG_TMS	I		**JTAG test mode select**
B6	JTAG_TDO	O		**Test data out**
B5	JTAG_TDI	I		**Test data in**
A2	JTAG_ntRST	I		**Asynchronous reset (active low)**

2.1.2.6 WLAN 802.11g Signals

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 6 P-BGA-289 Package WLAN Signals

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
F17	SYNDATA	IO	-	**Data in out for RF 3-wire interface**
F16	SYNCLK	O		**Clock out for RF 3-wire interface**
G15	LEIFZ	O		**Synthesizer interface select**
B17	PWDN	O		**Power Down** Power down or MAC sleep signal output, active level set by WCSR18.PD.
A17	TRSW	O		**TX/RX switch select**
F15	B7	IO		**RF Control Bus**
D16	B6	IO		
C16	B5	IO		
B16	B4	IO		
A16	B3	IO		
F14	B2	IO		
E13	B1	IO		
E15	B0	IO		**Mixed with RXHP**
E14	PAPE	O		**PA power enable**
A15	PA_ON_A	O		**PA power enable for 11a**
B15	ANTSEL	O		**Antenna select**
C15	RXPE	O		**RF RX enable**
A14	TXPE	O		**RF TX enable**
B14	GNDA_CKGEN	P		**Regulator ground**
D15	CKREF	I		**40MHZ input**
A13	VDDAL_CKGEN	P		**PLL 1.8 V**
A12	VCTRL	AO		**Regulator control (spare purpose)**
C14	VDDAH_CKGEN	P		**Regulator power 3.3 V**
D12	RXVGC	AO		**Analogue receive variable gain control output: 1.2 V to 2.0 V**
A11, D14	VDDAL_AFE	P		**AFE analogue power 1.8 V**
D13	RXI_P	AI		**RX I channel analogue input +**
C13	RXI_M	AI		**RX I channel analogue input -**
B13	RXQ_M	AI		**RX Q channel analogue input +**
B12	RXQ_P	AI		**RX Q channel analogue input -**
D11	RSSI	AI		**Receiver signal strength indicator analogue input**
A10	REF_RES	AI		**External 1% accuracy 11.5K resistor pin**
D9, D10	VDDAH_AFE	P		**AFE analogue power 3.3 V**
C12	TXI_P	AO		**TX I channel analogue output +**
C11	TXI_M	AO		**TX I channel analogue output -**
B11	TXQ_M	AO		**TX Q channel analogue output +**
B10	TXQ_P	AO		**TX IQ channel analogue output -**

Table 6 P-BGA-289 Package WLAN Signals (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
A8	PWR_SENSE	AI	-	**TSSI sense pin 1**
C10	PWR_REF	AI		**TSSI reference pin 1**
A7	PWR_SENSE2	AI		**TSSI sense pin 2 for 11a**
D7	PWR_REF2	AI		**TSSI reference pin 2 for 11a**
E11, E12, F11, F12	GNDA_AFE	P		**GND for AFE**
G17	GPIO2	IO		**Wireless driver controlled GPIO2**
G16	GPIO1	IO		**Wireless driver controlled GPIO1**
G14	GPIO0	IO		**Wireless driver controlled GPIO0**
C9	WLED_LINKACK	O		**LinkAct** On: associatedOff: activities

2.1.2.7 Port 1

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 7 P-BGA-289 Package Port 1

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
U13	VCCPLL	P	-	**Analogue power 1.8 V for PLL**
R13	GNDPLL	P		**Ground for PLL**
U14	CONTROL	A		**FET control for 3.3 V to 1.8 V regulator**
P13	VREF	P		**Analogue power 1.8 V**
T14	GNDBSRG	P		**Analogue ground**
U15	RTX	AI		**TX resister * ohm**
T15	VCCBSRG	P		**Analogue power 3.3 V for bias block**
P14	VCCA20	P		**Analogue power 1.8 V**
R14	TXP	A		**TX +**
R15	TXN	A		**TX -**
U16	GNDTR	P		**Analogue ground**
P15	RXP	A		**RX +**
P16	RXN	A		**RX -**
U17	VCCAD	P		**Analogue power 3.3 V for RX line driver**
T7	XTLP	I		**25MHZ X'tal input (No connection when P_W2UE_PD =0)**
U7	XTLN	O		**25MHZ X'tal output (No connection when P_W2UE_PD =0)**
H14	LED_LKACT	O		**LED LinkAct** Flash: activities On: Link
F13	LED_SPEED	O		**LED Speed** On: 100MHZ Off: 10MHZ
D17	LED_FDCOL	O		**LED Duplex** On: full duplexOff: half duplex

2.1.2.8 Port 2

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 8 P-BGA-289 Package Port 2

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
T16	RMII_RXD3	I	-	**RXD [3]**
N14	RMII_RXD2	I		**RXD [2]**
R16	RMII_RXD1	I		**RXD [1]**
R17	RMII_RXD0	I		**RXD [0]**
N16	RMII_RXDV	I		**RXDV**
P17	RMII_RXCLK	I		**RMII Rx Clock** Output when Reverse-MII mode Input when MII mode
M16	RMII_TXCLK	I		**RMII Tx Clock** Output when Reverse-MII mode Input when MII mode
L15	RMII_TXEN	O		**TXEN**
K15	RMII_TXD3	O		**TXD [3]**
K17	RMII_TXD2	O		**TXD [2]**
K16	RMII_TXD1	O		**TXD [1]**
L14	RMII_TXD0	O		**TXD [0]**
K14	L2_PHY_RSTZ	O		**Internal power on reset output**

2.1.2.9 USB

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 9 P-BGA-289 Package USB

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
T10	GNDC_A	P	-	**PLL digital ground**
R10	VDDC_A	P		**PLL digital power 1.8 V**
U9	GNDBG_A	P		**USB Analogue Ground**
P10	AVDD3_A	P		**Analogue TX power 3.3 V**
T11	DP	AIO		**USB data pin +**
T12	DM	AIO		**USB data pin -**
U10	GNDBG_A	P		**USB Analogue Ground**
U11	RREF	AI		**Pull down resistor 2.7K +/- 1% ohm**
R11	AGND_A	P		**Analogue Ground**
P11	AVDD_A	P		**Analogue Power 1.8 V**
U12	VDDBG_A	P		**Analogue RX Power 3.3 V**
P12	GNDBG_A	P		**USB Analogue Ground**
U5	XTLP_usb	I		**12MHZ X'tal input (No connection when P_W2UE_PD =0)**
U6	XTLN_usb	O		**12MHZ X'tal output(No connection when P_W2UE_PD =0)**

2.1.2.10 VOIP(PCM and SPI)

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 10 P-BGA-289 Package VOIP(PCM and SPI)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
P6	FXS_DX	I	-	**PCM Data transmit**
T8	FXS_DR	O		**PCM Data receive**
R9	FXS_FSC	O		**PCM Frame control**
U8	FXS_PCLK	O		**PCM clock**
T9	FXS_RESETZ	O		**Reset**
M14	FXS_INTZ	IO		**VOIP gpio0**
T17	RELAY_CONTROLZ	IO		**Relay control by software control**
N15	FXS_SCLK	O		**SPI clock**
M15	FXS_SDO	I		**SPI data out**
N13	FXS_SDI	O		**SPI data in**
N17	FXS_CSZ	O		**SPI chip select0**
M17	FXO_CSZ	O		**SPI chip select1**
L17	FXO_INTZ	IO		**VOIP gpio1**
L16	Voipclkin	I		**Clock source for PCM clock. Please check PCM application note to see the relationship between Voipclkin and PCM clock.**

2.1.2.11 NAND FLASH

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 11 P-BGA-289 Package NAND FLASH

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
J13	nNF_WP	O	-	**Write protect**
J14	NF_RY_BY	I		**Ready/busy**
J15	nNF_WE	O		**Write enable**
H15	nNF_RE	O		**Read enable**
E17	NF_ALE	O		**Address latch enable**
C17	nNF_CE	O		**Chip enable**
E16	NF_CLE	O		**Command latch enable**

2.1.2.12 Power / Ground

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 12 P-BGA-289 Package Power / Ground

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
D6, E10, G5, J4, K5, K13, L13, M5, N6, N8, N9, N10, N11, N12	VDD	P	-	**1.8 V for digital core**
E5, E6, E7, E8, E9, F5, G13, H5, H13, J5, L5, N5, N7	DVDD	P		**3.3 V for I/O ring**
D8, F6, F7, F8, F9, F10, G6, G7, G8, G9, G10, G11, G12, H6, H7, H8, H9, H10, H11, H12, J6, J7, J8, J9, J10, J11, J12, K4, K6, K7, K8, K9, K10, K11, K12, L6, L7, L8, L9, L10, L11, L12, M6, M7, M8, M9, M10, M11, M12, P7, P8, P9	VSS_DVSS	P		**GND for digital core and IO**
R12	AGND_W2UE	P		**PLL ground**
T13	AVDD_W2UE	P		**PLL power 1.8 V**

2.1.2.13 Miscellaneous

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 13 P-BGA-289 Package Miscellaneous

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
B8	XnRESET_IN	I	-	**External power on reset input (active high)**
J17	TestReset_in	I		**For testing purpose**
J16	TestClk	I		**For testing purpose**
H17	Test_in	I		**For testing purpose**
R8	CRGPIO2	IO		**Controller by configuration registers or as RDY pin when CR24[27] =1.** This can only be used with nSMCxCS2 **T6**
R7	CRGPIO1	IO		**Controller by configuration registers**
P5	CRGPIO0	IO		**Controller by configuration registers**
E1	P_W2UE_PD	I		**12M / 25M Internal or External** 0_B , use internal 12M (XTLP_usb, XTLN_usb) and 25M (XTLP, XTLN) 1_B , use external 12M (XTLP_usb, XTLN_usb) x'tal and 25Mx'tal (XTLP, XTLN)
M13	W20MHZ_SEL	I		**Non Connect**
H16	LED_BOOTACT	O		**LED BootAct** On: power on Flash: during boot sequence

2.2 Interface Description - ADM8668F

2.2.1 WildPass Ball Diagram

2.2.1.1 352BGA

Below the ball diagram for the 352-Ball BGA version is displayed.

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y
1	PCI_AD[21]	XD[1]	XD[2]	PCI_CBE[3]	XD[7]	XD[14]	PCI_AD[29]	PCI_AD[31]	XD[9]	PCI_REQ1	SDCXDQM[0]	PCI_GNT2	NSDCRASOUT	SCLK	IDE_PCS0N	XA[11]	XA[10]	XA[9]	IDE_PDACKN	IDE_PIOWN
2	PCI_AD[17]	PCI_AD[20]	PCI_IDSEL[1]	XD[3]	XD[5]	PCI_AD[26]	PCI_AD[28]	XD[11]	P_W2UE_PD	XD[8]	PCI_GNT1	PCI_CLK33	NSDCXCS[1]	XA[13]	XA[12]	IDE_PADD[2]	IDE_PIRQ	XA[6]	XA[4]	IDE_PIDE[15]
3	PCI_FRAME	PCI_AD[16]	PCI_AD[19]	PCI_AD[23]	PCI_IDSEL[2]	PCI_AD[24]	PCI_AD[27]	XD[12]	PCI_REQ0	PCI_REQ2	NSDCWEOUT	NSDCXCS[0]	PCI_INTA2	IDE_PCS1N	IDE_PADD[1]	XA[8]	XA[5]	IDE_PDREQ	XA[2]	IDE_PIDE[14]
4	PCI_TRDY	NSMCXCS[1]	XD[0]	VDD	VDD	XD[4]	PCI_AD[25]	XD[13]	XD[10]	SDCXDQM[1]	NSDCCASOUT	PCI_INTA1	XA[14]	IDE_PPDIAG	IDE_PIORDY	IDE_PIORN	VDD	IDE_PIDE[0]	IDE_PIDE[1]	IDE_PIDE[2]
5	XA[17]	NSMCXOEN	PCI_IRDY	PCI_CBE[2]	PCI_AD[18]	PCI_AD[22]	VSS/DVSS	XD[15]	PCI_AD[30]	PCI_GNT0	PCI_RESET	VSS/DVSS	IDE_PADD[0]	XA[7]	XA[0]	XA[3]	IDE_PIDE[13]	IDE_PIDE[12]	IDE_PIDE[3]	IDE_PIDE[11]
6	PCI_PERR	PCI_STOP	PCI_DEVSEL	NSMCXCS[0]	DVDD	PCI_IDSEL[0]	DVDD	XD[6]	VSS/DVSS	DVDD	PCI_INTA0	VDD	DVDD	XA[1]	DVDD	VDD	SDCXDQM[3]	SDCXDQM[2]	XD[31]	XD[30]
7	PCI_PAR	PCI_SER	XA[19]	XA[20]	VSS/DVSS	VDD									DVDD	VDD	XD[29]	XD[28]	XD[27]	XD[26]
8	PCI_AD[15]	XA[15]	PCI_CBE[1]	XA[16]	XA[18]	DVDD									VDD	XD[16]	XD[17]	XD[18]	XD[24]	XD[25]
9	JTAG_NTRST	JTAG_TDI	PCI_AD[13]	JTAG_TMS	PCI_AD[14]	DVDD			VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS			DVDD	NSMCXCS[2]	XD[22]	XD[21]	XD[20]	XD[19]
10	PCI_AD[12]	JTAG_TCK	PCI_AD[11]	JTAG_TDO	NUART_CTS	DVDD			VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS			DVDD	CRGPIO[1]	CRGPIO[0]	XA[22]	XA[21]	XD[23]
11	PCI_AD[10]	XNRESET_IN	PCI_AD[9]	PCI_CBE[0]	NUART_DCD	DVDD			VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS			VDD	FXS_DR	FXS_DX	CRGPIO[2]	XTLN_USB	XTLP_USB
12	PCI_AD[8]	UART_TXD	PCI_AD[7]	XCRYSTAL_OUT	PCI_AD[2]	GNDA_AFE			VSS/DVSS	VSS/DVSS	VSS/DVSS	VSS/DVSS			VSS/DVSS	AVDD3_A	GNDC_A	FXS_FSC	XTLN	XTLP
13	UART_RXD	NUART_DSR	XCRYSTAL	PCI_AD[3]	VDDAH_AFE	GNDA_AFE									VDD	VDDBG_A	DP	DM	FXS_RESETZ	FXS_PCLK
14	PCI_AD[6]	PCI_AD[5]	PCI_AD[1]	PWR_REF	VDDAH_AFE	GNDA_AFE									VSS/DVSS	VSS/DVSS	REG_BASE	RREF	RPU	VDDC_A
15	WLED_LINKACK	PCI_AD[4]	TXQ_P	TXI_M	RXI_P	GNDA_AFE	GNDA_CKGEN	DVDD	VSS/DVSS	DVDD	VSS/DVSS	VDD	VDD	GNDTR	VDD	CONTROL	AVDD_W2UE	AGND_W2UE	AGND_A	GNDBG_A
16	PCI_AD[0]	PWR_SENSE2	TXQ_M	TXI_P	RXI_M	VSS/DVSS	B[2]	B[7]	GPIO[0]	TEST_IN	IDE_PIDE[7]	FXS_CSZ	RMII_RXDV	RELAY_CONTRO	VDD	VCCA20	VCCBSRG	RTX	VCCPLL	AVDD_A
17	PWR_REF2	PWR_SENSE	RXVGC	VSS/DVSS	VDDAL_CKGEN	PA_ON_A	B[4]	LEIFZ	NF_CLE	NNF_RE	L2_PHY_RSTZ	RMII_TXD1	RMII_TXEN	IDE_PIDE[6]	FXS_SCLK	RMII_RXD2	VSS/DVSS	TXN	TXP	GNDPLL
18	REF_RES	RXQ_P	RXQ_M	TXPE	ANTSEL	B[1]	TRSW	SYNDATA	NNF_CE	LED_BOOTACT	NNF_WE	RMII_TXD2	VOIPCLKIN	FXO_CSZ	FXS_SDI	RMII_RXD0	RMII_RXD3	RXN	RXP	VREF
19	RSSI	VDDAL_AFE	VCTRL	RXPE	B[0]	B[5]	PWDN	GPIO[1]	LED_FDCOL	NF_ALE	TESTRESET_IN	NNF_WP	IDE_PRESETN	IDE_PIDE[8]	RMII_TXCLK	IDE_PIDE[5]	FXS_SDO	IDE_PIDE[4]	VCCAD	GNDBSRG
20	VDDAL_AFE	VDDAH_CKGEN	CKREF	PAPE	B[3]	B[6]	SYNCLK	GPIO[2]	LED_SPEED	LED_LKACT	TESTCLK	NF_RY_BY	RMII_TXD3	RMII_TXD0	FXO_INTZ	IDE_PIDE[9]	RMII_RXCLK	IDE_PIDE[10]	RMII_RXD1	FXS_INTZ

Figure 5 BGA352 Ball Diagram

2.2.2 Ball Description by Function

WildPass balls are categorized into one of the following groups:

- **Chapter 2.1.2.1** UART Interface
- **Chapter 2.1.2.2** Memory Bus
- **Chapter 2.1.2.3** SDRAM control signals
- **Chapter 2.1.2.4** FLASH/SDRAM control signals
- **Chapter 2.1.2.5** JTAG signals
- **Chapter 2.1.2.6** WLAN signals
- **Chapter 2.1.2.7** LAN 1
- **Chapter 2.1.2.8** LAN 2
- **Chapter 2.1.2.9** USB
- **Chapter 2.2.2.10** PCI
- **Chapter 2.2.2.11** IDE
- **Chapter 2.1.2.10** VoIP (PCM and SPI)
- **Chapter 2.1.2.11** NAND Flash
- **Chapter 2.1.2.12**Power/Ground

- Chapter 2.1.2.13Miscellaneous

2.2.2.1 UART Interface

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 14 352 BGA Package UART Interface

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
E10	nUART_CTS	I	-	**Clear to send, active low**
E11	nUART_DCD	I		**Data carrier detect, active low**
B13	nUART_DSR	I		**Data send ready, active low**
A13	UART_RXD	I		**Receive serial data input**
B12	UART_TXD	O		**Transmit Serial Data Output**
C13	XCRYSTAL	I		**UAST Crystal** UART X'tal in 3.6864MHZ ~ 73MHZ
D12	XCRYSTAL_OUT	O		**UART X'tal output**

2.2.2.2 Memory Bus

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 15 352 BGA Package Memory Bus

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
W6	XD31	IO	-	**Data Bus** Data bus[31] for SDRAM, FLASH
Y6	XD30	IO		**Data Bus** Data bus[30] for SDRAM, FLASH
U7	XD29	IO		**Data Bus** Data bus[29] for SDRAM, FLASH

Table 15 352 BGA Package Memory Bus (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
V7	XD28	IO	-	**Data Bus** Data bus[28] for SDRAM, FLASH
W7	XD27	IO		**Data Bus** Data bus[27] for SDRAM, FLASH
Y7	XD26	IO		**Data Bus** Data bus[26] for SDRAM, FLASH
Y8	XD25	IO		**Data Bus** Data bus[25] for SDRAM, FLASH
W8	XD24	IO		**Data Bus** Data bus[24] for SDRAM, FLASH
Y10	XD23	IO		**Data Bus** Data bus[23] for SDRAM, FLASH
U9	XD22	IO		**Data Bus** Data bus[22] for SDRAM, FLASH
V9	XD21	IO		**Data Bus** Data bus[21] for SDRAM, FLASH
W9	XD20	IO		**Data Bus** Data bus[20] for SDRAM, FLASH
Y9	XD19	IO		**Data Bus** Data bus[19] for SDRAM, FLASH
V8	XD18	IO		**Data Bus** Data bus[18] for SDRAM, FLASH
U8	XD17	IO		**Data Bus** Data bus[17] for SDRAM, FLASH
T8	XD16	IO		**Data Bus** Data bus[16] for SDRAM, FLASH
H5	XD15	IO		**Data Bus** Data bus[15] for SDRAM, FLASH
F1	XD14	IO		**Data Bus** Data bus[14] for SDRAM, FLASH
H4	XD13	IO		**Data Bus** Data bus[13] for SDRAM, FLASH
H3	XD12	IO		**Data Bus** Data bus[12] for SDRAM, FLASH
H2	XD11	IO		**Data Bus** Data bus[11] for SDRAM, FLASH
J4	XD10	IO		**Data Bus** Data bus[10] for SDRAM, FLASH
J1	XD9	IO		**Data Bus** Data bus[9] for SDRAM, FLASH
K2	XD8	IO		**Data Bus** Data bus[8] for SDRAM, FLASH
E1	XD7	IO		**Data Bus** Data bus[7] for SDRAM, FLASH

Table 15 352 BGA Package Memory Bus (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
H6	XD6	IO	-	**Data Bus** Data bus[6] for SDRAM, FLASH
E2	XD5	IO		**Data Bus** Data bus[5] for SDRAM, FLASH
F4	XD4	IO		**Data Bus** Data bus[4] for SDRAM, FLASH
D2	XD3	IO		**Data Bus** Data bus[3] for SDRAM, FLASH
C1	XD2	IO		**Data Bus** Data bus[2] for SDRAM, FLASH
B1	XD1	IO		**Data Bus** Data bus[1] for SDRAM, FLASH
C4	XD0	IO		**Data Bus** Data bus[0] for SDRAM, FLASH
V10	XA22	IO		**Data Bus for SDRAM and Flash** SDRAM address is XA[14:0].FLASH, SRAM address is XA[22:0]Please reference the Appendix for Reset information. *Note: WildPass has internal address shifting function, i.e. the XA0 is byte addressing when FLASH is byte width, the XA0 is word addressing (16-bit) when FLASH is word width, the XA0 is double word addressing when FLASH is 32 bits.GPIO[2] will be configured as nSIROUT (output), and GPIO[1] will be SIRIN (input) by pull-up reset latched pin XA[20]*
W10	XA21	IO		
D7	XA20	IO		
C7	XA19	IO		
E8	XA18	IO		
A5	XA17	IO		
D8	XA16	IO		
B8	XA15	IO		
N4	XA14	IO		
P2	XA13	IO		
R2	XA12	IO		
T1	XA11	IO		
U1	XA10	IO		
V1	XA9	IO		
T3	XA8	IO		
P5	XA7	IO		
V2	XA6	IO		
U3	XA5	IO		
W2	XA4	IO		
T5	XA3	IO		
W3	XA2	IO		
P6	XA1	IO		
R5	XA0	IO		

2.2.2.3 SDRAM Control Signals

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 16 352 BGA Package SDRAM Control Signals

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
P1	SCLK	O	-	**SDRAM clock**
M3	nSDCxCS0	O		**Bank Size** Minimum bank0 size = 64MB.Maximum bank0 size = 128MB.
N2	nSDCxCS1	O		**Address Rage** Address range continues from bank0
N1	nSDCRASout	O		**Address Strobe** SDRAM raw address strobe, active low
L4	nSDCCASout	O		**Col Address Strobe** SDRAM, column address strobe, active low
U6	SDCxDQM3	O		**SDRAM, byte data mask** Data bus width 8 : [0] SDRAM_DQMData bus width 16 : [1:0] SDRAM_DQM Data bus width 32: [3:0] SDRAM_DQM
V6	SDCxDQM2			
K4	SDCxDQM1			
L1	SDCxDQM0			
L3	nSDCWEout	O		**Write Enable Active Low** SDRAM, write enable, active low

2.2.2.4 FLASH/SRAM Control Signals

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 17 352 BGA Package FLASH/SRAM Control Signals

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
T9	nSMCxCS2	O	-	**Chip Select Active Low 1** Chip select for external FLASH/SRAM, active low. Address range is from 1080_0000 to 10ff_ffff when XA[12] reset latch = 0. Address range starts from 0000_0000 when XA[12] reset latch =1
B4	nSMCxCS1	O		**Chip Select Active Low 2** Chip select for external FLASH/SRAM, active low. Address range is from1000_0000 to 107f_ffff
D6	nSMCxCS0	O		**Chip Select External Flash** Chip select for external FLASH, active low.Address range starts from $1FC0_H$_0000
B5	nSMCxOEN	O		**Output Enable** Output enable, active low.
L3	SMC_WEZ	O		**Write enable, active low. (multiplexed with nSDCWEout), dedicated for 16/32-bit FLASH**
U6	SMC_BLS3	O		**Bank Select3 Active Low 3** Bank select3, active low (multiplexed with SDCxDQM [3]) for 8-bit FLASH.
V6	SMC_BLS2	O		**Bank Select3 Active Low 2** Bank select3, active low (multiplexed with SDCxDQM [2]) for 8-bit FLASH.
K4	SMC_BLS1	O		**Bank Select3 Active Low 1** Bank select3, active low (multiplexed with SDCxDQM [1]) for 8-bit FLASH.
L1	SMC_BLS0	O		**Bank Select3 Active Low 0** Bank select3, active low (multiplexed with SDCxDQM [0]) for 8-bit FLASH.

2.2.2.5 JTAG Signals

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 18 352 BGA Package JTAG Signals

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
B10	JTAG_TCK	I	-	**JTAG test clock**
D9	JTAG_TMS	I		**JTAG test mode select**
D10	JTAG_TDO	O		**Test data out**
B9	JTAG_TDI	I		**Test data in**
A9	JTAG_ntRST	I		**Asynchronous reset (active low)**

2.2.2.6 WLAN 802.11g Signals

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 19 352 BGA Package WLAN Signals

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
H18	SYNDATA	IO	-	**Data in out for RF 3-wire interface**
G20	SYNCLK	O		**Clock out for RF 3-wire interface**
H17	LEIFZ	O		**Synthesizer interface select**
G19	PWDN	O		**Power Down** Power down or MAC sleep signal output, active level set by WCSR18.PD.
G18	TRSW	O		**TX/RX switch select**
H16	B7	IO		**RF Control Bus**
F20	B6	IO		
F19	B5	IO		
G17	B4	IO		
E20	B3	IO		
G16	B2	IO		
F18	B1	IO		
E19	B0	IO		**Mixed with RXHP**
D20	PAPE	O		**PA power enable**
F17	PA_ON_A	O		**PA power enable for 11a**
E18	ANTSEL	O		**Antenna select**
D19	RXPE	O		**RF RX enable**
D18	TXPE	O		**RF TX enable**
G15	GNDA_CKGEN	P		**Regulator ground**
C20	CKREF	I		**40MHZ input**
E17	VDDAL_CKGEN	P		**PLL 1.8 V**
C19	VCTRL	AO		**Regulator control (spare purpose)**
B20	VDDAH_CKGEN	P		**Regulator power 3.3 V**
C17	RXVGC	AO		**Analogue receive variable gain control output: 1.2 V to 2.0 V**
A20, B19	VDDAL_AFE	P		**AFE analogue power 1.8 V**
E15	RXI_P	AI		**RX I channel analogue input +**
E16	RXI_M	AI		**RX I channel analogue input -**
C18	RXQ_M	AI		**RX Q channel analogue input +**
B18	RXQ_P	AI		**RX Q channel analogue input -**
A19	RSSI	AI		**Receiver signal strength indicator analogue input**
A18	REF_RES	AI		**External 1% accuracy 11.5K resistor pin**
E13, E14	VDDAH_AFE	P		**AFE analogue power 3.3 V**
D16	TXI_P	AO		**TX I channel analogue output +**
D15	TXI_M	AO		**TX I channel analogue output -**
C16	TXQ_M	AO		**TX Q channel analogue output +**
C15	TXQ_P	AO		**TX IQchannel analogue output -**

Table 19 352 BGA Package WLAN Signals (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
B17	PWR_SENSE	AI	-	**TSSI sense pin 1**
D14	PWR_REF	AI		**TSSI reference pin 1**
B16	PWR_SENSE2	AI		**TSSI sense pin 2 for 11a**
A17	PWR_REF2	AI		**TSSI reference pin 2 for 11a**
F12, F13, F14, F15	GNDA_AFE	P		**GND for AFE**
H20	GPIO2	IO		**Wireless driver controlled GPIO2**
H19	GPIO1	IO		**Wireless driver controlled GPIO1**
J16	GPIO0	IO		**Wireless driver controlled GPIO0**
A15	WLED_LINKACK	O		**LinkAct** On: associatedOff: activities

2.2.2.7 Port 1

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 20 352 BGA Package Port 1

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
W16	VCCPLL	P	-	**Analogue power 1.8 V for PLL**
Y17	GNDPLL	P		**Ground for PLL**
T15	CONTROL	A		**FET control for 3.3 V to 1.8 V regulator**
Y18	VREF	P		**Analogue power 1.8 V**
Y19	GNDBSRG	P		**Analogue ground**
V16	RTX	AI		**TX resister * ohm**
U16	VCCBSRG	P		**Analogue power 3.3 V for bias block**
T16	VCCA20	P		**Analogue power 1.8 V**
W17	TXP	A		**TX +**
V17	TXN	A		**TX -**
P15	GNDTR	P		**Analogue ground**
W18	RXP	A		**RX +**
V18	RXN	A		**RX -**
W19	VCCAD	P		**Analogue power 3.3 V for RX line driver**
Y12	XTLP	I		**25MHZ X'tal input (No connection when P_W2UE_PD =0)**
W12	XTLN	O		**25MHZ X'tal output (No connection when P_W2UE_PD =0)**
K20	LED_LKACT	O		**LED LinkAct** Flash: activities On: Link
J20	LED_SPEED	O		**LED Speed** On: 100MHZ Off: 10MHZ
J19	LED_FDCOL	O		**LED Duplex** On: full duplexOff: half duplex

2.2.2.8 Port 2

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 21 352 BGA Package Port 2

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
U18	RMII_RXD3	I	-	**RXD [3]**
T17	RMII_RXD2	I		**RXD [2]**
W20	RMII_RXD1	I		**RXD [1]**
T18	RMII_RXD0	I		**RXD [0]**
N16	RMII_RXDV	I		**RXDV**
U20	RMII_RXCLK	I		**RMII Rx Clock** Output when Reverse-MII mode Input when MII mode
R19	RMII_TXCLK	I		**RMII Tx Clock** Output when Reverse-MII mode Input when MII mode
N17	RMII_TXEN	O		**TXEN**
N20	RMII_TXD3	O		**TXD [3]**
M18	RMII_TXD2	O		**TXD [2]**
M17	RMII_TXD1	O		**TXD [1]**
P20	RMII_TXD0	O		**TXD [0]**
L17	L2_PHY_RSTZ	O		**Internal power on reset output**

2.2.2.9 USB

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 22 352 BGA Package USB

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
U12	GNDC_A	P	-	**PLL digital ground**
Y14	VDDC_A	P		**PLL digital power 1.8 V**
W14	GNDBG_A	P		**USB Analogue Ground**
T12	AVDD3_A	P		**Analogue TX power 3.3 V**
U13	DP	AIO		**USB data pin +**
V13	DM	AIO		**USB data pin -**
Y15	GNDBG_A	P		**USB Analogue Ground**
V14	RREF	AI		Pull down resistor 2.7K +/- 1% ohm
W15	AGND_A	P		**Analogue Ground**
Y16	AVDD_A	P		**Analogue Power 1.8 V**
T13	VDDBG_A	P		**Analogue RX Power 3.3 V**
U14	GNDBG_A	P		**USB Analogue Ground**
Y11	XTLP_usb	I		**12MHZ X'tal input (No connection when P_W2UE_PD =0)**
W11	XTLN_usb	O		**12MHZ X'tal output(No connection when P_W2UE_PD =0)**

2.2.2.10 PCI (only in 352BGA)

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 23 352 BGA Package PCI (only in 352BGA)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
H1	PCI_AD31	IO	-	**PCI address bus [31]**
J5	PCI_AD30	IO		**PCI address bus [30]**
G1	PCI_AD29	IO		**PCI address bus [29]**
G2	PCI_AD28	IO		**PCI address bus [28]**
G3	PCI_AD27	IO		**PCI address bus [27]**
F2	PCI_AD26	IO		**PCI address bus [26]**
G4	PCI_AD25	IO		**PCI address bus [25]**
F3	PCI_AD24	IO		**PCI address bus [24]**
D3	PCI_AD23	IO		**PCI address bus [23]**
F5	PCI_AD22	IO		**PCI address bus [22]**
A1	PCI_AD21	IO		**PCI address bus [21]**
B2	PCI_AD20	IO		**PCI address bus [20]**
C3	PCI_AD19	IO		**PCI address bus [19]**
E5	PCI_AD18	IO		**PCI address bus [18]**
A2	PCI_AD17	IO		**PCI address bus [17]**
B3	PCI_AD16	IO		**PCI address bus [16]**
A8	PCI_AD15	IO		**PCI address bus [15]**
E9	PCI_AD14	IO		**PCI address bus [14]**
C9	PCI_AD13	IO		**PCI address bus [13]**
A10	PCI_AD12	IO		**PCI address bus [12]**
C10	PCI_AD11	IO		**PCI address bus [11]**
A11	PCI_AD10	IO		**PCI address bus [10]**
C11	PCI_AD9	IO		**PCI address bus [9]**
A12	PCI_AD8	IO		**PCI address bus [8]**
C12	PCI_AD7	IO		**PCI address bus [7]**
A14	PCI_AD6	IO		**PCI address bus [6]**
B14	PCI_AD5	IO		**PCI address bus [5]**
B15	PCI_AD4	IO		**PCI address bus [4]**
D13	PCI_AD3	IO		**PCI address bus [3]**
E12	PCI_AD2	IO		**PCI address bus [2]**
C14	PCI_AD1	IO		**PCI address bus [1]**
A16	PCI_AD0	IO		**PCI address bus [0]**
E3	PCI_IDSEL2	O		**ID select**
C2	PCI_IDSEL1	O		
F6	PCI_IDSEL0	O		

Table 23 352 BGA Package PCI (only in 352BGA) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
D1	PCI_CBE3	IO	-	**Command byte enable**
D5	PCI_CBE2	IO		
C8	PCI_CBE1	IO		
D11	PCI_CBE0	IO		
K3	PCI_REQ2	I		**Request2**
K1	PCI_REQ1	I		**Request1**
J3	PCI_REQ0	I		**Request0**
M1	PCI_GNT2	O		**Grant2**
L2	PCI_GNT1	O		**Grant1**
K5	PCI_GNT0	O		**Grant0**
M2	PCI_CLK33	O		**31.25 MHZ clock**
L5	PCI_RESET	O		**Reset**
N3	PCI_INTA2	I		**Interrupt**
M4	PCI_INTA1	I		
L6	PCI_INTA0	I		
A6	PCI_PERR	IO		**Parity check**
B6	PCI_STOP	IO		**Stop**
C6	PCI_DEVSEL	IO		**Device select**
A4	PCI_TRDY	IO		**Target ready**
A3	PCI_FRAME	IO		**Frame**
A7	PCI_PAR	IO		**Parity error**
B7	PCI_SER	IO		**System error**
C5	PCI_IRDY	IO		**Initiator ready**

2.2.2.11 IDE (only in 352BGA)

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 24 352 BGA Package IDE (only in 352BGA)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
R1	IDE_PCS0n	O	-	**IDE select data /command (low active)**
P3	IDE_PCS1n	O		**IDE select data /command (low active)**
T2	IDE_PADD2	O		**Address**
R3	IDE_PADD1	O		**Address**
N5	IDE_PADD0	O		**Address**
P4	IDE_PPDIAG	I		**Passed diagnostics/Cable assembly type identifier**
U2	IDE_PIRQ	I		**Interrupt**
W1	IDE_PDACKn	O		**DMA transfer acknowledge**
R4	IDE_PIORDY	I		**Ready, allow IDE device to extend I/O cycle**
T4	IDE_PIORn	O		**Read strobe**
Y1	IDE_PIOWn	O		**Write strobe**
V3	IDE_PDREQ	I		**DMA transfer request**
Y2	IDE_PIDE15	IO		**IDE data**
Y3	IDE_PIDE14			
U5	IDE_PIDE13			
V5	IDE_PIDE12			
Y5	IDE_PIDE11			
V20	IDE_PIDE10			
T20	IDE_PIDE9			
P19	IDE_PIDE8			
L16	IDE_PIDE7			
P17	IDE_PIDE6			
T19	IDE_PIDE5			
V19	IDE_PIDE4			
W5	IDE_PIDE3			
Y4	IDE_PIDE2			
W4	IDE_PIDE1			
V4	IDE_PIDE0			
N19	IDE_PRESETn	O		**Reset (low active)**

2.2.2.12 VOIP (PCM and SPI)

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 25 352 BGA Package VOIP (PCM and SPI)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
U11	FXS_DX	I	-	**PCM Data transmit**
T11	FXS_DR	O		**PCM Data receive**
V12	FXS_FSC	O		**PCM Frame control**
Y13	FXS_PCLK	O		**PCM clock**
W13	FXS_RESETZ	O		**Reset**
Y20	FXS_INTZ	IO		**VOIP gpio0**
P16	RELAY_CONTROLZ	IO		**Relay control by software control**
R17	FXS_SCLK	O		**SPI clock**
U19	FXS_SDO	I		**SPI data out**
R18	FXS_SDI	O		**SPI data in**
M16	FXS_CSZ	O		**SPI chip select0**
P18	FXO_CSZ	O		**SPI chip select1**
R20	FXO_INTZ	IO		**VOIP gpio1**
N18	Voipclkin	I		**Clock source for PCM clock. Please check PCM application note to see the relationship between Voipclkin and PCM clock.**

2.2.2.13 NAND FLASH

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 26 352 BGA Package NAND FLASH

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
M19	nNF_WP	O	-	**Write protect**
M20	NF_RY_BY	I		**Ready/busy**
L18	nNF_WE	O		**Write enable**
K17	nNF_RE	O		**Read enable**
K19	NF_ALE	O		**Address latch enable**
J18	nNF_CE	O		**Chip enable**
J17	NF_CLE	O		**Command latch enable**

2.2.2.14 Power / Ground

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 27 352 BGA Package Power / Ground

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
D4, E4, F7, M6, M15, N15, R8, R10, R11, R13, R15, R16, T6, T7, U4	VDD	P	-	**1.8 V for digital core**
E6, F8, F9, F10, F11, G6, H15, K6, K15, N6, R6, R7, R9	DVDD	P		**3.3 V for I/O ring**
D17, E7, F16, G5, J6, J9, J10, J11, J12, J15, K9, K10, K11, K12, L9, L10, L11, L12, L15, M5, M9, M10, M11, M12, R12, R14, T14, U17	VSS_DVSS	P		**GND for digital core and IO**
V15	AGND_W2UE	P		**PLL ground**
U15	AVDD_W2UE	P		**PLL power 1.8 V**

2.2.2.15 Miscellaneous

Note: Buffer Types are not relevent for the WildPass package and therefore all Buffer columns are blank.

Table 28 352BGA Package Miscellaneous

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
B11	XnRESET_IN	I	-	**External power on reset input (active high)**
L19	TestReset_in	I		**For testing purpose**
L20	TestClk	I		**For testing purpose**
K16	Test_in	I		**For testing purpose**
V11	CRGPIO2	IO		**Controller by configuration registers** RDY pin when CR24[27] =1. This can only be used with nSMCxCS2 **T9**.
T10	CRGPIO1	IO		**Controller by configuration registers**
U10	CRGPIO0	IO		**Controller by configuration registers**
J2	P_W2UE_PD	I		**12M / 25M Internal or External** 0_B , use internal 12M (XTLP_usb, XTLN_usb) and 25M (XTLP, XTLN) 1_B , use external 12M (XTLP_usb, XTLN_usb) x'tal and 25Mx'tal (XTLP, XTLN)
K18	LED_BOOTACT	O		**LED BootAct** On: power on Flash: during boot sequence

Note: W20MHZ_SEL is NC (Non Connect).

2.3 Memory Map

The memory map for WildPass is shown below.

SRAM_CS2Z/SDRAM_CS0Z share the same address range and is selected by power up reset latched XA [12].

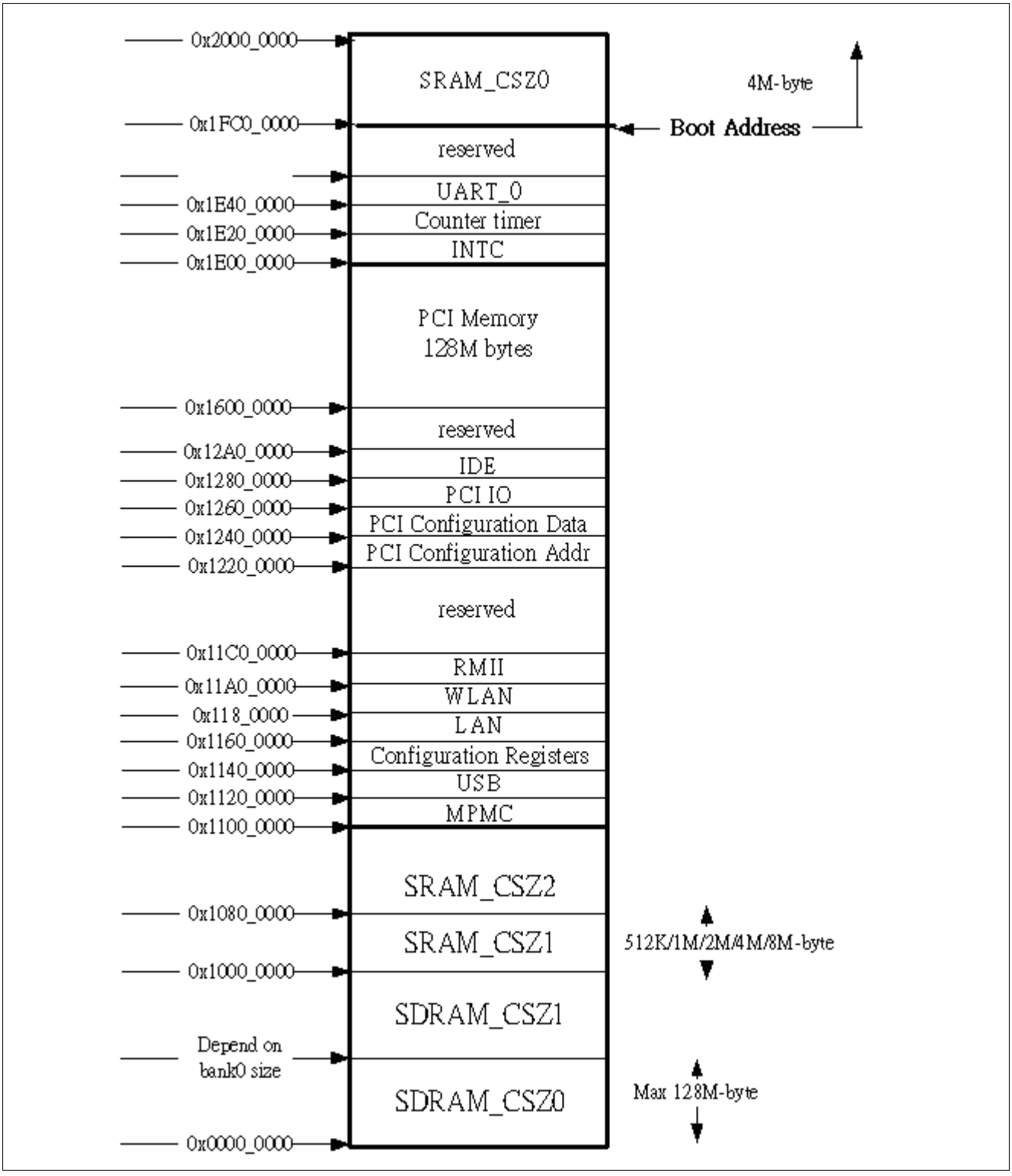

Figure 6 Memory Map

3 Function Description

3.1 IEEE 802.11 MAC+BBP

This hardware based wireless 802.11a/b/g MAC and BBP only needs very limited CPU computing power to process wireless operations. Apart from the basic IEEE 802.11a/b/g functions, 802.11i for security, 802.11e for QoS and 802.11h for radar detection are also embedded. In the transmit path, the CPU only needs to provide necessary parameters to the MAC and BBP to do related tasks such as rate selection, de-fragmentation, encryption, authentication and QoS channel access, etc. In the receive path, MAC and BBP will perform on-the-fly packet decryption and authentication verification to off load the CPU's computing power.

The MAC/BBP block diagram is shown below. The Buffer Manager provides a DMA service to move data between wireless and host memories. The Protocol Engine deals with the 802.11 protocols. The BBP block handles different data rates in DSSS and OFDM. The 5G and 2.4G RF are supported by the BBP block.

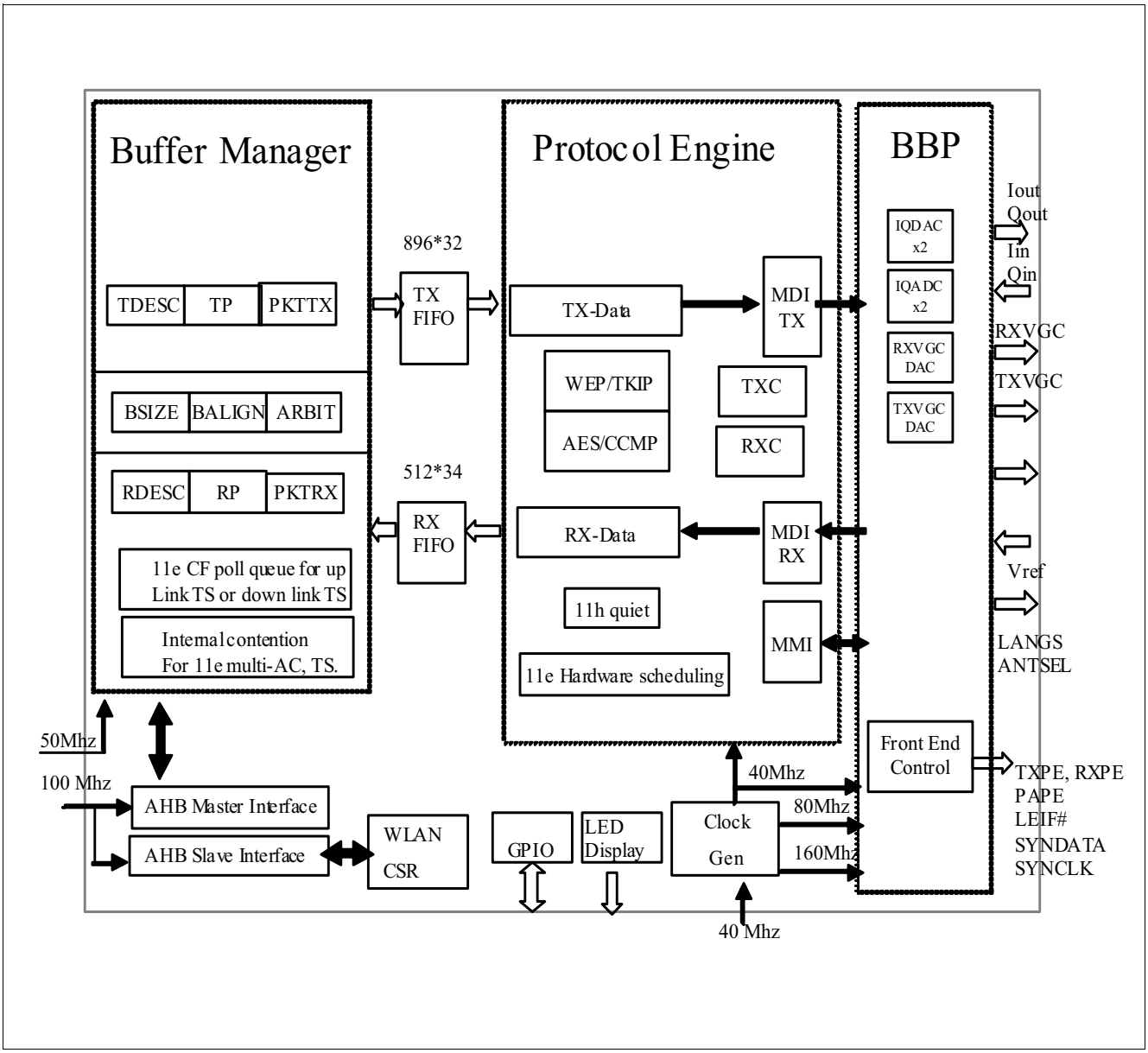

Figure 7 IEEE802.11 MAC + BBP Block Diagram

The IEEE 802.3 a/b/g MAC features include:

- AP/STA/STA converter/AP repeater operation
- Infrastructure, Ad-hoc under DCF
- RTS/CTS generation, fragmentation, beacon monitor/loss detection/generation
- CTS-to-self protection mechanism
- Probe response/Beacon generation by H/W or S/W
- Auto 2, high or low, rate switching
- RX DA address filtering (multicast) with 64 entries
- TIM field decoding at Beacon frame reception
- Short slot time
- Packet burst with programmable packet number
- Front end chip power sequence control
- Power save mode support.

The IEEE 802.11i features include:

- TKIP hardware fully supports 802.11i
- AES /CCMP fully support
- Beacon / probe response supports RSN information element
- TKIP 48bit Sequence Counter supports for each MPDU for anti-replay purpose
- TKIP MIC value hardware calculation for transmission
- TKIP MIC value hardware verification for receive
- WPA, WPA2 support
- KEY number: 4 Shared KEYs and 64 individual KEYs are stored in hardware MAC for fully hardware WEP/TKIP/AES support. Software can have more keys stored in software driver.
- Key length: 40 and 104 bit for RC4/WEP. 128 bit for TKIP, 128 bit for AES/CCMP

The IEEE 802.11e QOS features include:

- HCF contention-based channel access (EDCA)
  - Programmable AIFS for each AC
  - Programmable contention window for each AC
  - Hardware admission control
  - Hardware TXOP does not exceed TBTT
  - Last MPDU can still be transmitted when TXOP expires
  - 4 AC hardware queues supported

The IEEE 802.11h features include:

- Quiet support for one shot or periodic
- ISM (In Service Monitoring) support
- Basic, CCA, and RPI histogram support

The BBP (Base Band Processor) features include:

- DBPSK, DQPSK, OFDM modulation scheme
- DSSS/CCK: 1, 2, 5.5, 11Mbits/s
- DFDM: 6, 9, 12, 18, 24, 36, 48, 54Mbits/s
- Supports long and short preamble
- RX AGC control
- TX Power Control, PABias control, 6bits DAC
- Integrates TX RX IQ ADC/DAC, 10bits/60MHz
- Antenna Diversity
- Integrates RSSI, TSSI ADC, 6bits
- Integrates RXVGC DAC, 7bits

The 3 wire RF interface supports:

- Infineon Lucky Warp (PEF8820 dual-band WLAN RF transceiver)

- AIROHA AL2230

3.2 USB Host Controller and Transceiver

The USB2.0 host controller is a DMA master that can directly move data between system memory and a USB device.

The various blocks in the USB2.0 host controller are shown below in **Figure 8**.

The DMA Engine Block is responsible for moving all of the data to be transferred over the USB between the USB2.0 host core and buffers in system memory.

The Protocol Engine parses all the USB tokens and generates the response packets. It is responsible for all error checking, check field generation, formatting all the handshake, ping and data response packets on the bus and for any signals that must be generated based on a USB based timeframe. In host mode, the Protocol engine also generates all of the token packets required by the USB protocol. The Protocol engine contains several sub-functions:

1. The token state machines track all of the tokens on the bus and filter the traffic based on the address and endpoint information in the token. In host mode, these state machines also generate the tokens required for data transfer and bus control.
2. The CRC5 and CRC16 CRC generator/checker circuits check and generate the CRC check fields for the token and data packets.
3. The data and handshake state machines generate any responses required on the USB and move the packet data through the dual port memory FIFOs to the DMA controller block.
4. The Interval timers provide timing strobes that identify important bus timing events: the bus timeout interval, the microframe interval, the start of frame interval, and the bus reset, resume, and suspend intervals.
5. Reports all transfer status to the DMA engine. The Register Based FIFO Controller includes two register based buffers providing elasticity between the DMA controller and the transaction translator. The buffers include the FIFO control logic and the FIFO buffers. Because of their small size, the buffers are implemented as registers. The Transaction Translator supports full and low speed USB host functions in a USB 2.0 environment. This block moves the transaction translator function normally associated with a USB 2.0 high speed hub and is inside the host controller. The internal transaction translator takes split transaction requests addressed to Hub 0 and issues the corresponding full and low speed transactions on directly connected full or low speed ports. The Port Controller block interfaces to our embedded USB2.0 transceiver.

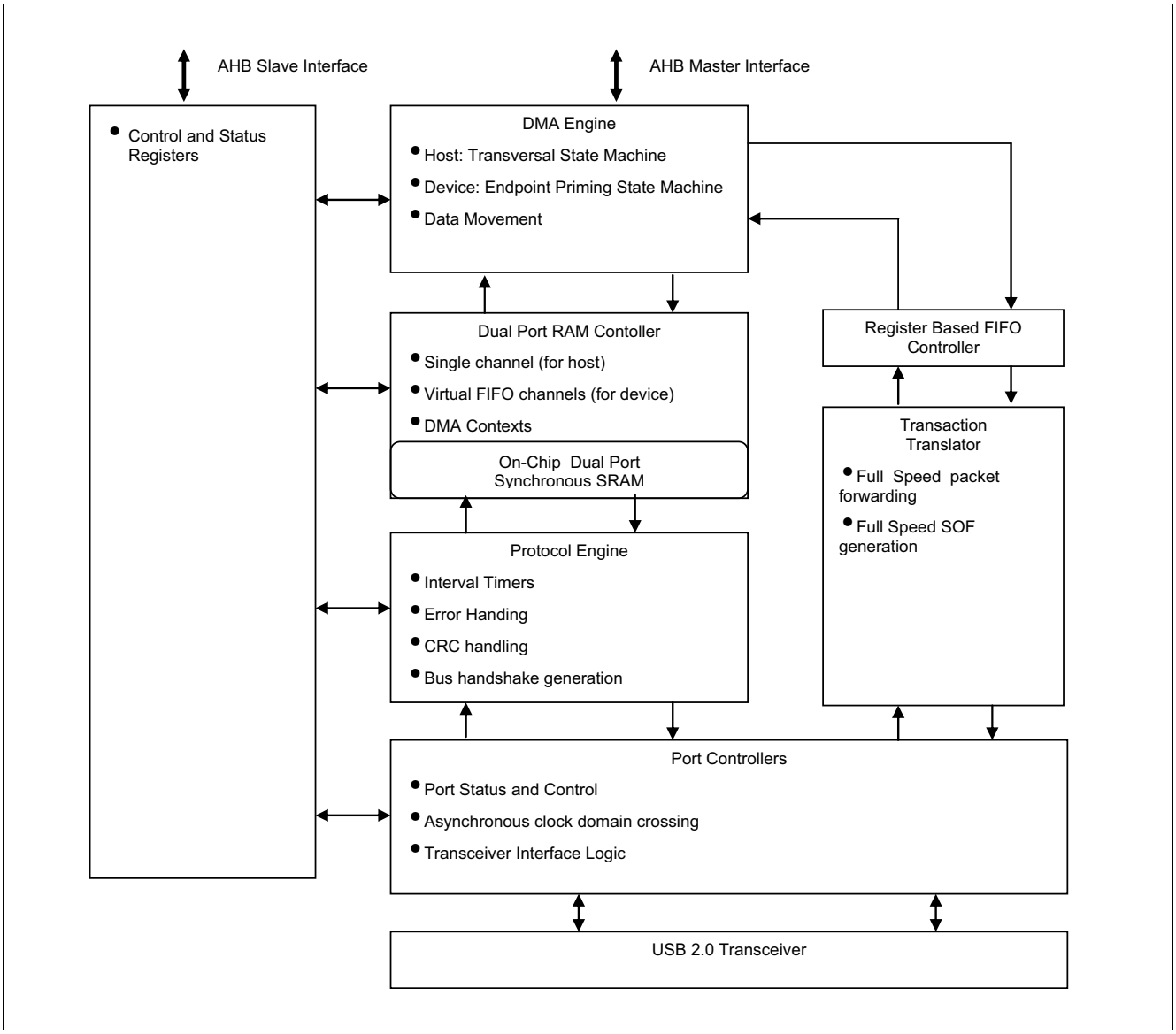

Figure 8 USB Host Controller and Transceiver

3.3 IDE Controller

This IDE host controller is an ATA/ATAPI-7 host implementation. The ATA (AT Attachment) interface, also known as IDE (Integrated Drive Electronics) interface, provides a simple interface to low cost non-volatile memories like hard-disk drives, DVD players, CD-ROM players/writers, CompactFlash and PC-Card devices.

The IDE host controller provides an interface between the CPU and up to two ATA/ATAPI devices.

An overview of each block is shown below.

The Host I/F block implements the CPU interface function, including one AHB master and one AHB slave. The DMA block is a scatter-gather descriptor-based master engine. Its operation is controlled by the ATA Bus Master Command register. The DMA engine automatically accesses (read or write) data blocks in main memory, which is described with PRD (Physical Region Descriptor). The IDE I/F block implements PIO, multiword DMA, and ultra DMA ATA interface functions. It is compliant to ATA/ATAPI-7. The timing control block implements all the needs of ATA access timing control. Many different kinds of timing controls are needed to support a variety of ATA modes. The IDE controller operation is controlled by configuration of the CSR. Software can read the controller status in the CSR. There is also a CSR-based PIO access mode.

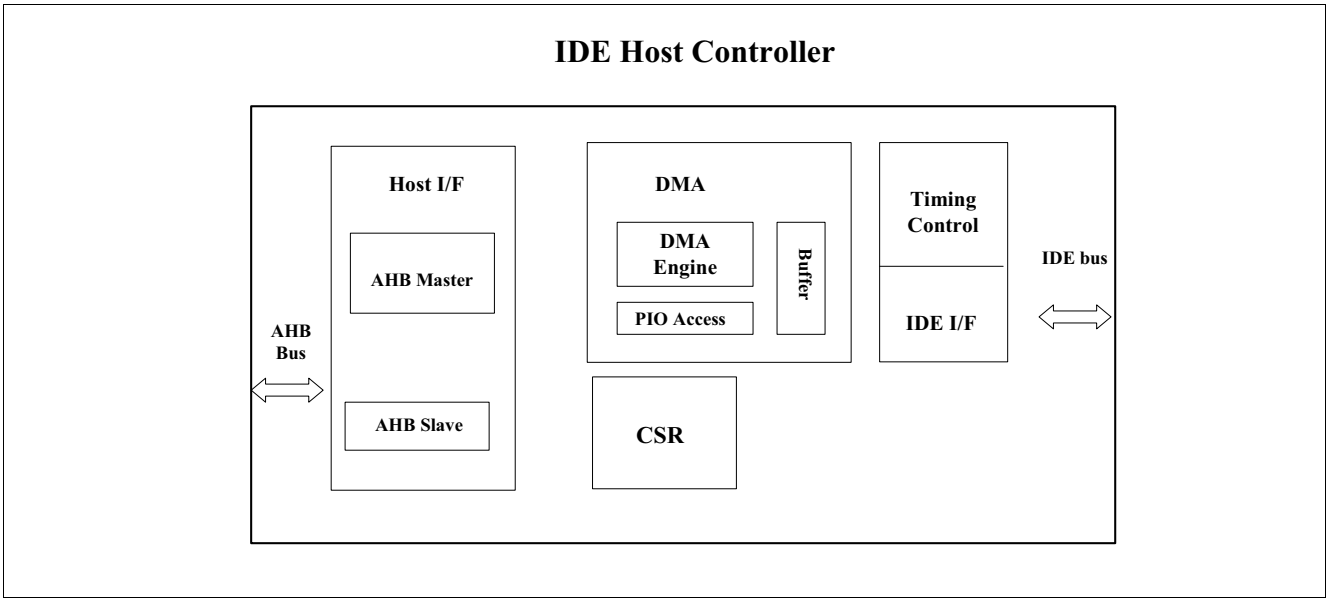

Figure 9 IDE Host Controller

The IDE controller includes the following features:

- Programmable I/O modes 0, 1, 2, 3 & 4
- Multi-word DMA modes 0, 1 & 2
- Ultra ATA-33, -66, -100 and -133 modes 0, 1, 2, 3, 4, 5 & 6
- Scatter-gather descriptor-based DMA engine
- Synchronous DMA interface for data transfer
- Supports primary and secondary channels with independent buffers
- Supports post write and read pre-fetch
- Supports DMA-assisted PIO access
- 32-bit AHB host interface

3.4 Hardware NAT Engine

WildPass supports 2 802.3 MACs, one is Port1 with embedded 10/100 PHY, the other is Port2 without 10/100 PHY. These two ports can be configurable to LAN or WAN ports depending on the system requirements. Pure hardware NAT for bi-direction 64 byte packet bridging (concurrently from LAN to WAN and from WAN to LAN) with minimum IFG is reachable. The reverse MII interface is capable of connecting to a switch for more LAN port applications. Port2 can also perform hardware NAT individually for LAN, WAN packet transformation via a VLAN partitioned switch.

Hardware NAT engine includes the following features:

- Supports up to 128 entries for Hardware NAT engine to replace some elements inside packets to achieve NAT function. For each entry, the following features are supported:
  - IP filter or NAT transform
  - TCP or UDP
  - PPPoE insert/remove
  - NAT hit/non-hit
  - Fast path can be turned off for CPU monitoring even when NAT is performed
  - Supports up to 4 entries to set rules for H/W to identify where the starting address of IP header is. Ethernet packets are automatically detected by the H/W NAT engine
  - Supports up to 4 entries to set rules to bypass the hardware NAT process
  - Automatically detects VLAN or non-VLAN mode without any register setting

  - LAN/WAN port is configurable
- Statistics
  - NAT queue forwarded packet byte count
  - NAT queue forwarded packet count
- Per packet Indication for CPU's reference:
  - VLAN processed
  - NAT transform hit
  - IP filter hit
  - Layer-3/4 CRC error
- Configurable NAT/Normal queue transmit arbitration ratio

3.5 Port 1

WildPass provides one 10/100 PHY using Port1. The 100Base-TX section of the device implements the following functional blocks:

- 100Base-X physical coding sub-layer (PCS)
- 100Base-X physical medium attachment (PMA)
- 100Base-TX physical medium dependent (PMD)

The 10Base-TX section of the device implements the following functional blocks:

- 10Base-T physical layer signaling (PLS)
- 10Base-T physical medium attachment (PMA)

The 100Base-X and 10Base-T sections share the following functional blocks:

- Clock synthesizer module
- MII Registers
- IEEE 802.3u auto negotiation

The interfaces used for communication between PHY block and switch core is MII interface. Auto MDIX function is supported.

3.6 Port2

The reverse-MII interface is provided by Port2 to connect a switch for more LAN port applications. MII or reverse-MII can be programmed by reset latched pin XA[9]. The full-duplex mode between WildPass and the switch is shown below.

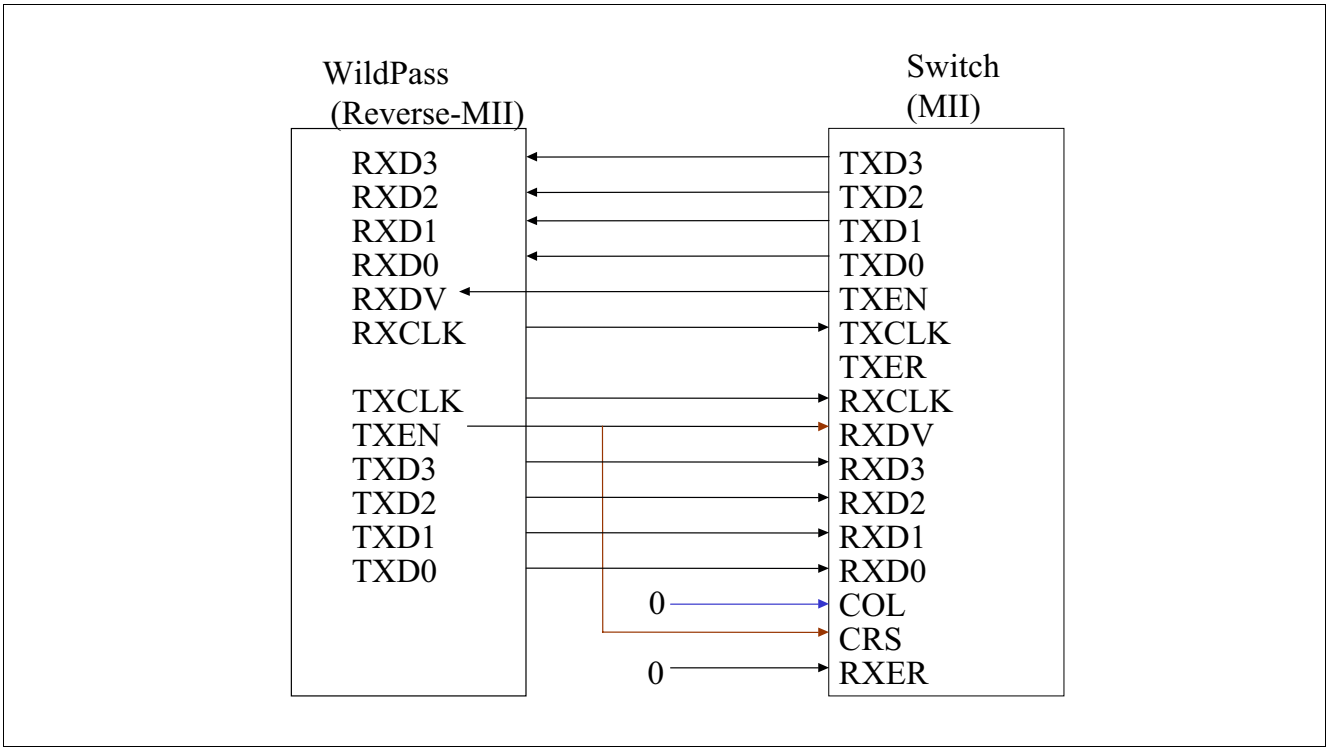

Figure 10 Reverse MII Connection

3.7 PCI Bridge

The following features are implemented as part of the PCI Bridge:

- PCI bridge supports 3 PCI devices
- PCI spec 2.2 compliant
- Downstream access allows CPU to access PCI devices
- Upstream access allows PCI devices to access host memory
- 16 double word burst is allowed
- PCI type 0, type 1 configuration access
- Supports target retry, disconnect, abort and wait state insertion
- Parity generation and parity detection

3.8 Memory Controller

The Memory Controller provides SRAM (or flash memory) and SDRAM accesses. 3 SRAM (or flash memory) chip selects are provided. 2 SDRAM chip selects are provided. Please note that SRAM chip select 2 can use addresses from 0000_0000 by hardware pin XA[12] pull up setting while chip is power on. The detail is shown in the memory map in **Figure 6 "Memory Map" on Page 45**. SRAM's write enable (SMC_WEZ) is shared with SDRAM write enable (nSDCWEout), and SRAM's byte/line selects (SMC_BLS) are shared with SDRAM's SDCxDQM.

The addressing range of SDRAM bank 0 is from a minimum 64M bytes to maximum 128M bytes. The addressing range of SDRAM bank 1 continues from the end of bank 0.

3.9 NAND Flash Interface

Please set reset latched value of XA[21] =1 and XA[18:17] = 10_B to enable NAND flash boot sequence. The boot sequence is shown in the following:

NAND flash boot engine starts fetching the first 4K bytes of code into internal SRAM. The ECC checking and repair procedure are concurrently performed. CPU halts while NAND flash boot engine is working.

CPU executes this 4K bytes code to move the following code in NAND flash to SDRAM. Please reference NAND flash programming guide for CPU access NAND flash.

Three kinds of NAND flash configurations can be programmed using the following 2 reset latched values:

XA[22], XA[8] = 00: 512+16byte/page, 4T (OLD 1Gb flash)

XA[22], XA[8] = 01: 512+16byte/page, 3T

XA[22], XA[8] = 10: 2048+64 byte/page, 4T (new 1Gb flash select this)

XA[22], XA[8] = 11: not allowed

3.10 UART Interface

The UART controller offers similar functionality to the industry-standard 16C550UART device. It is connected to the Advanced Peripheral Bus (APB), performing serial/parallel conversion on data from/to a peripheral device. An internal clock source is provided for the UART controller to save BOM cost. Using an external clock source up to 920 K baud rate can be supported. Program the value of reset latched [XA19] for UART clock source selection:

XA[19]=1: external crystal (3.6864MHZ to 73MHZ)

XA[19]=0: internal free running 62.5MHZ (default)

The UART includes an Infrared Data Association (IrDA) Serial Infrared (SIR) protocol encoder and decoder (Endec).

The following key parameters are programmable:

- Communication baud rate
- Number of data bits
- Number of stop bits
- Parity mode
- FIFO enable (16-byte depth) or disable (1-byte depth)
- Internal nominal 1.8432 MHz clock frequency (1.42-2.12MHz) to generate low-power mode shorter bit duration
- Additional test registers and modes are implemented for functional verification and manufacturing test

Setting the value of reset latched XA[20] =1 enables the IrDA SIR protocol Endec to have GPIO[2] become nSIROUT (output), and have GPIO[1] become SIRIN (input). Please note that the UARTXD is held HIGH and UARTRXD has no effect.

3.11 SPI Interface

Here we provide one flexible 4-wire SPI interface for different 3rd party components. Both MISO and MOSI modes are supported. MISO mode is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high impedance state if the slave device is not selected. MOSI mode is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge that the slave device uses to latch the data. Some SPI features are introduced as below:

- The SPI clock (FXS_SCLK) can be programmable up to 10.4MHZ without needing any external clock source
- Each address and data phase in one command can be any integer multiple of 8 bits
- There are four possible timing relationships between FXS_SCLK and SPI data out (FXS_SDO) and SPI data in (FXS_SDI) that can be chosen using register programming
- Suitable for synchronous full-duplex communication with low bandwidth peripherals
- Devices communicate with a master/slave relationship, where the master initiates the data frame. When the master generates a clock and selects a slave device, data may be transferred in either or both directions simultaneously. Master means WildPass, slave means external 3rd party components.
- No acknowledgement mechanism to confirm receipt of data
- No flow control mechanism
- No particular higher-level protocol for master-slave dialog

- In some applications, a higher-level protocol, such as a command-response protocol, may be necessary. The master must initiate the frames for both its command and the slave's response
- Please reference SPI application note for detail

3.12 PCM Interface

WildPass supports a PCM interface with 8 bits per channel. To support such devices with 16 bits per channel, software needs to recognize two 8-bit channels provided by WildPass. Please reference PCM Application Notes for details. The features include:

- The PCM clock (FXS_PCLK) derived from external clock source (Voipclkin) and can be further programmed by register setting to meet desired channel number. The durable maximum Voipclkin is 16.384 MHz
- The supported channel number per frame is 1, 2, 4, 8, 16, 32, 64

3.13 JTAG Interface

JTAG interface is used for ICE debugging

3.14 General Purpose IO Pins

All the GPIOs can be inputted when level or edge trigger, and output values depends on driver's setting. There are 3 groups of GPIOs:

- 3 GPIOs (CrGPIO[2:0]) are supported in configuration space
- 3 GPIOs (GPIO[2:0]) are supported in wireless driver space
- 2 GPIOs (FXS_INTZ, FXO_INTZ) are supported in VOIP driver space

3.15 Clock Strategy

The 40MHZ oscillator via pin CKREF should be always there. The 12MHZ crystal via pins XTLP_usb and XTLN_usb for USB 2.0 PHY and 25MHZ crystal via pins XTLP and XTLN for 10/100 PHY can be removed for BOM saving by setting 0_B to pin P_W2UE_PD because internal PLL can provide these clocks.

3.16 200MHz MIPS Core

The WildPass has one embedded MIPS4Kc CPU which has 8K byte I cache and 8K byte D cache with TLB (Translation Look-aside Buffer) MMU included.

4 Electrical Characteristics

4.1 Absolute Maximum Rating

The absolute maximum ratings of the WildPass are listed in Table 29. The nominal values of voltages are

Table 29 Absolute Maximum Rating

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ambient temperature under bias	T_A	-40	–	85	°C	–
Storage temperature	T_{stg}	-55	–	155	°C	–
Digital I/O supply voltage(3.3V)	DV_{DD}	-0.3	–	+0.3	V	–
Core supply voltage(1.8V)	V_{DD}	-0.18	–	+0.18	V	–
USB analog supply voltage 1 (3.3V)	AV_{DD3_A}	-0.3	–	+0.3	V	–
USB analog supply voltage 2 (3.3V)	V_{DDBG_A}	-0.3	–	+0.3	V	–
USB analog supply voltage (1.8V)	V_{ADD_A}	-0.18	–	+0.18	V	–
EthPHY analog supply voltage (1.8V)	V_{CCA20}	-0.18	–	+0.18	V	–
EthPHY bias circuit analog supply voltage (3.3V)	V_{CCBS}	-0.3	–	+0.3	V	–
EthPHY A/D Converter analog supply voltage (3.3V)	V_{CCRG}	-0.3	–	+0.3	V	–
EthPHY line driver analog supply voltage (3.3V)	V_{CCAD}	-0.3	–	+0.3	V	–
PLLx5 PLL analog supply voltage (1.8V)	V_{CCPLL}	-0.18	–	+0.18	V	–
W2UE PLL analog supply voltage (1.8V)	AV_{DD_W2UE}	-0.18	–	+0.18	V	–
Reg_CLKGEN PLL analog supply voltage (1.8V)	V_{DDAL_CKGEN}	-0.18	–	+0.18	V	–
Reg_CLKGEN Regulator supply voltage (3.3V)	V_{DDAH_CKGEN}	-0.3	–	+0.3	V	–
AFE analog supply voltage (3.3V)	V_{DDAH_AFE}	-0.3	–	+0.3	V	–
AFE analog supply voltage (1.8V)	V_{DDAL_AFE}	-0.18	–	+0.18	V	–
ESD Rating	ESD	–	–	1.5	kV	–

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

4.2 Recommended Operating Conditions

The recommended operating conditions of the WildPass are listed in Table 30.

Table 30 Recommended Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ambient temperature	T_A	0	–	70	°C	–
Supply voltage 1.8 V	V_{DD} V_{ADD_A} V_{CCA20} V_{CCPLL} AV_{DD_W2UEI} V_{DDAL_CKGENI} V_{DDAL_AFE}	1.71	–	1.89		–
Supply Voltage 3.3 V	DV_{DD} AV_{DD3_A} V_{DDBG_A} V_{CCBS} V_{CCRG} V_{CCAD} V_{DDAH_CKGEN} V_{DDAH_AFE}	3.13	–	3.47	V	–
Ground	$DV_{SS}V_{SS}$	0	–	0	V	–

Note: The functions specified in this User's Manual are only fulfilled within this operating range.

4.3 DC Characteristics

This chapter includes the DC characteristics of the I/O interfaces, which are as listed in **Table 31**.

Table 31 DC Characteristics for 3.3 V Operation

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Low Voltage	V_{IL}	–	–	0.8	V	–
Input High Voltage	V_{IH}	2.0	–		V	–
Low Level Output Voltage	V_{OL}	–	–	0.4	V	–
High Level Output Voltage	V_{OH}	2.4	–		V	–
Average power supply current at V_{DD} supply	I_{DD18}	–	–	1015	mA	–
Average power supply current at DV_{DD} supply	I_{DD33}	–	–	188	mA	–
Input leakage current	I_{LI}	–	–	10	µA	–
Output leakage current	I_{LO}	–	–	10	µA	–
Input pull-up Resistance	R	–	4.7	–	kΩ	V_{IL}=0 or V_{IH}=V_{DVDD}

4.4 AC Characteristics

T_A=0 to 70 °C, $V_{DD(3.3V)}$ = 3.3 ± 0.3 V, $V_{DD(1.8V)}$ =1.8 ± 0.18 V, V_{SS} = 0 V

Timing measurements are made at 2.0 V for a logical 1 and at 0.8 V for a logical 0.

The AC testing input/output waveforms are shown in **Figure 11**.

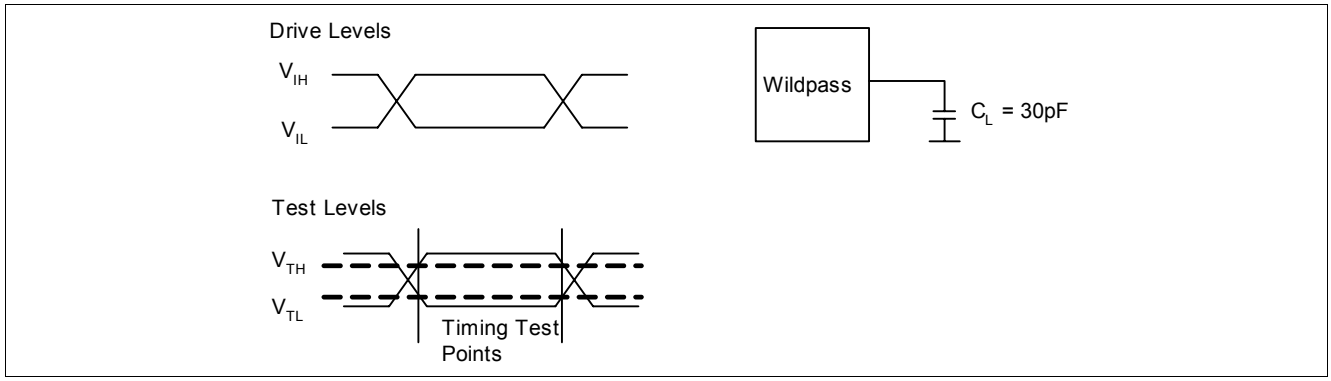

Figure 11 Input/Output Waveform for AC Test

4.5 Timing Characteristics

Please see WildPass product specification for details.

5 Package

5.1 ADM8668T - 289 BGA 19X19X1.8

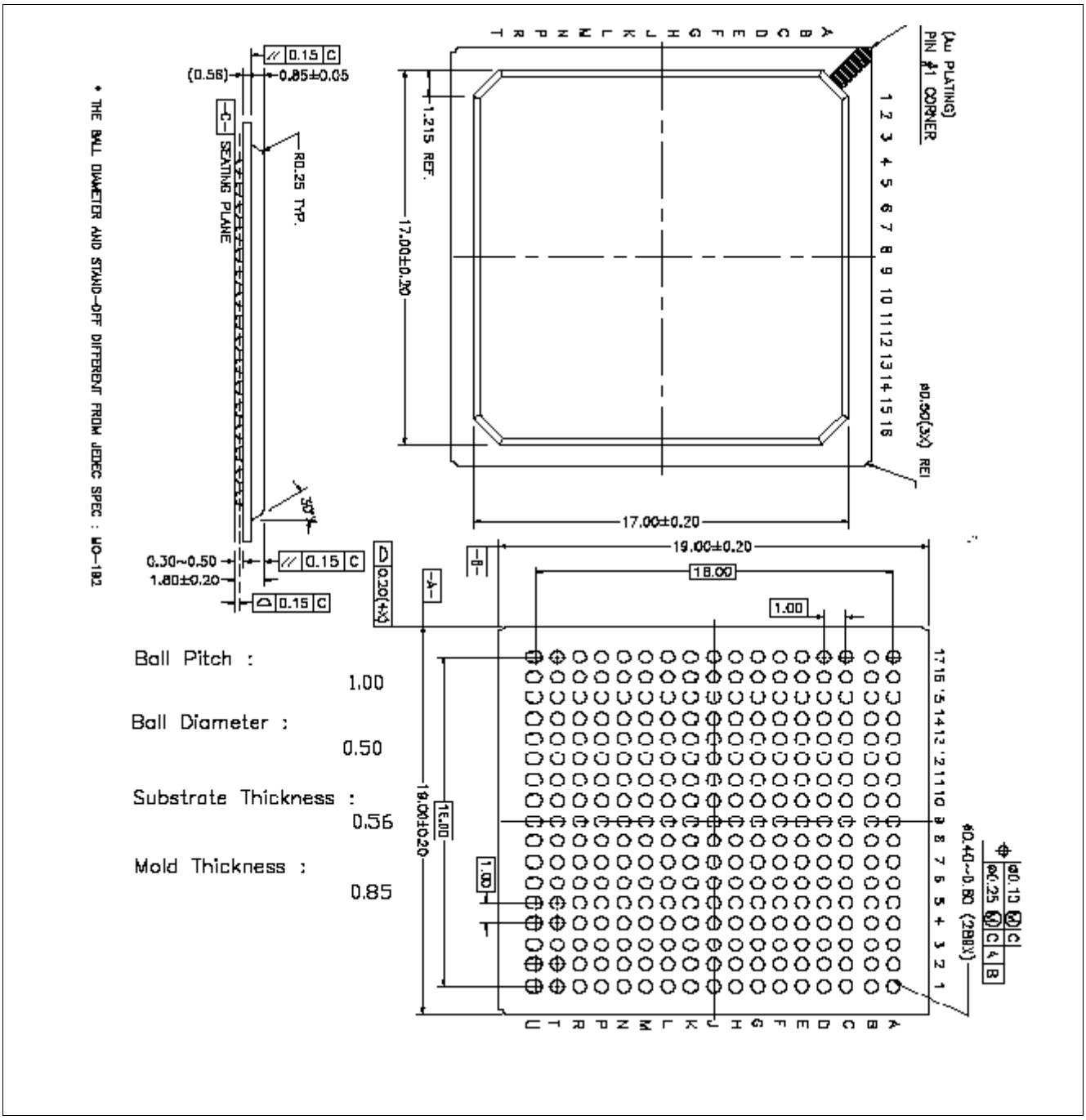

Figure 12 Wildpass 289 BGA Package Outline

5.2 ADM8668F - 352 BGA 27X27X2.33

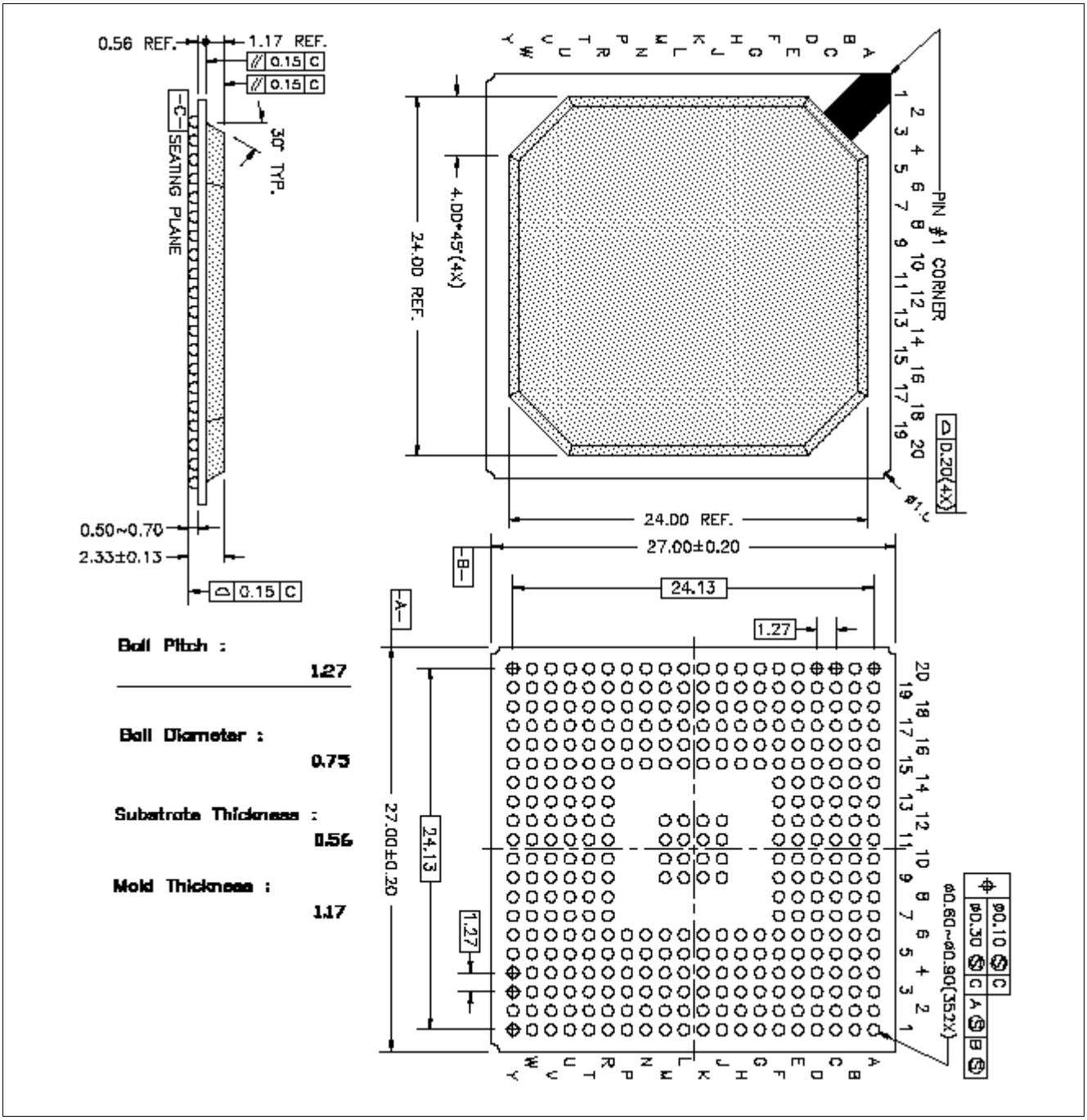

Figure 13 Wildpass 352 BGA Package Outline

6 Appendix - Chip Configuration

Reset latch group
XA[22] = NAND flash configuration.
1: 1024+64 bytes
0: 512 + 16Byte. (default)
XA[21] = NAND flash support
1: NAND flash support.
0: No NAND flash support. (default)

XA[20] = IrDA support
1: IrDA enable.
0: IrDA disable (default)

XA[19] = UART clock selection
1: external crystal (3.6864MHZ to 73MHZ)
0: internal free running 62.5MHZ (default)

XA[18:17] = Flash width reset latch for SMC_CSZ[0]
00: 8bit (default)
01: 16bis
10: 32bits
11: reserved

XA[16] = Endian select.
0: little ending (default)
1: big ending for all masters.

XA[15:14] = CPU: AHB speed ratio
00: 3:2
01: 2:1 (default)
10: 1:1
11: reserved

XA[13] = AHB pipeline
1: bypass
0: enable(default)

XA[12] = SDRAM (SDRAM_CS0Z) / SRAM (SRAM_CS2Z) selector for address range from 0000_0000.
0: SDRAM_CS0Z (default), note: SRAM_CS2Z starts from 1080_0000.
1: SRAM_CS2Z, note: SDRAM_CS0Z is useless.

XA[11] = test pin output enable (only for 324 BGA/pci pads)
1: output enable
0: output disable(default)

XA[10] = test pin output enable for clock and reset.
1: output enable
0: output disable(default)

XA[9] = RMII enable
1: L2_RMII
0: L2_MII (default)

XA[8] = NAND flash 3 / 4 cycle
1: NAND flash 3 cycles.
0: NAND flash 4 cycles. (default)

XA[7] = Package type select
1'b0: XA[2:0] is chip mode
1'b1: XA[2:0] is package type (default)

XA[6:3] = PLL configuration reset latch
0000: 175MHZ
0101: 200MHZ (default)
1001: Reserved
1111: bypass
Other values are reserved.

XA[2:0] = Chip mode selection (Note: XA[7] should be reset latched to 0)
000: normal(default)
001: wireless mac only mode
010: reserved
011: reserved
100: skylark only mode
101: BBP test mode
110: LAN 1 PHY test mode
111: bootup membist test

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