Low Offset, Low Noise, RRO Operational Amplifier

Check for Samples: SM73308

FEATURES

(Unless Otherwise Noted, Typical Values at V_S = 2.7V)

- **Renewable Energy Grade**
- **Ensured 2.7V and 5V Specifications**
- **Maximum V_{OS} 850µV (Limit)**
- **Voltage noiseN**
  - **f = 100 Hz 12.5nV/√Hz**
  - **f = 10 kHz 7.5nV/√Hz**
- **Rail-to-Rail Output Swing**
  - **R_L = 600Ω 100mV From Rail**
  - **R_L = 2kΩ 50mV From Rail**
- **Open Loop Gain With R_L = 2kΩ 100dB**
- **V_{CM} 0 to V^+ −0.9V**
- **Supply Current 550µA**
- **Gain Bandwidth Product 3.5MHz**
- **Temperature Range −40°C to 125°C**

APPLICATIONS

- **Transducer Amplifier**
- **Instrumentation Amplifier**
- **Precision Current Sensing**
- **Data Acquisition Systems**
- **Active Filters and Buffers**
- **Sample and Hold**
- **Portable/battery Powered Electronics**
- **Automotive**

DESCRIPTION

The SM73308 is a single low noise precision operational amplifier intended for use in a wide range of applications. Other important characteristics include: an extended operating temperature range of −40°C to 125°C, the tiny SC70-5 package, and low input bias current.

The extended temperature range of −40°C to 125°C allows the SM73308 to accommodate a broad range of applications. The SM73308 expands TI's Silicon Dust™ amplifier portfolio offering enhancements in size, speed, and power savings. The SM73308 is ensured to operate over the voltage range of 2.7V to 5.0V and has rail-to-rail output.

The SM73308 is designed for precision, low noise, low voltage, and miniature systems. This amplifier provides rail-to-rail output swing into heavy loads. The maximum input offset is 850 µV at room temperature and the input common mode voltage range includes ground.

The SM73308 is offered in the tiny SC70-5 package.

Connection Diagram

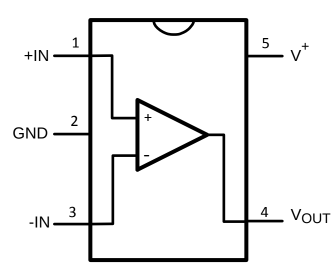
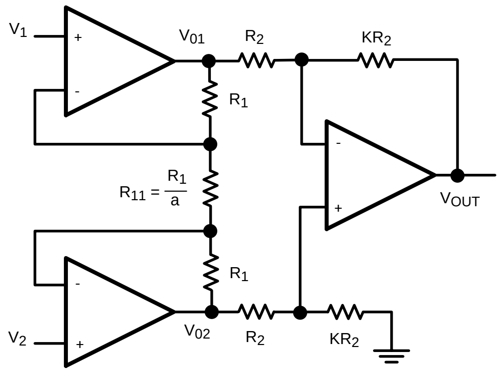


Figure 1. SC70-5 – Top View
See Package Number DCK

Instrumentation Amplifier



$$V_O = -K (2a + 1) (V_1 - V_2) \quad (1)$$

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

ESD Tolerance[3]	Machine Model	200V
	Human Body Model	2000V
Differential Input Voltage		± Supply Voltage
Voltage at Input Pins		$(V^+) + 0.3V, (V^-) – 0.3V$
Current at Input Pins		±10 mA
Supply Voltage $(V^+–V^-)$		5.75V
Output Short Circuit to V^+		See[4]
Output Short Circuit to V^-		See[5]
Mounting Temperture	Infrared or Convection (20 sec)	235°C
	Wave Soldering Lead Temp (10 sec)	260°C
Storage Temperature Range		−65°C to 150°C
Junction Temperature[6]		150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model is 1.5 kΩ in series with 100 pF. Machine Model is 0Ω in series with 20 pF.
(4) Shorting output to V^+ will adversely affect reliability.
(5) Shorting output to V^- will adversely affect reliability.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)}–T_A) / \theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Operating Ratings[1]

Supply Voltage	2.7V to 5.5V
Temperature Range	−40°C to 125°C
Thermal Resistance (θ_{JA})	440 °C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.

2.7V DC Electrical Characteristics(1)

Unless otherwise specified, all limits are ensured for T_A = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2 and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min(2)	Typ(3)	Max(2)	Units
V_{OS}	Input Offset Voltage			0.3	0.85 **1.0**	mV
TCV_{OS}	Input Offset Voltage Average Drift			−0.45		µV/°C
I_B	Input Bias Current(4)	V_{CM} = 1V		−0.1	100 **250**	pA
I_{OS}	Input Offset Current(4)			0.004	100	pA
I_S	Supply Current			550	900 **910**	µA
CMRR	Common Mode Rejection Ratio	0.5 ≤ V_{CM} ≤ 1.2V	74 **72**	80		dB
PSSR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 5V	82 **76**	90		dB
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	0		1.8	V
A_V	Large Signal Voltage Gain(5)	R_L = 600Ω to 1.35V, V_O = 0.2V to 2.5V	92 **80**	100		dB
		R_L = 2kΩ to 1.35V, V_O = 0.2V to 2.5V	98 **86**	100		
V_O	Output Swing	R_L = 600Ω to 1.35V V_{IN} = ± 100mV	0.11 **0.14**	0.084 to 2.62	2.59 **2.56**	V
		R_L = 2kΩ to 1.35V V_{IN} = ± 100mV	0.05 **0.06**	0.026 to 2.68	2.65 **2.64**	
I_O	Output Short Circuit Current	Sourcing, V_O = 0V V_{IN} = 100mV	18 **11**	24		mA
		Sinking, V_O = 2.7V V_{IN} = −100mV	18 **11**	22		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A.
(2) All limits are ensured by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm.
(4) Limits ensured by design.
(5) R_L is connected to mid-supply. The output voltage is set at 200mV from the rails. V_O = GND + 0.2V and V_O = V^+ −0.2V

2.7V AC Electrical Characteristics(1)

Unless otherwise specified, all limits are ensured for T_A = 25°C. V^+ = 5.0V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2 and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min(2)	Typ(3)	Max(2)	Units
SR	Slew Rate(4)	A_V = +1, R_L = 10 kΩ		1.4		V/µs
GBW	Gain-Bandwidth Product			3.5		MHz
Φ_m	Phase Margin			79		Deg
G_m	Gain Margin			−15		dB
e_n	Input-Referred Voltage Noise (Flatband)	f = 10kHz		7.5		nV/√Hz
e_n	Input-Referred Voltage Noise (l/f)	f = 100Hz		12.5		nV/√Hz
i_n	Input-Referred Current Noise	f = 1kHz		0.001		pA/√Hz
THD	Total Harmonic Distortion	f = 1kHz, A_V = +1 R_L = 600Ω, V_{IN} = 1 V_{PP}		0.007		%

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A.
(2) All limits are ensured by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm.
(4) The number specified is the slower of positive and negative slew rates.

5.0V DC Electrical Characteristics [(1)]

Unless otherwise specified, all limits are ensured for T_A = 25°C. V^+ = 5.0V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2 and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min [(2)]	Typ [(3)]	Max [(2)]	Units
V_{OS}	Input Offset Voltage			0.25	0.85 **1.0**	mV
TCV_{OS}	Input Offset Voltage Average Drift			−0.35		µV/°C
I_B	Input Bias Current [(4)]	V_{CM} = 1V		−0.23	100 **250**	pA
I_{OS}	Input Offset Current [(4)]			0.017	100	pA
I_S	Supply Current			600	950 **960**	µA
CMRR	Common Mode Rejection Ratio	0.5 ≤ V_{CM} ≤ 3.5V	80 **79**	90		dB
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 5V	82 **76**	90		dB
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	0		4.1	V
A_V	Large Signal Voltage Gain [(5)]	R_L = 600Ω to 2.5V, V_O = 0.2V to 4.8V	92 **89**	100		dB
		R_L = 2kΩ to 2.5V, V_O = 0.2V to 4.8V	98 **95**	100		
V_O	Output Swing	R_L = 600Ω to 2.5V V_{IN} = ± 100mV	0.15 **0.23**	0.112 to 4.9	4.85 **4.77**	V
		R_L = 2kΩ to 2.5V V_{IN} = ± 100mV	0.06 **0.07**	0.035 to 4.97	4.94 **4.93**	
I_O	Output Short Circuit Current [(4)(6)]	Sourcing, V_O = 0V V_{IN} = 100mV	35 **35**	75		mA
		Sinking, V_O = 2.7V V_{IN} = −100mV	35 **35**	66		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A.
(2) All limits are ensured by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm.
(4) Limits ensured by design.
(5) R_L is connected to mid-supply. The output voltage is set at 200mV from the rails. V_O = GND + 0.2V and V_O = V^+ −0.2V
(6) Continuous operation of the device with an output short circuit current larger than 35mA may cause permanent damage to the device.

5.0V AC Electrical Characteristics [(1)]

Unless otherwise specified, all limits are ensured for T_A = 25°C. V^+ = 5.0V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2 and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min [(2)]	Typ [(3)]	Max [(2)]	Units
SR	Slew Rate [(4)]	A_V = +1, R_L = 10 kΩ		1.4		V/µs
GBW	Gain-Bandwidth Product			3.5		MHz
Φ_m	Phase Margin			79		Deg
G_m	Gain Margin			−15		dB
e_n	Input-Referred Voltage Noise (Flatband)	f = 10kHz		6.5		nV/√Hz
e_n	Input-Referred Voltage Noise (l/f)	f = 100Hz		12		nV/√Hz
i_n	Input-Referred Current Noise	f = 1kHz		0.001		pA/√Hz
THD	Total Harmonic Distortion	f = 1kHz, A_V = +1 R_L = 600Ω, V_{IN} = 1 V_{PP}		0.007		%

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A.
(2) All limits are ensured by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm.
(4) The number specified is the slower of positive and negative slew rates.

Typical Performance Characteristics

V_{OS} vs. V_{CM} Over Temperature

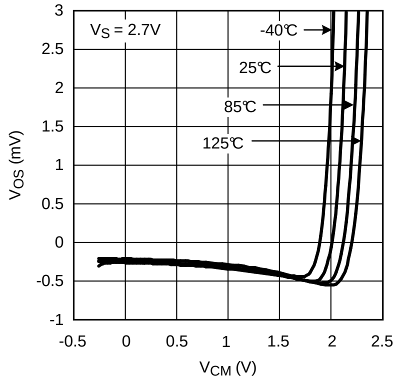


Figure 2.

V_{OS} vs. V_{CM} Over Temperature

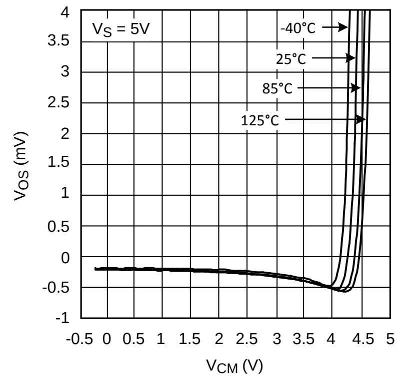


Figure 3.

Output Swing vs. V_S

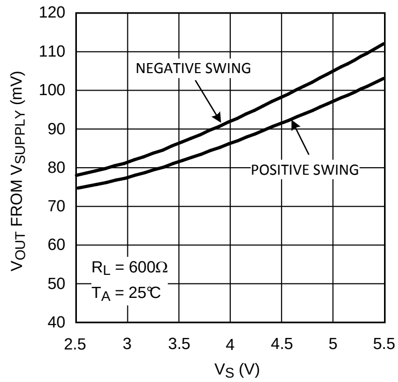


Figure 4.

Output Swing vs. V_S

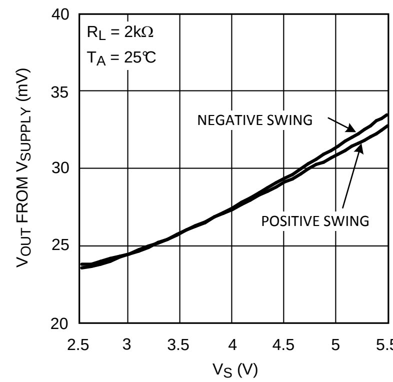


Figure 5.

Output Swing vs. V_S

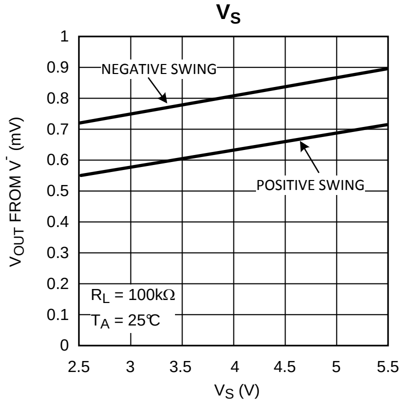


Figure 6.

I_S vs. V_S Over Temperature

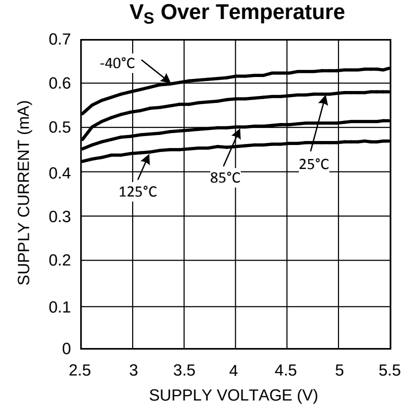


Figure 7.

Typical Performance Characteristics (continued)

V_{IN} vs. V_{OUT}

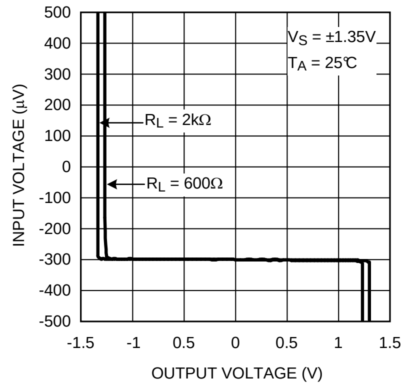


Figure 8.

V_{IN} vs. V_{OUT}

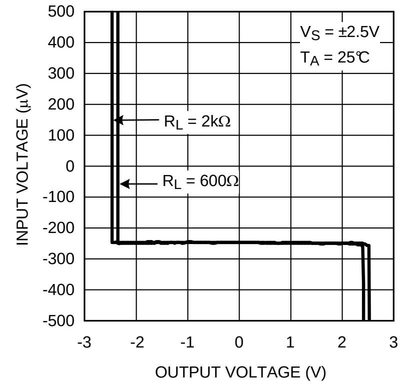


Figure 9.

Sourcing Current vs. V_{OUT}(1)

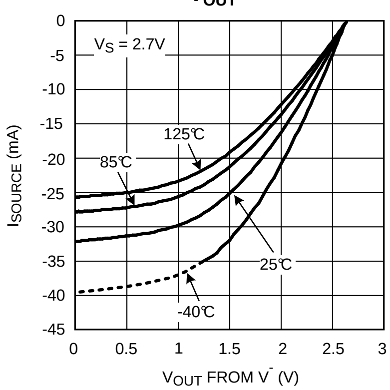


Figure 10.

Sourcing Current vs. V_{OUT}(1)

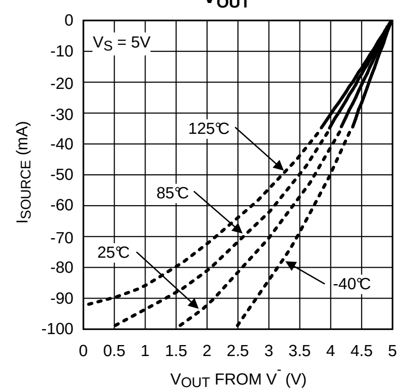


Figure 11.

Sinking Current vs. V_{OUT}(1)

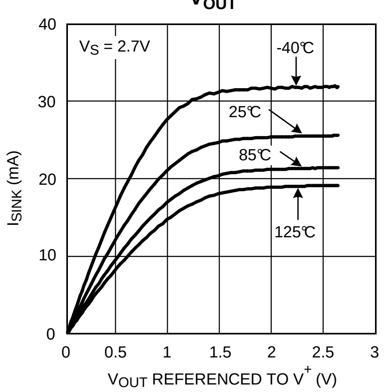


Figure 12.

Sinking Current vs. V_{OUT}(1)

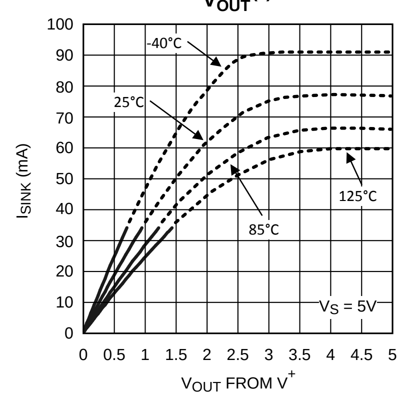


Figure 13.

(1) Continuous operation of the device with an output short circuit current larger than 35mA may cause permanent damage to the device.

Typical Performance Characteristics (continued)

Input Voltage Noise vs. Frequency

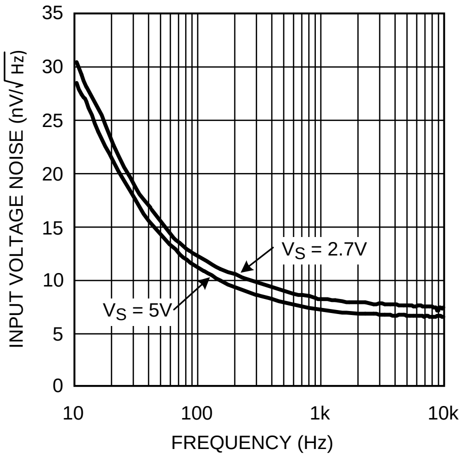


Figure 14.

Input Bias Current Over Temperature

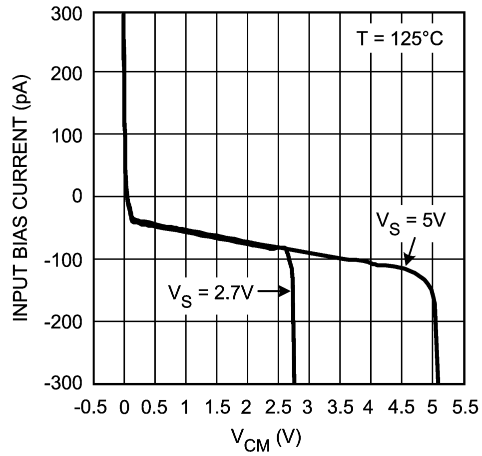


Figure 15.

Input Bias Current Over Temperature

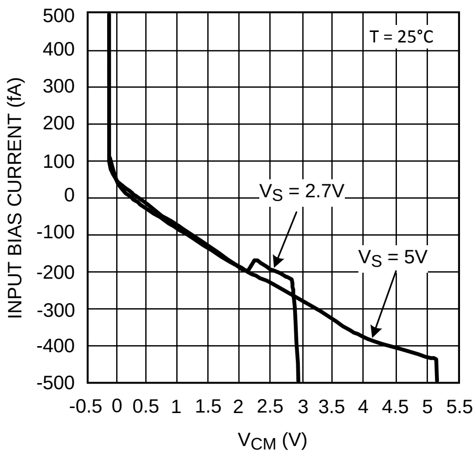


Figure 16.

Input Bias Current Over Temperature

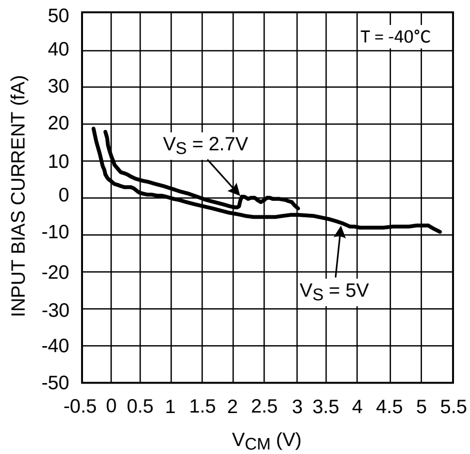


Figure 17.

THD+N vs. Frequency

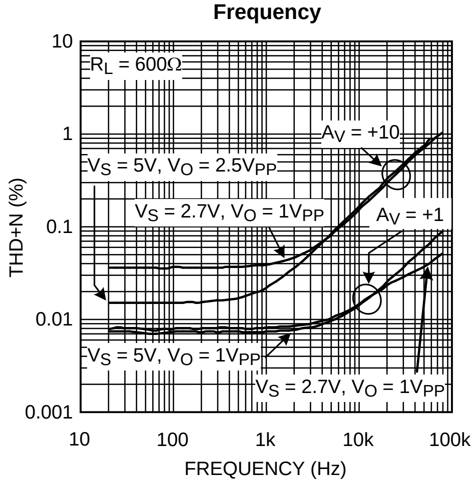


Figure 18.

THD+N vs. V_{OUT}

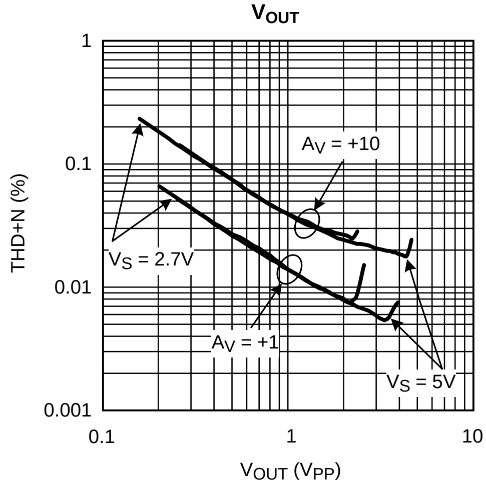


Figure 19.

Typical Performance Characteristics (continued)

Slew Rate vs. Supply Voltage

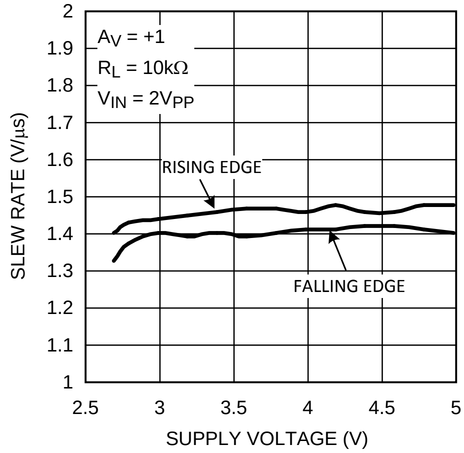


Figure 20.

Open Loop Frequency Response Over Temperature

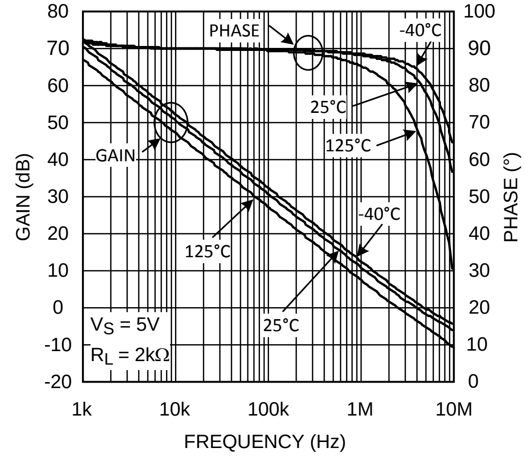


Figure 21.

Open Loop Frequency Response

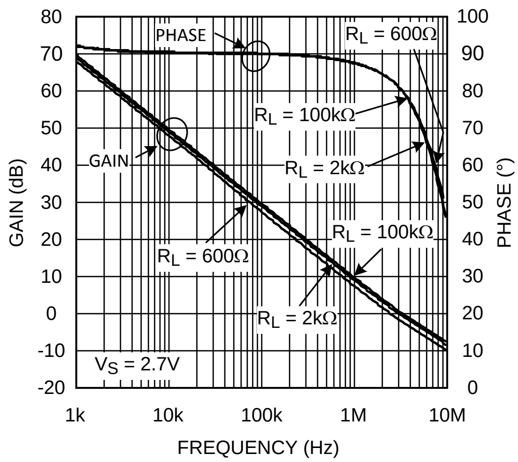


Figure 22.

Open Loop Frequency Response

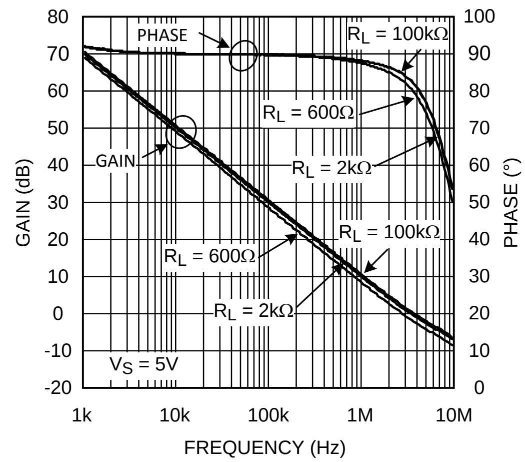


Figure 23.

Open Loop Gain & Phase with Cap. Loading

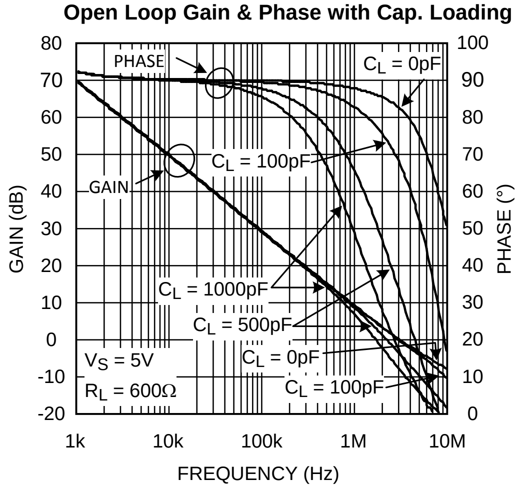


Figure 24.

Open Loop Gain & Phase with Cap. Loading

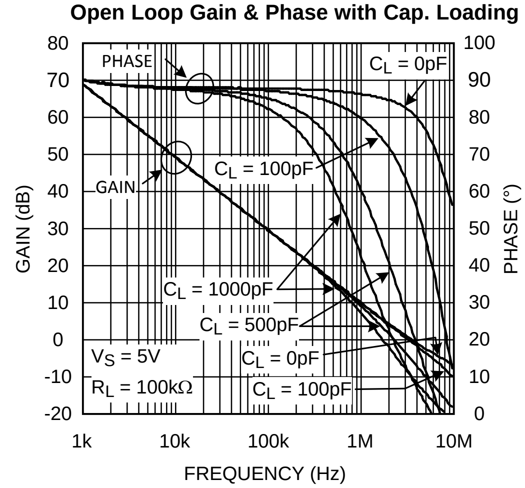


Figure 25.

Typical Performance Characteristics (continued)

Non-Inverting Small Signal Pulse Response

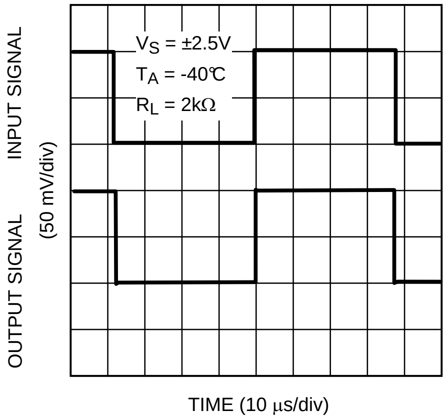


Figure 26.

Non-Inverting Large Signal Pulse Response

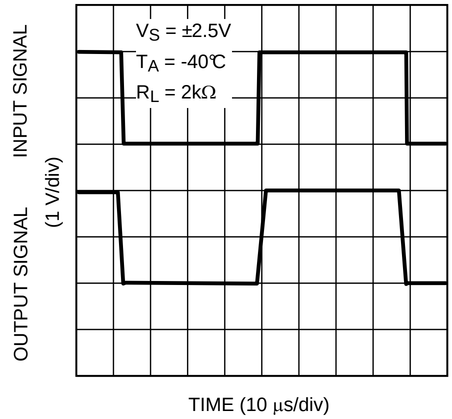


Figure 27.

Non-Inverting Small Signal Pulse Response

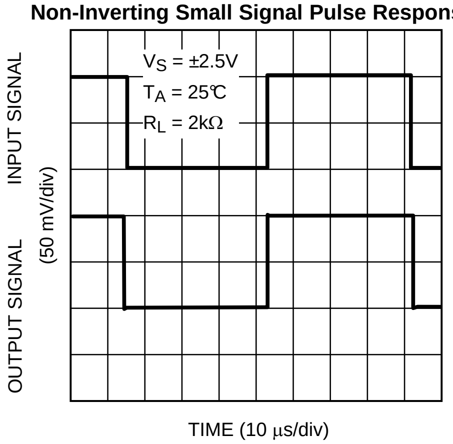


Figure 28.

Non-Inverting Large Signal Pulse Response

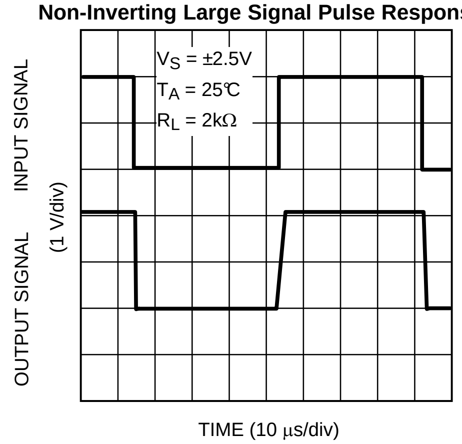


Figure 29.

Non-Inverting Small Signal Pulse Response

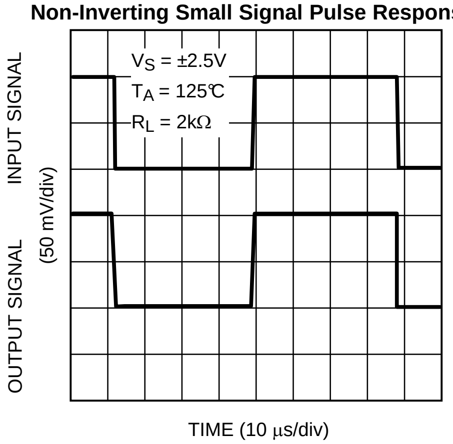


Figure 30.

Non-Inverting Large Signal Pulse Response

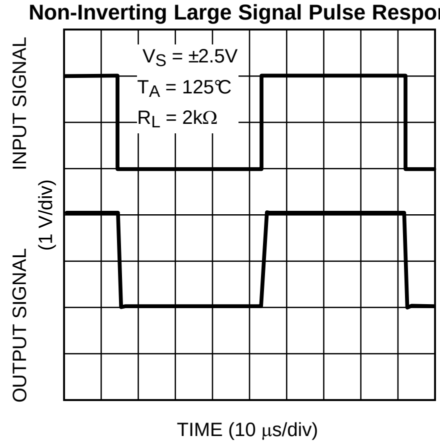


Figure 31.

Typical Performance Characteristics (continued)

Inverting Small Signal Pulse Response

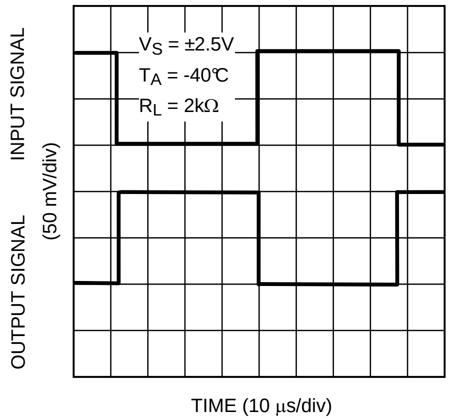


Figure 32.

Inverting Large Signal Pulse Response

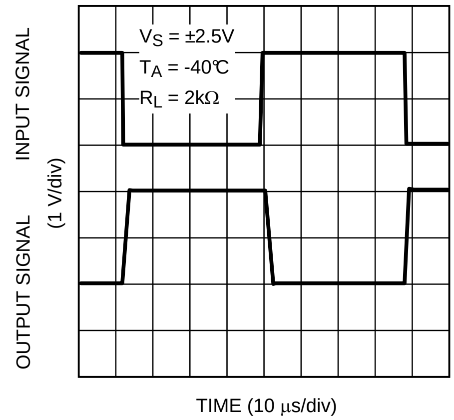


Figure 33.

Inverting Small Signal Pulse Response

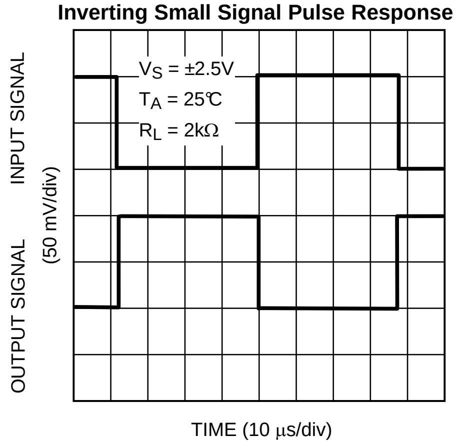


Figure 34.

Inverting Large Signal Pulse Response

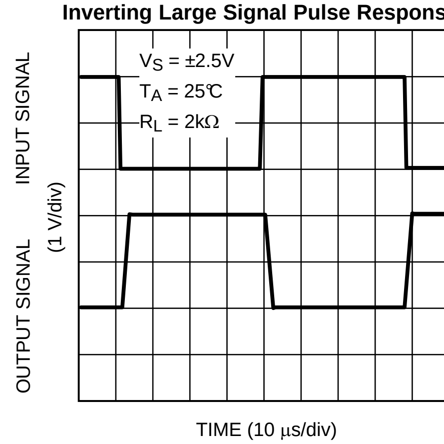


Figure 35.

Inverting Small Signal Pulse Response

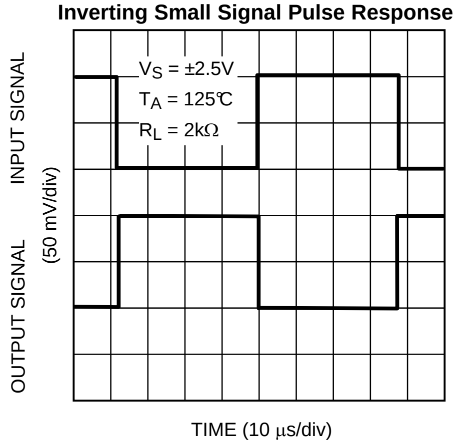


Figure 36.

Inverting Large Signal Pulse Response

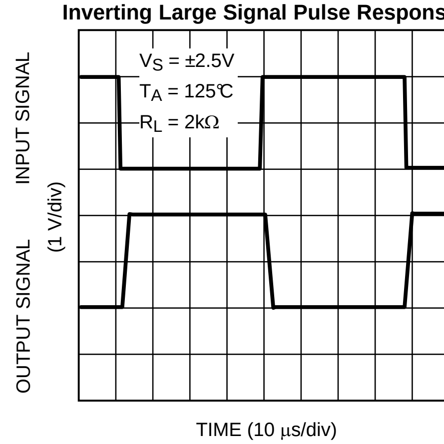


Figure 37.

Typical Performance Characteristics (continued)

Stability vs. V_{CM}

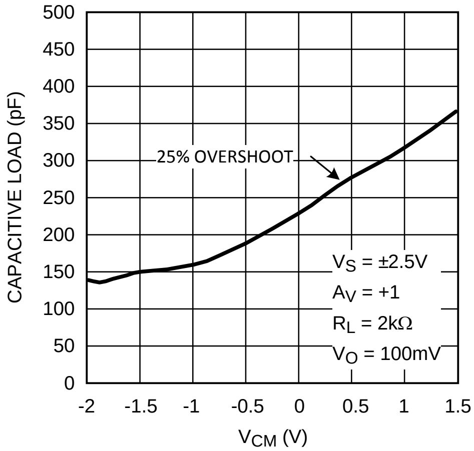


Figure 38.

Stability vs. V_{CM}

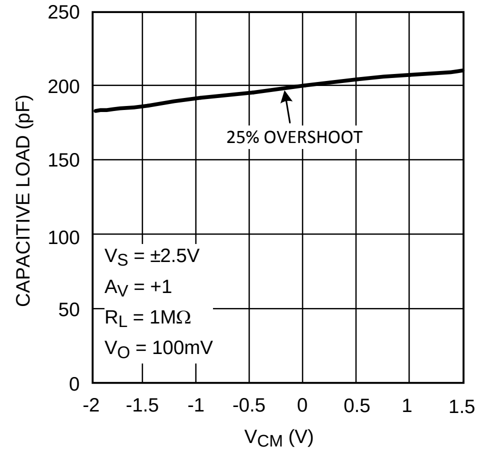


Figure 39.

PSRR vs. Frequency

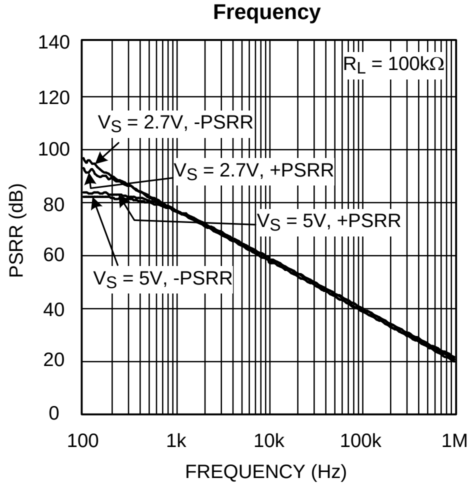


Figure 40.

CMRR vs. Frequency

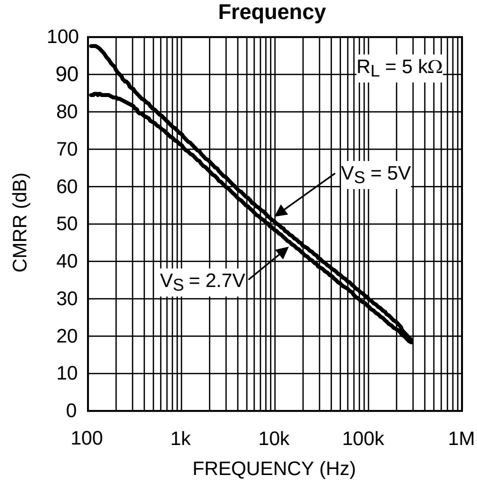


Figure 41.

APPLICATION NOTE

SM73308

The SM73308 is a precision amplifier with very low noise and ultra low offset voltage. SM73308's extended temperature range of −40°C to 125°C enables the user to design a variety of applications including automotive.

The SM73308 has a maximum offset voltage of 1mV over the extended temperature range. This makes the SM73308 ideal for applications where precision is important.

INSTRUMENTATION AMPLIFIER

Measurement of very small signals with an amplifier requires close attention to the input impedance of the amplifier, gain of the overall signal on the inputs, and the gain on each input since we are only interested in the difference of the two inputs and the common signal is considered noise. A classic solution is an instrumentation amplifier. Instrumentation amplifiers have a finite, accurate, and stable gain. Also they have extremely high input impedances and very low output impedances. Finally they have an extremely high CMRR so that the amplifier can only respond to the differential signal. A typical instrumentation amplifier is shown in Figure 42.

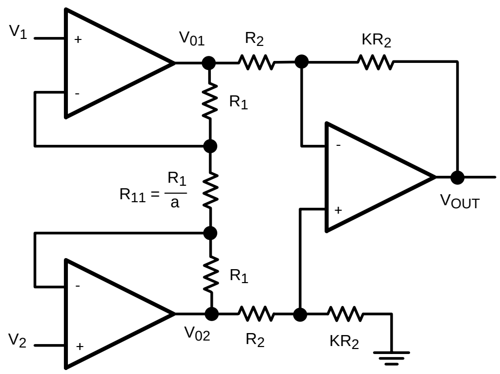


Figure 42. Instrumentation Amplifier

There are two stages in this amplifier. The last stage, output stage, is a differential amplifier. In an ideal case the two amplifiers of the first stage, input stage, would be set up as buffers to isolate the inputs. However they cannot be connected as followers because of real amplifier's mismatch. That is why there is a balancing resistor between the two. The product of the two stages of gain will give the gain of the instrumentation amplifier. Ideally, the CMRR should be infinite. However the output stage has a small non-zero common mode gain which results from resistor mismatch.

In the input stage of the circuit, current is the same across all resistors. This is due to the high input impedance and low input bias current of the SM73308. With the node equations we have:

$$\text{GIVEN: } I_{R_1} = I_{R_{11}} \quad (2)$$

By Ohm's Law:

$$V_{O1} - V_{O2} = (2R_1 + R_{11})\, I_{R_{11}}$$
$$= (2a + 1)\, R_{11} \bullet I_{R_{11}}$$
$$= (2a + 1)\, V_{R_{11}} \quad (3)$$

However:

$$V_{R_{11}} = V_1 - V_2 \quad (4)$$

So we have:

$$V_{O1} - V_{O2} = (2a + 1)(V_1 - V_2) \quad (5)$$

Now looking at the output of the instrumentation amplifier:

$$V_O = \frac{KR_2}{R_2}(V_{O2} - V_{O1}) = -K(V_{O1} - V_{O2}) \quad (6)$$

Substituting from Equation 5:

$$V_O = -K(2a + 1)(V_1 - V_2) \quad (7)$$

This shows the gain of the instrumentation amplifier to be:

$$-K(2a+1) \quad (8)$$

Typical values for this circuit can be obtained by setting: a = 12 and K= 4. This results in an overall gain of −100.

Figure 43 shows typical CMRR characteristics of this Instrumentation amplifier over frequency. Three SM73308 amplifiers are used along with 1% resistors to minimize resistor mismatch. Resistors used to build the circuit are: R_1 = 21.6kΩ, R_{11} = 1.8kΩ, R_2 = 2.5kΩ with K = 40 and a = 12. This results in an overall gain of −1000, −K(2a+1) = −1000.

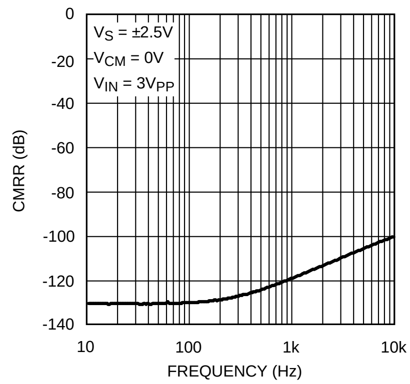


Figure 43. CMRR vs. Frequency

ACTIVE FILTER

Active filters are circuits with amplifiers, resistors, and capacitors. The use of amplifiers instead of inductors, which are used in passive filters, enhances the circuit performance while reducing the size and complexity of the filter.

The simplest active filters are designed using an inverting op amp configuration where at least one reactive element has been added to the configuration. This means that the op amp will provide "frequency-dependent" amplification, since reactive elements are frequency dependent devices.

LOW PASS FILTER

The following shows a very simple low pass filter.

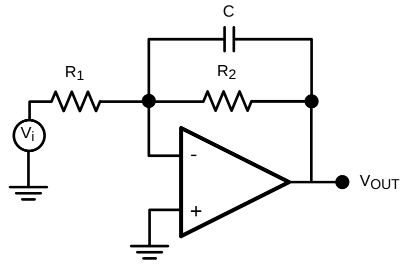


Figure 44. Lowpass Filter

The transfer function can be expressed as follows:

By KCL:

$$\frac{-V_i}{R_1} - \frac{V_O}{\left[\frac{1}{jwc}\right]} - \frac{V_O}{R_2} = O \tag{9}$$

Simplifying this further results in:

$$V_O = \frac{-R_2}{R_1}\left[\frac{1}{jwcR_2 + 1}\right]V_i \tag{10}$$

or

$$\frac{V_O}{V_i} = \frac{-R_2}{R_1}\left[\frac{1}{jwcR_2 + 1}\right] \tag{11}$$

Now, substituting ω=2πf, so that the calculations are in f(Hz) and not ω(rad/s), and setting the DC gain $H_O = -R_2/R_1$ and $H = V_O/V_i$

$$H = H_O\left[\frac{1}{j2\pi fcR_2 + 1}\right] \tag{12}$$

Set: $f_o = 1/(2\pi R_1C)$

$$H = H_O\left[\frac{1}{1 + j\,(f/f_o)}\right] \tag{13}$$

Low pass filters are known as lossy integrators because they only behave as an integrator at higher frequencies. Just by looking at the transfer function one can predict the general form of the bode plot. When the f/f_O ratio is small, the capacitor is in effect an open circuit and the amplifier behaves at a set DC gain. Starting at f_O, −3dB corner, the capacitor will have the dominant impedance and hence the circuit will behave as an integrator and the signal will be attenuated and eventually cut. The bode plot for this filter is shown in the following picture:

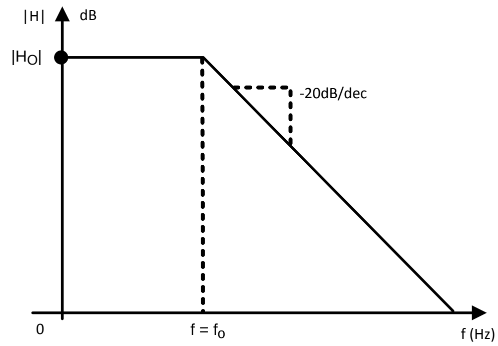


Figure 45. Lowpass Filter Transfer Function

HIGH PASS FILTER

In a similar approach, one can derive the transfer function of a high pass filter. A typical first order high pass filter is shown below:

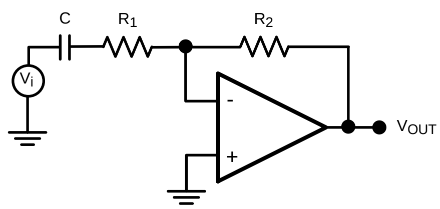


Figure 46. Highpass FIlter

Writing the KCL for this circuit :

(V_1 denotes the voltage between C and R_1)

$$\frac{V_1 - V_i}{\frac{1}{jwC}} = \frac{V_1 - V^-}{R_1} \quad (14)$$

$$\frac{V^- + V_1}{R_1} = \frac{V^- + V_O}{R_2} \quad (15)$$

Solving these two equations to find the transfer function and using:

$$f_O = \frac{1}{2\pi R_1 C} \quad (16)$$

(high frequency gain) $H_O = \frac{-R_2}{R_1}$ and $H = \frac{V_O}{V_i}$

Which results:

$$H = H_O \frac{j\,(f/f_o)}{1 + j\,(f/f_o)} \quad (17)$$

Looking at the transfer function, it is clear that when f/f_O is small, the capacitor is open and hence no signal is getting in to the amplifier. As the frequency increases the amplifier starts operating. At $f = f_O$ the capacitor behaves like a short circuit and the amplifier will have a constant, high frequency, gain of H_O. Figure 47 shows the transfer function of this high pass filter:

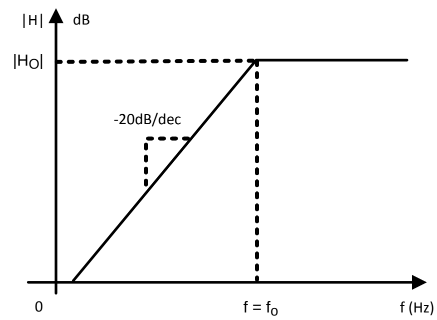


Figure 47. Highpass Filter Transfer Function

BAND PASS FILTER

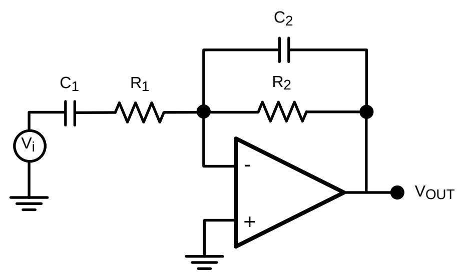


Figure 48. Bandpass Filter

Combining a low pass filter and a high pass filter will generate a band pass filter. In this network the input impedance forms the high pass filter while the feedback impedance forms the low pass filter. Choosing the corner frequencies so that $f_1 < f_2$, then all the frequencies in between, $f_1 \le f \le f_2$, will pass through the filter while frequencies below f_1 and above f_2 will be cut off.

The transfer function can be easily calculated using the same methodology as before.

$$H = H_O \frac{j\,(f/f_1)}{[1 + j\,(f/f_1)]\ [1 + j\,(f/f_2)]}$$

where

$$f_1 = \frac{1}{2\pi R_1 C_1}$$

$$f_2 = \frac{1}{2\pi R_2 C_2}$$

- $$H_O = \frac{-R_2}{R_1} \quad (18)$$

The transfer function is presented in the following figure.

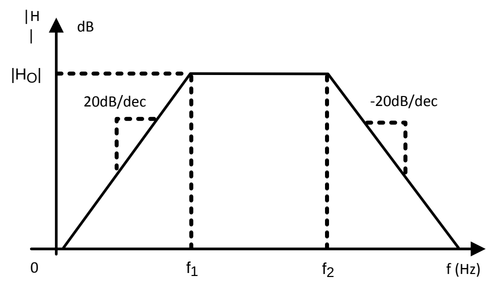


Figure 49. Bandpass filter Transfer Function

STATE VARIABLE ACTIVE FILTER

State variable active filters are circuits that can simultaneously represent high pass, band pass, and low pass filters. The state variable active filter uses three separate amplifiers to achieve this task. A typical state variable active filter is shown in Figure 50. The first amplifier in the circuit is connected as a gain stage. The second and third amplifiers are connected as integrators, which means they behave as low pass filters. The feedback path from the output of the third amplifier to the first amplifier enables this low frequency signal to be fed back with a finite and fairly low closed loop gain. This is while the high frequency signal on the input is still gained up by the open loop gain of the 1st amplifier. This makes the first amplifier a high pass filter. The high pass signal is then fed into a low pass filter. The outcome is a band pass signal, meaning the second amplifier is a band pass filter. This signal is then fed into the third amplifiers input and so, the third amplifier behaves as a simple low pass filter.

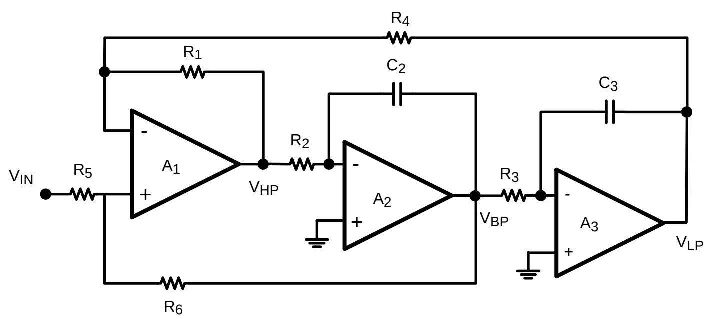
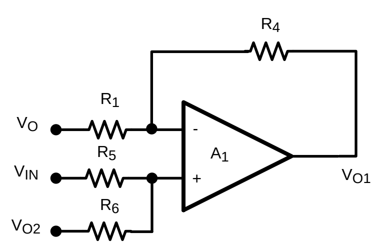
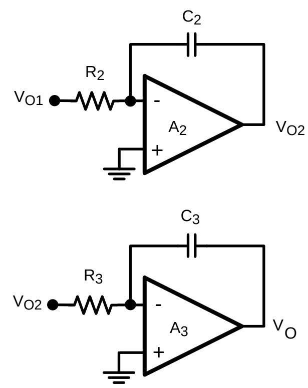


Figure 50. State Variable Active Filter

The transfer function of each filter needs to be calculated. The derivations will be more trivial if each stage of the filter is shown on its own.

The three components are:





For A_1 the relationship between input and output is:

$$V_{O1} = \frac{-R_4}{R_1} V_0 + \left[\frac{R_6}{R_5 + R_6}\right]\left[\frac{R_1 + R_4}{R_1}\right] V_{IN} + \left[\frac{R_5}{R_5 + R_6}\right]\left[\frac{R_1 + R_4}{R_1}\right] V_{O2} \quad (19)$$

This relationship depends on the output of all the filters. The input-output relationship for A_2 can be expressed as:

$$V_{O2} = \frac{-1}{s\,C_2R_2} V_{O1} \quad (20)$$

And finally this relationship for A_3 is as follows:

$$V_O = \frac{-1}{s\,C_3R_3} V_{O2} \quad (21)$$

Re-arranging these equations, one can find the relationship between V_O and V_{IN} (transfer function of the lowpass filter), V_{O1} and V_{IN} (transfer function of the highpass filter), and V_{O2} and V_{IN} (transfer function of the bandpass filter) These relationships are as follows:

Lowpass Filter

$$\frac{V_O}{V_{IN}} = \frac{\left[\frac{R_1 + R_4}{R_1}\right]\left[\frac{R_6}{R_5 + R_6}\right]\left[\frac{1}{C_2C_3R_2R_3}\right]}{s^2 + s\left[\frac{1}{C_2R_2}\right]\left[\frac{R_5}{R_5 + R_6}\right]\left[\frac{R_1 + R_4}{R_1}\right] + \left[\frac{1}{C_2C_3R_2R_3}\right]} \quad (22)$$

Highpass Filter

$$\frac{V_{O1}}{V_{IN}} = \frac{s^2\left[\frac{R_1 + R_4}{R_1}\right]\left[\frac{R_6}{R_5 + R_6}\right]}{s^2 + s\left[\frac{1}{C_2R_2}\right]\left[\frac{R_5}{R_5 + R_6}\right]\left[\frac{R_1 + R_4}{R_1}\right] + \left[\frac{1}{C_2C_3R_2R_3}\right]} \quad (23)$$

Bandpass Filter

$$\frac{V_{O2}}{V_{IN}} = \frac{s\left[\frac{1}{C_2R_2}\right]\left[\frac{R_1 + R_4}{R_1}\right]\left[\frac{R_6}{R_5 + R_6}\right]}{s^2 + s\left[\frac{1}{C_2R_2}\right]\left[\frac{R_5}{R_5 + R_6}\right]\left[\frac{R_1 + R_4}{R_1}\right] + \left[\frac{1}{C_2C_3R_2R_3}\right]} \quad (24)$$

The center frequency and Quality Factor for all of these filters is the same. The values can be calculated in the following manner:

$$\omega_C = \sqrt{\frac{1}{C_2C_3R_2R_3}}$$

and

$$Q = \sqrt{\frac{C_2R_2}{C_3R_3}}\left[\frac{R_5 + R_6}{R_6}\right]\left[\frac{R_1}{R_1 + R_4}\right] \quad (25)$$

A design example is shown here:

Designing a bandpass filter with center frequency of 10kHz and Quality Factor of 5.5

To do this, first consider the Quality Factor. It is best to pick convenient values for the capacitors. $C_2 = C_3 = 1000pF$. Also, choose $R_1 = R_4 = 30k\Omega$. Now values of R_5 and R_6 need to be calculated. With the chosen values for the capacitors and resistors, Q reduces to:

$$Q = \frac{11}{2} = \frac{1}{2}\left[\frac{R_5 + R_6}{R_6}\right] \quad (26)$$

or

$$R_5 = 10R_6 \; R_6 = 1.5k\Omega \; R_5 = 15k\Omega \quad (27)$$

Also, for f = 10kHz, the center frequency is $\omega_c = 2\pi f = 62.8kHz$.

Using the expressions above, the appropriate resistor values will be $R_2 = R_3 = 16k\Omega$.

The following graphs show the transfer function of each of the filters. The DC gain of this circuit is:

$$\text{DC GAIN} = \left[\frac{R_1 + R_4}{R_1}\right]\left[\frac{R_6}{R_5 + R_6}\right] = -14.8\text{ dB} \quad (28)$$

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	19

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SM73308MG/NOPB	Active	Production	SC70 (DCK) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	S08
SM73308MG/NOPB.A	Active	Production	SC70 (DCK) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	S08
SM73308MGE/NOPB	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	S08
SM73308MGE/NOPB.A	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	S08
SM73308MGX/NOPB	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	S08
SM73308MGX/NOPB.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	S08

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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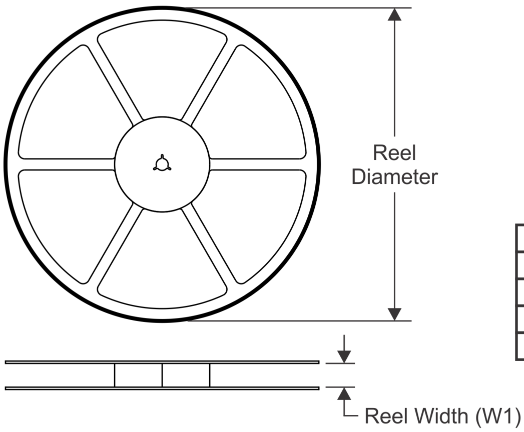
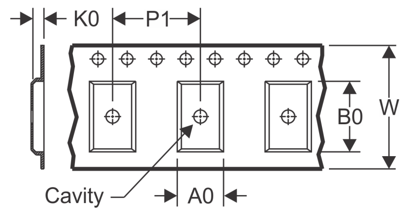
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

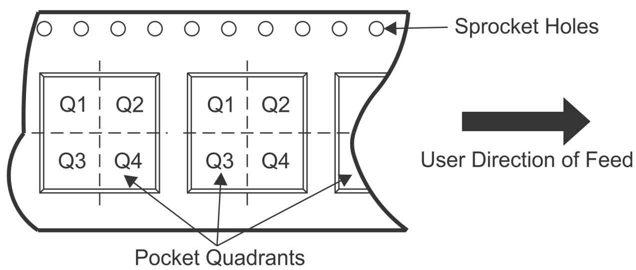


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

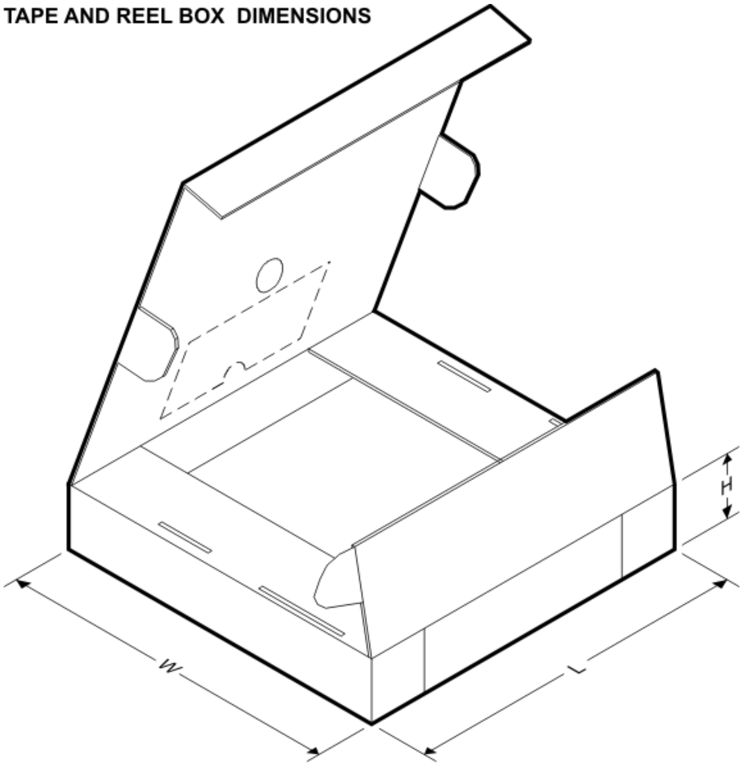
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

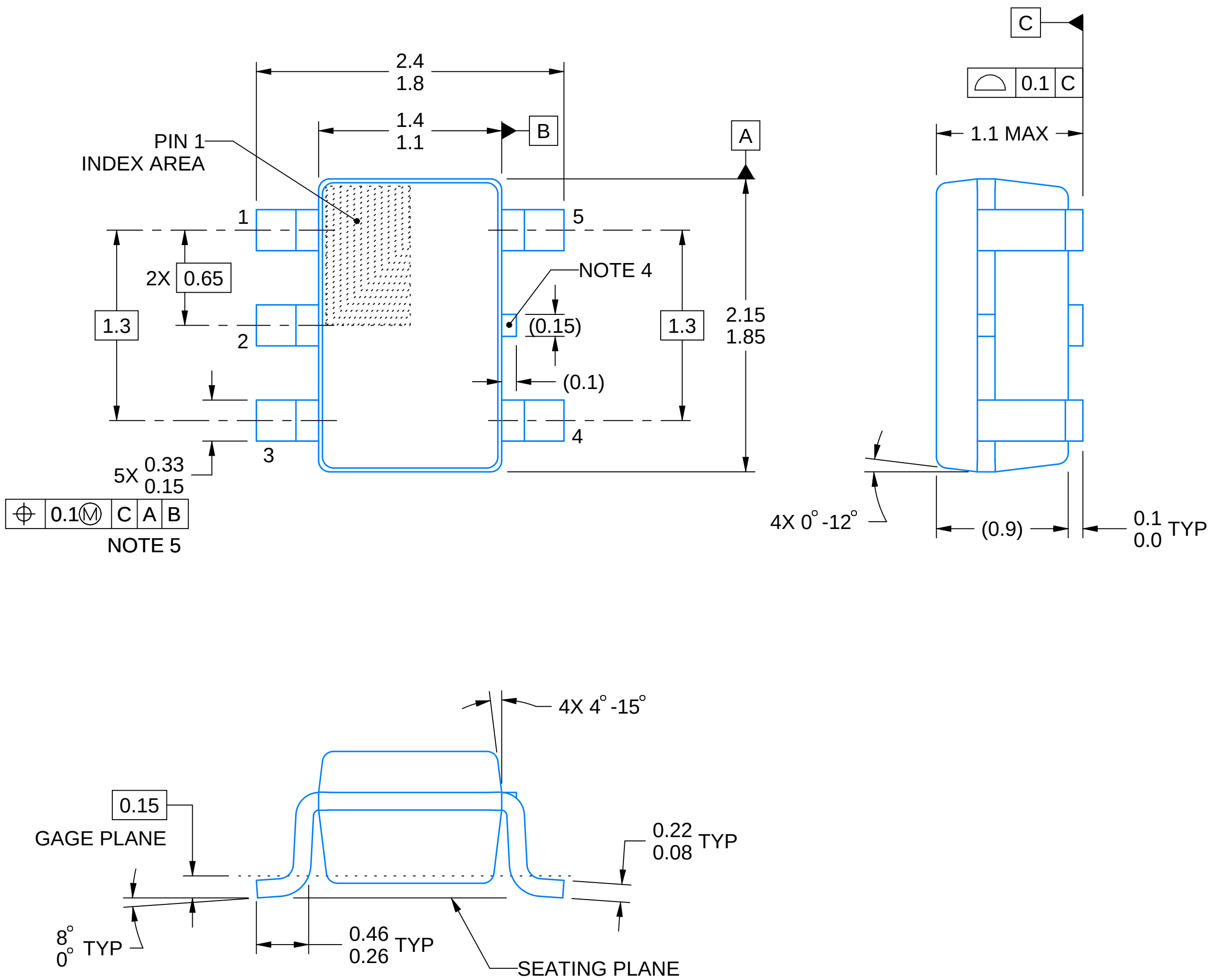
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SM73308MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SM73308MGE/NOPB	SC70	DCK	5	250	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SM73308MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SM73308MG/NOPB	SC70	DCK	5	1000	208.0	191.0	35.0
SM73308MGE/NOPB	SC70	DCK	5	250	208.0	191.0	35.0
SM73308MGX/NOPB	SC70	DCK	5	3000	208.0	191.0	35.0



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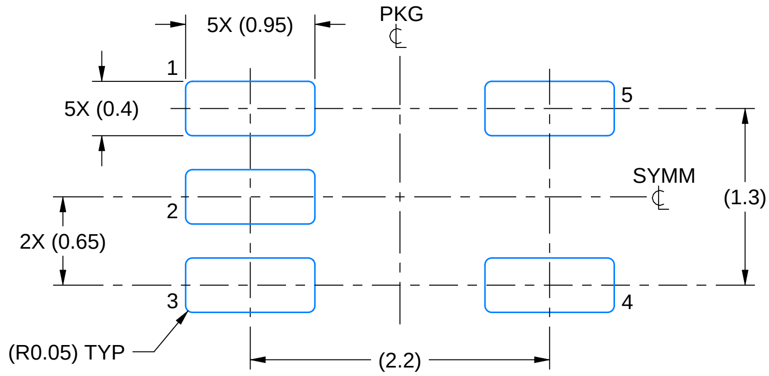
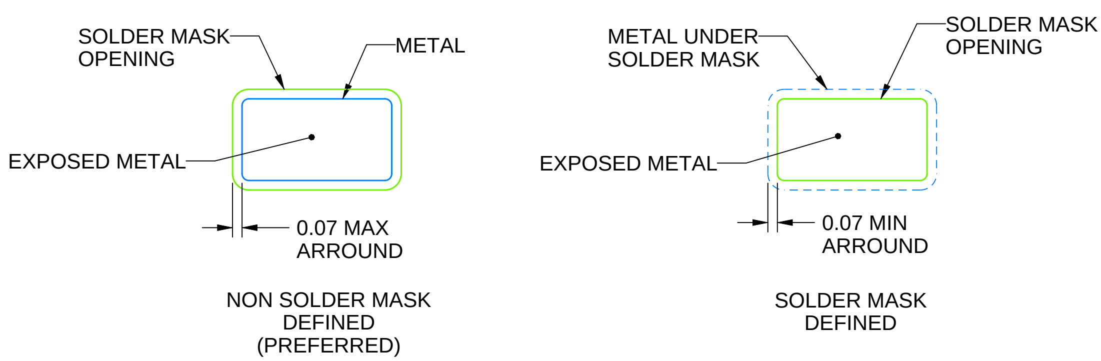
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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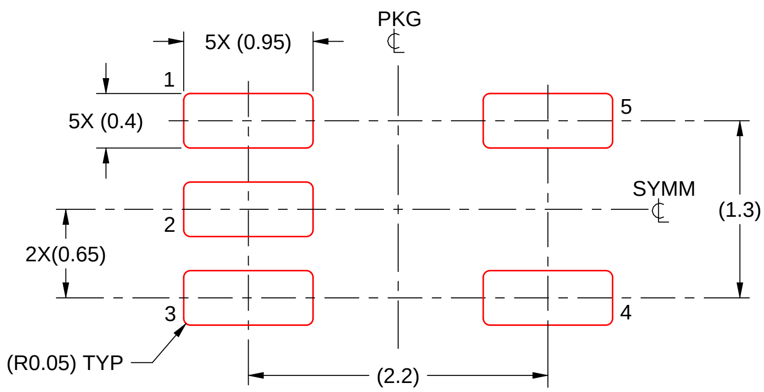
NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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